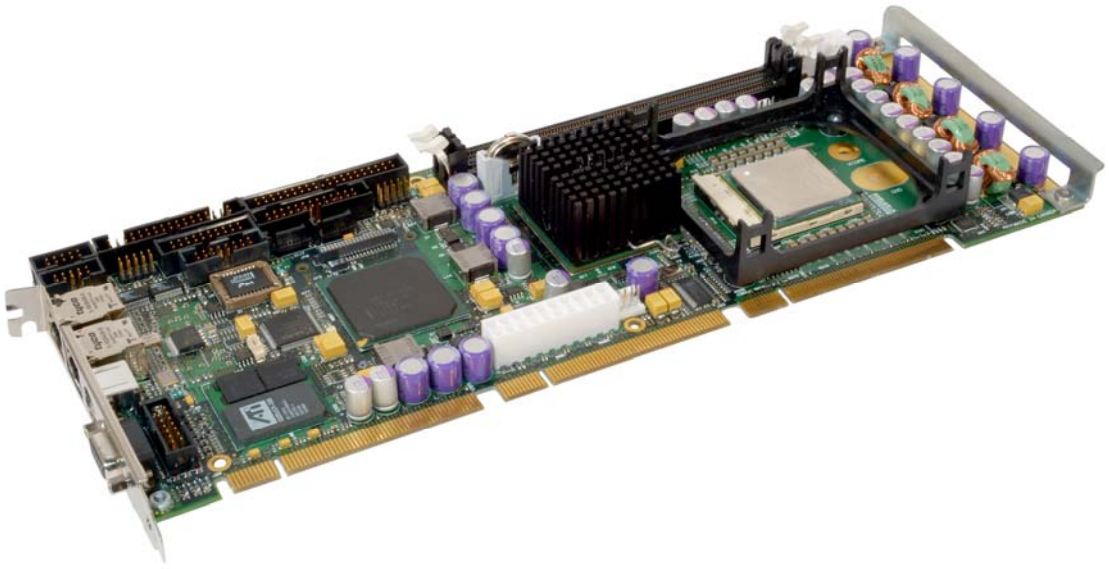
ePCI-201 User's Guide

Pentium 4 Full Size ePCI-X SHB

Document Revision 1.1



kontron

Ref. : M8004_TECH_0/ August 2005

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Contents

Safety Instructions

Contents

Before You Begin

Before handling the board, read the instructions and safety guidelines on the following pages to prevent damage to the product and to ensure your own personal safety. Refer to the "Advisories" section in the Preface for advisory conventions used in this user's guide, including the distinction between Warnings, Cautions, Important Notes, and Notes.

- Always use caution when handling/operating the computer. Only qualified, experienced, and authorized electronics service personnel should access the interior of the computer. The power supplies produce high voltages and energy hazards, which can cause bodily harm.

- Use extreme caution when installing or removing components. Refer to the installation instructions in this user's guide for precautions and procedures. If you have any questions, please contact Kontron Technical Support.

WARNING

High voltages are present inside the chassis when the unit's power cord is plugged into an electrical outlet. Turn off system power, turn off the power supply, and then disconnect the power cord from its source before removing the chassis cover. Turning off the system power switch does not remove power to components.

When Working Inside a Computer

Before taking covers off a computer, perform the following steps:

Turn off the computer and any peripherals.

Disconnect the computer and peripherals from power sources or subsystems to prevent electric shock or system board damage. This does not apply to when hot-swapping parts.

Follow the guidelines provided in “Preventing Electrostatic Discharge“ on the following page.

Disconnect telephone or telecommunications lines from the computer.

In addition, take note of these safety guidelines when appropriate:

- To help avoid possible damage to system boards, wait five seconds after turning off the computer before removing a component, removing a system board, or disconnecting a peripheral device from the computer.
- When you disconnect a cable, pull on its connector or on its strain-relief loop, not on the cable itself. Some cables have a connector with locking tabs. If you are disconnecting this type of cable, press in on the locking tabs before disconnecting the cable. As you pull connectors apart, keep them evenly aligned to avoid bending any connector pins. Also, before connecting a cable, make sure both connectors are correctly oriented and aligned.

CAUTION

Do not attempt to service the system yourself, except as explained in this user’s guide. Follow installation and troubleshooting instructions closely.

Preventing Electrostatic Discharge

Static electricity can harm system boards. Perform service at an ESD workstation and follow proper ESD procedure to reduce the risk of damage to components. Kontron strongly encourages you to follow proper ESD procedures, which means using wrist straps and smocks, when servicing equipment.

Take the following steps to prevent damage from electrostatic discharge (ESD):

- When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the component in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This discharges any static electricity that may have built up in your body.
- When transporting a sensitive component, first place it in an antistatic container or packaging.
- Handle all sensitive components at an ESD workstation. If possible, use antistatic floor pads and workbench pads.
- Handle components and boards with care. Do not touch the components or contacts on a board. Hold a board by its edges or by its metal mounting bracket.
- Do not handle or store system boards near strong electrostatic, electromagnetic, magnetic, or radioactive fields.

Working with Batteries

Care and Handling Precautions for Lithium Batteries

Your computer board has a standard, non-rechargeable lithium battery. To preserve the battery's lifetime, the battery enable jumper has been removed for shipping.

- Do not short-circuit
- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Do not mix different types or partially used batteries together
- Always observe proper polarities

Replacing Lithium Batteries

Exercise caution while replacing lithium batteries!

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries, following manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel. Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Puede explotar si la pila no este bien reemplazada. Solo reemplazca la pila con tipas equivalentes segun las instrucciones del manifacturo. Vote las pilas usads segun las instrucciones del manifacturo.

Preface

Contents

How to Use This Guide

This user's guide contains step-by-step instructions for installation and serves as a reference for operating, troubleshooting, and upgrading.

You can find the latest release of this User's Guide at:

http://www.kontron.com or at: ftp://ftp.kontron.ca/support/

For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

The following summarizes chapter contents:

- Chapter 1, Product Description
- Chapter 2, Onboard Features
- Chapter 3, Installing the board
- Chapter 4, Software Setup
- Appendix A, Memory & I/O Maps
- Appendix B, Interrupt Lines
- Appendix C, Kontron Extension Registers
- Appendix D, Connector Pinouts
- Appendix E, BIOS Setup Error Codes
- Appendix F, BIOS Update & Emergency Procedure
- Appendix G, Getting Help

Customer Comments

If you have difficulties using this user's guide, discover an error, or just want to provide some feedback, please send us a message at Tech.Writer@ca.kontron.com. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user's guide on our Web site. Thank you.

Advisory Conventions

Seven advisories are used throughout the user guides to provide helpful information or to alert you to the potential for hardware damage or personal injury. They are: Note, Signal Paths, Related Jumpers, BIOS Settings, Software Usage, Cautions, and Warnings. The following is an example of each type of advisory. Use caution when servicing electrical components.

Note:
Indicates information that is important for you to know.

Signal Paths:
Indicate the places where you can find the signal on the board.

Related Jumpers:
Indicate the jumpers that are related to this section.

BIOS Settings:
Indicate where you can set this option in the BIOS.

Software Usage:
Indicates how you can access this feature through software.

CAUTION

Indicates potential damage to hardware and tells you how to avoid the problem.

WARNING

Indicates potential for bodily harm and tells you how to avoid the problem.

Disclaimer: We have tried to identify all situations that may pose a warning or a caution condition in this user's guide. However, Kontron does not claim to have covered all situations that might require the use of a Caution or a Warning.

Unpacking

Follow these recommendations while unpacking:

- Remove all items from the box. If any items on the purchase order are missing, notify Kontron customer service immediately.
- Inspect the product for damage. If there is damage, notify Kontron customer service immediately.
- Save the box and packing material for possible return shipment.

Powering Up the System

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

If you encounter a problem, verify the following items:

- Make sure that all connectors are properly connected.
- Verify your boot devices.
- If the system does not start properly, try booting with only the video monitor connected to the board and without any other I/O peripherals attached, including Compact PCI or PMC adapters.

If you still cannot start your system, please refer to the Emergency Procedure in the Appendix Section of this User's Guide.

Make sure your system provides the minimum DC voltages required at the board's slot, especially if cables carry the DC power.

If you are still not able to get your board running, contact our Technical Support for assistance.

Adapter Cables

Because adapter cables come from various manufacturers, pinouts can differ. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

Storing Boards

Electronic boards are sensitive devices. Do not handle or store device near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Regulatory Compliance Statements

This section provides the FCC compliance statement for Class B devices and describes how to keep the system CE compliant.

FCC Compliance Statement for Class B Devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generated, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experience radio/TV technician for help.

WARNING

This is a Class B product. If not installed in a properly shielded enclosure and used in accordance with this User's Guide, this product may cause radio interference in which case users may need to take additional measures at their own expense.

UL Certification

This product bears the combined UL Recognized Component Mark for Canada and U.S. It indicates investigations to the UL Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment. It is destinated to be used in end-product equipment where the acceptability of the combination is determined by Underwriters Laboratories Inc.

CE Certification

The product(s) described in this user's guide complies with all applicable European Union (CE) directives if it has a CE marking. The CE declaration of conformity is provided on the last page of this user's guide. For computer systems to remain CE compliant, only CE-compliant parts may be used. Maintaining CE compliance also requires proper cable and cabling techniques. Although Kontron offers accessories, the customer must ensure that these products are installed with proper shielding to maintain CE compliance. Kontron does not offer engineering services for designing cabling systems. In addition, Kontron will not retest or recertify systems or components that have been reconfigured by customers.

Limited Warranty

Kontron Canada, Inc, ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

1 Product Description

Contents

1.1 Product Overview

The ePCI-201 is a generic processing engine board designed to support a broad range of applications requiring PCI bus support with high-performance processing, such as those found in automation, communications, medical and military environments. Combining high value, fast time-to-market and long life support, the ePCI-201 offers a host of design and integration possibilities for developers. It is especially suited for applications requiring high memory bandwidth combined with CPU intensive tasks such as image processing, VoIP, and HLR/SCP.

The ePCI-201 includes a rich set of standard features including the latest generation Intel® Pentium® 4 processor at up to 3.4GHz 800MHz FSB, dual channel memory DDR, 2-channel serial ATA, an onboard ATI MOBILITY™ RADEON™ M7 dual-screen video controller with TV output, dual gigabit Ethernet and 64-bit at 66MHz bus support. Additional onboard features include one EIDE hard disk interface, two Serial ATA disk interface, Compact Flash module support, four USB 2.0 ports, two serial ports, floppy disk controller, and board monitoring features. The ePCI-201 supports various operating systems including Windows 2000, Windows XP, Windows Server 2003 and Linux.

1.2 What's Included

This board is shipped with the following items:

1. One Quick Reference Sheet
2. One CD-ROM containing drivers
3. One ePCI-201 board
4. Cables listed on the order
5. One mezzanine with two USB connectors, one RCA connector and one video (DB15) connector.

If any item is missing or damaged, contact the supplier.

1.3 Board Specifications

FEATURES	DESCRIPTION
Supported Microprocessors	• Socket 478 Pentium-4 Desktop Northwood and Prescott Processors with a Front Side Bus (FSB) at 533 and 800MHz • Pentium-4 Mobile Northwood and Mobile Prescott with a Front Side Bus (FSB) at 533MHz
Cache Memory	• 512KB (Northwood)/1MB (Prescott) L2 on-die cache
Chipset	• Intel 875P
Bus Interface	• Front side bus at 533/800 MHz, 64-bit data, 32-bit address • Memory bus at 333/400 MHz, single/dual channel 144-bit ECC (128-bit non-ECC) data un-buffered DIMMS 2.5V • ePCI-X Bus A: PCI 32-bit / 33 MHz (3.3V & 5V) • ePCI-X Bus B: PCI-X 64-bit/66MHz (3.3V only)
System Memory	• Up to 2GB on 2 x 184-pin latching DIMM socket • DDR333 or DDR400 un-buffered DRAM
Flash Memory	• 1MB, upgrade on LPC • 64 bits Silicon Serial Number

I/O

Description	Faceplate / Video Mezzanine	Onboard	Total
Video	1 / 1	1	2
USB	- / 2	4	4
Serial	- / -	2	2
PS/2 Mouse	1 / -	1	1
PS/2 Keyboard	1 / -	1	1
Ethernet	2 / -	-	2
Hard Disk PATA (IDE)	- / -	2	2
Hard Disk SATA	- / -	2	2
Compact Flash	- / -	1	1
Floppy	- / -	1	1
Parallel	- / -	1	1

F / O	Faceplate or Onboard
Video	ATI Mobility Radeon M7 Video controller with up to 32 MB of memory. It supports 2 CRT with resolution up to 1920 x 1440, 32-bit colors On faceplate, female D-sub 15-pin.
USB	Four USB 2.0 ports
Serial	COM1 as RS-232, COM2 configurable as RS-232/RS-422/485
Ethernet	One 10Base-T/100Base-Tx/1000Base-TX (Intel 82547GI) One pseudo 10Base-T/100Base-Tx/1000Base-TX (Intel 82541ER)
Hard Disk	Ultra DMA/100, support for two IDE drives (in master / slave configuration) SATA, support for two SATA drives
Floppy Disk	Support for one drive
Compact Flash	Supports CompactFlash disk module (on secondary channel)

Board Specifications (continued)

Clock/Calendar	• Real-time clock with 256-byte battery backup CMOS RAM
Connectors on faceplate	**Front Plate** CRT: 15-pin D-Sub Ethernet 0 and 1: 2 x RJ-45 with built-in LEDs
Connectors on Video Mezzanine faceplate	**Video Mezzanine on Front Plate** CRT: 15-pin D-Sub USB 0 and 1: 1 x 4-pin USB female TV-out: 1 x 2-pin RCA connector
Connectors on Headers (onboard)	**Onboard Connectors** Serial Ports (2), USB (4), 12V CPU Power (1) CompactFlash (1), ATX Power Connector (1), SATA (2) Post Code (1), Hardware Monitor (1), Multifunction (1) EIDE (1), Floppy disk (1), Parallel Port (1) CPU Fan (1), MCH Fan (1), Video Fan (1) **Onboard Expansions** CompactFlash
BIOS Features	• AMI BIOS in Boot Block Flash with recovery code; save CMOS in Flash option, and Boot from LAN capability • Auto configuration, extended setup and VGA by jumper • Diskless, keyboardless, and videoless operation extensions • System, video and LAN BIOS shadowing • Programmable memory wait states • Advanced security feature for floppy and HDD & HDD S.M.A.R.T. support • Advanced Configuration and Power Interface (ACPI 2.0), Intelligent System Monitoring (advanced thermal management such as resume, overheat alarm and auto slow down) • Setup console redirection to serial port (VT100 mode) with CMOS setup access • All onboard peripherals can be enabled or disabled by software
Supervisory	• Dual-stage software programmable watchdog timer • Silicon Serial ID TAG for unique board identification accessible via software • Hardware system monitor (voltages, temperature), CPU temperature monitor / alarm; board temperature sensor, power failure / low battery detector; SMBus • 12V, 5V, 3.3V, VBAT and Vcore voltage supervisor • Ethernet activity & link • CPU overheat protection • CPU switcher overheat protection
OS Compatibility	• Microsoft Windows 2000 family • Microsoft Windows XP • Microsoft Windows Server 2003 • Linux Red Hat 9
Mechanical	338 x 130 x 40 mm at CPU / fan (133.33 x 4.80 x 1.6 in. at CPU / fan)

Board Specifications (continued)

Power Requirements	Supply Voltage VCC = +3.3V +5% -3% +5V +5% -3% +12V ± 5% -12V ± 5% ICC typ. +5V 4.7A ICC typ. +3.3V 4.4A ICC typ. +12V 7.8A ICC typ. –12V < 100mA (monitoring only) Tested with 2GB of PC3200 and a Prescott 3.0 GHz Pentium 4 processor		
Environmental		Operating	Storage and Transit
	Temperature	0-55°C/32-131°F	-40 to +70°C/-40 to 158°F
	Humidity	5% to 90% @40°C/104°F non-condensing	5% to 95% @ 40°C/104°F non-condensing
	Altitude*	4,000 m / 13,123 ft	15,000 m / 49,212 ft
	Shock*	5G each axis	Bellcore GR-63-CORE Section 4.3
	Vibration*	1.0G, 5-500Hz each axis	2.0G, 5-50Hz; 3.0G, 50-500Hz each axis
Reliability	• MTBF: > 120 000 hours @30°C / 86°F (Telcordia SR-332) • USB voltage protected by an active breaker • Mouse / keyboard voltage protected by self-resetting fuses		
Safety/EMC	Designed to meet or exceed: • Safety: UL 60950 3rd Ed.; CSA C22.2 No 60950-00; EN 60950:2000; IEC60950-1 • EMI/EMC: FCC 47 CFR Part 15, Class B; EN55022/EN55024		
Warranty	2 year limited warranty		

*** Designed to meet**

1.4 ePCI Compliance

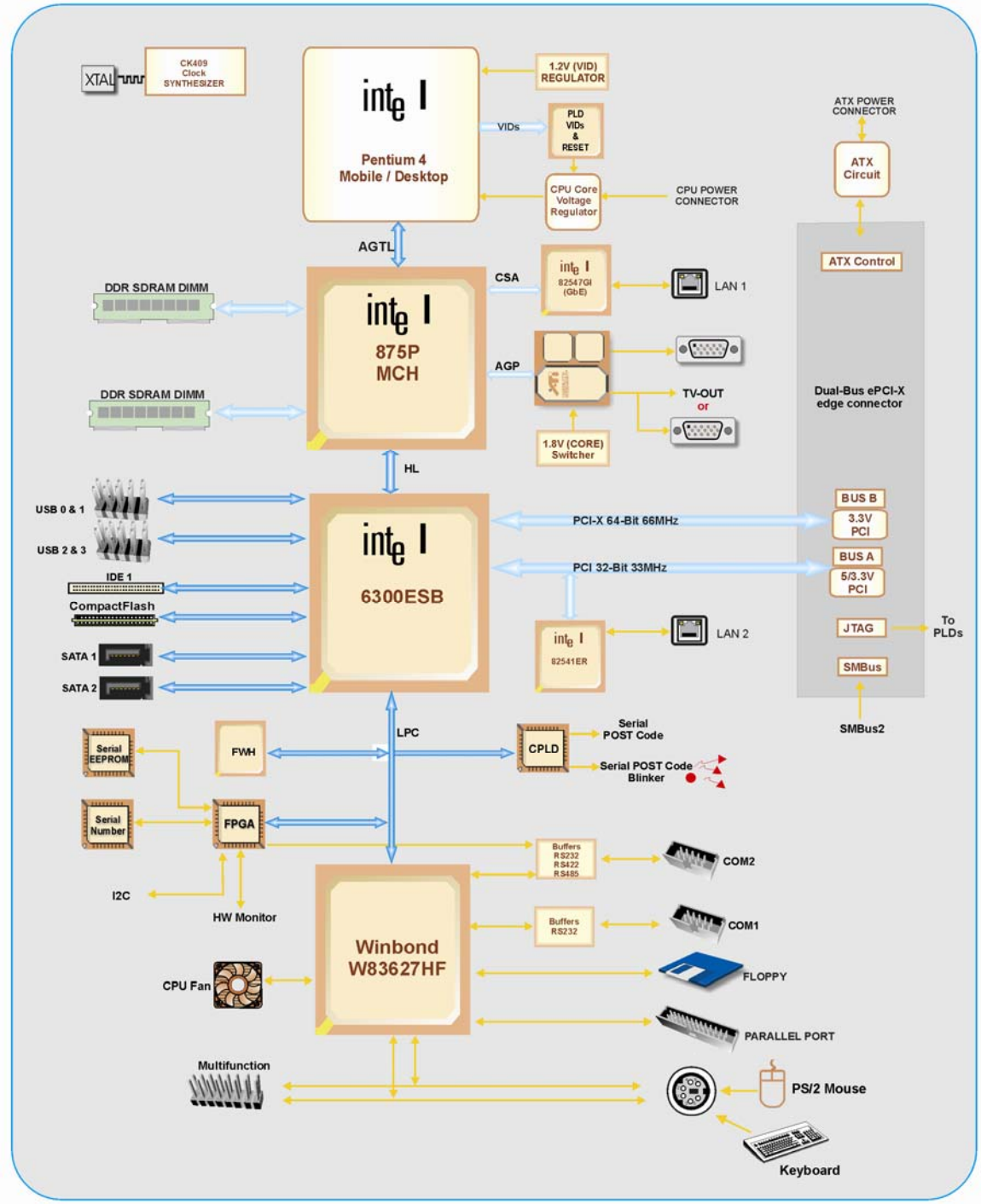
This product conforms to the following specifications:

- PICMG1.2 R1.0

2 Onboard Features

Contents

2.1 Block Diagram



2.2 System Core

2.2.1 Processors

The ePCI-201 is a full-size board that supports Intel's Pentium 4 processors.
Major CPU features include:

- Supports Intel® NetBurst® microarchitecture and may support Hyper-Threading Technology.
- On-die, up to 16-KB Level 1 data cache
- On-die, up to 1-MByte second level cache with Advanced Transfer Cache Architecture
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2) and 3 (SSE3) (SSE3 supported only with the Prescott)
- 533/800-MHz, Source-Synchronous processor system bus
- Advanced Power Management features including Enhanced Intel SpeedStep® technology on mobile processors
- 478-pin FC-PGA2/FC-mPGA4 packaging technologies

Please call Kontron to get the available CPU speed and configuration. See Intel's Web site for additional details about Pentium 4 architecture and instruction set.

2.2.2 Chipset Features

The ePCI-201 uses the Intel 875P chipset, which includes the following high-performance devices:

Host Interface Support

— Intel® Pentium 4 processor 0.13 micron process / Intel® Pentium 4 processor on 90 nm process
— 64-bit FSB frequencies of 533 MHz (133 MHz bus clock), and 800 MHz (200 MHz bus clock). Maximum theoretical BW of 6.4 GB/s.
— FSB Dynamic Bus Inversion on the data bus
— 32-bit addressing for access to 4 GB of memory space
— 12-deep In Order Queue
— Hyper-Threading Technology

System Memory Controller (DDR) Support

— Dual-channel (128 bits wide for non-ECC or 144 bits wide for ECC) DDR memory interface
— Single-channel (64 bits wide for non-ECC or 72 bits wide for ECC) DDR memory interface
— Symmetric and asymmetric memory dual-channel upgrade
— 128-Mb, 256-Mb, 512-Mb technologies implemented as x8, x16 devices
— Four bank devices
— Non-ECC and ECC 2.5V, un-buffered DIMMS only
— Up to 4 GB system memory (limited by DIMM availability)
— Up to 16 simultaneously-open pages (four per row) in dualchannel mode and up to 32 open pages in single-channel mode
— 4-KB to 64-KB page sizes (4 KB to 32 KB in single-channel, 8 KB to 64 KB in dual-channel)
— Opportunistic refresh
— SPD (Serial Presence Detect) Scheme for DIMM Detection
— DDR (Double Data Rate type 1)
— DDR channel operation at 266 MHz, 333 MHz and 400 MHz with a Peak BW of 2.1 GB/s, 2.7 GB/s, and 3.2 GB/s respectively per channel
— Burst length of 4 and 8 for single-channel (32 or 64 bytes per access, respectively); for dual-channel a burst of 4 (64 bytes per access)

Communication Streaming Architecture (CSA) Interface Support

— 8-bit Hub Interface 1.5 electrical/transfer protocols.
— 266 MB/s point-to-point connection to MCH
— Gigabit Ethernet (GbE) supported
— 1.5 V operation

Hub Interface (HI) Support

— Hub Interface 1.5
— 266 MB/s point-to-point Hub Interface to the ICH5
— 66 MHz base clock

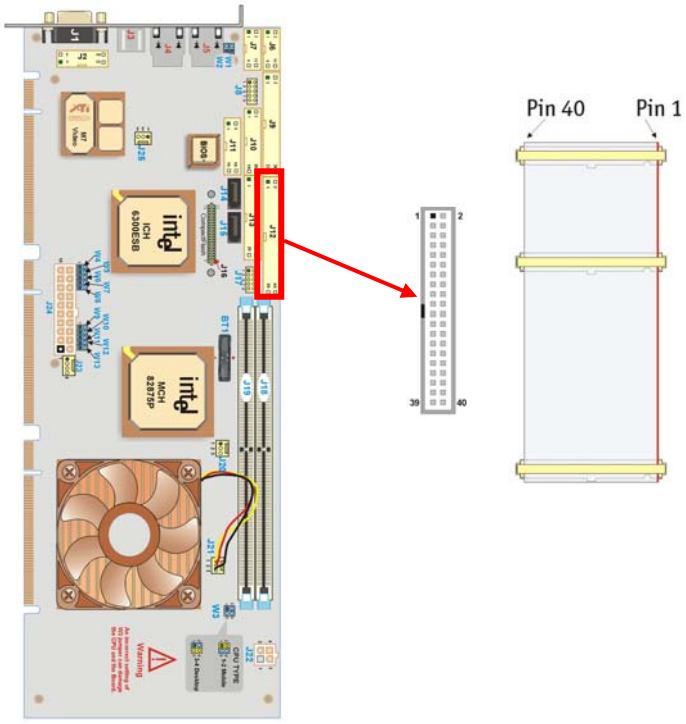
AGP Interface Support

— AGP 4X
— 32-bit 4X data transfers and 4X fast writes
— Peak BW of 1 GB/s.

2.3 Intel i875P

2.3.1 Enhanced IDE Interface (J12)

The board features a one-channel Bus Master PCI EIDE that is dedicated to Primary IDE logical interface. This channel supports up to two devices (including CD-ROMs and hard disks) with independent timings, using a Master/Slave combination.



Pin	Signal	Pin	Signal
1	RST#	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	N.C. (KEY)
21	REQ	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IORDY	28	PRIMPDI
29	DACK#	30	GND
31	IRQ	32	N.C. (IOCS16#)
33	A1	34	DIAG#
35	A0	36	A2
37	CS0#	38	CS1#
39	ACT#	40	GND

Signal Paths:
Primary IDE interface: J12 (40-pin header)

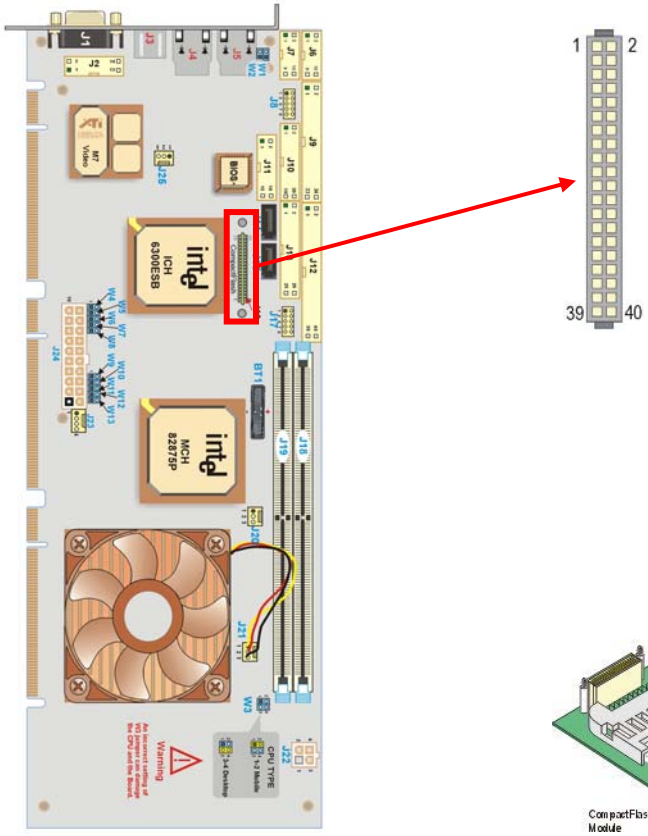
BIOS Settings:
Main \ Advanced \ IDE Configuration

CAUTION

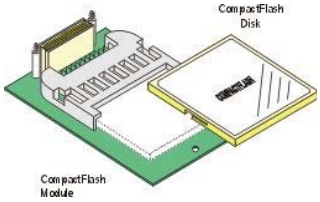
Two Master devices (or two Slave devices) must not be installed on the same interface at the same time.

2.3.2 CompactFlash Interface (J16)

This board supports an ATA/IDE compatible flash disk by using a CompactFlash carrier module. The CompactFlash disk connects directly on the secondary EIDE interface. Configure it the same way as a standard hard disk using the BIOS setup program (Autodetect function). No driver is needed to use a CompactFlash. The CompactFlash is always set in Master mode.



Pin	Signal	Pin	Signal
1	D11	2	GND
3	D12	4	D3
5	D13	6	D4
7	D14	8	D5
9	D15	10	D6
11	CS1#	12	D7
13	DMACK#	14	CS0#
15	DMARQ	16	IOR#
17	PDIAG#	18	IOW#
19	IRQ15	20	VCC
21	VCC	22	VCC
23	GND	24	GND
25	RESET#	26	GND
27	CSEL	28	A2
29	A1	30	DASP#
31	A0	32	IORDY
33	D0	34	D8
35	D1	36	D9
37	D2	38	D10
39	IOCS16#	40	GND



Signal Paths:

J16 (CompactFlash connector)

BIOS Settings:

Main \ Advanced \ IDE Configuration

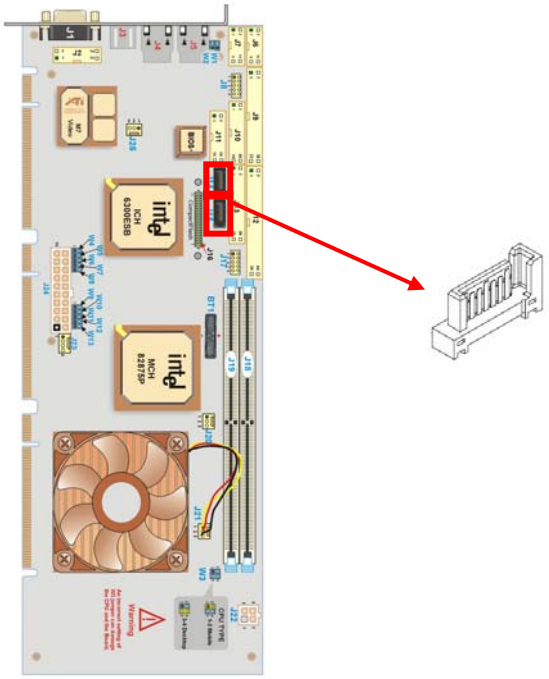
CAUTION

1. When using a CompactFlash, the operating temperature must not exceed 50°C/122°F.

2. Two master devices (or two slave devices) must not be installed on the same IDE channel at the same time.

2.3.3 SATA Interfaces (J14 & J15)

The board features a two-channel Bus Master PCI SATA. Each channel supports one device.



Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

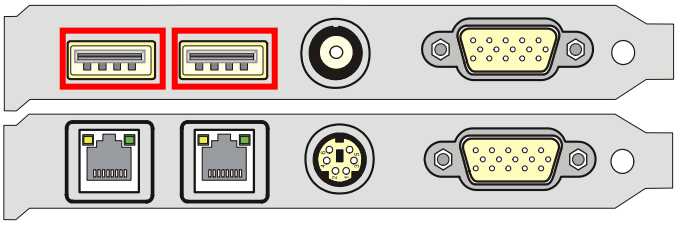
Signal Paths:
SATA interface: J14 & J15

BIOS Settings:
Main \ Advanced \ IDE Configuration

2.3.4 USB Interfaces

The USB 2.0 strengths are as follows: capability to daisy chain as many as 127 devices per interface, fast bi-directional, isochronous/asynchronous interface, 480Mbps transfer rate, and standardization of peripheral interfaces into a single format. USB supports Plug and Play and hot swapping operations (OS level). These user-friendly features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.

2.3.4.1 USB 0 & 1 (J1 & J2 on Video Mezzanine)



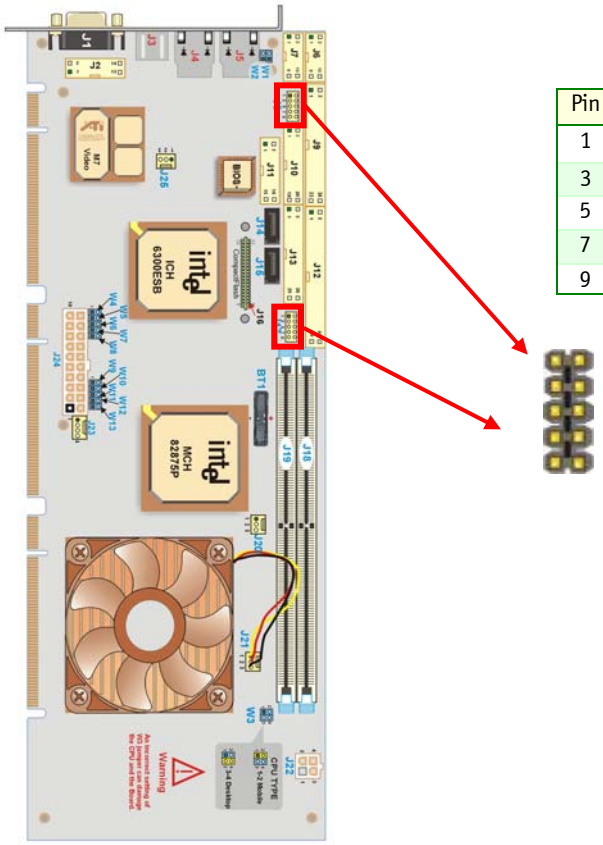
Pin	Signal
1	VCC
2	DATA-
3	DATA+
4	GND

Signal Paths:
USB0 & USB1 signals are available on faceplate through J1& J2 connector.

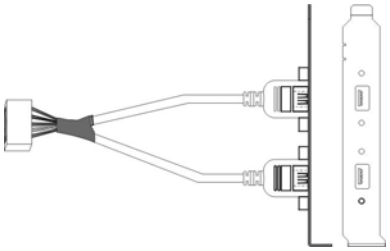
BIOS Settings:
Advanced \ USB configuration

2.3.4.2 USB0-1 and USB2-3 (J8 & J17)

If the USB port connectors on the faceplate are insufficient, a USB header is available for additional USB port connectors. Connect the two-port USB connector to the USB header and mount the USB bracket to an open slot in the chassis.



Pin	Signal USB 0 & 2	Pin	Signal USB 1 & 3
1	VCC	2	VCC
3	DATA-	4	DATA-
5	DATA+	6	DATA+
7	GND	8	GND
9	Shield Ground	10	Shield Ground



Signal Paths:

J8 & J17 (USB header for two ports)
J8 is used to connect to the video/USB mezzanine

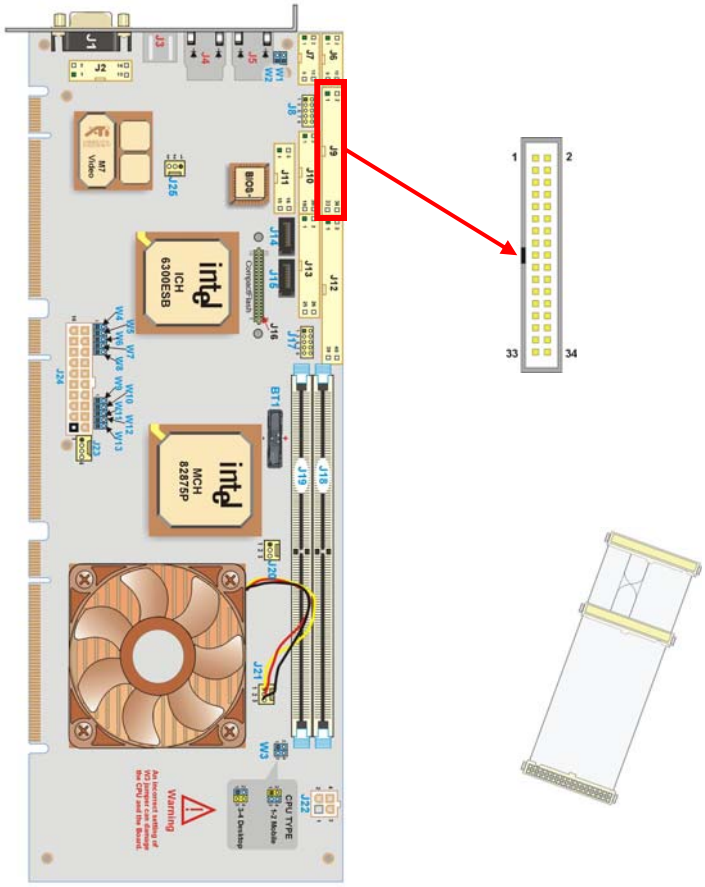
BIOS Settings:

To enable/disable the USB Host controller, refer to Section Advanced Menu selection, *USB configuration Sub-Menu*.
To support USB keyboard, refer to Advanced Menu, *USB Configuration, Legacy USB Support*.

2.4 Super I/O

2.4.1 Floppy Connector (J9)

The onboard floppy disk controller is IBM PC XT/AT compatible. One drive is supported.



Pin	Signal	Pin	Signal
1	GND	2	DENSEL#
3	GND	4	N.C.
5	GND	6	N.C.
7	GND	8	INDEX#
9	GND	10	MTR0#
11	GND	12	DSEL1#
13	GND	14	DSEL0#
15	GND	16	MTR1#
17	N.C.	18	DIR#
19	GND	20	STEP#
21	GND	22	WDATA#
23	GND	24	WGATE#
25	GND	26	TRK0#
27	N.C.	28	WRPROT#
29	FDETECT	30	RDATA#
31	GND	32	HDSEL#
33	N.C.	34	DSKCHG#

Signal Paths:

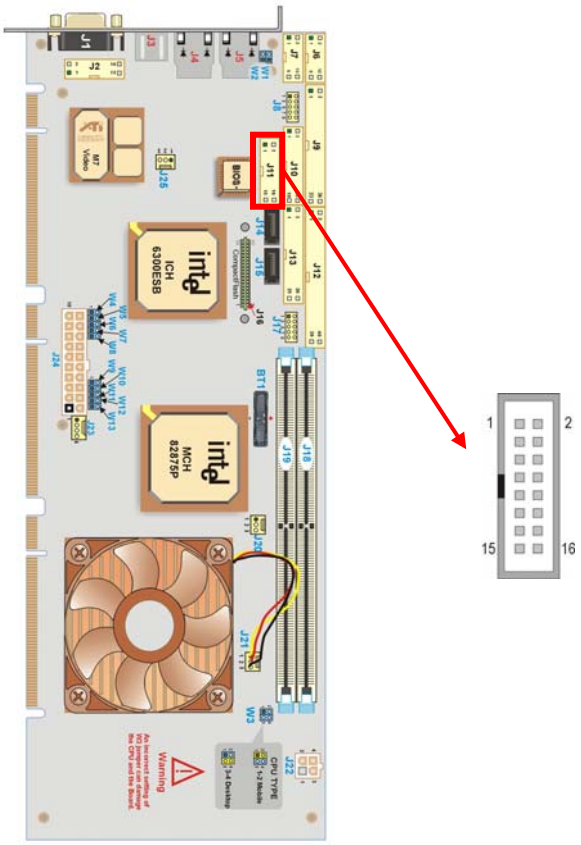
J9: Floppy disk interface on a standard header.

BIOS Settings:

Main \ Advanced \ SuperIO Configuration
OnBoard Floppy Controller (Enabled or Disabled)
Main \ Advanced \ Floppy Configuration
Floppy A (Disabled or 1.44 MB $3^{1/2}$")

2.4.2 Multifunction Connector (J11)

Standard PS/2 keyboard, PS/2 mouse, speaker output, reset and hard disk activity LED signals are available on the Multifunction connector.

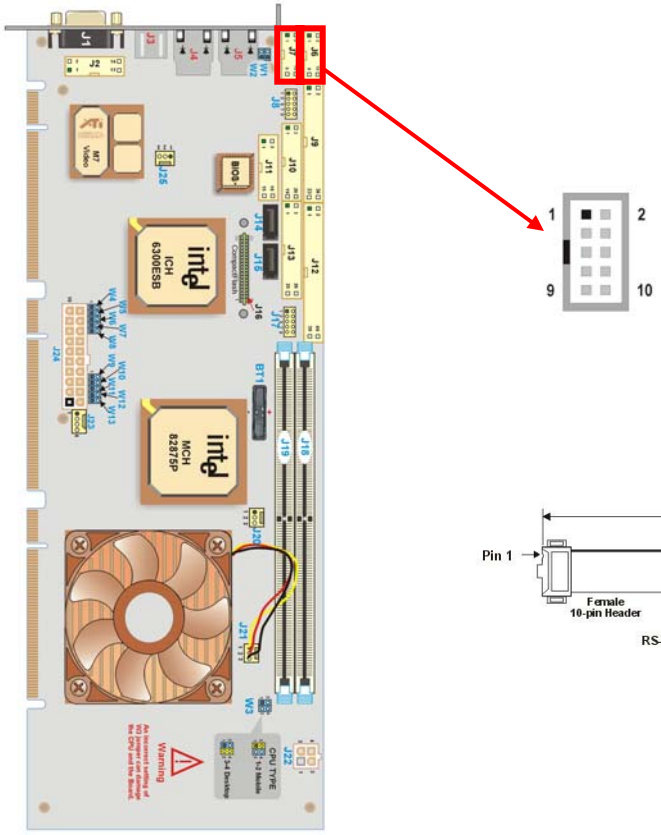


Pin	Signal	Pin	Signal
1	KB:CLK	2	GND
3	KB:DATA	4	GND
5	VCC	6	VCC
7	SPEAKER	8	VCC
9	MOUSE:CLK	10	GND
11	MOUSE:DATA	12	GND
13	PBRES#	14	GND
15	IDE:ACT#	16	VCC

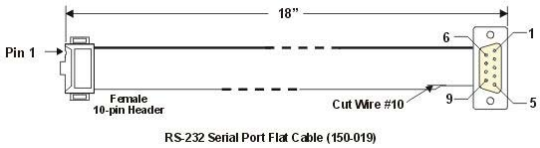
Signal Paths:
J11 (Multifunction Connector)

2.4.3 Serial Ports (J6 & J7)

Two fully functional serial ports are provided for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 300bps to 115Kbps.



Pin	Signal
1	DCD
2	DSR
3	RXD
4	RTS
5	TXD
6	CTS
7	DTR
8	RI
9	GND
10	N.C.



RS-232 Serial Port Flat Cable (150-019)

2.4.3.1 Serial Port 1 (J6)

This Serial Port is buffered for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

Signal Paths:
J6 Serial Port 1 (RS-232 Mode only)

BIOS Settings:
- Main \ Advanced \ SuperIO Configuration
- Serial port1 Address

2.4.3.2 Serial Port 2 (J7)

This serial port is buffered for RS-232, RS-422 or RS-485 operations. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

Signal Paths:
J7 Serial Port 2 (RS-232, RS-422 or RS485)

Related Jumpers:
W1 and W2: insert both jumpers if serial port 2 is used in RS-422 or RS-485 mode and need termination resistors. Termination resistors are 120-ohm.

BIOS Settings:

- Main \ Advanced \ SuperIO Configuration
- Serial port2 Address
- Serial Port2 Interface
- Reset on a Serial Port Break

Software Usage:
Register 0x190 provide buffer control. See appendix C for details.

Upon a power-up or reset, the Serial Port 2 interface circuit is automatically configured for the operation mode setup in the BIOS. This Serial Port signal assignation on the connector depends upon the operation mode (RS-232, RS-422, or RS-485) that has been set:

Pin	RS-232	RS-422	RS-485
1	DCD	RSV	RSV
2	RXD	RSV	RSV
3	TXD	RXB	485B
4	DTR	RXA	485A
5	GND	TSB	RSV
6	DSR	TXA	RSV
7	RTS	RSV	RSV
8	CTS	RSV	RSV
9	RI	GND	GND
10	CTS	N.C.	N.C.

RS-232 Protocol
When configured for RS-232 operation mode, the Serial Port 2 is 100% compatible with IBM-AT serial port signals.

RS-422 Protocol
The RS-422 protocol (Full Duplex) uses both RX and TX lines simultaneously during a communication session.

CAUTION

In RS-422 mode, W1 and W2 jumper caps must be installed to connect the 120-ohm line termination resistors.

RS-485 Protocol

During a communication session, the RS-485 protocol (Full Duplex) uses differential signals. It differs from the RS-422 mode by offering the ability to transmit and receive over the same pair of wires and allows the sharing of the communication line by multiple stations. This configuration (also known as Party Line) allows only one system to take control of the communication line at the time.

In RS-485 mode, the RX lines are used as the transceiver lines and the RTS signal controls the direction of the RS-485 buffer.

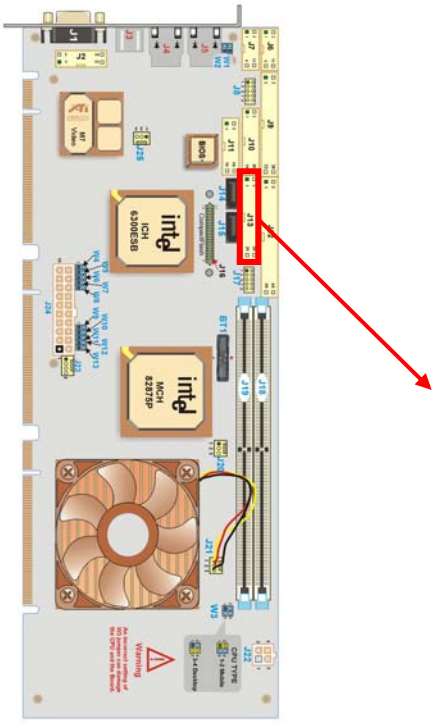
When set for RS-485 mode in the BIOS, upon power-up or reset, the transceiver is set by default in receiver mode to prevent unwanted disturbance on the line. The operation mode for party lines requires termination resistors to be installed at both ends of the network.

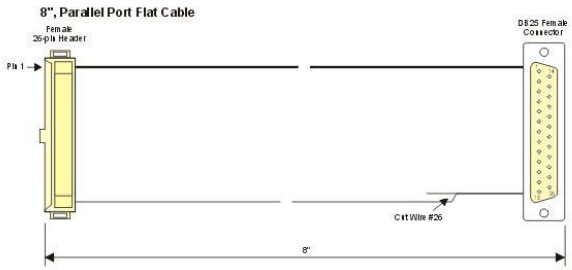
CAUTION

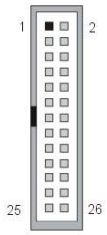
When installing the board at one end of the network, W1 and W2 jumper caps must be installed to connect the 120 ohms termination resistors.
(See *Setting Jumpers*).

2.4.4 Parallel Port (J13)

The board features one IEEE-1284 multi-mode parallel port. It is compatible with Standard Mode IBM PC/XT, PC/AT, and PS/2 compatible bi-directional parallel port, Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP).







Pin	Signal	Pin	Signal
1	STB#	2	ALF#
3	D0	4	ERR#
5	D1	6	INIT#
7	D2	8	SLCTIN#
9	D3	10	GND
11	D4	12	GND
13	D5	14	GND
15	D6	16	GND
17	D7	18	GND
19	ACK#	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	GND

Signal Paths:
J13: parallel port interface on header.

BIOS Settings:
- Main \ Advanced \ SuperIO Configuration
- Parallel Port Address
- Parallel Port Mode
- EPP Version
- ECP Mode DMA Channel
- Parallel Port IRQ

The differences between Standard, EPP, and ECP modes appear in the signal assignation of the pins on the connector.

Note:
To operate in EPP or ECP mode, ensure the peripheral is designed to work in this mode and the BIOS setup is configured to support it.

Standard Mode

The Standard mode is unidirectional and enables compatibility with the IBM PC standard.

EPP Mode

The Enhanced Parallel Port (EPP) mode consists of a hardware independent method of accessing a parallel port configured as EPP. It provides support for single I/O cycle as well as the high performance block I/O transfers. The EPP mode always uses the most optimum method for I/O transfers. For example, if the hardware supports it, EPP mode will perform 32-bit I/O block transfers.
EPP mode assumes that the parallel port can be used to connect more than one peripheral device using multiplexer or daisy chain configurations.
A multiplexer is an external device that permits up to eight parallel port devices to share a single parallel port.
A daisy chain device has two ports: input and output. The input port is connected either to the host parallel port or the daisy chain device in front of it. The output is used to connect the next peripheral device to the daisy chain. The last device, however, can be one without daisy chain support.

ECP Mode

The Extended Capabilities Port (ECP) mode works like the EPP mode, but it will take precedence over the EPP mode when addressing multiple logical devices in a single physical product. While the EPP mode may intermix read and write operations without overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgment from peripherals.

Note:
For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support Department.

Upon a power-up or reset, the Parallel Port interface circuit is automatically configured for the operation mode setup in the BIOS. This Parallel Port signal assignation on the connector depends upon the operation mode (STD, EPP, or ECP) it has been set:

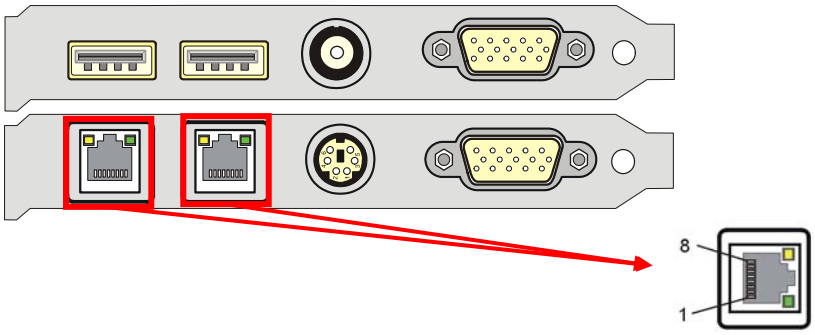
Pin	STD	EPP	ECP	
			Compatible Mode	High Speed Mode
1	STB#	WRITE#	STROBE#	STROBE#
2	ALF#	DATASTB#	AUTOFD	HOSTACK
3	D0	D0	D0	D0
4	ERR#	N.C.	FAULT	PERIPHRQST
5	D1	D1	D1	D1
6	INIT#	N.C.	INIT	REVERSERQST
7	D2	D2	D2	D2
8	SLCTIN#	ADDRSTRB#	SELECTIN	SELECTIN
9	D3	D3	D3	D3
10	GND	GND	GND	GND
11	D4	D4	D4	D4
12	GND	GND	GND	GND
13	D5	D5	D5	D5
14	GND	GND	GND	GND
15	D6	D6	D6	D6
16	GND	GND	GND	GND
17	D7	D7	D7	D7
18	GND	GND	GND	GND
19	ACK#	INTR	ACK#	ACK#
20	GND	GND	GND	GND
21	BUSY	WAIT	BUSY,PERIPHACK	BUSY,PERIPHACK
22	GND	GND	GND	GND
23	PE	N.C.	PERROR, ACKREVERSE	PERROR, ACKREVERSE
24	GND	GND	GND	GND
25	SLCT	N.C.	SELECT	SELECT
26	GND	GND	GND	GND

2.5 Ethernet Controllers (J4 and J5)

One Intel 82547GI and one 82541ER Ethernet controllers are used. These controllers support 10Base-T, 100Base-TX and 1000Base-TX operations: 10Mbps, 100Mbps and 1000Mbps network speeds are automatically detected and switched.

The 82547GI and the 82541ER offer automatic crossover. When connecting an ePCI-201 to another computer, a straight cable can be used and the controller will automatically swap the TX and RX pairs.

Use the 82547GI for more bandwith intensive link. The connector is identified as “high BW” on the backside of the board.



Pin	Signal
1	MDI0+
2	MDI0-
3	MDI1+
4	MDI2+
5	MDI2-
6	MDI1-
7	MDI3+
9	MDI3-

Signal Paths:

J4 and J5 RJ45 connectors on the bracket.

BIOS Settings:

- Main \ Advanced \ On-board Devices Configuration
- On-board Ethernet 1 Controller (82547GI)
- Option ROM, required for boot from LAN.
- On-board Ethernet 2 Controller (82541ER)
- Boot \ Boot Device Priority
- Select Boot priority for Boot LAN

Boot from LAN

The Boot from LAN capability is supported from the 82547GI only. To enable the option, use the BIOS Setup program (Boot Menu Selection).

Drivers

A CD-ROM is included. It contains network drivers for most common operating systems.

2.6 Video Interface

The onboard ATI Mobility Radeon M7 video interface supplies the video through:

- Standard VGA output located on the faceplate (DB-15 female connector)
- TV-Out or second VGA on 14-pin header/mezzanine.

The video controller with its two independent CRT controllers supports two asynchronous simultaneous display paths (CRT/TV and CRT/CRT), with drivers support. Resolution can go up to 1600x1200. BIOS support only (CRT1 and TV-OUT) with one display path.

2.6.1 Mobility Radeon M7 Highlights

- Exceptional 2D/3D/video performance
- 32MB integrated video DDR memory, expandable to 64MB with external memory.
- 260MHz engine clock/ 183MHz memory clock
- Dual DAC
- Integrated high-resolution TV-out (up to 1024x768)

2.6.2 Standard VGA output

Signal Paths:
J1 is the primary CRT output

Related Jumpers:
W6: when present, it disable the onboard video

2.6.3 TV-OUT or second VGA output

The Mobility Radeon includes an integrated TV with these TV-out characteristics:

- 10-bit DAC with 8-tap filter producing scaled, flicker removed, artifact suppressed display on a PAL or NTSC TV with Composite output.
- Support for Macrovision 7.02 copy protection standard (required by DVD players) – a fully programmable timing capability, it will accommodate potential changes in the Macrovision algorithm without any hardware changes.
- Line 21 Closed Caption and Extended Data Service support for encoding in Vertical Blanking Interval (VBI) of TV signal.
- CGMS-A DVD copy management support in VBI through Line-20 and/or Extended Data Service (Line-21 Field 2).
- UV filtering based on color averaging results in a sharper picture as well as reduced flicker.
- ATI's exclusive "Composite Dot Crawl" freeze option for PAL and NTSC to improve picture quality.

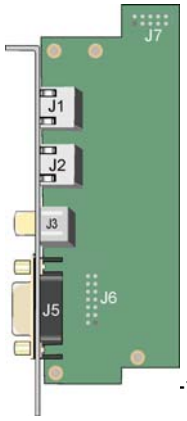
Signal Paths:
J2 is the second CRT and composite TV output on baseboard
J3 is the TV-out on the mezzanine
J5 is the CRT output on the mezzanine

Related Jumpers:
W6: when present, it disable the onboard video

BIOS Settings:
Main / Chipset / NorthBridge Configuration
- Primary Graphics Adapter
- On-board Primary Display
- TV-OUT Standard
- Graphics Aperture Size

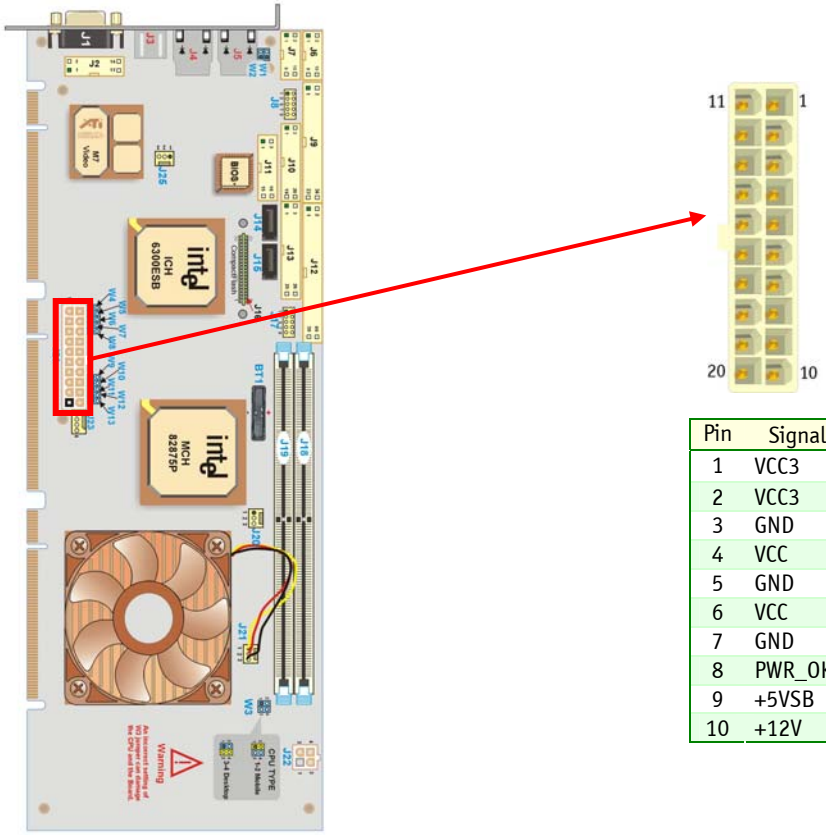
2.6.4 Video Mezzanine

The ePCI-201 comes with a video mezzanine to allow you to connect a second CRT. It also allows you to connect the secondary video on your TV with a RCA connector. The mezzanine also contains two USB connectors that connect to the J8 connector.



2.7 ATX Power Supply Control (J24)

If an ATX power supply is used, the SHB can control it either through its edge connector and the backplane or, if the SHB is used in standalone, through its ATX connector and hardware monitor connector pushbutton input.



Pin	Signal	Pin	Signal
1	VCC3	11	VCC3
2	VCC3	12	-12V
3	GND	13	GND
4	VCC	14	PS_ON#
5	GND	15	GND
6	VCC	16	GND
7	GND	17	GND
8	PWR_OK	18	N.C.
9	+5VSB	19	VCC
10	+12V	20	VCC

Signal Paths:

J24: ATX power connector for standalone use.

J10: Hardware monitor connector to connect the pushbutton in standalone use.

BIOS Settings:

- Main / Power
- Soft Off Support
- Restore on AC Power Loss

2.8 Debugging Features

2.8.1 Thermal Event LED

The red LED on the backside of the SHB turns ON when a CPU overheat condition or a CPU switcher overheat condition is detected. In overheat condition, the CPU runs at a speed slower than normal.

2.8.2 Bi-color Debug LED

The SHB has a bi-color LED (on the primary side of the board) that is very useful for debugging. Its meaning is context dependent as shown below.

Time	LED usage
During reset	RED and GREEN are ON. No blinking.
After reset, during the boot process	Postcode blinker (blinking) or bad CPU type indication (GREEN is OFF and RED is ON, no blinking). In the later case, the boot sequence is aborted.
After the boot process, while the operating system is loading.	GREEN reflects hard disk activity and RED is not used.
While the application software is running.	Application software does not use the LED. GREEN reflects hard disk activity and RED is not used.
	Application software uses the LED to display status information.

Software Usage:

Register 0x19A provide buffer control. See appendix C for details.

2.8.2.1 Post Code Blinker

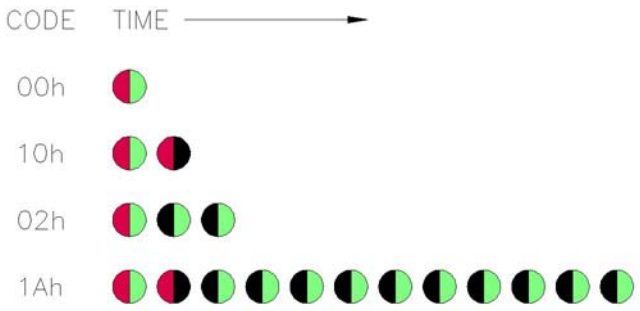
The postcode blinker circuit uses a blinking sequence to display the current post code value. This sequence restarts every time the post codes value changes. Since post codes changes all the time during a normal boot process, the blinker does not have enough time to complete its sequence and the debug LED blinks in a meaningless way.

If the boot process is successful, the post code value has no interest and the BIOS will automatically disable the post code blinker prior to operating system launch.

If the boot sequence fails or the CPU hangs, the postcode blinker will stay operational and will repeat indefinitely the last postcode blink sequence defined below.

1. Blink simultaneously RED and GREEN one time: start of the sequence
2. Blink RED “R” times while GREEN stays off. “R” range from 0 to 15.
3. Blink GREEN “G” times while RED stays off. “G” range from 0 to 15.
4. Repeat the sequence (go to step 1)

"R" is the first (most significant) digit of the post code value in hexadecimal while "G" is the second digit (i.e. post code value is RGh). Some examples are shown in the following figure.



2.8.2.2 Application Software Use of the Debug LED

A status LED can be very useful for software development and for system level troubleshooting. Consult register 0x19A description for software usage (appendix C).

2.8.3 Serial Post Codes

The 16-bit content of I/O addresses 80h and 81h is serialized into a proprietary protocol and output on the J23 connector. In manufacturing, Kontron uses a display board to deserialize and display the POST code value on 7-segment LED modules. This approach enables you to see POST codes before PCI initialization and avoid using a PCI POST code display board.

The display board is not offered with this product. It is used for manufacturing.

Postcodes can be a useful tool when debugging application software. If the display board interests you, please ask your Kontron representative for it.

2.8.4 Reset History

When an unwanted reset of the board occurs, it is of interest to know the reset source. The reset history circuit logs reset sources. There are two ways to obtain the reset history:

- Let the BIOS read and clear the reset history and display the reset source in the summary screen.
- The end-user software read and clear the reset history.

BIOS Settings:

- Main / Boot
- Quick Boot
- Show PCI Device List
- Main / Chipset
- Display & Clear Reset History

Software Usage:

Register 0x191 and 0x192. See appendix C for details.

2.9 System Management Features

2.9.1 Thermal Management

The SHB includes a user-defined temperature sensor, which provides thermal monitoring of the processor, using the Winbond W83627HF. In addition, the Pentium 4 includes an active thermal control circuit (TCC) that can automatically throttle the CPU clock when exceeding the maximum operating temperature.

A user application or software can read the CPU temperature.

BIOS Settings:
Main / Advanced / Hardware Health configuration
- Chipset Temperature
- CPU Die Temperature
- Video Temperature
- VRM Temperature

CPU overheating can happen if system fans fail. If overheated, the CPU will slow-down. If the CPU temperature keeps rising, the CPU switcher will be shutdown and the board power needs to be cycled to restart it.

Note:
If the CPU overheats, the CPU asserts the THERMTRIP# signal, which stops power.
To restart the board, cycle the power or the power button.

2.9.2 Power Supply Monitoring

All onboard supplies are monitored and the board is kept in reset if any voltage is out of specification.

Power supply voltages are also monitored and can be viewed in the BIOS setup.

BIOS Settings:
Main / Advanced / Hardware Health configuration
- Vcore
- Vcc3 3.3V
- Vcc 5V
- Vin 12V
- Vin –12V

2.9.3 Programmable Watchdog

A dual-stage digital watchdog timer with software programmable time-out period is available.

Following a reset of any source, the watchdog is disabled. Software enables the watchdog.

BIOS Settings:

Main / Chipset / SouthBridge

- Watchdog After POST

Software Usage:

- See Intel 6300ESB ICH Watchdog device for details.

2.10 Miscellaneous Features

In a PCI-only system, it can be expensive to add a couple of I/Os for LEDs, relays or switches. This simple I^2C controller goes to the backplane and to the hardware monitor connector. It's an easy and cost effective way to add some slow I/Os to a system.

2.10.1 Simple I2C Controller

Software Usage:

- See register 0x1A8 to 0x1AC in Appendix C for details.

2.10.2 Serial Number

A DS2401 silicon serial number comes standard on the ePCI-201. The number can be read from register 0x193. (See Appendix C).

3 Installing the board

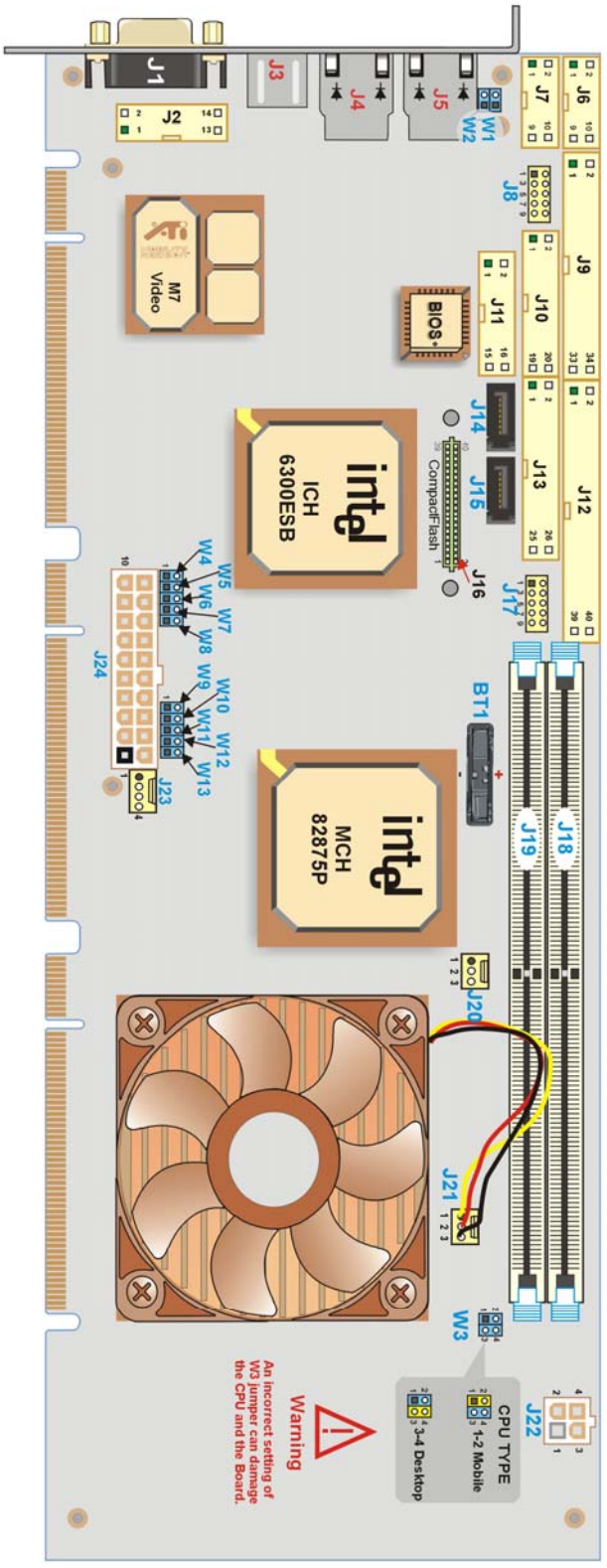
Contents

3.1 Setting Jumpers

3.1.1 Jumper Description

Description		
Serial COM2 Termination	Use these jumpers to connect or disconnect the termination resistors of Serial COM2 when set for RS-422/RS-485 operation mode 0.	**W1** **W2**
CPU Type Selection	Select the type of CPU that is installed on your board. Set the jumper to position 1-2 if it's a mobile and to position 3-4 if it's a desktop.	**W3**
Test Mode	This jumper is reserved for internal use only	**W4**
Console Redirection	When enabled, allows VT100 or ANSI terminal connection (data serial download from a remote computer).	**W5**
Onboard Video	Use this jumper to disable the onboard video feature.	**W6**
B_M66EN override	Disabled 66MHz PCI on bus B	**W7**
B_PCIXCAP override	Disabled PCI-X on Bus B	**W8**
CPU Front Side Bus Speed	Those jumpers are use to downclock the front side bus speed	**W9** **W10**
Clear CMOS	When inserted, all CMOS information is cleared.	**W11**
Battery Source connect the battery.	This jumper is used to disconnect the battery. Put the jumper in to	**W12**
ATX Control Override	Put the jumper in to turn Power supply ON.	**W13**

3.1.2 Setting Jumper & Locations



JUMPER SETTINGS
(* : Default Setting)

W1, W2 - COM2 Terminations		
RS-422/485 modes only	W1	W2
* Without termination resistors	Out	Out
With termination resistors	In	In

W3 - CPU Type Selection	
Mobile	1-2
* Desktop	3-4

This jumper is critical

W4 - Test Mode	
* Reserved	Out

W5 - Console Redirection	
* Disabled	Out
Enabled	In

W6 - Onboard Video	
* Enabled	Out
Disabled	In

W7 - B_M66EN override	
* Autodetect PCI Mode	Out
Prohibit PCI-66MHz operation	In

W8 - B_PCIXCAP override	
* Autodetect PCI-X Mode	Out
Prohibit PCI-X operation	In

W9, W10 - CPU Front Side Bus Speed		
	W9	W10
* Autodetect FSB Frequency	Out	Out

W11 - Clear CMOS	
* Normal Operation	Out
Clear CMOS Memory	In

W12 - Battery Source	
* Battery Disconnected	Out
Battery Connected	In

W13 - ATX Control Override	
* Normal Operation	Out
Bypass ATX	In

3.2 Processor

This product ships with the CPU installed but the heatsink is shipped beside. You will need to install it. Please refer to M8004_INST to get the installation procedure.

3.2.1 Processor Installation

Always use a processor listed in the approved CPU list below. For high power CPU, make sure that the system provides enough airflow.

Manufacturer Part Number	Description
RK80532PE056512 SL6PC	Intel Pentium 4 2.4GHz with a 533 MHz FSB
RK80532PE056512 SL6DV	Intel Pentium 4 2.4GHz with a 533 MHz FSB
RK80532PE072512 SL6PF	Intel Pentium 4 2.8GHz with a 533 MHz FSB
RK80546PG0801M SL7PM	Intel Pentium 4 Prescott 3.0GHz with a 800 MHz FSB
RK80546PG0801M SL7E4	Intel Pentium 4 Prescott 3.0GHz with a 800 MHz FSB

WARNING

STATIC ELECTRICITY

Since static electricity can cause damage to electronic devices, the following precautions should be taken:

1. Keep the board in its anti-static package, until you are ready to install it.

2. Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.

3. Handle the board by the edges.

WARNING

1. Once the CPU is installed you must handle the board carefully and hold it on the heatsink side.

2. The CPU Power cable must be installed on connector J21. If not installed, the board will not start.

WARNING

- Make sure jumper W3 is set to the proper CPU type. With some CPU type, a miss-configuration can damage the CPU.

3.3 Memory

Only use validated memory with this product. Currently recommended part numbers are:

Manufacturer Part Number	Description	Company
VM381L6423E-CCS (samsung)	DIMM ECC 512MB 400/PC3200	Virtium
VM381L6423E-CCM (micron)	DIMM ECC 512MB 400/PC3200	Virtium
VM381L2923E-CCS (samsung)	DIMM ECC 1GB 400/PC3200	Virtium
VM381L2923E-CCM (micron)	DIMM ECC 1GB 400/PC3200	Virtium
VM381L3223E-CCS (samsung)	DIMM ECC 256MB 400/PC3200	Virtium
VM381L3223E-CCM (micron)	DIMM ECC 256MB 400/PC3200	Virtium
UG732D7488KS-GJKA	DIMM ECC 256MB 400/PC3200	Unigen
UG764D7488LS-GJKA	DIMM ECC 512MB 400/PC3200	Unigen

Memory should have the following characteristics:

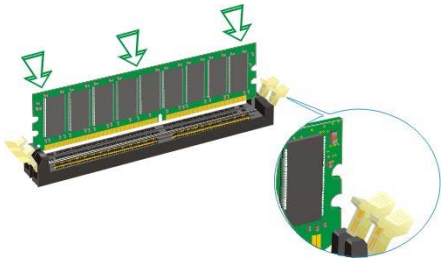
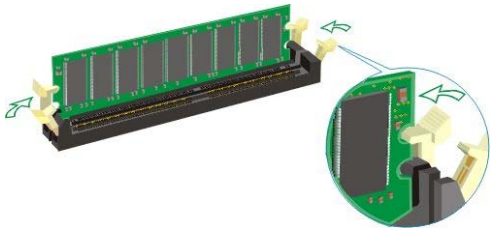
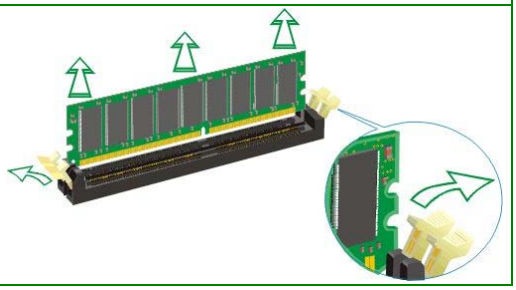
- DDR333 or DDR400
- 2.5V, un-buffered DIMMs only
- Single-sided or double-sided
- X8 or X16 configuration supported
- Serial Presence Detect (SPD) EEPROM
- 64-bit and 72-bit DIMMs supported

WARNING

Because static electricity can cause damage to electronic devices, take the following precautions:

- Keep the board in its anti-static package, until you are ready to install memory.
- Wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
- Handle the board by the faceplate or its edges.

3.3.1 Installing Memory

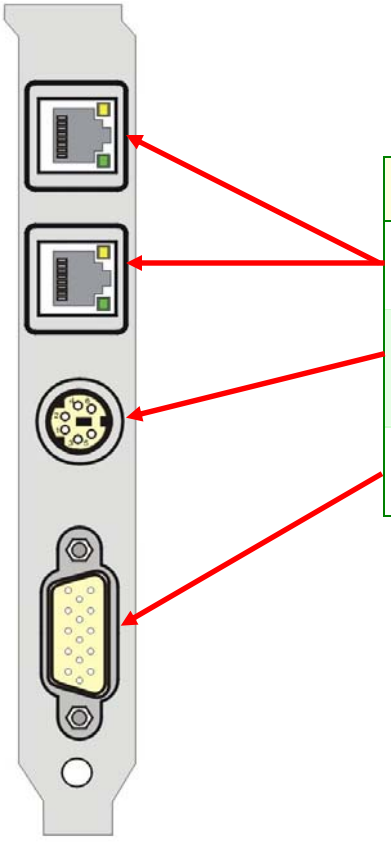
On an anti-static plane, place the board so that you are facing the DIMM sockets (the edge bracket must be located on the right).	
Insert the DIMM into any available socket, aligning the notches on the module with the socket's key inserts.	
Push vertically the DIMM into the socket until the retaining clips on each side snap on.	
Repeat these steps to populate the other sockets.	
To remove a DIMM from a socket, push down the retaining clips on each side of the socket, to release the module. Pull the module upward to remove.	

3.4 Onboard Interconnectivity

3.4.1 Onboard Connectors and Headers

Description	Connector	Comments	
Ethernet LAN2	J4	RJ-45 connector with built-in activity and link indicators	These connectors are located on the faceplate.
Ethernet LAN1	J5	RJ-45 connector with built-in activity and link indicators	
PS/2 Mouse/Keyboard	J3	6-pin PS/2 connector	
VGA	J1	15-pin DSUB female connector	
Secondary Video & TV-Out	J2	14-pin connector	
Serial Port 1	J6	10-pin connector	
Serial Port 2	J7	10-pin connector	
USB 0-1	J8	10-pin connector	
Floppy Disk	J9	34-pin connector	
Hardware Monitor	J10	16-pin connector	
Multifunction	J11	16-pin connector	
EIDE	J12	40-pin connector	
Parallel Port	J13	26-pin connector	
SATA 1	J14	7-pin SATA connector	
SATA 2	J15	7-pin SATA connector	
Compact Flash	J16	40-pin connector	
USB 2-3	J17	10-pin connector	
Memory Socket	J18-J19	DIMM 184-pin	
MCH Fan	J20	3-pin locking	
CPU Fan	J21	3-pin locking	
12V CPU Power	J22	4-pin connector	
POST Code	J23	4-pin locking	
ATX Power Connector	J24	20-pin connector	
Battery	BT1	CMOS backup battery socket	

3.4.2 Front Plate Connectors and Indicators

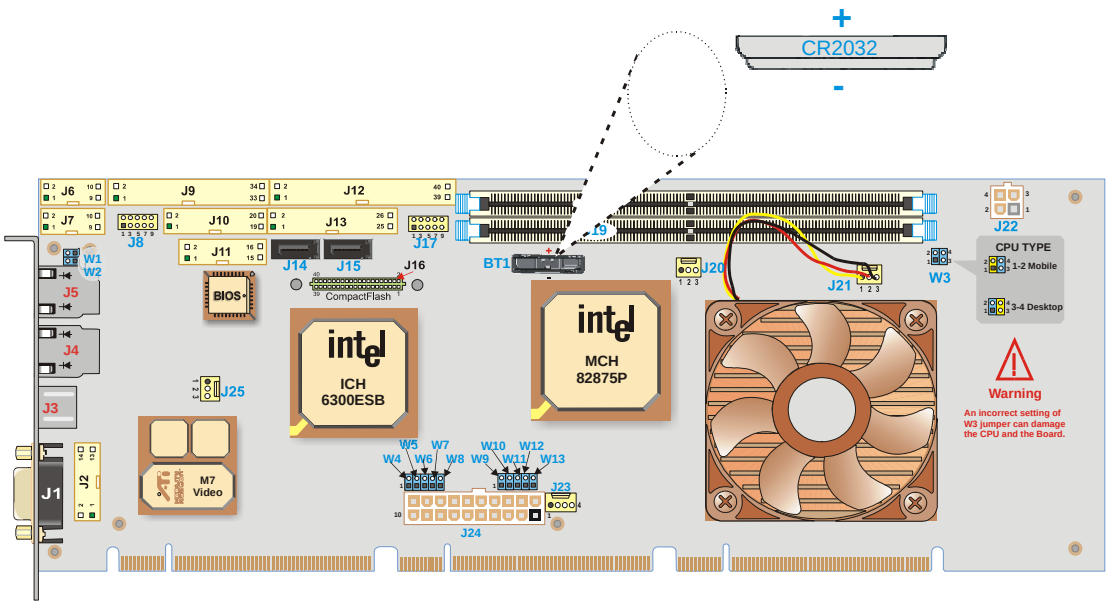


Connector	Description	Comments
J4, J5	LAN1 and LAN2	Ethernet RJ-45 connectors with built-in activity and link indicators
J3	PS/2 Mouse / Keyboard	PS/2 connector to connect the mouse and the keyboard via an adapter cable
J1	Video Connector	Standard 15-pin DSUB female connector

3.5 Backup Battery

An onboard 3V lithium battery provides back-up BIOS setup values and the real-time clock (RTC). When replacing, connect the battery as follows:

1. Remove the battery from the socket.
2. Insert a new battery in place with respect to the positive and negative location.



WARNING

There is a danger of explosion if you replace the battery incorrectly.
Replace the battery with the same or equivalent type recommended by the manufacturer.
Dispose of used batteries according to the manufacturer's instructions.

3.5.1 Operation and Preventative Maintenance

The operational battery voltage must be between 2.4 and 3.0 volts.

When the board is stored in its original package, replace the battery if it falls below 2.4 volts.

For preventive operational maintenance, verify the battery voltage after four years. After that, check the safety voltage more often. Battery life expectancy depends upon board use.

- Kontron ordering MRP: 100-004
- Battery description: CR2032 3V battery

4 Software Setup

Contents

4.1 AMI BIOS Setup Program

All relevant information for operating the board and connected peripherals is stored in the CMOS memory. A battery-backed up memory holds this information when the board is powered off, the BIOS Setup program is required to make changes to the setup.

4.1.1 Accessing the BIOS Setup Utility

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the ePCI-201 SHB. It uses the AMI Setup program, a setup utility in flash memory that is accessed by pressing the <DELETE> key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

CAUTION

Before modifying CMOS setup parameters, ensure that the battery protection tape is removed to enable the CMOS battery back up.

To run the AMI Setup program incorporated in the ROM BIOS:

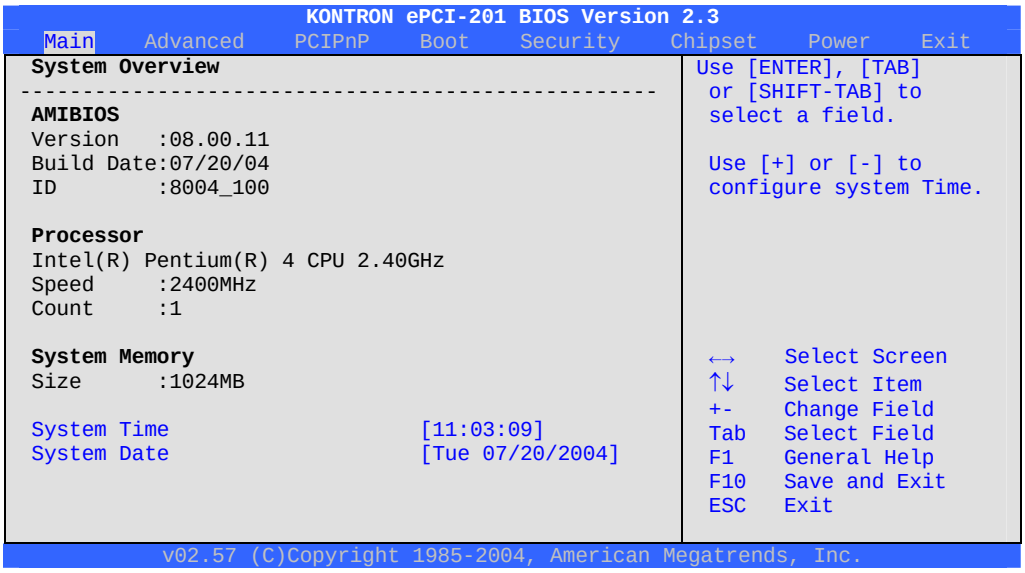
- Turn on or reboot the system.
- When you get the following messages, hit <DELETE> key (or F4 on Remote Keyboard) to enter SETUP.

AMIBIOS(C)2003 American Megatrends, Inc.
KONTRON ePCI-201 BIOS Version 2.0
CPU : Mobile Intel(R) Pentium(R) 4 CPU 3.20GHz
Speed : 3.20 GHz

Press DEL to run Setup (F4 on Remote Keyboard)
Press F11 for BBS POPUP (F3 on Remote Keyboard)
DDR Frequency 333 Mhz, Dual-Channel

(C) American Megatrends, Inc.
64-0100-000001-00101111-092804-CANTWOOD-8004_100-Y2KC

The main menu of the AMI BIOS CMOS Setup Utility appears on the screen.



If you are not sure about a setting, refer to the list of default values. The list is provided if you wish to restore a setting to its default value. Loading the SETUP defaults affects all parameters and resets options that have been altered.

Setup Default values provide **optimum performance** settings for all devices and system features.

Note:
The CMOS setup option described in this section is based on **BIOS Version 2.3**. The options and default settings may change in a new BIOS release.

CAUTION

These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

4.1.2 Menu Bar

The Menu Bar at the top of the window lists these selections:

Menu Selection	Description
Main	Use this menu for basic system configuration.
Advanced	Use this menu to set the Advanced Features available on your system.
PCIPnP	Use this menu to configure PCI and PnP features.
Boot	Use this menu to determine the booting device order.
Security	Use this menu to configure Security features.
Chipset	Use this menu to configure chipset features.
Power	Use this menu to configure Power Management features and system monitoring.
Exit	Use this menu to choose Exits option.

Use the left and right ← and → arrows keys to make a selection.

4.1.2.1 Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates.

Key	Function
<F1>	General Help windows (see 4.1.2.2).
<Esc>	Exit this menu.
← → arrow keys	Select a different menu.
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to top or bottom of window.
<->	Select the Previous Value for the field.
<+>	Select the Next Value for the field.
<F2> and <F3>	Change colors used in Setup.
<F7>	Discard the changes for all menus.
<F8>	Load the Failsafe Default Configuration values for all menus.
<F9>	Load the Optimal Default Configuration values for all menus.
<F10>	Save and exit.
<Enter>	Execute Command, display possible values for this field or Select the sub-menu.

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-or-minus value keys to select a value for that field. To save value commands in the Exit Menu, saves the values displayed in all menus.

To display a submenu, use the arrow keys to move the cursor to the submenu you want. Then press <Enter>. A pointer ( ) marks all sub-menus.

4.1.2.2 Field Help Window

The help window on the right side of each menu displays the help text for the selected field. It updates as you move the cursor to each field.

4.1.2.3 General Help Windows

Pressing <F1>on any menu brings up the General Help window that describes the legend keys and their alternates:

General Help	
←→ Select Screen	↑↓ Select Item
+- Change Option/Field	Enter Go to Sub Screen
PGDN Next Page	PGUP Previous Page
HOME Go to Top of Screen	END Go to Bottom of Screen
F2/F3 Change Colors	F7 Discard Changes
F8 Load Failsafe Defaults	F9 Load Optimal Defaults
F10 Save and Exit	ESC Exit
[OK]	

4.1.2.4 Main Menu Selection

The scroll bar at the right of any window indicates that there is more than one page of information in the window. You can make the following selections in the Main Menu itself. Use submenus for other selections.

Feature	Options	Description
Version	N/A	AMIBIOS Core version used with this BIOS.
Build Date	N/A	Build Date.
ID	N/A	OEM Identification code.
Processor	N/A	Displays CPU Brand Name (show maximum CPU Speed available).
Speed	N/A	Displays current CPU Speed.
System Memory	N/A	Displays the amount of RAM memory detected during boot up.
System Time	HH:MM:SS	Set system time.
System Date	MM/DD/YYYY	Set system date.

4.1.2.5 Advanced Menu Selection

Feature	Options	Description
CPU Configuration	This is a Sub-Menu.	Additional setup options to configure CPU settings.
IDE Configuration	This is a Sub-Menu.	Additional setup options to configure IDE devices.
Floppy Configuration	This is a Sub-Menu.	Floppy Drive configuration.
SuperIO Configuration	This is a Sub-Menu.	Configure SuperIO Chipset Win627.
Hardware Health Configuration	This is a Sub-Menu.	Configure and Monitor Hardware Health.
ACPI Configuration	This is a Sub-Menu.	Configure Advanced ACPI.
Event Log Configuration	This is a Sub-Menu.	Read, Clear or View Event Log statistics..
MPS Configuration	This is a Sub-Menu.	Configure the Multi-Processor Table.
On-Board Device Configuration	This is a Sub-Menu.	Peripheral configuration.
SMBIOS Configuration	This is a Sub-Menu.	SMBIOS configuration.
Remote Access Configuration	This is a Sub-Menu.	Additional options to configure console.
USB Configuration	This is a Sub-Menu	Configure the USB Support.

4.1.2.5.1 CPU Configuration

Feature	Options	Description
Module Version	N/A	Internal AMI module version used for CPU support.
Manufacturer	N/A	CPU Manufacturer, always Intel.
CPU Brand String	N/A	Displays CPU Brand Name (show maximum CPU Speed available).
Frequency	N/A	Displays current CPU Speed.
FSB Speed	N/A	Display the current Front Side Bus Speed used by the CPU.
Cache L1	N/A	Size of the Internal CPU L1 Cache.
Cache L1	N/A	Size of the Internal CPU L1 Cache.
Cache L3 (hidden if not supported)	N/A	Size of the Internal CPU L3 Cache.
Ratio Status	N/A	Will display if CPU ratio is locked or unlocked and the minimum/maximum ratios available.
Ratio CMOS Setting	Varies. Values available are based on minimum/maximum ratios available.	Will display if CPU ratio is locked or unlocked and the minimum/maximum ratios available.
Max CPUID Value Limit	Disabled Enabled	This should be enabled in order to boot legacy OSes that cannot support CPUs with extended CPUID functions.
No-Execute Memory Protection (hidden if not supported)	Disabled Enabled	This should be enabled in order to enable or disable the NX Support. Need Prescott E0 stepping (CPUID F41) or above. Execute Disable Bit capability is an enhancement to 32-bit Intel® architecture. An IA-32 processor with Execute Disable Bit capability can protect data pages against being used by malicious software to execute code. The processor provides page protection in either of the following modes: - Legacy protected mode, if Physical Address Extension (PAE) is enabled. - IA-32e mode, when Intel® Extended Memory 64 Technology (Intel® EM64T) is enabled. Note that entering IA-32e mode requires enabling PAE. While the Execute Disable Bit capability does not introduce new instructions, it does require operating systems to operate in a PAE-enabled environment and to establish a page-granular protection policy for memory.
Hardware Prefetcher (hidden if not supported)	Disabled Enabled	This should be enabled in order to enable or disable the Hardware Prefetcher Disable Feature. Need Prescott (CPUID F30) or above.
Adjacent Cache Line Prefetch (hidden if not supported)	Disabled Enabled	This should be enabled in order to enable or disable the Adjacent Cache Line Prefetch Disable Feature. Need Prescott (CPUID F30) or above.
Hyper-Threading technology (hidden if not supported)	Disabled Enabled	Set Enabled for Windows XP and Linux 2.4.x (OS optimized for Hyper-Threading Technology).

Intel(R) SpeedStep(tm) Tech.	Minimum Speed Maximum Speed	[Maximum Speed]: CPU speed is set to Maximum Speed (high power, high frequency). [Minimum Speed]: CPU speed is set to Minimum Speed (low power, low frequency).

4.1.2.5.2 IDE Configuration

Feature	Options	Description
IDE Configuration	Disabled P-ATA Only S-ATA Only P-ATA & S-ATA	Select IDE Mode. P-ATA Only: 4 P-ATA & 2 S-ATA S-ATA Only: 2 S-ATA P-ATA & S-ATA: 2 P-ATA & 2 S-ATA
S-ATA Running Enhanced Mode (P-ATA Only)	Yes No	Set S-ATA Running Enhanced Mode.
P-ATA Channel Selection (P-ATA Only)	Primary Secondary Both	Select P-ATA Channel.
S-ATA Ports Definition (P-ATA Only)	P0-3rd./P1-4th. P0-4th./P1-3rd.	Select S-ATA Ports.
S-ATA Ports Definition (S-ATA Only)	P0-1st./P1-2nd. P0-2nd./P1-1st.	Select S-ATA Ports.
Combined Mode Option (P-ATA & S-ATA)	P-ATA 1st Channel S-ATA 1st Channel	Select Combined Mode.
S-ATA Ports Definition (P-ATA & S-ATA)	P0-Master/P1-Slave P0-Slave/P1-Master	Select S-ATA Ports.
Primary IDE Master	This is a sub-menu	
Primary IDE Slave	This is a sub-menu	
Secondary IDE Master	This is a sub-menu	
Secondary IDE Slave	This is a sub-menu	
Third IDE Master	This is a sub-menu	
Fourth IDE Master	This is a sub-menu	
Hard Disk Write Protect	Disabled Enabled	Disables/Enables device write protection. This will be effective only if device is accessed through BIOS.
IDE Detect Time Out (sec)	0, 5, 10, 15, 20, 25, 30, 35	Select the time out value for detecting ATA/ATAPI device(s)

4.1.2.5.2.1 Primary IDE Master

Feature	Options	Description
Device Vendor Size LBA Mode Block Mode PIO Mode Async DMA Ultra DMA S.M.A.R.T.	N/A	This is a list of modes and features supported by the drive, not how it is setup.
Type	Not installed Auto CD/DVD ARMD	Select the type of device connected to the system.
LBA/Large Mode	Disabled Auto	Disabled: Disables LBA Mode. Auto: Enables LBA Mode if the device supports it and the device is not already formatted with LBA Mode3 disabled
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: the data transfer from and to the device occurs one sector at a time. Auto: the data transfer from and to the device occurs multiple sector at a time if the device supports it.
PIO Mode	Auto 0 1 2 3 4	Select PIO Mode.
DMA Mode	**Auto** SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4 UDMA5 UDMA6	Select DMA Mode. Auto: Auto detect SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn UDMAn: UltraDMAn
S.M.A.R.T.	Auto Disabled Enabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology
32Bit Data Transfer	Disabled Enabled	Enable/Disabled 32-bit Data Transfer.

4.1.2.5.2.2 Primary IDE Slave

Feature	Options	Description
Device Vendor Size LBA Mode Block Mode PIO Mode Async DMA Ultra DMA S.M.A.R.T.	N/A	This is a list of modes and features supported by the drive, not how it is setup.
Type	Not installed Auto CD/DVD ARMD	Select the type of device connected to the system.
LBA/Large Mode	Disabled Auto	Disabled: Disables LBA Mode. Auto: Enables LBA Mode if the device supports it and the device is not already formatted with LBA Mode3 disabled
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: the data transfer from and to the device occurs one sector at a time. Auto: the data transfer from and to the device occurs multiple sector at a time if the device supports it.
PIO Mode	Auto 0 1 2 3 4	Select PIO Mode.
DMA Mode	**Auto** SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4 UDMA5 UDMA6	Select DMA Mode. Auto: Auto detect SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn UDMAn: UltraDMAn
S.M.A.R.T.	Auto Disabled Enabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology
32Bit Data Transfer	Disabled Enabled	Enable/Disabled 32-bit Data Transfer.

4.1.2.5.2.3 Secondary IDE Master

Feature	Options	Description
Device Vendor Size LBA Mode Block Mode PIO Mode Async DMA Ultra DMA S.M.A.R.T.	N/A	This is a list of modes and features supported by the drive, not how it is setup.
Type	Not installed Auto CD/DVD ARMD	Select the type of device connected to the system.
LBA/Large Mode	Disabled Auto	Disabled: Disables LBA Mode. Auto: Enables LBA Mode if the device supports it and the device is not already formatted with LBA Mode3 disabled
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: the data transfer from and to the device occurs one sector at a time. Auto: the data transfer from and to the device occurs multiple sector at a time it the device supports it.
PIO Mode	Auto 0 1 2 3 4	Select PIO Mode.
DMA Mode	**Auto** SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4 UDMA5 UDMA6	Select DMA Mode. Auto: Auto detect SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn UDMAn: UltraDMAn
S.M.A.R.T.	Auto Disabled Enabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology
32Bit Data Transfer	Disabled Enabled	Enable/Disabled 32-bit Data Transfer.

4.1.2.5.2.4 Secondary IDE Slave

Feature	Options	Description
Device Vendor Size LBA Mode Block Mode PIO Mode Async DMA Ultra DMA S.M.A.R.T.	N/A	This is a list of modes and features supported by the drive, not how it is setup.
Type	Not installed Auto CD/DVD ARMD	Select the type of device connected to the system.
LBA/Large Mode	Disabled Auto	Disabled: Disables LBA Mode. Auto: Enables LBA Mode if the device supports it and the device is not already formatted with LBA Mode3 disabled
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: the data transfer from and to the device occurs one sector at the time. Auto: the data transfer from and to the device occurs multiple sector at a time it the device supports it.
PIO Mode	Auto 0 1 2 3 4	Select PIO Mode.
DMA Mode	**Auto** SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4 UDMA5 UDMA6	Select DMA Mode. Auto: Auto detect SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn UDMAn: UltraDMAn
S.M.A.R.T.	Auto Disabled Enabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology
32Bit Data Transfer	Disabled Enabled	Enable/Disabled 32-bit Data Transfer.

4.1.2.5.2.5 Third IDE Master

Feature	Options	Description
Device Vendor Size LBA Mode Block Mode PIO Mode Async DMA Ultra DMA S.M.A.R.T.	N/A	This is a list of modes and features supported by the drive, not how it is setup.
Type	Not installed Auto CD/DVD ARMD	Select the type of device connected to the system.
LBA/Large Mode	Disabled Auto	Disabled: Disables LBA Mode. Auto: Enables LBA Mode if the device supports it and the device is not already formatted with LBA Mode3 disabled
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: the data transfer from and to the device occurs one sector at the time. Auto: the data transfer from and to the device occurs multiple sector at a time it the device supports it.
PIO Mode	Auto 0 1 2 3 4	Select PIO Mode.
DMA Mode	**Auto** SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4 UDMA5 UDMA6	Select DMA Mode. Auto: Auto detect SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn UDMAn: UltraDMAn
S.M.A.R.T.	Auto Disabled Enabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology
32Bit Data Transfer	Disabled Enabled	Enable/Disabled 32-bit Data Transfer.

4.1.2.5.2.6 Fourth IDE Master

Feature	Options	Description
Device Vendor Size LBA Mode Block Mode PIO Mode Async DMA Ultra DMA S.M.A.R.T.	N/A	This is a list of modes and features supported by the drive, not how it is setup.
Type	Not installed Auto CD/DVD ARMD	Select the type of device connected to the system.
LBA/Large Mode	Disabled Auto	Disabled: Disables LBA Mode. Auto: Enables LBA Mode if the device supports it and the device is not already formatted with LBA Mode3 disabled
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: the data transfer from and to the device occurs one sector at a time. Auto: the data transfer from and to the device occurs multiple sector at a time it the device supports it.
PIO Mode	Auto 0 1 2 3 4	Select PIO Mode.
DMA Mode	**Auto** SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4 UDMA5 UDMA6	Select DMA Mode. Auto: Auto detect SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn UDMAn: UltraDMAn
S.M.A.R.T.	Auto Disabled Enabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology
32Bit Data Transfer	Disabled Enabled	Enable/Disabled 32-bit Data Transfer.

4.1.2.5.3 Floppy Configuration

Feature	Options	Description
Floppy A	Disabled 1.44 MB 3 ½	Select the type of floppy drive connected to the system.

4.1.2.5.4 SuperIO Configuration

Feature	Options	Description
OnBoard Floppy Controller	Disabled Enabled	Allows BIOS to Enable or Disable Floppy Controller
Serial Port1 Address	Disabled 3F8/IRQ4 3E8/IRQ4 2E8/IRQ3	Allows BIOS to Select Serial Port1 Base Address.
Serial Port2 Address	Disabled 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Allows BIOS to Select Serial Port2 Base Address.
Serial Port2 Interface	RS-422 RS-485 RS-232	Allows BIOS to Select Transmitters/Receivers Interface Circuits for Serial Port2.
Reset on a Serial Port Break	Never Reset Serial Port 1 Serial Port 2	Allows Com Port Break sequence to Reset the system.
Parallel Port Address	Disabled 378 278 3BC	Allow BIOS to Select Parallel Port Base Address.
Parallel Port Mode	Normal Bi-Directionnal ECP EPP ECP & EPP	Allows BIOS to Select Parallel Port Mode.
ECP Mode DMA Channel	DMA0 DMA1 DMA3	Allow BIOS to Select Parallel Port ECP DMA.
Parallel Port IRQ	IRQ5 IRQ7	Allow BIOS to Select Parallel Port IRQ

4.1.2.5.5 Hardware Health Configuration

Feature	Options	Description
H/W Health Function	Disabled Enabled	Enables Hardware Health Monitoring Device.
H/W External configuration	This is a sub-menu	
Chipset Temperature		
CPU Die Temperature		
Video Temperature		
VRM Temperature		Voltage Regulator Module Temperature. If VRM is too hot, CPU throttling will be initiated and the Thermal Event LED light.
Fan CPU Speed		Present only with if J21 is used.
Fan Chipset Speed		Present only with if J20 is used.
Fan Video Speed		Present only with if J25 is used.
Vcore		
Vcc3 3.3V		
Vcc 5V		
Vin 12V		
Vin –12V		
Vbat		

4.1.2.5.5.1 H/W External configuration

Feature	Options	Description
FAN 1, Tics Per Turn	**2 Tics,** 4 Tics	Number of tics per turn (depends in fan type, typically 2 or 4)
FAN 2, Tics Per Turn	**2 Tics,** 4 Tics	Number of tics per turn (depends in fan type, typically 2 or 4)
FAN 3, Tics Per Turn	**2 Tics,** 4 Tics	Number of tics per turn (depends in fan type, typically 2 or 4)
FAN 4, Tics Per Turn	**2 Tics,** 4 Tics	Number of tics per turn (depends in fan type, typically 2 or 4)
FAN 5, Tics Per Turn	**2 Tics,** 4 Tics	Number of tics per turn (depends in fan type, typically 2 or 4)
FAN 6, Tics Per Turn	**2 Tics,** 4 Tics	Number of tics per turn (depends in fan type, typically 2 or 4)
FAN 1 Speed	Speed in RPM	
FAN 2 Speed	Speed in RPM	
FAN 3 Speed	Speed in RPM	
FAN 4 Speed	Speed in RPM	
FAN 5 Speed	Speed in RPM	
FAN 6 Speed	Speed in RPM	

4.1.2.5.6 ACPI Settings

Feature	Options	Description
Advanced ACPI Configuration	This is a sub-menu	Advanced ACPI Configuration settings Use this section to configure additional ACPI options
Chipset ACPI Configuration	This is a sub-menu	Chipset ACPI related configuration settings

4.1.2.5.6.1 Advanced ACPI Configuration

Feature	Options	Description
ACPI 2.0 Features	No Yes	Enable RSDP pointers to 64-bit Fixed System Description Tables.
ACPI APIC support	Disabled Enabled	Include ACPI APIC table Pointer to RSDT pointer list.
AMI OEMB table	Disabled Enabled	Include OEMB table pointer to R(X)SDT pointer List

4.1.2.5.6.2 Chipset ACPI Configuration

Feature	Options	Description
APIC ACPI SCI IRQ	Disabled Enabled	Enable/Disable APIC ACPI SCI IRQ. Disabled will select IRQ 9, Enabled IRQ 20

4.1.2.5.7 Event Log Configuration

Feature	Options	Description
View Event Log		View all unread events on the Event Log
Mark all Events as read		Mark all unread events as read.
Clear Event Log		Discard all events in the Event log.
ECC Event logging	Disabled Enabled	Enables or Disables ECC Event logging

4.1.2.5.8 MPS Configuration

Feature	Options	Description
MPS Revision	1.1 1.4	Configure the Multiprocessor specifications (MPS) revision level. Some operating systems will require revision 1.1 for compatibility reasons.

4.1.2.5.9 On-board Devices Configuration

Feature	Options	Description
On-board Ethernet 1 Controller	Disabled Enabled	Enables/ disables on-board Ethernet 1 controller
Option ROM	Disabled Enabled	Initialize device expansion ROM
On-board Ethernet 2 Controller	Disabled Enabled	Enables/ disables on-board Ethernet 2 controller

4.1.2.5.10 Smbios Configuration

Feature	Options	Description
Smbios SMI Support	Disabled Enabled	SMBIOS SMI Wrapper support for PnP Func 50h-54h.

4.1.2.5.11Remote Access Configuration

Feature	Options	Description
Console Redirection Jumper	Installed Not Installed	This indicates the state of the Console Redirection jumper (W5). If Installed, "Remote Access" will be forced enabled, even if the option "Remote Access" is set to Disabled. In that case, if the jumper is removed, the "Remote Access" will be disabled.
Remote Access	Disabled Enabled	Select Remote Access Type
Serial Port number	COM1 COM2	Select Serial Port for console redirection Make sure the selected port is enabled
Serial Port Mode	115200 8,n,1 57600 8,n,1 38400 8,n,1 19200 8,n,1 09600 8,n,1	
Flow Control	None Hardware Software	
Redirection After BIOS POST	Disabled Boot Loader Always	Disable: Turns off the redirection after POST Boot Loader: Redirection is active during POST and during Boot Loader. Always: Redirection is always active. (Some OS may not work if set to Always)
Terminal Type	ANSI VT100 VT-UTF8	Select the target terminal type
VT-UTF8 Combo Key Support	Disabled Enabled	Enable VT-UTF8 combination key Support for ANSI/VT100 terminals.
Serial Redirection	This is a sub-menu	

4.1.2.5.11.1 Serial Redirection

Feature	Options	Description
Sredir memory display delay	None, 1sec, 2 sec, 4 sec	Gives the delay in seconds to display memory information of the serial redirection.
Delay to add for display	None, 1sec, 2 sec, 4 sec	Add a delay in seconds to display different screen information at different POST.

4.1.2.5.12USB Configuration

Feature	Options	Description
USB Devices Enabled:	Varies	List the devices detected.
USB Function	Disabled 2 USB Ports All USB Ports	Enables USB Host controllers.
Legacy USB Support	Disabled Enabled Auto	Enables Support for legacy USB. Auto option disables legacy support if no USB device are connected
USB 2.0 Controller	Enabled Disabled	Enables the USB 2.0 controller
USB 2.0 Controller Mode	FullSpeed HiSpeed	Configure the USB 2.0 Controller in HiSpeed (480Mbps) or FullSpeed (12Mbps)
BIOS EHCI Hand-Off	Disabled Enabled	This is a workaround for OS without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.
USB Mass Storage Device Configuration	This is a sub-menu	Configure the USB Mass Storage Class Devices. (Present only if at least one device is detected)

4.1.2.5.12.1 USB Mass Storage Device Configuration

Feature	Options	Description
USB Mass Storage Reset Delay	10 Sec 20 sec 30 sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Device #1-6		Mass Storage Device identification
Emulation Type (for each devices)	Auto Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

4.1.2.6 PCIPnP

Feature	Options	Description
Clear NVRAM	No Yes	Clear NVRAM during System Boot This is information stored in a Flash sector (like the Event Log).
Plug & Play O/S	No Yes	No: lets the BIOS configure all the devices in the system. Yes: lets the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.
PCI Latency Timer	32 64 93 128 160 192 22 248	Value in units of PCI clocks for PCI device latency timer register.
Allocate IRQ to PCI VGA	Yes No	Yes: Assings IRQ to PCI VGA card if card requests IRQ No: Does not assign IRQ to PCI VGA card even if card requests an IRQ.

4.1.2.7 Boot

Feature	Options	Description
Boot Setting Configuration	This is a sub-menu	Configure Settings during System Boot.
Boot Device Priority	This is a sub-menu	Specifies the Boot Device Priority sequence.
Hard Disk Drives	This is a sub-menu	Specifies the Boot Device Priority sequence from available Hard Drives.
Removable Drives	This is a sub-menu	Specifies the Boot Device Priority sequence from available Removable Drives.
CD/DVD Drives	This is a sub-menu	Specifies the Boot Device Priority sequence from available CD/DVD Drives.

4.1.2.7.1 Boot Settings Configuration

Feature	Options	Description
Quick Boot	Disabled Enabled	Allows BIOS to skip certain tests while booting. The System Configure Summary will be skipped. This will decrease the time needed to boot the system.
Show PCI Device List (hidden if Quick Boot is enabled)	Disabled Enabled	Controls the display of the PCI Device List in the System Configuration Summary.
Quiet Boot	Disabled Enabled	Disabled: Display normal POST messages. Enabled: Display OEM Logo instead of POST messages. If Console Redirection is Enabled (jumpers or Setup), it will automatically be put back to Disabled.
Hot Key Help Over Logo (hidden if Quiet Boot is disabled)	Disabled Enabled	Display Hot Key Help Over Logo.
Add-On ROM Display Mode	Force BIOS Keep Current	Set display mode for Option ROM
Bootup Num-Lock	On Off	Select Power-on state for Num-Lock
PS/2 Mouse Support	Disabled Enabled Auto	Select support for PS/2 Mouse.
Wait For F1 If error	Disabled Enabled	Wait for F1 key to be pressed if error occurs
Hit DEL Message Display	Disabled Enabled	Display "Press DEL to run Setup" in POST.
Interrupt 19 Capture	Disabled Enabled	Allows option ROM to trap interrupt 19. This is required by some PCI cards that provide a ROM based setup utility.
Retry Boot Sequence	Disabled Enabled	Enable this option to retry the Boot Sequence (infinite retries)
Save CMOS in FLASH	Disabled Enabled	Saving CMOS memory content into Flash Memory will prevent loosing CMOS options when Battery fails.
Serial Transmitter Output	POST Codes Status Bits	The Serial Transmitter can output POST Codes or output LANs LEDs status and other status bits. Consult User<s Guide for details.

4.1.2.7.2 Boot Device Priority

Feature	Options	Description
1st Boot Device	Varies	Specifies the boot sequence from the available devices. A device enclosed in parenthesis has been disabled in the corresponding type menu.
Nth Boot Device	Varies	Number of entries will vary based on system configuration.

Note: The easiest way to select the desired priority is to select the 1st Boot Device, Hit Enter and choose a device from the options presented. Repeat this process for 2nd to Nth Boot Devices.

4.1.2.7.3 Hard Disk Drives

Feature	Options	Description
1st Drive	Varies	Specifies the boot sequence from the available devices.
Nth Drive	Varies	Number of entries will vary based on system configuration.

Note: The easiest way to select the desired priority is to select the 1st Drive, Hit Enter and choose a device from the options presented. Repeat this process for 2nd to Nth Drives.

4.1.2.7.4 Removable Drives

Feature	Options	Description
1st Drive	Varies	Specifies the boot sequence from the available devices.
Nth Drive	Varies	Number of entries will vary based on system configuration.

Note: The easiest way to select the desired priority is to select the 1st Drive, Hit Enter and choose a device from the options presented. Repeat this process for 2nd to Nth Drives.

4.1.2.7.5 CD/DVD Drives

Feature	Options	Description
1st Drive	Varies	Specifies the boot sequence from the available devices.
Nth Drive	Varies	Number of entries will vary based on system configuration.

Note: The easiest way to select the desired priority is to select the 1st Drive, Hit Enter and choose a device from the options presented. Repeat this process for 2nd to Nth Drives.

4.1.2.8 Security

Feature	Options	Description
Change Supervisor Password		Install or change the password.
User Access Level	No Access View Only Limited Full Access	LIMITED: allows only limited fields to be changed such as Date and Time. NO ACCESS: preventsUser access to the Setup Utility. VIEW ONLY: allows access to the Setup Utility but the fields can not be changed. FULL: allows any field to be changed except the Supervisor password.
Change User Password		Install or change the password.
Clear User Password		Immediately clears the User Password.
Password Check	Setup Always	Setup: Check password while invoking setup. Always: Check password while invoking setup as well as on each boot.
Boot Sector Virus Protection	Disabled Enabled	Enable/Disable Boot Sector Virus Protection.
Chassis Intrusion	Disabled, Enabled	Enables/disables detection of Chassis Intrusion.
Secured Chassis (Hidden when Chassis Intrusion is disabled)	Disabled, Enabled	If set to Enabled and a Chassis Intrusion is detected, the user is required to enter SETUP and set the option "Reset Chassis Intrusion" to "Yes", before the system is allowed to complete the boot.
Reset Chassis Intrusion (Hidden when Chassis Intrusion is disabled)	No, Yes	Selecting 'Yes' will reset the Chassis Intrusion circuitry on the next boot.

4.1.2.9 Chipset

Feature	Options	Description
NorthBridge Configuration	This is a sub-menu	Options for NB
SouthBridge Configuration	This is a sub-menu	Options for SB
Display & Clear Reset History	Disabled Enabled	When Enabled, displays in the system Configuration Summary the type of Reset detected by the FPGA. The History bits in FPGA will also be cleared.
FPGA IRQ	Disabled IRQ3 IRQ4 IRQ5 IRQ7 IRQ10 IRQ11	Select FPGA IRQ for I2C Controller. Fan Fault and External Fault events. WARNING: Avoid IRQ conflict with SuperIO devices.

4.1.2.9.1 NorthBridge Configuration

Feature	Options	Description
DRAM Frequency	266 MHz 333 MHz 400 MHz Auto	Select DRAM Frequency.
Configure DRAM Timing by SPD	Disabled Enabled	Enabled: Lets BIOS program memory timings from SPD data. Disabled: User need to select appropriate timings. The following 5 options will available .
DRAM CAS# Latency	2.5 2 3	Select DRAM CAS# Latency
DRAM RAS# Precharge	4 Clocks 3 Clocks 2 clocks	Select DRAM RAS# Precharge
DRAM RAS# to CAS# Delay	4 Clocks 3 Clocks 2 Clocks	Select DRAM RAS# to CAS# Delay.
DRAM Precharge Delay	8 Clocks 7 Clocks 6 Clocks 5 Clocks	Select DRAM Precharge Delay.
DRAM Burst Length	4 8 (only if single-channel)	Select DRAM Burst Length. Forced to 4 when used in Dual-Channel.
DRAM Integrity Mode	Disabled ECC	Enable/Disable DRAM Integrity Mode.
Primary Graphics Adapter	On-Board External	Select which graphic controller to use as the primary boot device.
On-Board Primary Display	CRT1 CRT1/CRT2 CRT1/TV-OUT TV-OUT	On-board Primary Display will only work for device(s) attached to the on-board ATI video Chip. Usage of external video card as Primary Adapter will void this option.
TV-Out Standard	NTSC PAL	On-board TV-OUT Standard to use at Boot time. Usage of external video card as primary adapter will void this option.
Graphics Aperture Size	4MB 8MB 16MB 32MB 64MB 128MB 256MB	Size of the AGP Aperture

4.1.2.9.2 SouthBridge Configuration

Feature	Options	Description
Watchdog After POST	Disabled 16 seconds 1 minute 4 minutes	Enables the watchdog circuit after the POST sequence. Application software must refresh the Watchdog to prevent System Reset. The ePCI-201 uses the SouthBridge Watchdog (PCI device: Bus 0, Device 29, Function 4).

4.1.2.10 Power

Feature	Options	Description
Soft Off Support	Disabled Enabled	Enable this option to use the Power Button feature. Disable this option when the Power Supply Mode is set in "Rocker Switch Mode" or in "Power Supply Always On"
Restore on AC Power Loss	Power Off Power On Last State	
Resume On PME#	Disabled Enabled	Disable/Enable PME to generate a wake event.

4.1.2.11 Exit

Feature	Options	Description
Save Changes and Exit		Exit system setup after saving the changes. F10 key can be used for this operation.
Discard Changes and Exit		Exit system setup without saving any changes. ESC key can be used for this operation.
Discard Changes		Discard Changes done so far to any of the setup questions. F7 key can be used for this operation.
Load Optimal Defaults		Load Optimal Default values for all the setup questions. F9 key can be used for this operation.
Load Failsafe Defaults		Load Failsafe Default values for all the setup questions. F8 key can be used for this operation.

4.1.2.12 Boot Utilities

AMI Boot Utilities are: AMI Logo
Boot Menu POP-UP

AMI Logo displays a graphic illustration rather than the traditional POST messages while keeping you informed of diagnostic problems.

Boot Menu POP-UP is a boot screen that displays a selection of boot devices from which you can boot your operating system.

4.1.2.13 AMI Logo

Right after you turn on or reset the computer, AMI displays the Logo Screen if the Setup option Quiet Boot is enabled. This Logo is a graphic illustration created by the computer manufacturer instead of the text-based POST screen, which displays a number of PC diagnostic messages.

To exit the Logo screen and run Setup or display the Boot Menu POP-UP, you can press one of the hot keys described below.

The Logo Screen stays up until just before the operating system loads unless:

- You press <Del> (or <F4> from a Console Redirection terminal) to enter Setup.
- You press <F11> (or <F3> from a Console Redirection terminal) to enter the BOOT Menu POP-UP.
- POST issues an error message.
- The BIOS or an option ROM requests keyboard input.

The following explains each of these situations.

4.1.2.14 Pressing <Del> (or <F4> from a Console Redirection terminal)

Pressing < Del > (or <F4> from a Console Redirection terminal) during POST enters Setup.

4.1.2.15 Pressing <F11> (or <F3> from a Console Redirection terminal)

Pressing <F11> (or <F3> from a Console Redirection terminal) displays the Boot Menu POP-UP with these options:

1. Load the operating system from a boot device of your choice.
2. Exit the Boot Menu POP-UP (with <ESC>) and load the operating system from the boot devices in the order specified in Setup.

4.1.2.16 Keyboard Input Request

If the BIOS or an Option ROM (add-on card) requests keyboard input, the Logo switches over to the POST screen and the Option ROM display prompts for entering the information. POST continues from there with the regular POST screen.

4.1.2.17 BOOT Menu POP-UP

The BOOT Menu POP-UP expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, CDROM, Flash Disk, SCSI or LAN. You can select your boot device in Setup, or you can choose a different device each time you boot during POST by selecting your boot device in t**he Boot device** <F11> (or <F3> from a Console Redirection terminal**)**.

4.2 Installing Drivers

4.2.1 Video Drivers

Various drivers are provided for different operating systems and software. To install a driver, refer to the CD-ROM provided with your board.

4.2.2 Ethernet Drivers

Various drivers are provided for different operating systems and software. To install a driver, refer to the CD-ROM provided with your board.

4.2.3 Other Drivers

For other operating system drivers and installation instructions or for more information, visit our Web site at www.kontron.com or our FTP site at ftp.kontron.ca/support/ or you can also contact Kontron's Technical Support department.

4.3 Console Redirection (VT100 Mode)

The VT100 operating mode allows remote setup of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

4.3.1 Requirements

The terminal should emulate a VT100 or an ANSI terminal. Terminal emulation programs such as Telix© or ProComm© can also be used.

4.3.2 Setting Up and Configuring

To set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the "Advanced" page, "Remote Acces Configuration" menu.
3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable.

Note:
If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines, loop them back as shown in VT100 Partial Setup cable diagram.

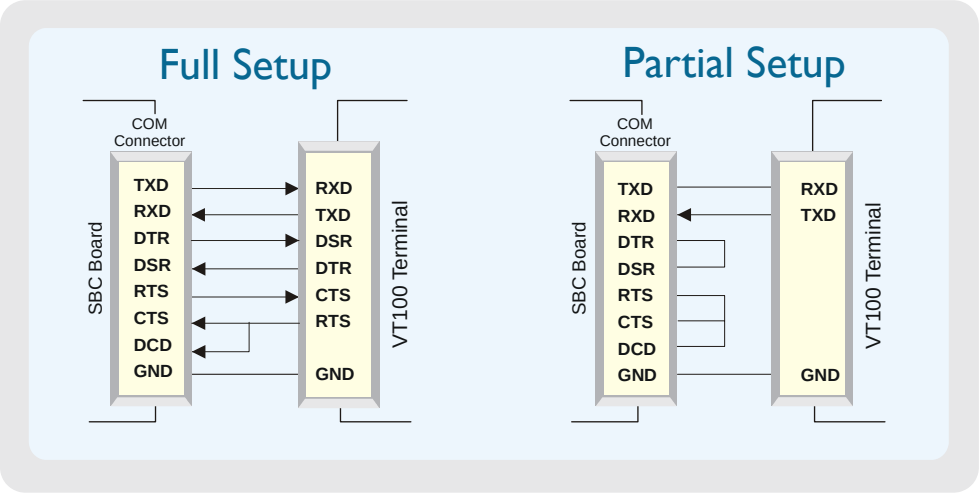
5. Configure your terminal to communicate using the same parameters as in CMOS Setup.
6. Install the Console Redirection jumper (will force VT100 enabled regardless of Setup option). Reboot the board.
7. Use the remote keyboard and display to set up the BIOS.
8. Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.

Console Redirection is done by refreshing the video address @ B8000h at the selected baud rate. This means that a low baud rate refreshes the screen slowly, but the CPU time is maximized for the applications. A high baud rate refreshes the screen rapidly, but the display frequently interrupts the serial port.

Console Redirection provided by AMI based BIOS can reset the target system using the sequence “Ctrl Shift –“.

4.3.3 Running Without a Terminal

The board can boot up without a screen or terminal attached. If the speed is set to Auto and no terminal is connected, the speed is set to 115,200 bauds.
You can run without a console by not enabling VT100 Mode and by disabling the onboard video.

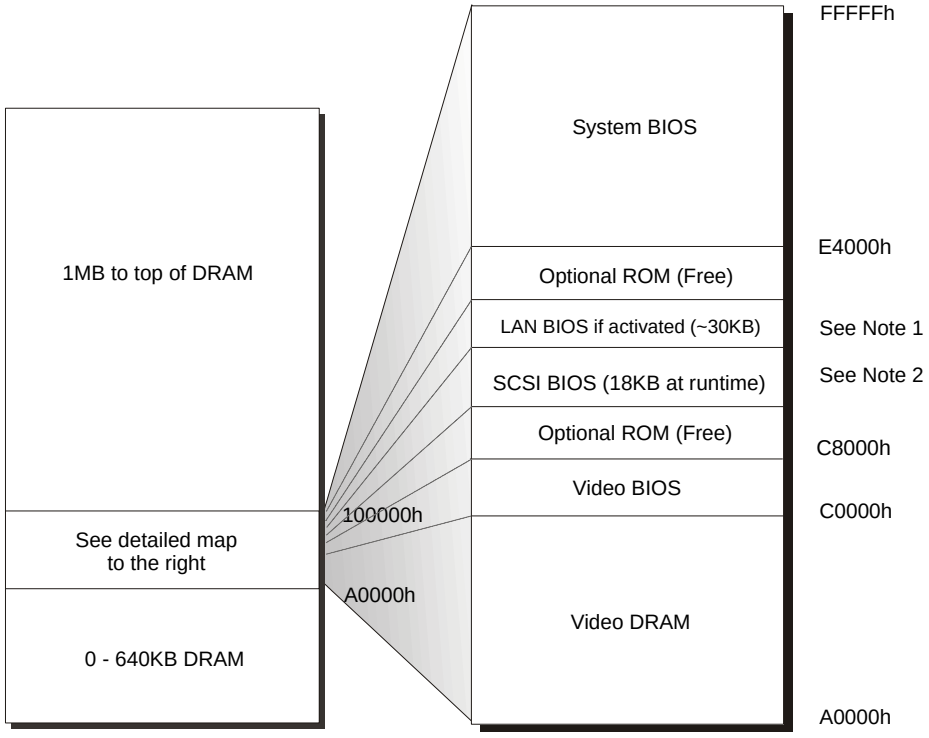


Appendix

Contents

A. Memory & I/O Maps

A.1 Memory Mapping



Note 1 : LAN BIOS address may vary

Note 2 : SCSI BIOS address may vary.
Size is only 2KB if no device.

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CFFFF	Video BIOS
C8000-E3FFF	Optional ROM (Free)
	LAN BIOS around 30KB if activated, address may vary
	External SCSI BIOS 18KB-64KB , address may vary
E4000-FFFFF	System BIOS
100000-PCI Memory	DRAM available
PCI memory-4GB	Hole for PCI memory, APIC and BIOS flash device
4GB and up	DRAM available

A.2 I/O Mapping

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
190-1B8				Kontron Control Port
1F0-1F7, 3F6				Primary IDE
170-177, 376				Secondary IDE
3F0-3F7				Floppy Disk
3F8-3FF (COM1)	2F8-2FF (COM2)			Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)			Serial Port 2 (COM2 by default)
400-0FFF				Chipset Reserved

B. Kontron Extension Registers

B.1 FPGA/CPLD Registers Definition

Unused (shaded) bits are reserved. It is strongly recommended not to modify unused bit to insure compatibility with other product. The base address is fixed. Bits marked NU are not used on this board. Writing to such bit does nothing and reading is undefined; either 0 or 1 may be returned. Bits with name in green and italics are for reference only; they are used on other Kontron CPCI SBC but not on this board.

Legend:

Symbol		Signification
U	=	Unchanged (stay unchanged after reset)
X	=	Not Defined (bit not used on this board)
NU	=	Not Used

B.2 Registers Summary

Address	Function
190h	Serial Ports Mode and Buffers Control
191h	Reset history and CpuFault
192h	Lock and History Clear
193h	Hardware Monitor, ID Chip
194-195h	Reserved
196h	Watchdog Control
197-199h	Reserved
19Ah	Debug LED Control
19B-19Ch	Reserved
19Dh	SpeedStep Control
19E-19Fh	Reserved
1A0h	FPGA Interrupt Number
1A1h	FPGA Interrupt Enables
1A2h	FPGA Interrupt Requests
1A3-1A7h	Reserved
1A8h	I2C Controller: Address register
1A9h	I2C Controller: Transmit buffer
1AAh	I2C Controller: Receive buffer
1ABh	I2C Controller: Flags
1ACh	I2C Controller Hub
1AD-1AFh	Reserved
1B0h	Fan #1 Tachometer measurement & limit
1B1h	Fan #2 Tachometer measurement & limit
1B2h	Fan #3 Tachometer measurement & limit
1B3h	Fan #4 Tachometer measurement & limit
1B4h	Fan #5 Tachometer measurement & limit
1B5h	Fan #6 Tachometer measurement & limit
1B6-1B7h	Reserved
1B8h	Fan tachometers SMI request bits

B.3 Serial Ports Mode and Buffers Control

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x190	Read	*NU*	Break1	Break0	RS485	RS232	ST1	*NU*	*NU*
	Write	*NU*	Break1	Break0	RS485	RS232	ST1	*NU*	*NU*
	Reset	*X*	0	0	0	1	0	*X*	*X*

Break[1..0] Reset on a serial port break (locked when bit LOCK=1):
00: never reset from serial port
01: reset from break on serial port 1
10: reset from break on serial port 2
11: prohibited

RS485 Serial port buffer control, see table below

RS232 Serial port buffer control, see table below

ST1 Serial port buffer control, see table below

RS485	RS232	ST1	Description
0	1	X	RS232 mode (default)
1	0	0	RS485/422 point-to-point mode. - RX is always enable: - TX enabled when COM2 RTS is asserted.
1	0	1	RS485 party line mode: - RX enabled when COM2 RTS is deasserted, - TX enabled when COM2 RTS is asserted.
1	1	X	Illegal. This puts the buffers in RS232 mode.
0	0	X	Illegal. This puts the buffers in RS232 mode. This is the condition on power up. Value is changed by the BIOS.

B.4 Reset history and CpuFault

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x191	Read	PBRST	COM	WDO	CpuFlt	FFRpt	*NU*	*NU*	*NU*
	Write	*NU*	*NU*	*NU*	CpuFlt	FFRpt	*NU*	*NU*	*NU*
	Reset	PBRST	COM	WDO	1	0	*X*	*X*	*X*

PBRST A pushbutton reset was trapped by the reset history circuit.

COM A com port reset was trapped by the reset history circuit.

WDO A watchdog reset was trapped by the reset history circuit.

CpuFlt A "1" indicate a fault by pulling pin CPUFAULT# to GND on the hardware monitor connector. Set on reset by the hardware and cleared by the BIOS. Actual CPU_FAULT# signal on the hardware monitor connector reflect this bit. Over-temperature conditions and fan fault alarms are combined in this signals but have no effect on the bit state.

FFRpt A "1" will enable all Fan Tachometers Alarms (see register 0x1B8) to be reported on the signal CpuFlt#

B.5 Lock and History Clear

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x192	Read	*NU*	*NU*	*NU*	*NU*	*NU*	Lock	*NU*	ClrHis#
	Write	*NU*	*NU*	*NU*	*NU*	*NU*	Lock	*NU*	ClrHis#
	Reset	*X*	*X*	*X*	*X*	*X*	1	*X*	1

Lock When “1”, prohibit modification of some critical control bits (watchdog enable, reset from serial port,etc.).

ClrHis# Clear and bring back to 1 to clear the reset history.

B.6 Hardware Monitor & ID Chip

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x193	Read	AppFlt	GPIO2	GPIO1	FanFlt#	IDChip	ExtFlt#	*NU*	*NU*
	Write	AppFlt	GPIO2	GPIO1	*NU*	IDChip	*NU*	*NU*	*NU*
	Reset	1	1	1	*X*	1	*X*	*X*	*X*

AppFlt	Application Fault: inverted state of pin APPFAULT# on the hardware monitor connector. Set on reset by the hardware and normally cleared by the application software.
GPIO[2..1]	General purpose I/O pins on the hardware monitor connector.
FanFlt#	Return the state of pin FanFlt# in the hardware monitor connector.
ExtFlt#	Return the state of pin ExtFlt# in the hardware monitor connector.
IDChip	ID Chip (DS2401 serial number) control. Open-drain output with pin readback.

B.7 Watchdog Control

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x196	Read	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	WDEN
	Write	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	WDEN
	Reset	*X*	*X*	*X*	*X*	*X*	*X*	*X*	0

WDEN	Enable reset of the board by the watchdog. When this bit is set, a '0' on WDT_TOUT# will reset the board. See the 6300ESB documentation on Intel website for more details on the watchdog functionnality (device 29, function 4). Normally controlled by the BIOS. Note that bit LOCK in register 192h must be '0' to modify this bit.

B.8 Debug LED Control

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x19A	Read	*NU*	*NU*	ENFP	EnPost	HD_Act	Red	Green	*NU*
	Write	*NU*	*NU*	ENFP	EnPost	HD_Act	Red	Green	*NU*
	Reset	*X*	*X*	0	1	0	0	0	*X*

ENFP	Enable Front Pannel mode for serial post code. Instead of transmitting the post code, the transmitter will output LANs LEDs status and other status bits.
EnPost	Enable usage of the debug LED to display the last post code of the boot.
HD_Act	Setting this bit will tie IDE_ACT to the debug green LED
Red	Set this bit to turn on the debug red LED.
Green	Set this bit to turn on the debug green LED.

About debug LED: The idea is that the LED will light red when in reset (this is hardware). As soon as the FPGA is programmed, the LED lights yellow and is enabled for post-code display (see bellow). If the BIOS fail, it is possible to read the post-code. If the BIOS succeed, it will disable the post-code and enable HD activity on the green LED. If needed, the application software can then disable hard disk activity reporting and directly control the bi-color LED for status reporting.

How to read the 8-bit post-code:

- Yellow: start of post sequence
- Red blink: This is the high nibble. 0 to 15 blinks represent hexadecimal 0 to F.
- Green blink: This is the low nibble. 0 to 15 blinks represent hexadecimal 0 to F.

Serial post code stream:

Bit	PostCode Mode	Front Panel Mode
16	Board Reset	Board reset (hardcoded)
15	Post code bit 15	FPGA3: Reserved for future use (1 for now)
14	Post code bit 14	FPGA2: Overtemp# (mirror of SHB thermal LED)
13	Post code bit 13	FPGA1: HM_CpuFlt#
12	Post code bit 12	FPGA0: HM_AppFlt#
11	Post code bit 11	PATA_LED#
10	Post code bit 10	SATA_LED#
9	Post code bit 9	RED LED (mirror of SHB bi-color debug LED)
8	Post code bit 8	GREEN LED (mirror of SHB bi-color debug LED)
7	Post code bit 7	Lan1_activity# (82547GI)
6	Post code bit 6	Lan1_up#
5	Post code bit 5	Lan1_1000#
4	Post code bit 4	Lan1_100#
3	Post code bit 3	Lan0_activity# (82541ER)
2	Post code bit 2	Lan0_up#
1	Post code bit 1	Lan0_1000#
0	Post code bit 0	Lan0_100#

B.9 SpeedStep Control

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x19D	Read	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*
	Write	*X*	*X*	*X*	*X*	*X*	*X*	*X*	BOM
	Reset	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*

BOM 1: Battery Optimized Mode (low power, low frequency).
0: Performance optimized mode (high power, high frequency).

X Don't care.

This register is used by the BIOS to change the CPU mode. The user application doesn't need to access this register.

B.10 FPGA Interrupt Number

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A0	Read	*NU*	*NU*	*NU*	*NU*	Legacy ISA Interrupt number			
	Write	*NU*	*NU*	*NU*	*NU*	Legacy ISA Interrupt number			
	Reset	*X*	*X*	*X*	*X*	0000b			

During the boot process, the BIOS assign a legacy interrupt to the FPGA and writes the interrupt number in this register. A driver that needs to use the interrupt read this register to find out what interrupt is used.

B.11 FPGA Interrupt Enables

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A1	Read	*NU*	*NU*	I2CEn	FanFlt	ExtFlt	*NU*	*NU*	*NU*
	Write	*NU*	*NU*	I2CEn	FanFlt	ExtFlt	*NU*	*NU*	*NU*
	Reset	*X*	*X*	0	0	0	*X*	*X*	*X*

I2C Enable interrupt by the I2C controller.
FanFlt Enable an interrupt by signal FanFlt# on the hardware monitor connector.
ExtFlt Enable an interrupt by signal ExtFlt# on the hardware monitor connector.

Interrupts can also be generated by the fan tachometers (see registers 0x1B0 to 0x1B5).

B.12 FPGA Interrupt Requests

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A2	Read	*NU*	*NU*	I2C	FanFlt	ExtFlt	*NU*	*NU*	*NU*
	Write	*NU*	*NU*	I2C	FanFlt	ExtFlt	*NU*	*NU*	*NU*
	Reset	*X*	*X*	0	*X*	*X*	*X*	*X*	*X*

I2C Set when bit BUSY in the I2C controller switche from 1 to 0 (i.e. task completion).
FanFlt Set when the harware monitor signal FANFLT# changes state.
ExtFlt Set when the harware monitor signal EXTFLT# changes state.

Interrupt requests are generated regardless of the state of the interrupt enable bits.
To clear a request bit, write a "1" at this bit location. Following a reset, a false request can occurs. Always clear a pending request before enabling an interrupt source.

Request bits use an edge detection circuit. The are set when the interrupt condition is detected (transition of the monitored signal). For example, when the signal FanFlt# in the hardware monitor connecter is asserted (i.e. fall to GND) the correspondig request is set. If the request is clear, the circuit will wait for a transition on FanFlt# to assert the request again. The interrupt service can read register 0x193 to find the actual state of the signal.

B.13 I^2C Controller: Address register

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A8	Read	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
	Write	A6	A5	A4	A3	A2	A1	A0	Read
	Reset	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*

A[6..0] I^2C device address.
READ 1: to read from the I^2C device, 0: to write to the I^2C device.

Writing to this register triggers the generation of a START sequence and will transmit the address and READ bit. Bit OPEN and BUSY in the flags register will turn to 1. When the sequence is completed, bit BUSY will return to 0 but bit OPEN will stay to 1. At this moment, bit RXACK in the flags register will indicate the I2C device acknowledge.

B.14 I²C Controller: Transmit buffer

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A9	Read	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
	Write	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
	Reset	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*

Writing to this register trigger a data-transmit operation.

B.15 I²C Controller: Receive buffer

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1AA	Read	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
	Write	Write anything to trigger reception							
	Reset	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*

Write anything at this location to start clocking a byte out of the I²C device.

This register hold the last received data. Since the receiver operates all the time, including during address or data transmission, a pin readback of the last transmission is available at the end of any transmission.

B.16 I²C Controller: Flags

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1AB	Read	V1	V0	BUSY	OPEN	TXACK	RXACK	SCL	SDA
	Write	*NU*	*NU*	*NU*	OPEN	TXACK	*NU*	SCL	SDA
	Reset	V1	V0	0	0	0	*X*	1	1

V[1..0]	Version/capability. 00 for now.
BUSY	Operation in progress. Don't write any I2C register when this bit is set.
OPEN	Connection open. Set to "1" when opening the connection. Clearing this bit will send a STOP condition on the I2C bus.
TXACK	Acknowledge to transmit on I2C byte reception. Should always be 1 at the exception of the last byte to be received.
RXACK	Acknowledge received from device on the last I2C byte transmission. Should be 0 if an I2C device acknowledged the transfer.
SCL & SDA	Direct reading and control of SCL and SDA lines. Allow software control of the lines when the controller doesn't use them. For debugging purpose only. When not in use, leave to 1. Those bit are forced to 1 when bit OPEN is set. On read, give the pin status.

B.17 I²C Hub Configuration

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1AC	Read	*NU*	*NU*	*NU*	*NU*	*NU*	I2C2	I2C1	I2C0
	Write	*NU*	*NU*	*NU*	*NU*	*NU*	I2C2	I2C1	I2C0
	Reset	*X*	*X*	*X*	*X*	*X*	0	0	0

I2C[2..0] 000: I2C controller not connected to any bus, default.
001: I2C controller connected to on-board PROM
010: I2C controller connected to hardware monitor connector
100: I2C controller connected to ePCI-X SMBus
011: I2C controller connected to on-board PROM and hardware monitor
101: I2C controller connected to on-board PROM and ePCI-X
110: I2C controller connected to hardware monitor and ePCI-X
111: I2C controller connected to on-board PROM, hardware monitor and ePCI-X

I2C bus routing is used mostly in case of conflictual I2C addresses. In absence of addresses conflicts, connect the controller to all busses. It will act like a hub: every data transmitted is sent to all busses and data received is "ored" from all the busses.

When connected to the hardware monitor connector, the I2C link connect as follow:

- SDA connect to GPIO1
- SCL connect to GPIO2

B.18 Fan Tachometers Speed & Limit

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1B0 to 0x1B5	Read	*NU*	FAN Measured Period						
	Write	EnIRQ	FAN Low Period Limit						
	Reset	0	0000000b						

Let

TT = Number of tics per turn (depends on fan type; typically 2 or 4)
Tac = Tachometer reading in one of the above registers

Then

Speed(RPM) = 60 / (1ms * (Tac+1) * TT)

Reverse rule for tachometer speed limit.

B.19 Fan Tachometers Alarms

For a given fan input, if the EnIRQ bit in its SPEED register is set and the fan speed is slower than the specified limit then the alarm bit for this fan will be set.

When one or more alarm bit are set, an IRQ is generated.
To clear an alarm, write a 1 at its bit position in the alarm register.

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1B8	Read	*NU*	*NU*	FAN6	FAN5	FAN4	FAN3	FAN2	FAN1
	Write	*NU*	*NU*	FAN6	FAN5	FAN4	FAN3	FAN2	FAN1
	Reset	*X*	*X*	0	0	0	0	0	0

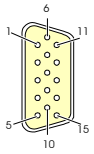
C. Connector Pinouts

C.1 Connectors and Headers Summary

Connector	Description
J1	Primary Video
J2	Secondary Video and TV-OUT
J3	PS/2 Keyboard / Mouse
J4	Gigabit Ethernet LAN (low BW)
J5	Gigabit Ethernet LAN (high BW)
J6	Serial Port A (header)
J7	Serial Port B (header)
J8 & J17	USB[0:1] and USB[2:3]
J9	Floppy
J10	Hardware monitor
J11	Multifunction
J12	Parallel ATA
J14 & J15	Serial ATA
J13	Parallel Port
J16	CompactFlash disk
J18 & J19	DIMM Sockets
J22	CPU Power
J20	MCH Fan

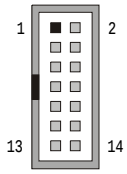
C.2 CRT VGA Interface (J1)

Signal		Signal		Signal	
RED	1	Analog GND	6	N.C.	11
GREEN	2	Analog GND	7	SDATA	12
BLUE	3	Analog GND	8	HSYNC	13
N.C.	4	N.C.	9	VSYNC	14
GND	5	GND	10	SCLK	15



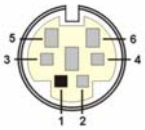
C.3 TV-OUT/Secondary Video (J2)

Signal	Pin		Pin	Signal
(TV-Out Composite out) COMP	1		2	GND
(TV-Out S-Video Chroma) C	3		4	Y (TV-Out S-Video Luma)
GND	5		6	RED (Secondary CRT)
GND	7		8	GND
GND	9		10	BLUE (Secondary CRT)
GND	11		12	HSYNC (Secondary CRT)
GND	13		14	VSYNC (Secondary CRT)



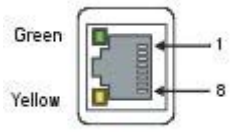
C.4 PS/2 Keyboard / Mouse (J3)

Signal	
KB:DATA	1
MOUSE:DATA	2
GND	3
VCC	4
KB:CLK	5
MOUSE:CLK	6



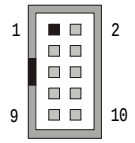
C.5 Ethernet 10/100/1000 Base-T (J4 & J5)

Signal	Pin
MDI0+	1
MDI0-	2
MDI1+	3
MDI2+	4
MDI2-	5
MDI1-	6
MDI3+	7
MDI3-	8



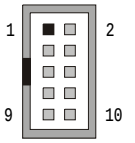
C.6 Serial Port 2 & 1 (J6 & J7) RS-232

Signal	Pin		Pin	Signal
DCD	1		2	DSR
RXD	3		4	RTS
TXD	5		6	CTS
DTR	7		8	RI
GND	9		10	N.C.



Serial Port 1 - (J1) RS-232/RS-422/RS-845

Signal	Pin		Pin	Signal
RSV	1		2	RSV
RX-	3		4	RX+
TX-	5		6	TX+
RSV	7		8	RSV
GND	9		10	N.C.

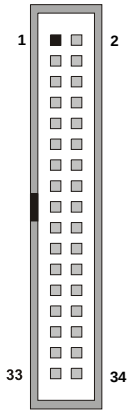


C.7 USB Header (J8 & J17)

Signal	Pin		Pin	Signal
USB0:VCC	1		2	USB1:VCC
USB0:DATA-	3		4	USB1:DATA-
USB0:DATA+	5		6	USB1:DATA+
USB0:GND	7		8	USB1:GND
GND	9		10	GND

C.8 Floppy Drive (J9)

Signal	Pin		Pin	Signal
GND	1		2	DENSEL#
GND	3		4	N.C.
GND	5		6	N.C.
GND	7		8	INDEX#
GND	9		10	MTR0#
GND	11		12	DSEL1#
GND	13		14	DSEL0#
GND	15		16	MTR1#
N.C.	17		18	DIR#
GND	19		20	STEP#
GND	21		22	WDATA#
GND	23		24	WGATE#
GND	25		26	TRK0#
N.C.	27		28	WRPROT#
FDETECT	29		30	RDATA#
GND	31		32	HDSEL#
N.C.	33		34	DSKCHG#

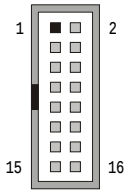


C.9 Hardware Monitor (J10)

Signal	Pin		Pin	Signal
GND	1		2	PWRBT#
Reserved	3		4	GND
GPIO1/SMBDATA	5		6	GPIO2/SMBCLK
APPFLT#	7		8	CPUFLT#
EXTFLT#	9		10	GND
FANFLT#	11		12	GND
CHASINT#	13		14	GND
FAN_TACH1	15		16	FAN_TACH2
FAN_TACH3	17		18	FAN_TACH4
FAN_TACH5	19		20	FAN_TACH6

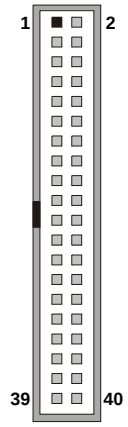
C.10 Multi-Function (J11)

Signal	Pin		Pin	Signal
KB:CLK	1		2	GND
KB:DATA	3		4	GND
VCC	5		6	VCC
SPEAKER	7		8	VCC
MOUSE:CLK	9		10	GND
MOUSE:DATA	11		12	GND
PBRES#	13		14	GND
IDE:ACT#	15		16	VCC



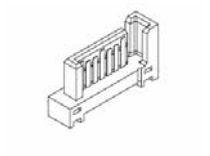
C.11 Parallel ATA - IDE1- (J12)

Signal	Pin		Pin	Signal
RST#	1		2	GND
D7	3		4	D8
D6	5		6	D9
D5	7		8	D10
D4	9		10	D11
D3	11		12	D12
D2	13		14	D13
D1	15		16	D14
D0	17		18	D15
GND	19		20	KEY
DMARQ	21		22	GND
IOW#	23		24	GND
IOR#	25		26	GND
IORDY	27		28	CSEL
DMACK#	29		30	GND
IRQ	31		32	N.C.
A1	33		34	DIAG#
A0	35		36	A2
CS0#	37		38	CS1#
DASP#/ACT#	39		40	GND



C.12 Serial ATA (J14 & J15)

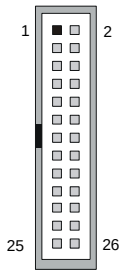
Signal	Pin
GND	1
TX+	2
TX-	3
GND	4
RX-	5
RX+	6
GND	7



C.13 Parallel Port

Standard Mode

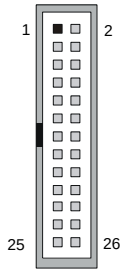
Signal	Pin		Pin	Signal
STB#	1		2	ALF#
D0	3		4	ERR#
D1	5		6	INIT#
D2	7		8	SLCTIN#
D3	9		10	GND
D4	11		12	GND
D5	13		14	GND
D6	15		16	GND
D7	17		18	GND
ACK#	19		20	GND
BUSY	21		22	GND
PE	23		24	GND
SLCT	25		26	GND



Active Low Signal

EPP Mode

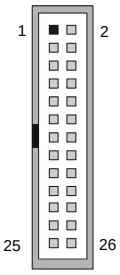
Signal	Pin		Pin	Signal
WRITE#	1		2	DATASTB#
D0	3		4	N.C.
D1	5		6	N.C.
D2	7		8	ADDRSTRB#
D3	9		10	GND
D4	11		12	GND
D5	13		14	GND
D6	15		16	GND
D7	17		18	GND
INTR	19		20	GND
WAIT#	21		22	GND
N.C.	23		24	GND
N.C.	25		26	GND



Active Low Signal

ECP Mode

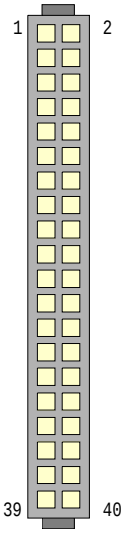
Signal	Pin		Pin	Signal	
				Compatible Mode	High Speed Mode
STROBE#	1		2	AUTOFD	HOSTACK
D0	3		4	FAULT	PERIPHRQST
D1	5		6	INIT	REVERSERQST
D2	7		8	SELECTIN	SELECTIN
D3	9		10	GND	
D4	11		12	GND	
D5	13		14	GND	
D6	15		16	GND	
D7	17		18	GND	
ACK#	19		20	GND	
BUSY, PERIPHACK	21		22	GND	
PERROR, ACKREVERSE	23		24	GND	
SELECT	25		26	GND	



Active Low Signal

C.14 CompactFlash™ (J16)

Signal	Pin		Pin	Signal
D11	1		2	GND
D12	3		4	D3
D13	5		6	D4
D14	7		8	D5
D15	9		10	D6
CS1#	11		12	D7
DMACK#	13		14	CS0#
DMARQ	15		16	IOR#
PDIAG#	17		18	IOW#
IRQ15	19		20	VCC
VCC	21		22	VCC
GND	23		24	GND
RESET#	25		26	GND
CSEL	27		28	A2
A1	29		30	DASP#
A0	31		32	IORDY
D0	33		34	D8
D1	35		36	D9
D2	37		38	D10
IOCS16#	39		40	GND



C.15 CPU FAN Header (J21)

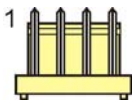
Signal	
SENSE	1
+12V	2
GND	3

C.16 Chipset Fab Header (J20)

Signal	
Sense	1
+5V	2
GND	3

C.17 POST Code Debug (J23)

Signal	Pin
+3.3V	1
POST:DATA	2
POST:CLOCK	3
GND	4

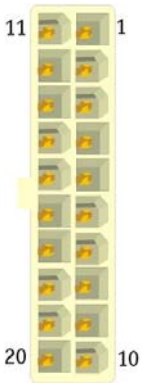


C.18 CPU Power (J22)

Signal	Pin		Pin	Signal
+12V	3		1	GND
+12V	4		2	GND

C.19 ATX-Type Board Power (J24)

Signal	Pin		Pin	Signal
VCC3	11		1	VCC3
-12V	12		2	VCC3
GND	13		3	GND
PS_ON#	14		4	VCC
GND	15		5	GND
GND	16		6	VCC
GND	17		7	GND
N.C.	18		8	PWROK
VCC	19		9	5VSB
VCC	20		10	+12V



D. BIOS Setup Error Codes

D.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS:

Checkpoint	Description
Before D1	Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable CACHE before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See *Bootblock Recovery Code Checkpoints* section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See *POST Code Checkpoints* section of document for more information.
E1-E8 EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

D.2 NorthBridge Specific POST Errors

The detection and setup of the memory is done after POST D3 from the Bootblock Initialization Code Checkpoints.

Checkpoint	Description
A0	Start of MCH Memory detection.
01	Verify all DIMMs are DDR, unbuffered, and if ECC is supported.
03	Verify all DIMMs are single or double sided and not mixed.
04	Verify all DIMMs are x8 or x16 width.
05	Find a common CAS latency between the DIMMS and the MCH.
06	Determine the memory frequency and CAS latency to program.
07	Determine the smallest common TRAS for all DIMMs.
08	Determine the smallest common TRP for all DIMMs.
09	Determine the smallest common TRCD for all DIMMs.
10	Determine the smallest refresh period for all DIMMs.
11	Check what burst lengths are supported.
12	Determine the DIMM configuration for each channel.
13	Program the correct memory frequency.
14	Determine the mode of operation for the memory channels.
15	Program the receive enable reference timing control register.
16	Program the DQS input timing control register.
17	Program the RCOMP SRAM registers.
18	Program the DRAM clock crossing registers.
19	Program the DRAM Timing & and DRAM Control registers.
20	Program the DRAM Row Attributes and DRAM Row Boundary registers
21	Perform JEDEC memory initialization for all memory rows.
22	Disable all clocks on unpopulated rows.
23	Program DRAM throttling and throttling event registers.
24	Setup DRAM control register for normal operation and enable periodic RCOMP.
25	Clear DRAM initialization bit in the ICH.
26	ECC initialization. This routine might take long time for large memory configuration.
AF	MCH Memory detection completed.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
E1-E8 EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.
E0	Unsupported DIMM detected.
E1	Unsupported number of sides.
E2	Unsupported DIMM width.
E3	Timing problem with the DIMM.
E4	Unsupported CAS Latencies.
E5	Unsupported refresh rate.
E6	Unsupported config populated.
E7	Unsupported frequency combo.

D.3 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

D.4 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Init SMI handler, USB controller and prepare to display Logo.
24	Uncompress and initialize any platform specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.

38	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, ... etc.) successfully installed in the system and update the BDA, EBDA...etc.
50	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7A	Initializes remaining option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
8F	Generate the final ESCD image, compares with the existing image and writes to NVRAM if ESCD image is changed.
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
00-12	Init each SMBIOS structures and display on POST which one is currently initialized.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A8	Prepare CPU for OS boot including final MTRR values.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitializes the ADM module.
AB	Prepare BBS for Int 19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Passes control to OS Loader (typically INT19h).
61-70	OEM POST Error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

D.5 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system busses. The following table describes the main checkpoints where the DIM module is accessed:

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.

1 = func#1, static devices initialization on the BUS concerned.

2 = func#2, output device initialization on the BUS concerned.

3 = func#3, input device initialization on the BUS concerned.

4 = func#4, IPL device initialization on the BUS concerned.

5 = func#5, general device initialization on the BUS concerned.

6 = func#6, error reporting for the BUS concerned.

7 = func#7, add-on ROM initialization for all BUSes.

8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).

1 = On-board System devices.

2 = ISA devices.

3 = EISA devices.

4 = ISA PnP devices.

5 = PCI devices.

D.6 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events:

Checkpoint	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01, 02, 03, 04, 05	Entering sleep state S1, S2, S3, S4, or S5.
10, 20, 30, 40, 50	Waking from sleep state S1, S2, S3, S4, or S5.

D.7 Beep Codes

The following table describes the beep codes that are used by AMIBIOS:

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error
3	Main memory read / write test error.
4	Motherboard timer not operational
5	Processor error
6	Keyboard controller BAT test error.
7	General exception error.
8	Display memory error.
9	ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory bad

D.7.1 Troubleshooting BIOS Beep Codes

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards cards except the video adapter. • If the beep codes are generated even when all other expansion cards are absent, the motherboard has a serious problem. Consult your system manufacturer. • If the beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning add-in card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

E. BIOS Update & Emergency Procedure

E.1 BIOS Update Precedure

The BIOS update procedure is detailed in a ReadMe file included with the BIOS package as well as the update utility. This package can be downloaded from our website www.kontron.com or from our FTP site ftp://ftp.kontron.ca/Support

E.2 Emergency Procedure

Symptoms:

- No POST code on a power up (when using a POST card).
- Board does not boot, even after usual hardware and connection verifications.
- At power up, there is floppy disk led activity, which is one sign that the BIOS as detected a corrupted BIOS CRC prior POST and fallen back automatically to Emergency Recovery Mode looking for the floppy Emergency disk.

The Emergency Recovery procedure is detailed in a ReadMe file included with the Emergency BIOS package as well as the update utility. This package can be downloaded from our website http://www.kontron.com or from our FTP site ftp://ftp.kontron.ca/Support

F. Getting Help

At Kontron, we take great pride in our customers' successes. We believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, contact our Technical Support at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Kontron, our products, or services, visit our Web site at: www.kontron.com

You also can contact us by E-mail at: support@ca.kontron.com

Or at the following address:

Kontron Canada, Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

RETURNING DEFECTIVE MERCHANDISE

If your Kontron product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682 or at 1 (800) 354-4223. Make certain you have the following at hand:
   - The Kontron Invoice number
   - Your purchase order number
   - The serial number of the defective board.
2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.
3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.
4) Prior to returning any merchandise, make certain you receive an RMA number from Kontron's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:
   - Make a copy of the request form on the following page.
   - Fill out the form and be as specific as you can about the board's problem.
   - Fax it to us.
5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.
6) When returning a Kontron board:
   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.
   ii) Ship prepaid to (but not insured, since incoming units are insured by Kontron):

Kontron Canada, Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

Return to Manufacturer Authorization Request

Contact Name:			
Company Name:			
Street Address:			
City:		Province/State:	
Country:		Postal/Zip Code:	
Phone Number:		Extension:	
Fax Number:		E-Mail:	

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Kontron Canada, Inc., 616 Curé Boivin, Boisbriand, Québec, Canada, J7G 2A7

Fax this form to Kontron's Technical Support department in Canada at (450) 437-8053