ePCI-200

Pentium 4 SHB

Technical Reference Manual
Version 1.1, July 2005

The latest releases of the Technical Reference Manuals are available at:
http://www.kontron.com or at: ftp://ftp.kontron.ca/Support

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Ref. : M8003_TECH_1

- **FOREWORD**

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Printed in Canada.

FCC Compliance Statement

Warning

Changes or modifications to this unit not expressly approved by the party responsible for the compliance could void the user's authority to operate this equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generated, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

European Statement

Warning

This is a class B product. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

Safety Standard

UL Recognized Component, File # E186339 Vol. 1

Care and handling precautions for Lithium batteries

- Do not short circuit
- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Do not mix different types or partially used batteries together
- Always observe proper polarities

READ ME FIRST

Your computer board has a standard non-rechargeable lithium battery. To preserve the battery lifetime, **the battery enable jumper is removed when you receive the board.**

EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type of battery recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ATTENTION

Il y a danger d'explosion si la pile n'est pas installée correctement.

Remplacer uniquement par une pile du même type ou d'un type équivalent recommandé par le fabricant. Mettre au rebut les piles usagées conformément aux instructions du fabricant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel. Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Hay un peligro de explosion sido la pila no ha si bien remplazada. Remplace la pila con el mismo tipo o con aquellas recomendadas por el fabricante. Para desacerce de las pilas usadas, siga las instructiones del fabricante.

POWERING-UP THE BOARD

If you should encounter a problem, verify the following items:

Make sure that all connectors are properly connected.

Check your boot diskette.

If the board still does not start up properly, you should try booting your system with the ePCI-200 installed in the system, a monitor and a mouse connected to the board. This is the minimum required to verify the board's operation.

If you still are not able to verify your board, please refer to the emergency Procedure in the Appendix Section.

If you still are not able to get your board up and running, contact our Technical Support department for assistance (see Appendix G, Getting Help).

ADAPTER CABLES

While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

UNPACKING AND SAFETY PRECAUTIONS

Static Electricity

Since static electricity can cause damage to electronic devices, the following precautions should be taken:

1. Keep the board in its anti-static package, until you are ready to install it.
2. Always touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

Storage Environment

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Power Supply

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

Unpacking

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its anti-static wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage or missing items, notify Kontron immediately.

When unpacking you will find:

1. One ePCI-200 SHB.
2. One Quick Reference sheet.
3. One CDROM containing drivers.
4. One Cable Kit.

APPENDICES

PART 1

1 PRODUCT OVERVIEW

1. INTRODUCTION
2. FEATURE SET SUMMARY
3. ePCI-X COMPLIANCE GRID
4. REFERENCES

1.1 Introduction

The ePCI-200 will reach new levels of performance in PICMG CPU boards. It comes standard with a rich set of features including the latest generation 478-pin processor technology, PCI-X support up to 133MHz, up to 4Gig of DDR SDRAM, an onboard ATI Mobility™ Radeon™ with integrated 16MB of DDR SDRAM and a dual Fast Ethernet controller. Additional features include two USB ports, a floppy controller, two serial ports, a parallel port, PS/2 keyboard and mouse ports, a hardware monitor and a dual stage watchdog timer.

This generic single board computer is targeted at a broad range of applications requiring a high performance processing with a good graphic solution in a PICMG environment (where ISA bus support is not necessary). Those requirements can be found for applications in most of the markets : automation, communications, medical and military.

The ePCI-200 is a mPGA-478 Pentium 4 full-size dual-bus ePCI-X (PICMG 1.2) r1.0 SHB.

1.2 Feature Set Summary

ePCI-200 Feature Set Summary Sheet	
Features	**Description**
CPU	▸ mPGA-478 socket Mobile or Desktop Intel Pentium 4 at 400/533MHz FSB ▸ 512KB Advanced Transfer Cache (on-die, full speed L2 cache with ECC)
Chipset	▸ Serverworks Grand-Champion SL (CMIC-SL, CSB5, CIOB-X2) ▸ National PC87417 super I/O
ePCI-X	▸ Full-size dual-bus (see ePCI-X compliance grid for details)
Memory	▸ Three 184-pin, registered, 2.5V DDR200/266 SDRAM DIMMs ▸ Up to 4GB of memory; all 4 GB cacheable (per CPU) ▸ ECC support
Video	▸ Dual-head PCI video controller ATI Mobility Radeon M6-C16H ▸ 16MB on chip video memory ▸ Supports CRT with resolution up to 1600 x 1200 x 32-bit ▸ Dual-Head monitor support (through header connector) ▸ Composite or S-Video TV output (through header connector) ▸ LVDS flat panel interface (JILI)
I/O on bracket	▸ Video (female DB-15) ▸ Two 10/100Base-TX Ethernet (RJ-45 with link / activity indicators) ▸ PS/2 keyboard and mouse (6-pin female minidin)
I/O on headers	▸ Two USB 1.1 compliant ports ▸ Two serial Ports: one RS-232, and one RS-232/422/485 ▸ One Parallel Port (bi-directional with all IEEE 1284 protocols supported with BIOS selectable IRQs and addressing ▸ Two UDMA100 interface: support for four IDE drives (in master / slave configuration); PIO Mode 4, Bus Master IDE synchronous DMA mode transfer up to 100MB/s ▸ CompactFlash module interface (on secondary channel) ▸ Floppy Disk: support for one drive ▸ System monitoring ▸ Second CRT and TV-out (through header connector) ▸ Serial post codes (for debugging use) ▸ JILI interface for flat panel (flex cable)

ePCI-200 Technical Specification Sheet (cont'd)	
Features	**Description**
BIOS Features	▸ Phoenix BIOS in Boot Block Flash with recovery code ▸ Save CMOS in Flash option ▸ Boot from LAN capability ▸ Setup console redirection to serial port (VT100 mode) with CMOS setup access ▸ All onboard peripherals (except VGA enable / disable by jumper) can be enabled or disabled by software ▸ Diskless, keyboardless, and videoless operation extensions. Keyboardless and videoless operation need console redirection ▸ System, video and LAN BIOS shadowing ▸ Advanced security feature for floppy and HDD; DMI & HDD S.M.A.R.T. support ▸ Advanced Configuration and Power Interface (ACPI 1.0) ▸ Intelligent System Monitoring (advanced thermal management such as resume, overheat alarm and auto slow down) ▸ ATX support with SOFTOFF software enable/disable

ePCI-200 Technical Specification Sheet (cont'd)	
Features	**Description**
Supervisory	▸ Two-stage software programmable watchdog timer (time out from 16msec to 4.5 min) ▸ On-board voltage monitoring ▸ CPU fan monitoring as well as six external fans ▸ CPU Temperature monitoring ▸ CPU Switcher temperature monitoring ▸ Board temperature sensor ▸ Power failure / low battery detector ▸ External events and error reporting ▸ SMBus
Remote operation	▸ Console redirection to a serial port (VT100 mode). ▸ Remote reset from a serial port (via a break).
Miscellaneous	▸ DS2401 silicone serial number. ▸ Optional user I^2C EEPROM (not standard, contact Kontron)
OS Compatibility	▸ Microsoft Windows XP ▸ Microsoft Windows 2000 ▸ Microsoft Windows 2000 Server ▸ Linux ▸ Free BSD ▸ QNX 6.2.0

ePCI-200 Technical Specification Sheet (cont'd)			
Features	**Description**		
Mechanical	▸ 338 x 130 (13.33 x 4.80) ▸ Full-size PICMG 1.2 (ePCI-X) Rev 1.0, see appendix D for details.		
Power Requirements	▸ +3.3V 3A ▸ +5V 6A ▸ +12V 1A (fingers) ▸ +12V 6A (CPU power cable with desktop at 2.8GHz) ▸ -12V 20mA (not required) ▸ +5Vaux 50mA (required for ATX control only) ▸ +3.3Vaux not used Tested with a 2.8GHz CPU and 2GB of Memory.		
Environmental		**Operating**	**Storage and Transit**
	Temperature (w/100LFM airflow)	0° to 45°C/32° to 113°F	-40° to +70°C/-40° to 158°F
	Humidity	5% to 90% @ 40°C/104°F non-condensing	5% to 95% @ 40°C/104°F non-condensing
	Altitude	4,000m / 13,123ft	15,000m / 49,212ft
	Shock	5G, 11ms half-sine, each axis	Bellcore GR-63-CORE, Section 4.3
	Vibration	5 to 500Hz, 1G, each axis	5 to 50Hz, 2G; 50 to 500Hz, 3G, each axis
MTBF	> 150 000 hours (Telcordia SR-332, Issue 1)		
Reliability	▸ Keyboard and mouse voltage protected by self-resetting fuses ▸ USB voltage protected by silicone breaker ▸ 2 year limited warranty		
Safety	▸ Designed to meet or exceed UL 60950 3rd Ed.; CSA C22.2 No 60950-00; EN 60950:2000; IEC60950-1		
EMI/EMC	▸ FCC 47 CFR Part 15, Class B; CE Mark to EN55022/EN55024		

1.3 ePCI-X Compliance Grid

ePCI-200 Compliance Grid		
Board size		Full-size with ISA retainer
Backplane compatibility		Dual-bus, single-bus and stand-alone
Bus A	Bus width	32-bit (64-bit friendly)
	Bus mode	PCI
	Frequency	33MHz
	Electrical keying	Universal (5V and 3.3V)
	Clock distribution	Open-loop assuming 4.5” on backplane.
	Scanned devices	AD27, AD30, AD29, AD28
Bus B	Bus width	64-bit
	Bus mode	PCI and PCI-X
	Frequency	33/66MHz for PCI, 66/100/133MHz for PCI-X
	Electrical keying	3.3V only
	Clock distribution	Closed-loop
	Scanned devices	AD31, AD30, AD29, AD28
I^2C/SMBus	Master	Yes
	Slave	No
	Multimaster aware	No
	Pull-up voltage	3.3V
Power Supply	+12V, +5V, +3.3V	Required
	+5Vaux	Required if ATX control is used
	-12V	Monitored but not used
	+3.3Vaux	not used
ATX support		Yes
JTAG		Yes, **Reserved for Kontron internal use only**

NOTES

1. When using Kontron's backplane, IDSEL AD31 must be changed to AD27 by setting the related jumper. When using any third party backplane, do not use slot AD31.

2. Can be changed to +3.3Vaux on request.

3. JTAG is reserved for Kontron's internal use only. Any attempt to use this port may damage the board.

1.4 References

- Latest version of this manual can be found on Kontron WEB site or:
  ftp://ftp.kontron.ca/support

- General information on ePCI-X and ePCI-X product by Kontron.
  http://www.epci-x.com

- Information on JILI flat panel interface.
  http://www.dr-berghaus.de

- PICMG web site to get the ePCI-X (PICMG 1.2) specification.
  http://www.picmg.com

- PCI SIG web site to get the PCI and PCI-X specifications.
  http://www.pcisig.com

- ServerWorks web site for chipset information.
  http://www.serverworks.com

- National web site for super I/O information.
  http://www.national.com

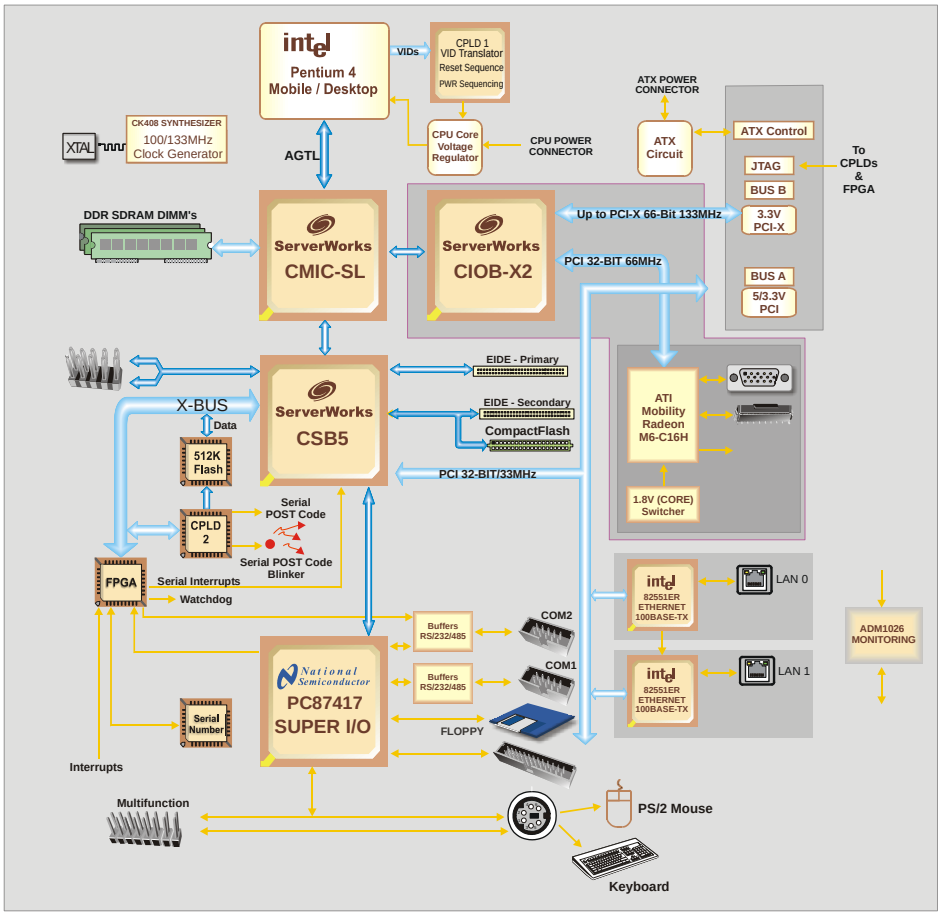
- Intel developer's site for CPU and LANs information.
  http://developer.intel.com

PART 2

2 BOARD FEATURES

1. BLOCK DIAGRAM
2. SYSTEM CORE
3. ETHERNET CONTROLLERS
4. VIDEO CONTROLLER
5. SUPER I/O PC87417
6. ATX POWER SUPPLY CONTROL
7. SYSTEM MANAGEMENT FEATURES
8. DEBUGGING FEATURES
9. MISCELANEOUS FEATURES

2.1 Block Diagram



2.2 System Core

2.2.1 Processors

The ePCI-200 accepts Pentium 4 in mPGA-478 package. Both desktop and mobile CPUs are supported.

See installation for actual types.

Related Jumpers

- W14: CPU front side bus and memory speed.
- W15: CPU type selection (critical).

BIOS Settings

- Advanded \ Advanced Processor Options
  - Performance or battery optimized mode, for mobile CPU only.

CAUTION

Improper installation may damage the board and/or the CPU.

Before changing or installing a processor on your board, read the section on processor installation first.

2.2.2 Chipset

The ePCI-200 uses Serverworks Grand Champion SL Chipset.

CMIC-SL

- Processor Interface
  - 400/533MHz Front Side Bus;
- Memory Controller
  - One DDR200/266 channel
  - Up to 4GB of memory
  - ECC – 128-bit algorithm; 16-bit detection; 8-bit correction
  - Fault isolation

CIOB-X2

- Dual PCI-X Buses; supports PCI 2.2 and PCI-X 1.0
- 64-bit; 33/66/100/133MHz

CSB5

- PCI 2.2 32-bit/33MHz
- Legacy functions (8237 DMA, 8259 PIC, 8254 timer)
- PCI to LPC Bridge
- USB 1.1 interface
- Two ATA channels supporting up to 4 hard disk drives

2.2.3 Memory

The ePCI-200 supports three DIMMs (up to 4Gbytes, limited by the amount of PCI memory used) of DDR200/266 SDRAM. 2.5V registered memory is required.

Signal Paths

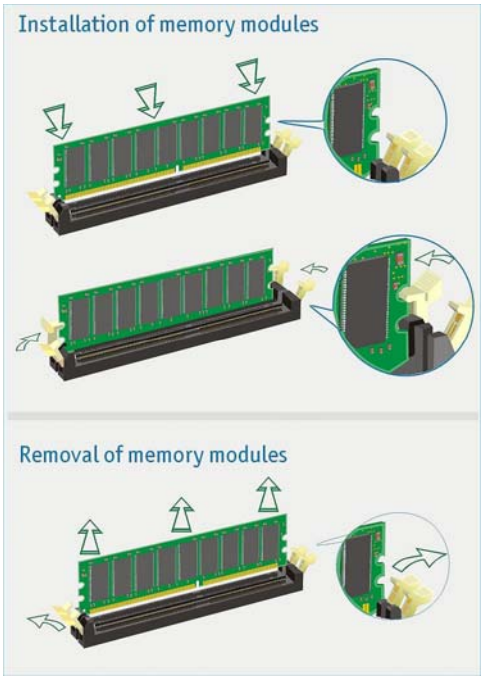
- J17, J18 and J19 DIMM sockets.

Related Jumpers

- W14: CPU front side bus and memory speed.

BIOS Settings

- Advanded \ Advanced Processor Options \ Cache Memory
- Advanced \ Boot Setting Configuration
  - Extended RAM Test Step



2.2.4 Hard Disks Interface

2.2.4.1 Enhanced IDE Interfaces

The ePCI-200 features two channels Bus Master PCI EIDE dedicated to Primary IDE logical interface. Each channel supports up to two devices (including CD-ROMs, hard disks, CompactFlash) with independent timings, in Master/Slave combination.

Signal Paths

- Primary IDE interface: J13 (40-pin header).
- Secondary IDE interface: J14 (40-pin header) and J16 (CompactFlash connector)

Related Jumpers

- W7: when jumper is present, the CompactFlash is in “master” mode, otherwise it is in “slave” mode.

BIOS Settings

- Main
  - Specify disk type
- Advanced \ \ PCI Configuration
  - Local Bus IDE adapter

The IDE interface supports PIO mode 4 transfers up to 14MB/sec and Bus Master IDE transfer up to 100MB/sec (Ultra-DMA 100).

2.2.4.2 CompactFlash Interface

The ePCI-200 board supports an ATA/IDE compatible flash disk by using a CompactFlash carrier module.

The CompactFlash disk connects directly on the secondary IDE interface. It must be configured the same way as a standard hard disk using the BIOS setup program (Autodetect function). There is no driver needed to use a CompactFlash.

CAUTION

1. When using a CompactFlash, the operating temperature must not exceed 50°C/122°F
2. When connecting a CompactFlash on J16 (secondary IDE port) and a hard disk on J14 (header for the secondary IDE port), make sure that you configure one device as master and the other as slave. Two master devices (or two slave devices) must not be installed on the same IDE channel at the same time.
3. Use a cable 40 wires (part # 150-050) in order to get proper detection.

2.2.4.3 USB Interfaces

USB supports Plug and Play and hot swapping operations (OS level). These user-friendly features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.
The SHB fully supports the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible.

Signal Paths

- J8: USB header for both ports.

BIOS Settings

- Advanced \ PCI Configuration
  - USB Host controller
  - USB BIOS Legacy Support

2.3 Ethernet Controllers

Two Intel 82551ER Ethernet controllers are used. This controller supports 10Base-T and 100Base-TX operations: 10Mbps and 100Mbps network speeds are automatically detected and switched.

A useful feature of the 82551ER is the automatic crossover. When connecting an ePCI-200 to another computer, a straight cable can be use and the 82551ER will automatically swap the TX and RX pairs.

Signal Path

- J4 and J5 RJ45 connectors on I/O bracket.

BIOS Settings

- Advanced \ PCI Configuration \ Embedded LAN
  - Onboard Ethernet 1 Controller.
  - OptionROM ScanOnboard Ethernet 2 Controller
  - Option ROM Scan
- Boot
  - Boot from IBA (Intel Boot Agent) only present if Option ROM Scan is Enabled.

2.3.1.1 Boot from LAN

The Boot from LAN capability is supported. To enable the option, use the BIOS Setup program (Boot Menu Selection and Enable Option ROM Scan).

2.3.1.2 Drivers

A CDROM is included with the ePCI-200. It contains network drivers for most common operating systems.

2.4 Video Controller

The onboard ATI Mobility Radeon M6-C16H video interface supplies the video through:

- Standard VGA output located on the faceplate (DB-15 female connector)
- TV-Out or second VGA on 14-pin header with a I/O Mezzanine.
- LVDS panel output on Jumptec JILI 40-pin flex connector.

The video controller with its two independent CRT controllers supports two asynchronous simultaneous display paths (LVDS/CRT, LVDS/TV, CRT/TV and CRT/CRT), with drivers support. Resolution can go up to 1600x1200. BIOS support only (LVDS, CRT1, CRT1/LVDS, TV-OUT) with one display path.

2.4.1 Mobility Radeon M6-C16h Highlights

- Two independent CRT controllers to support two asynchronous simultaneous display paths.
- Dual-channel LVDS interface up to 85MHz per channel. Supports up to XGA resolution.
- Integrated enhanced TV encoder with 10-bit DAC (shared between second CRT DAC and TV)
- Fully compliant with PC 2001 requirements.
- Unique enhanced TCA (Triple-Cache Architecture) incorporates texture, pixel and vertex caches to maximize effective memory bandwidth.
- Bus mastering of 2D&3D display lists.
- Direct walk of Direct3D/OpenGL vertex list.
- Triple 10-bit palette DAC supports pixel rates to 350MHz.

2.4.2 Standard VGA output

Signal Path

- J1 is the primary CRT output.

Related Jumpers

- W9: when present, disable onboard video.

BIOS Settings

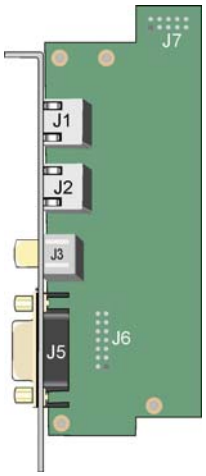
- Advanced \ PCI Configuration
  - Default Primary Video Adapter
  - Onboard Primary Display
  - Onboard LVDS Panel Type

2.4.3 TV-OUT or second VGA output

The Mobility Radeon includes an integrated TV with these TV-out characteristics:

- 10-bit DAC with 8-tap filter producing scaled, flicker removed, artifact suppressed display on a PAL or NTSC TV with Composite output.
- Support for Macrovision 7.02 copy protection standard (required by DVD players) – a fully programmable timing capability, it will accommodate potential changes in the Macrovision algorithm without any hardware changes.
- Line 21 Closed Caption and Extended Data Service support for encoding in Vertical Blanking Interval (VBI) of TV signal.
- CGMS-A DVD copy management support in VBI through Line-20 and/or Extended Data Service (Line-21 Field 2).
- UV filtering based on color averaging results in a sharper picture as well as reduced flicker.
- ATI's exclusive "Composite Dot Crawl" freeze option for PAL and NTSC to improve picture quality.

I/O Mezzanine



Signal Path

- J2 is the secondary CRT and composite/s-video TV output.

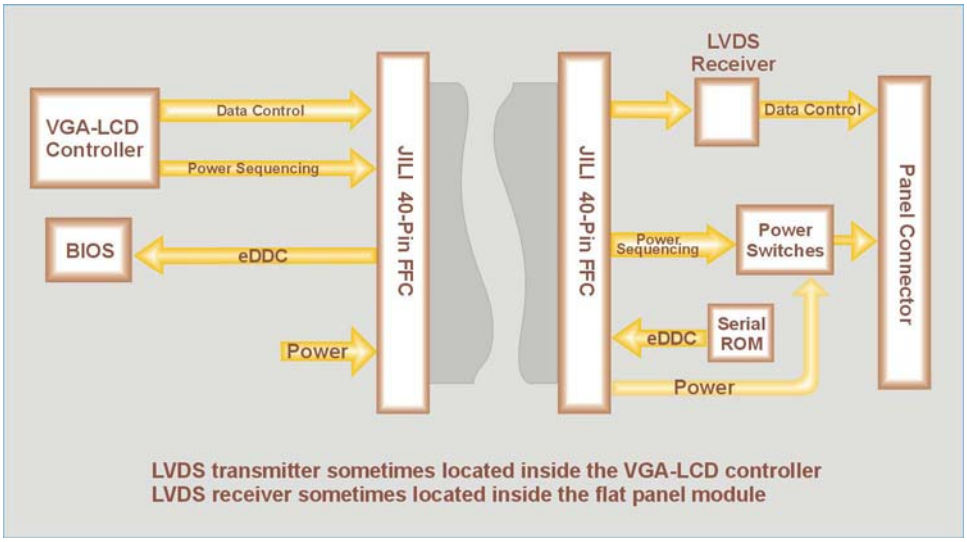
Related Jumpers

- W9: when present, disable onboard video.

BIOS Settings

- Advanced \ PCI Configuration
  - Default Primary Video Adapter
  - Onboard Primary Display
  - Onboard LVDS Panel Type

2.4.4 Flat Panel Interface (JILI)



The JILI interface use LVDS signaling to transmit video data to a LVDS flat panel or a LVDS receiver.

For more information about the JILI interface, please visit the Jumptec web site at the following address: http://www.jumptec.de/product/data/jili/

Signal Path

- J12 is the JILI interface connector for flat panel.

Related Jumpers

- W9: when present, disable onboard video.

BIOS Settings

- Advanced \ PCI Configuration
  - Default Primary Video Adapter
  - Onboard Primary Display
  - Onboard LVDS Panel Type

2.5 Super I/O PC87417

2.5.1 PS/2 Keyboard - PS/2 Mouse Interface

The onboard keyboard controller is 8042 software compatible.

Signal Path

- J3 on I/O bracket: Direct connection for the keyboard. If the mouse is needed use a splitter cable.
- J11: keyboard and mouse on header connector.

BIOS Settings

- Advanced \ Boot Setting Configuration
  - Summary Screen Delay

2.5.2 Multifunction Connector

Standard AT keyboard PS2 mouse, speaker output, reset and hard disk activity LED signals are available on the J11 Multifunction connector.

2.5.3 Parallel Port

The ePCI-200 features one IEEE-1854 multi-mode parallel port. It is compatible with Standard Mode IBM PC/XT, PC/AT, and PS/2 compatible bi-directional parallel port, Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP).

Signal Path

- J15: parallel Port interface on header.

BIOS Settings

- Advanced \ On-Board Devices Configuration
  - Parallel port
  - Mode
  - Interrupt
  - DMA channel (this opion is not used for all mode)

The differences between Standard, EPP, and ECP modes appear in the signal assignation of the pins on the connector.

NOTE
To operate in EPP or ECP mode, ensure the peripheral is designed to work in this mode and the BIOS setup is configured to support it.

2.5.3.1 Ouput only

The Standard mode is unidirectional. It is supported to maintain the compatibility with the IBM PC standard.

2.5.3.2 Bi-directional

2.5.3.3 EPP Mode

The EPP (Enhanced Parallel Port) mode consists of a hardware independent method of accessing a parallel port configured as EPP. It provides support for single I/O cycle as well as the high performance block I/O transfers. The EPP mode always uses the most optimum method for I/O transfers. For example, if the hardware supports it, EPP mode will perform 32-bit I/O block transfers.
EPP mode assumes that the parallel port can be used to connect more than one peripheral device using multiplexer or daisy chain configurations.
A multiplexer is an external device that permits up to eight parallel port devices to share a single parallel port.
A daisy chain device has two ports: input and output. The input port is connected either to the host parallel port or the daisy chain device in front of it. The output is used to connect the next peripheral device to the daisy chain. The last device, however, can be one without daisy chain support.

2.5.3.4 ECP Mode

ECP (Extended Capabilities Port) works the same as EPP mode, but it will take precedence over the EPP mode when addressing multiple logical devices in a single physical product. While the EPP mode may intermix read and write operations without any overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgment from the peripheral.

NOTE

For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department (See appendix G).

2.5.4 Serial Ports

Two full function serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50bps to 115Kbps.

2.5.4.1 Serial Port 1

Serial Port 1 is buffered for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

Signal Path

- J6: serial port 1. RS-232 only.

BIOS Settings

- Advanced \ On-Board Devices Configuration
  - Serial port A
  - Base I/O address

2.5.4.2 Serial Port 2

The serial port 2 is buffered for RS-232, RS-422 or RS-485 operations. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

Signal Path

- J7: serial port 2: RS-232, RS-422 or RS485.

Related Jumpers

- W1 and W2: insert both jumper if serial port 2 is used in RS-422 or RS-485 mode and need termination resistors. Termination resistors are 120-ohm.

BIOS Settings

- Advanced \ On-Board Devices Configuration
  - Serial port B
  - Base I/O address
  - Mode

Mode**Software usage**

- Register 0x190 provide buffer control. See appendix C for details.

2.5.4.2.1 RS-232 Protocol:

When configured for RS-232 operation mode, the Serial Port 2 is 100% compatible with the IBM-AT serial port signals.

2.5.4.2.2 RS-422 Protocol:

The RS-422 protocol (Full Duplex) uses both RX and TX lines simultaneously during a communication session.

CAUTION

In RS-422 mode, W1 and W2 jumper caps must be installed to connect the 120-ohm line termination resistors (See Section 3.1 Setting Jumpers).

2.5.4.2.3 RS-485 Protocol:

During a communication session, the RS-485 protocol (Full Duplex) uses differential signals. It differs from the RS-422 mode as it offers the ability to transmit and receive over the same pair of wires and allows the sharing of the communication line by multiple stations. This configuration (also known as Party Line) allows only one system to take control of the communication line at the time.
In RS-485 mode, the RX lines are used as the transceiver lines and the RTS signal is used to control the direction of the RS-485 buffer.
When set for RS-485 mode in the BIOS, upon power-up or reset, the transceiver is set by default in receiver mode to prevent unwanted disturbance on the line. Party line operation mode requires termination resistors to be installed at both ends of the network.

2.5.5 Floppy Disk Interface

The onboard floppy disk controller is IBM PC XT/AT compatible. It handles 3.5” and 5.25”, low and high-density disks. Up to one drives are supported in any combination.

Signal Paths

- J9: Floppy disk interface on standard header.

BIOS Settings

- Main
  - Select type of drive
- Main Advanced \ On-Board Devices Configuration
  - Floppy Disk Controller
  - Base I/O address

2.6 ATX Power Supply Control

If an ATX power supply is used, the SHB can control it either through its edge connector and the backplane or, if the SHB is used in standalone, through its ATX connector and hardware monitor connector pushbutton input.

Signal Path

- J25: ATX power connector for stand-alone use.
- J10: Hardware monitor connector to connect the pushbutton in stand-alone use.

Related Jumpers

- W4: insert to turn-on the power supply regardless of the pushbutton input. When this is done, the power supply is always on and softoff does not work, you must be disable Soft Off support in BIOS setup to provide OS shutdown correctly.

BIOS Settings

- Power
  - Soft Off Support
  - After Power Failure
  - Wake On PCI PME#

2.7 System Management Features

2.7.1 Power Supply Monitoring

All on-board supplies are monitored and the board is kept in reset if any voltage is out of specification.

Power supply voltages are also monitored and can be viewed in the BIOS setup.

BIOS Settings

- Power \ Intelligent System Monitor
  - Beep Codes for non-Thermal Events
  - Hardware Monitor Voltage Inputs
  - Control Voltage Events

2.7.2 CPU Fan and System Fans Monitoring

The CPU fan and up to six external fans can be monitored.

Signal Path

- J22: CPU fan connector.
- J21: Chipset fan connector (if present).
- J10: hardware monitor connector with 6 inputs for off-board fans.

BIOS Settings

- Power \ Intelligent System Monitor
  - Beep Codes for non-Thermal Events
  - Hardware Monitor Temperature
  - Control Voltage Events

2.7.3 CPU Temperature Monitoring

The Pentium 4 has an internal circuit that monitors the silicone die temperature and slow down the CPU in case of an overheat condition.

When an overheat condition occurs, the overhead LED (red) on the backside of the board is turned ON.

BIOS Settings

- Power \ Intelligent System Monitor
  - Thermal Audio Alarm
  - Hardware Monitor Temperature
  - Control Voltage Events

2.7.4 CPU Switcher Temperature Monitoring

When a high power CPU is used, system airflow is required. In the event of a system fan failure, the on-board CPU switching power supply could overheat and damage itself, the CPU and the chipset.

The ePCI-200 uses a digital thermostat to sense the printed circuit board temperature in the switcher area and slow down the CPU in case of an overheat condition. This is a reflex survival mechanism and, as such, it cannot be disabled. Temperature limit is factory set and cannot be changed.

The overheat LED on the backside of the SHB will turn on when an overheat condition occurs.

2.7.5 System or External Faults Monitoring and Error Reporting

The hardware monitor connector has six fan speed inputs and a pushbutton input for ATX power supply control in a stand-alone configuration.
It provides two inputs that can generate an interrupt as well as two outputs that gives a status information on the SHB and user application software.

Two general purpose I/O pins are also available. They are generic I/O but can be connected to the SHB I^2C controller.

Signal Path

- J10: hardware monitor connector.

Software usage

- Functionality is spread across multiple registers. See appendix C for details.
- See application note AN03002A for I^2C controller usage and a software example on our ftp site at: ftp://ftp.kontron.ca/support/.

BIOS Settings

- Advanced \ Advanced Chipset Control
  - FPGA IRQ

2.7.6 Programmable Dual-Stage Watchdog

The ePCI-200 provides a two-stage digital watchdog with software programmable time-out period.

Following a reset of any source, the watchdog is disabled. The watchdog is enabled by software.

BIOS Settings

- Advanced \ Advanced Chipset Control
  - Enable watchdog automatically before OS launch

Software usage

- See registers 0x190 and 0x196 description in appendix C for details.

See application note AN030001A for watchdog usage.

BIOS Settings

- Advanced \ Advanced Chipset Control
  - Watchdog After POST
  - Watchdog Duration
  - FPGA IRQ

2.7.7 Remote Reset From Serial Port

It is possible to do a hardware reset (equivalent to the reset switch) of the SHB through a serial port. Used in conjunction with the VT100 mode, this can be a very powerful feature for remote operated systems.

The selected serial port incoming data line is monitored. If RXD stay at « space » for more than 100ms (i.e. break condition), the board is reset.

Note that if modems are used, the modems have to be configured to properly repeat the break condition across the telephone line.

Software usage

- See registers 0x190 and 0x192 description in appendix C for details.

2.8 Debugging Features

2.8.1 Thermal Event LED

The red LED on the backside of the SHB turn ON when a CPU overheats condition or a CPU switcher overheats condition is detected. In overheat condition, the CPU run at a speed slower than normal.

2.8.2 Bi-color Debug LED

The SHB has a bi-color LED (on the primary side of the board) that is very useful for debugging. Its meaning is context dependent as shown below.

Time	LED usage
During reset	RED and GREEN are ON. No blinking.
After reset, during the boot process	Postcode blinker (blinking) or bad CPU type indication (GREEN is OFF and RED is ON, no blinking). In the later case, the boot sequence is aborted.
After the boot process, while the operating system is loading.	GREEN reflects hard disk activity and RED is not used.
While the application software is running.	Application software does not use the LED. GREEN reflects hard disk activity and RED is not used.
	Application software uses the LED to display status information.

Software usage

- See register 0x19A description in appendix C for details.

2.8.2.1 Post Code Blinker

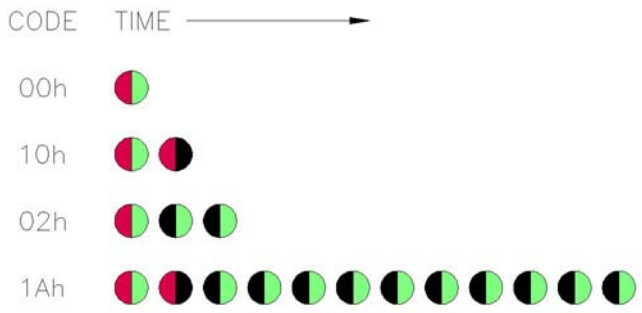
The postcode blinker circuit uses a blinking sequence to display the current post code value. This sequence restarts every time the post codes value changes. Since post codes changes all the time during a normal boot process, the blinker does not have enough time to complete its sequence and the debug LED blinks in a meaningless way.

If the boot process is successful, the post code value has no interest and the BIOS will automatically disable the post code blinker prior to operating system launch.

If the boot sequence fails or the CPU hangs, the postcode blinker will stay operational and will repeat indefinitely the last postcode blink sequence defined below.

1. Blink simultaneously RED and GREEN one time: start of the sequence
2. Blink RED “R” times while GREEN stays off. “R” range from 0 to 15.
3. Blink GREEN “G” times while RED stays off. “G” range from 0 to 15.
4. Repeat the sequence (go to step 1)

“R” is the first (most significant) digit of the post code value in hexadecimal while “G” is the second digit (i.e. post code value is RGh). Some examples are shown in the following figure.



2.8.2.2 Application Software Use of the Debug LED

A status LED can be very useful for software development and for system level troubleshooting. Consult register 0x19A description for software usage (appendix C).

2.8.3 Serial Post Codes

The 8-bit content of I/O address 80h is serialized into a proprietary protocol and output on connector J24. In manufacturing, Kontron use a special display board to de-serialize and display the post code value on 7-segment LEDs modules.

This approach enables us to see post codes prior to PCI initialization and avoid using a PCI postcode display board.

Postcodes can be a useful tool when debugging application software. If the display board (T2603) is of interest to you, ask your Kontron representative for it.

2.8.4 Reset History

When an unwanted reset of the board occurs, it is of interest to know the reset source. The reset history circuit logs reset sources. There are two ways to obtain the reset history:

- Let the BIOS read and clear the reset history and display the reset source in the summary screen.
- The end-user software read and clear the reset history.

BIOS Settings

- Advanced \ Advanced Chipset Control
  - Display and Clear Reset History

Software usage

- See registers 0x191 and 0x192 description in appendix C for details.

2.9 Miscellaneous Features

2.9.1 Simple I²C Controller

The ePCI-200 offers a simple, master-only I^2C controller. It can be used to access an optional on-board EEPROM or off-board I^2C/SMBus devices.

Signal Path

- ePCI-X I^2C/SMBus backplane link.
- Optional on-board EEPROM, consult you Kontron representative.
- J10: hardware monitor connector
- J12: JILI panel interface

Software usage

- See registers 0x1A8 through 0x1AC in appendix C for details.
- See application not AN03002A for I^2C controller usage and a software example.

2.9.2 Silicone Serial Number

A DS2401 silicone serial number comes standard on the ePCI-200. It can be read from register 0x193 (see appendix C).

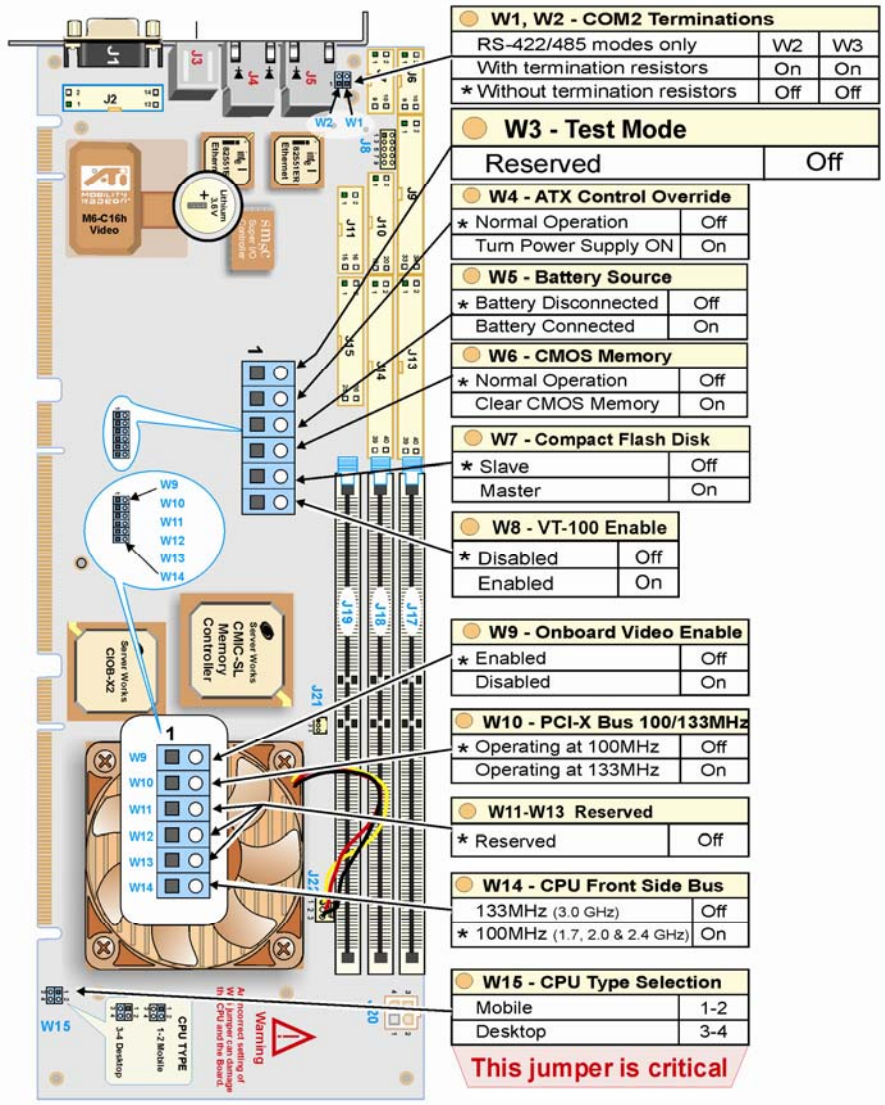
PART 3

3 INSTALLING THE BOARD

1. SETTING JUMPERS
2. PROCESSOR INSTALLATION
3. MEMORY INSTALLATION
4. BATTERY INSTALLATION
5. I/O MEZZANINE INSTALLATION
6. POWER SUPPLY CABLING
7. PCI/PCI-X SETTINGS

3.1 Setting Jumpers

Several jumpers are provided to setup the board. Their functions are summarized below:



3.2 Processor Installation

Always use a processor listed in the approved CPU list below. For high power CPU, make sure that the system provides enough airflow.

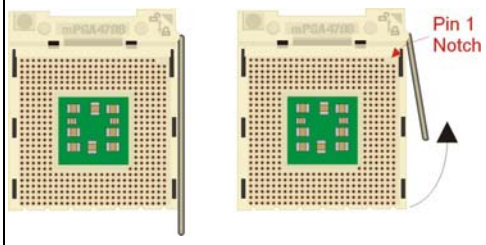
Intel part number	Description
RH80532GC029512 SL6FG	CPU P4 1.7GHZ/400MHZ FCPGA 478 TRAY
RK80532PC041512 SL6GQ	CPU P4 2A GHZ/400MHZ FCPGA2 478 TRAY
RK80532PE056512 SL6DV	CPU P4 2.40B GHZ/533MHZ FCPGA2 478 TRAY

WARNING

STATIC ELECTRICITY

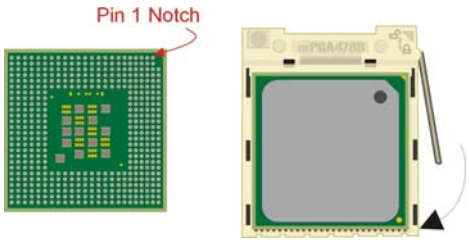
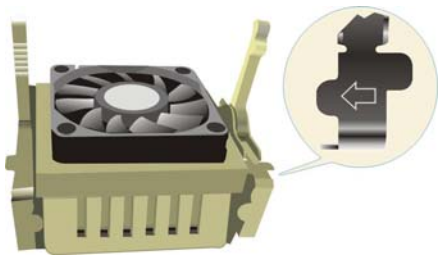
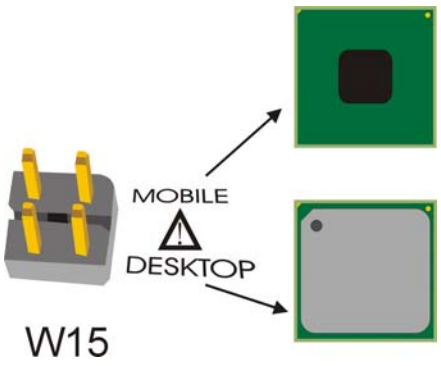
Since static electricity can cause damage to electronic devices, the following precautions should be taken:

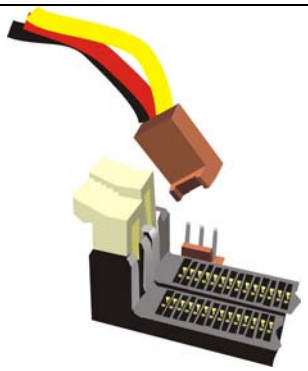
1. Keep the board in its anti-static package, until you are ready to install it.
2. Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.



Raise the Socket Actuation Lever up to 90º.

Locate the Pin 1 Notch.

	Locate the Pin 1 Notch on the CPU. Install the CPU onto Socket (match the pin 1 of CPU with Pin 1 of Socket. Lower the Socket Actuation Lever.
	Install the CPU Heatsink onto the CPU and fix the bracket. Attention : You must apply pressure equally on both side of the heatsink when you fasten the side brackets.
	Make sure jumper W15 is set to the proper CPU type. With some CPU type, a miss-configuration can damage the CPU and the board.

	Connect the CPU Fan cable to the CPU fan connector (J22) located near Memory Sockets.

WARNING

1. Once the CPU is installed you must handle the board carefully and hold it on the heatsink side.
2. The CPU Power cable must be installed on connector J20. If not installed, the board will not start.

WARNING

Make sure jumper W15 is set to the proper CPU type. With some CPU type, a miss-configuration can damage the CPU and the board.

WARNING

To ensure proper immunity against ESD (Electrostatic discharge), the I/O bracket must be carefully grounded to chassis host at both ends.

3.3 Memory Installation

The recommended DIMM devices are listed in the table below.

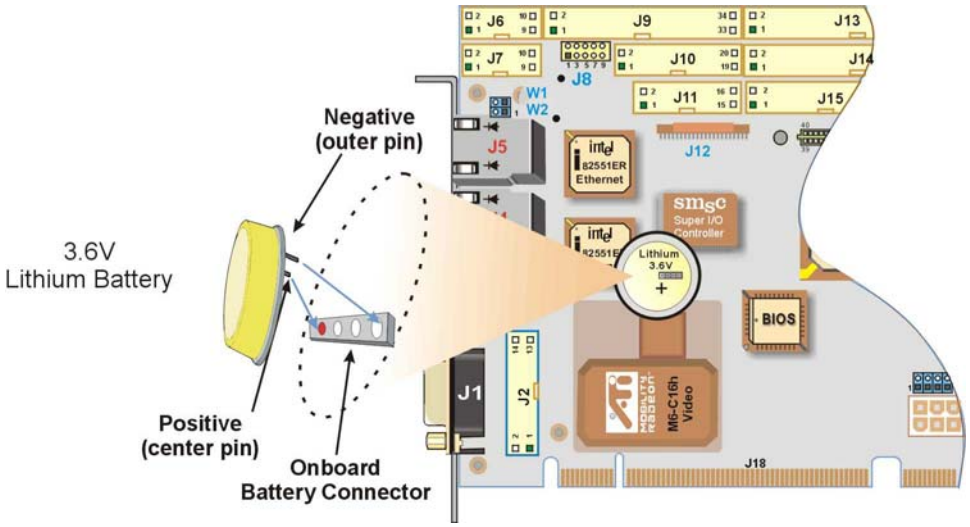
Manufacturer part number	DIMM's description	Manufacturer
M312L6420CT0-CA200	DIMM ECC RSDRAM 512MB 64M*72 DDR266 1.2"	SAMSUNG
M312L6420DT0-CA200	DIMM ECC RSDRAM 512MB 64M*72 DDR266 1.2"	SAMSUNG
UG764D7584KM-EZKA	DIMM ECC RSDRAM 512MB 64M*72 DDR266 1.2"	UNIGEN
VM383L6420E-A2S	DIMM ECC RSDRAM 512MB 64M*72 DDR266 1.2"	VIRTIUM
UG7128D7584KV-EZKA	DIMM ECC RSDRAM 1GB 128M*72 DDR266 1.2"	UNIGEN
M312L2828DT0-CA200	DIMM ECC RSDRAM 1GB 128M*72 DDR266 1.2"	SAMSUNG
M312L2828CT0-CA200	DIMM ECC RSDRAM 1GB 128M*72 DDR266 1.2"	SAMSUNG
VM383L2826E-A2S	DIMM ECC RSDRAM 1GB 128M*72 DDR266 1.2"	VIRTIUM
M312L3223DT0-CA200	DIMM ECC RSDRAM 256MB 32M*72 DDR266 1.2"	SAMSUNG
UG732D7588KZ-DZKA	DIMM ECC RSDRAM 256MB 32M*72 DDR266 1.2"	UNIGEN
M312L3223DT0-CB0	DIMM ECC RSDRAM 256MB 32M*72 DDR266 1.2"	SAMSUNG
VM383L3223E-B0S	DIMM ECC RSDRAM 256MB 32M*72 DDR266 1.2"	VIRTIUM
M312L3223CT0-CA200	DIMM ECC RSDRAM 256MB 32M*72 DDR266 1.2"	SAMSUNG
UG7256D75Q4MQ-EZKA	DIMM ECC RSDRAM 2GB 256M*72 DDR266 1.2"	UNIGEN
VM383L5626E-A2S	DIMM ECC RSDRAM 2GB 256M*72 DDR266 1.2"	VIRTIUM
M312L5628MT0-CA200	DIMM ECC RSDRAM 2GB 256M*72 DDR266 1.2"	SAMSUNG

WARNING

Since static electricity can cause damage to electronic devices, the following precautions should be taken:
Keep the board in its anti-static package, until you are ready to install it.
Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
Handle the board by the edges.

3.4 Battery Installation

An onboard lithium battery is provided to backup BIOS setup values and the real time clock (RTC). The battery must be connected as follows:



NOTE

The board is shipped with W5 (on board enable/disable battery jumper) not installed. Install this jumper prior to run the ePCI-200.
Running the board without installing W5 will cause a CMOS memory error.

WARNING

Danger of explosion if battery is incorrectly replaced

Replace only with the same or equivalent type of battery recommended by the manufacturer. Dispose of used batteries according to the instructions of the manufacturer.

The battery specifications are as follows: 3.6V Lithium battery, 0.37A/h

Signal Path

- BT1: Polarized battery holder

Related Jumpers

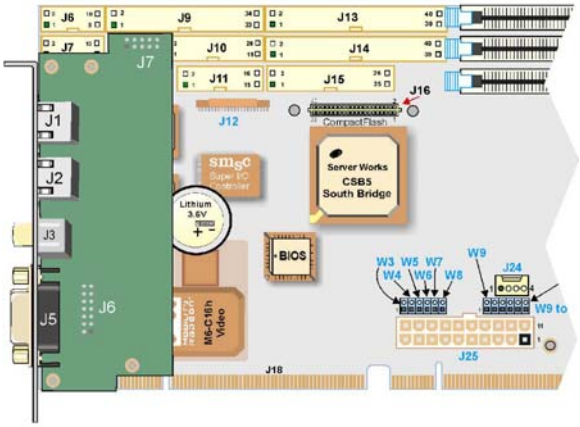
- W5: Battery connection. A jumper must be present for normal operation.

Connect the battery to the BT1 header. The positive terminal of the battery holder is located at the bottom center.

3.5 I/O Mezzanine Installation

To Install the I/O Mezzanine, you have to:

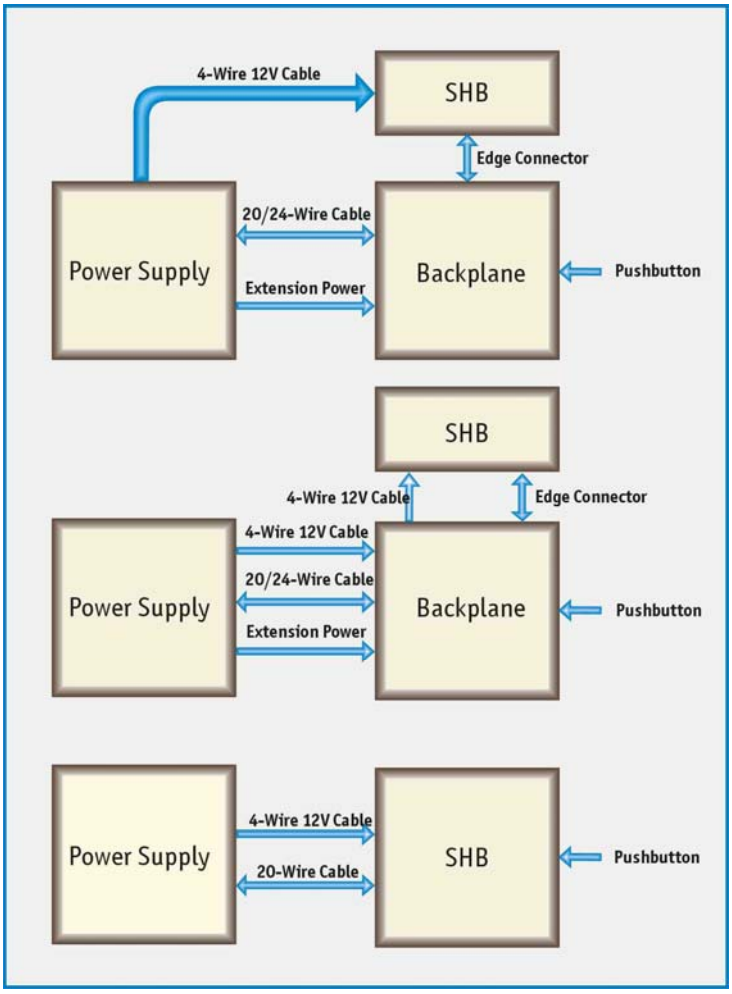
- Place the ePCI-200 board in front of you so the faceplate is facing you.
- Remove the two screws that are on the two metallic standoffs under the mezzanine
- Inline J2 header from the ePCI-200 with J6 on the I/O mezzanine and J8 header from the ePCI-200 with J7 on the I/O mezzanine.
- When these two connectors are connected, flip the ePCI-200 and put back the two screws that you have removed before to fix the mezzanine to the ePCI-200.



3.6 Power Supply Cabling

The three ways to power the SHB are shown in the following figure.

1. Through a backplane with a direct connection for the CPU power.
2. Same as 1 but using the backplane facility for the CPU power because power supply cable is too short.
3. In stand-alone.



3.7 PCI/PCI-X Settings

PCI bus "A" being restricted to 33MHz PCI, there are no special settings for this bus. Bus "B" will normally auto-configured itself at reset time to run at the fastest mode supported by all PCI devices on the bus.

For test purpose, it is possible to force bus "B" to operate in conventional PCI instead of PCI-X and to downclock the bus frequency. It is not possible to use the bus at a faster speed than the auto-detection mode.

			PCI		PCI-X	
W11	**W12**	**W13**	**33MHz**	**66MHz**	**66MHz**	**100/133MHz**
out	out	out	Possible	Possible	Possible	Possible
in	out	out	Possible	Prohibited	Possible	Possible
out	out	in	Possible	Possible	Possible	Prohibited
out	in	in	Possible	Possible	Prohibited	Prohibited
in	in	in	Possible	Prohibited	Prohibited	Prohibited

When the bus operates at maximum PCI-X speed, the bus can run at 100 or 133MHz. A single jumper selects 100 or 133MHz maximum speed as follow.

W10	Maximum PCI-X frequency
out	100MHz (default)
in	133MHz

Select the maximum PCI-X frequency according to your backplane documentation. In doubt, leave it to 100MHz.

PART 4

4 SOFTWARE SETUP

1. PHOENIX BIOS SETUP PROGRAM
2. BOOT UTILITIES
3. INSTALLING DRIVERS
4. CONSOLE REDIRECTION

4.1 PHOENIX BIOS Setup Program

All relevant information for operating the board and connected peripherals is stored in the CMOS memory. A battery-backed up memory holds this information when the board is powered off, the BIOS Setup program is required to make changes to the setup.

NOTE

Make sure you setup the BIOS Setup software prior to installing your operating system and your drivers.

For systems that need the BIOS to first attempt to boot from LAN, follow these steps:

Set the “Network Boot”, IBA (Intel Boot Agent) or “Landesk Service Agent II” as the first boot service in the BIOS setup (Boot Menu Selection).

4.1.1 Accessing the BIOS setup program

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the ePCI-200 peripheral processor. The ePCI-200 uses the Phoenix Setup program, a setup utility in flash memory that is accessed by pressing the <DELETE> key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

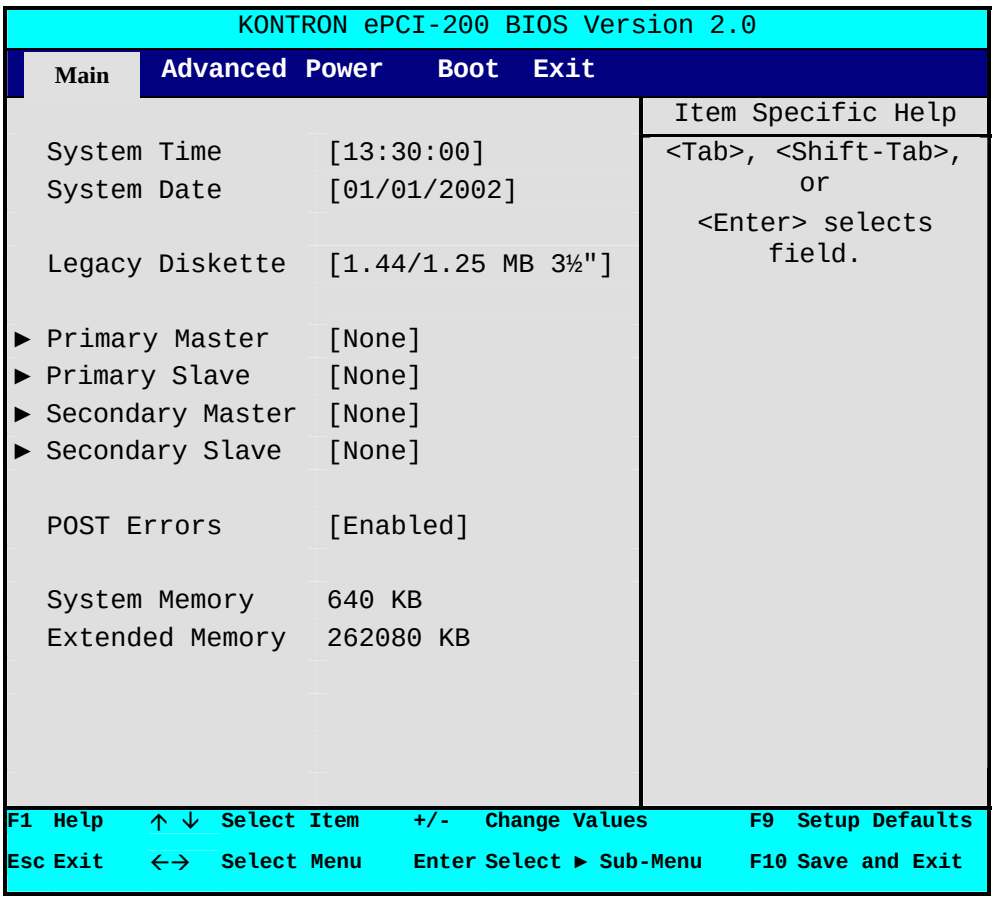
> ➢ **CAUTION**
>
> Before modifying CMOS setup parameters, ensure that the W5 battery selection jumper is installed to enable the CMOS battery back up.

To run the Phoenix Setup program incorporated in the ROM BIOS:

- Turn on or reboot the system.
- When you get the following message in bottom of screen, hit <DELETE> key to enter SETUP

```
Press <DEL> to enter SETUP
```

4.1.1.1 The main menu of the Phoenix BIOS CMOS Setup Utility appears on the screen.



Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the SETUP defaults will affect all parameters and will reset options previously altered.

The Setup Defaults values provide **optimum performance** settings for all devices and system features.

CAUTION

These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

NOTE

The CMOS setup option described in this section is based on **BIOS Version 2.0**. The options and default settings may change in a new BIOS release.

4.1.1.2 The Menu Bar

The Menu bar at the top of the window lists these selections:

Menu selection	Description
Main	Use this menu for basic system configuration
Advanced	Use this menu to set the Advanced Features available on your system
Power	Use this menu to configure Power Management features and system monitoring
Security	Use this menu to configure Security features
Boot	Use this menu to determine the booting device order.
Exit	Use this menu chose Exits option

Use the left and right ← and → arrows keys to make a selection.

4.1.1.3 The Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates:

Key	Function
<F1> or <Alt-H>	General Help windows (see 4.1.2.2)
<Esc>	Exit this menu.
← → arrow keys	Select a different menu
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to top or bottom of window.
<F5> or <->	Select the Previous Value for the field.
<F6> or <+> or <Space>	Select the Next Value for the field.
<F9>	Load the Default Configuration values for all menus
<F10>	Save and exit.
<Enter>	Execute Command, display possible value for this field or Select the Sub menu

To select an item, use the arrow keys to move the cursor to the field your want. Then use the plus-and-minus value keys to select a value for that field. To save values commands in the Exit Menu save the values currently displayed in all the menus.

To display a sub-menu, use the arrow keys to move the cursor to the sub menu your want. Then press <Enter>. A pointer (►) marks all sub menus.

4.1.1.4 The Field Help Window

The help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field.

4.1.1.5 The General Help Windows

Pressing <F1> or <Alt-H> on any menu brings up the General Help window that describes the legend keys and their alternates:

```
                    General Help

Setup changes system behavior by modifying the BIOS
configuration. Selecting incorrect values may
cause system boot failure; load Setup Default values to
recover.

<Up/Down> arrows select fields in current menu.
<PgUp/PgDn> moves to previous/next page on scrollable menus.
<Home/End> moves to top/bottom item of current menu.

Within a field, <F5> or <-> selects next lower value and
<F6>, <+>, or <Space> selects next higher value.

<Left/Right> arrows select menus on menu bar.
<Enter> displays more options for items marked with ▪ .

<F9> loads factory installed Setup Default values.
<F10> saves current settings and exists Setup.

<Esc> or <Alt-X> exits Setup; in sub-menus, pressing these keys
returns to the previous menu.

<F1> or <Alt-H> displays General Help (this screen).

                        [Continue]
```

4.1.2 Main Menu Selection

The scroll bar on the right of any windows indicates that there is more than one page of information in the windows. Use <PgUp> and <PgDn> to display all the pages. Pressing <Home> and <End> displays the first and last page. Main Menu Selection

You can make the following selections on the Main Menu itself. Use the sub menus for other selections.

Feature	Options	Description
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.
Legacy Diskette A:	Disabled 360Kb 5.1/4” 1.2MB, 5.1/4” 720 Kb 3 1/2” 1.44/1. 25 MB 3 1/2” 2.88 MB 3 1/2	Select the type of floppy disk drive installed in your system. **Note :** 1.25MB 3 1/2” references a 1024 byte/sector Japanese media format. The 1.25MB, 3 1/2 diskette requires a 3-Mode floppy-disk drive.

Feature	Options			Description
Primary Master	Type	None		None : No booting device installed.
		CD-ROM	Multi-Sector Transfers LBA Mode Control 32 BIT I/O Transfer Mode Ultra DMA Mode SMART Monitoring	**Multi-Sector Transfers** Choices : Disabled, 2,4,8, and 16 sectors Any selection except Disabled determines the number of sectors transferred per block. Standard is 16 sectors per block. **LBA Mode Control** Choices : Disabled, Enabled Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, heads, and Sectors. **32 Bit I/O** Choices : Disabled, Enabled Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus. **Transfer Mode** Choices : Standard, Fast PIO 1, Fast PIO 2, Fast PIO 3, Fast PIO 4, FPI0 3 / DMA 1, FPIO 4 / DMA2. Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform. **Ultra DMA Mode** Choices : Disabled, Mode 0, 1, 2, 3, 4. Select the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode. **SMART Monitoring** Display type of Monitoring. This field is a “Display Only”. This option can be changed in the Advanced Menu.
		ATAPI Removable		Same choices as CD-ROM

Main Menu Selection (continued)

Feature	Options			Description
Primary Master (Continued)	Type (continued	IDE Removable		Same choices as CD-ROM
		Other ATAPI		Same choices as CD-ROM
		(USER)	Cylinders	**Cylinders** Set the number of cylinders
			Heads	**Heads** Set the number of heads. Choices are 1 to 16
			Sectors	**Sectors** Set the number of sectors per track
			Maximum Capacity	**Maximum Capacity** Maximum capacity is displayed according to the cylinders, heads and sectors selected.
			Multi-Sector Transfers	**Multi-Sector Transfers** Choices are : Disabled, 2, 4, 8 and 16 sectors. Specify the number of sectors per block for multiple sector transfers. "MAX" refers to the size the disk returns when queried.
			LBA mode Control	**LBA Mode Control** Choices are : Enabled, Disabled Enabling LBA cause Logical Block Addressing to be used in place of Cylinders Heads and Sectors
			32 Bit I/O	**32 Bit I/O** Choices are : Enabled, Disabled. This setting enables or disables 32 bit IDE data transfers.
			Transfer Mode	**Transfer Mode** Choices are : Standard, Fast PIO 1, Fast PIO 2, Fast PIO 3, Fast PIO 4, FPI0 3 / DMA 1, FPIO 4 / DMA2. Select the method for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.
			Ultra DMA Mode	**Ultra DMA Mode** Choices are: Disabled, Mode 0 to 4. Select the Ultra DMA mode used for moving data to/from the drive Autotype the drive to select the optimum transfer mode.
			SMART Monitoring	**SMART Monitoring** IDE Failure Prediction

Main Menu Selection (continued)

Feature	Options		Description
		Auto	BIOS auto-detects the hard disk installed
Primary Slave			Same as Primary Master
Secondary Master	Same as Primary Master		
Secondary Slave	Same as Primary Master		
POST Errors	Enabled Disabled		Pauses and displays SETUP entry or resume boot prompt if error occurs on boot. If disabled, system always attempts to boot.
System Memory			Displays the amount of RAM memory available before 1 Mbyte.
Extended Memory	Depends on the memory installed on your computer		Displays the amount of RAM memory detected during boot up minus the base memory (1 Mbyte).

4.1.2.1 Advanced Menu Selection

You can make the following selections on the Advanced Menu. Use the sub menus for other selections.

Feature	Options	Description
Boot Setting Configuration	**This is a Sub-Menu, see section 4.1.2.1.1**	Additional setup menus to configure Boot Setting.
PCI Configuration	**This is a Sub-Menu, see section 4.1.2.1.2**	Additional setup menus to configure PCI device.
On-board Device Configuration	**This is a Sub-Menu, see section 4.1.2.1.3**	Peripheral Configuration
Advanced Chipset Control	**This is a Sub-Menu, see section 4.1.2.1.4**	Select Options for Advanced Chipset feature.
Console Redirection	**This is a Sub-Menu, see section 0**	Additional setup menus to configure console. Useful sequences: Esc O P = F1 ESC [2 0 ~ = F9 ESC O p = F10 Esc Del = Warm Restart
Advanced Processor Options	**This is a Sub-Menu, see section 4.1.2.1.6**	

4.1.2.1.1 Boot Setting Configuration

You can make the following selections on the Boot Setting Configuration Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
Installed O/S	Other Win95 Win98 WinMe Win2000	Other : General Setting Win95/Win98/WinMe/Win2000: Specific Settings **Note :** An incorrect setting can cause some operating systems to display unexpected behavior.
Enable ACPI	No Yes	Enable/Disable ACPI BIOS (Advanced Configuration and Power Interface).
Reset Configuration Data	No Yes	Select "Yes" if you want to clear the Extended System Configuration Data (ESCD) area.
Boot-time Diagnostic Screen	Enabled Disabled	Displays the Diagnostic Screen during Boot. Always Enabled when Console Redirection is activated.
Hot Key Help Over Logo	Enabled Disabled	Display Hot Key Help Over Logo.
Extended RAM Test Step	Every Location First KB First 64 KB	Select how will perform Extended Memory tests. First KB : Test First KB of each MB. First 64 KB : Test First 64 KB of each MB.
Summary Screen Delay	None 5 seconds	Delay to display the system configuration at boot time.
Save CMOS in FLASH	Disabled Enabled	Saving CMOS memory content into Flash Memory will prevent loosing CMOS options when battery fails.
Retry Boot Sequence	Disabled Enabled	Enable this option to Retry the Boot sequence until a successful boot. (infinite Retry)
PS/2 Mouse	Disabled Enabled	"Disabled prevent any installed PS/2 mouse from functioning, but frees up IRQ 12."Enabled forces the PS/2 mouse port to be enabled regardless if a mouse is present.
Use Multiprocessor Specification	1.1 1.4	Configures the multiprocessor specification (MPS) revision level. Some operating systems will require revision 1.1 for compatibility reasons.

4.1.2.1.2 PCI Configuration

You can make the following selections on the PCI Configuration Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
Embedded LAN	**This is a Sub-Menu, see section 4.1.2.1.2.1**	Additional setup menus to configure embedded Ethernet Controller
PCI Performance setting	**This is a Sub-Menu, see section 4.1.2.1.2.2**	Additional setup menus to configure PCI Performance settings.
Default Primary Video Adapter	External OnBoard	Select "External to have a PCI video card (must be installed) to be set as the Boot Display Device. Select "Onboard" to have the OnBoard video controller as the Boot Display Device.
Onboard Primary Display	LVDS CRT1 CRT1/LVDS TV-OUT	Onboard primary display will only work for device attached to ATI M6 onboard video chip. Usage of external video card as primary adapter will void this option.
Onboard LVDS Panel Type	Auto(JILI) 800x600 1024x768(1CH) 1024x768(2CH) 1280x1024 1400x1050 1600x1200	Auto requires a JILI adapter. If the JILI adapter is missing or does not correspond to your hardware, panel type is automatically set to none. ******* WARNING ******** Improper selection of panel type may damage your panel. Some panels may not work with the fixed resolution tables.
Delay before PCI Initialization	1 to 7	Delay in seconds before PCI Initialization. Some external cards may require a minimum delay after reset before they can accessed. Cards with onboard CPU that emulate a PCI Controller (ex.: RAID) are more likely to require a delay.
Local Bus IDE adapter	Disabled Both	Enabled the integrated local bus IDE adapter.
USB Host Controller	Enabled Disabled	Enables or Disable the USB hardware (Disabled resources will be freed up for other uses).
USB BIOS Legacy Support	Auto Enabled Disabled	Enables or Disables support for USB devices. (Enable for use with a non-USB aware Operating System or boot from a USB device) Select Auto to Enable USB Legacy ONLY if BIOS does not detect PS/2 keyboard. This option does not support boot from USB.

4.1.2.1.2.1 Embedded LAN

Feature	Options	Description
Onboard Ethernet 1 Controller		Enables/Disables Onboard Ethernet 1 Controller on Bus 00 and Device 01.
Option ROM	Enabled Disabled	Initialize device expansion ROM
Onboard Ethernet 1 Controller		Enables/Disables Onboard Ethernet 1 Controller on Bus 00 and Device 02.
Option ROM	Enabled Disabled	Initialize device expansion ROM

4.1.2.1.2.2 PCI Performance Setting

Feature	Options	Description
PCI Bridges Cache Line Size	**0** 2 8 16	**Set the Cache Line Size in DWORDS.**

4.1.2.1.3 On-board Device Configuration

You can make the following selections on the On-board Device Configuration Sub-Menu.

Feature	Options	Description
Serial port A	Enabled Disabled Auto	Configure serial port A using options: **Disabled :** No configuration **Enabled :** User configuration **Auto :** BIOS or OS chooses configuration
Base I/O address	3F8/IRQ 4 2F8/IRQ 3 3E8/IRQ 4 2E8/IRQ 3	Sets the base I/O address for serial port A.
Serial port B	Enabled Disabled Auto	Configure serial port B using options: **Disabled :** No configuration **Enabled :** User configuration **Auto :** BIOS or OS chooses configuration
Mode	RS-422 RS-485 RS-232	Set the mode for Serial Port B.
Base I/O address	3F8/IRQ 4 2F8/IRQ 3 3E8/IRQ 4 2E8/IRQ 3	Sets the base I/O address for serial port B.
Parallel port	Enabled Disabled Auto	Configure Parallel port using options: **Disabled :** No configuration **Enabled :** User configuration **Auto :** BIOS or OS chooses configuration
Mode	Output only Bi-directional EPP ECP EPP & ECP	Set the mode for the parallel Port using option: Output only Bi-directional EPP ECP
Base I/O address	378, 278 or 3BC	Sets the base I/O address for Parallel port.
Interrupt	IRQ5 or IRQ7	Sets the interrupt for Parallel port.
DMA channel	DMA 1 or DMA 3	Sets the DMA channel for Parallel port.
Floppy Disk Controller	Enabled Disabled Auto	Configure Floppy Disk Controller using options: **Disabled :** No configuration **Enabled :** User configuration **Auto :** BIOS or OS chooses configuration

4.1.2.1.4 Advanced Chipset Control

You can make the following selections on the Advanced Chipset Control Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
Watchdog After POST	Disabled Enabled	Enables the Watchdog circuit after the POST sequence. Application software must refresh the Watchdog to prevent System Reset.
Watchdog Duration	16 seconds 1 minute 4 minutes	Select the duration time of the Watchdog timing circuitry.
FPGA IRQ	Disabled IRQ 5 IRQ 7	Select FPGA IRQ for WATCHDOG, I^2C controller, Fan Fault and External Fault events.
Display and Clear Reset History	Enabled Disabled	Enable/disable Display FPGA Reset History in Summary Screen and Clear FPGA History.

4.1.2.1.5 Console Redirection

You can make the following selections on the Console Redirection Sub-Menu.

Feature	Options	Description
Console Redirection	Disabled Enabled	If enabled, Console Redirection work withou the VT100 jumper to use the console Redirection. This option is only used when jumper is not present.
Com Port Address	On-board COMA On-Board COMB	Install the VT100 jumper to enable the Console Redirection using the selected port.
Baud Rate	300, 1200, 2400, 9600, 19.2K, 38.4K, 57.6K, 115.2K	Enables the specified baud rate.
Console Type	VT-100 VT-100, 8bit PC-ANSI, 7bit PC ANSI	Enables the specified console type.
Flow Control	None XON/XOFF CTS/RTS	Enables Flow Control
Continue C.R. after POST	Off, On	Enables Console Redirection after OS has loaded.

4.1.2.1.6 Advanced Processor Options

You can make the following selections on the Console Redirection Sub-Menu.

Feature	Options	Description
Cache Memory	**This is a Sub-Menu, see section 4.1.2.1.6.1**	Determines how to configure the specified block of memory.
Speed Step Support	POM BOM	BOM: Battery Optimized Mode (lower power, low frequency). POM: Performance optimized mode (high power, high frequency).
Hyper-Threading Technology	Disabled Enabled	Enabled for Windows XP and Linux 2.4.x (OS optimized for Hyper-Threading Technology). Disabled for other OS (OS not optimized for Hyper-Threading Technology).

4.1.2.1.6.1 Cache Memory

You can make the following selections on the Cache Memory Sub-Menu.

Feature	Options	Description
Memory Cache	Enabled Disabled	Sets the state of memory cache.
Cache System BIOS area	Uncached Write Protect	Controls caching of system BIOS area.
Cache Video BIOS area	Uncached Write Protect	Controls caching of video BIOS area.
Cache Base 0-512K	Uncached Write Through Write Protect Write Back	Controls caching of 512K base memory.
Cache Base 512K-640K	Uncached Write Through Write Protect Write Back	Controls caching of 512K-640K base memory.
Cache Extended Memory Area	Uncached Write Through Write Protect Write Back	Controls caching of system memory.

4.1.2.2 Power Menu Selection

You can make the following selections on the Advanced Menu. Use the sub menus for other selections.

Feature	Options	Description
Intelligent System Monitoring	**This is a Sub-Menu, see section 4.1.2.2.1**	
Soft Off Support	**Enabled** **Disabled**	Enable this option to use the Power Button feature.
After Power Failure	**Stay Off** **Last State**	[[Stay Off] Keep the power off until the power button is pressed. [Last State] Restores the previous power state after power loss occurred. Note: Last State work only with battery.
Wake On PCI PME#	**Disabled** **Enabled**	Enable this option to Wake from S5 (Soft Off) with PCI PME#.

4.1.2.2.1 Intelligent System Monitoring

You can make the following selections on the Intelligent System Monitoring Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
Delay prior to enabling the TCC	Disabled 2 Minutes 4 Minutes 8 Minutes 16 Minutes 32 Minutes	The Thermal Control Circuit (TCC) must be disabled just prior to transferring control to the Operating System. System's timing calibration to complete accurately.
Chassis Instruction	Disabled Enabled	Enables/Disables detection of Chassis Intrusion.
Secured Chassis	Disabled Enabled	Controls the Secure Chassis feature. If set to Enable and a Chassis Intrusion is detected, the user is required to enter SETUP and set the option "Reset Chassis Intrusion" to "Yes", before the system is allowed to complete the boot.
Reset Chassis Intrusion	Yes No	Selecting 'Yes' will reset the Chassis Intrusion.
Beep codes for non-thermal events	Disabled Enabled	Produces beep codes when the Intelligent System Monitoring events occur for either the chassis, the fan or the voltages. Codes are as follows: One long beep plus: 2 short beeps for chassis intrusion 3 short beeps for fan events 4 short beeps for voltage events This alarm may not be supported by the operating system.
Hardware Monitor Temp. and Fans	**This is a Sub-Menu, see section 4.1.2.2.1.1**	
Hardware Monitor Voltage Inputs	**This is a Sub-Menu, see section 0**	
Control Temperature Events	**This is a Sub-Menu, see section 0**	
Control Voltage Events	**This is a Sub-Menu, see section 0**	

4.1.2.2.1.1 Hardware Monitor Temp. and Fans.

Feature	Options	Description
System board Temperature	**Displays a Status and limit set in other menu.**	
CPU 1 Die Temperature		
Fan CPU 1 (RPM)		
Fan Chipset (RPM)		
Fan Tach. 1 (RPM)		
Fan Tach. 2 (RPM)		
Fan Tach. 3 (RPM)		
Fan Tach. 4 (RPM)		
Fan Tach. 5 (RPM)		
Fan Tach. 6 (RPM)		

4.1.2.2.1.2 Hardware Monitor Voltage Input.

Feature	Options	Description
Vcore	**Displays a Status and limit set in other menu.**	
Vcc3 3.3V		
Vcc 5V		
Vin 2.5V		
Vtt		
Vin 1.5V		
Vbat		
Vin 12V		
Vin -12		
VGA Vdd 1.8		

4.1.2.2.1.3 Control Temperature Events.

Feature	Options	Description
Fan CPU 1 Interrupt	Enabled Disabled	This option enables Temperature events handling.
Fan Chipset Interrupt	Enabled Disabled	This option enables Temperature events handling.
Fan Tach. 1 Interrupt	Enabled Disabled	This option enables Temperature events handling.
Fan Tach. 2 Interrupt	Enabled Disabled	This option enables Temperature events handling.
Fan Tach. 3 Interrupt	Enabled Disabled	This option enables Temperature events handling.
Fan Tach. 4 Interrupt	Enabled Disabled	This option enables Temperature events handling.
Fan Tach. 5 Interrupt	Enabled Disabled	This option enables Temperature events handling.
Fan Tach. 6 Interrupt	Enabled Disabled	This option enables Temperature events handling.

4.1.2.2.1.4 Control Voltage Events.

Feature	Options	Description
Vcore Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vcc3 3.3V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vcc 5V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vin 2.5V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vtt Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vbat Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vin 1.5V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vin 12V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vin -12 Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
VGA Vdd 1.8V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.

4.1.2.3 Security Menu Selection

You can make the following selections on the Advanced Menu. Use the sub menus for other selections.

Feature	Options	Description
Set User Password	Enter Password	User Password controls access to the system at boot
Set Supervisor Password	**Enter Password**	Supervisor Password controls access to the setup utility
Password on boot	**Disabled** **Enabled**	Enables password entry on boot.
Fixed disk access	**Normal** **Write Protect**	Write protects boot sector on hard disk to protect against viruses.
Diskette access	**User** **Supervisor**	Controls access to diskette.

4.1.2.4 Boot Menu Selection

Feature	Options	Description
	Hard Drive Bootable Add-in Cards Primary Master - (PM) Primary Slave - (PS) Secondary Master - (SM) Secondary Slave - (SS) SCSI drive Removable Devices Legacy Floppy Drives CD-ROM Drive IBA 4.0.19 Slot XXXX	Keys used to view or configure devices: **<Enter>** expands or collapses devices with a **+** or **–** **<Ctrl+Enter>** expands all **<Shift + 1>** enables or disables a device **<+>** or **<->** moves the device up or down **<n>** May move removable device between Hard Disk or Removable Disk **<d>** Remove a device that is not installed. ***** Note : The hard drives and SCSI drives detected will be listed in this section and the first drive in the list will be the boot drive.

4.1.2.5 Exit Menu Selection

Feature	Options		Description
	Exit Saving Changes	Yes / No	**Exit Saving Changes** Setup and save your changes to CMOS.
	Exit Discarding Changes	Yes / No	**Exit Discarding Changes** Exit utility without saving Setup data to CMOS.
	Load Setup Defaults	Yes / No	**Load Setup Defaults** Exit utility without saving Setup data to CMOS.
	Discard Changes	Yes / No	**Load Setup Defaults** Load default values for all SETUP items.
	Saves Changes	Yes / No	**Discard Changes** Load previous values from CMOS for all SETUP items.
			Save Changes Save Setup Data to CMOS.

4.2 Boot Utilities

Phoenix Boot Utilities are: Phoenix QuietBoot™
Phoenix MultiBoot™

Phoenix QuietBoot displays a graphic illustration rather than the traditional POST messages while keeping you informed of diagnostic problems.

Phoenix MultiBoot is a boot screen that displays a selection of boot devices from which you can boot your operating system.

4.2.1 Phoenix Quiet Boot

Right after you turn on or reset the computer, Phoenix QuietBoot displays the QuietBoot Screen, a graphic illustration created by the computer manufacturer instead of the text-based POST screen, which displays a number of PC diagnostic messages.

To exit the QuietBoot screen and run Setup, display the Multiboot menu, or simply display the PC diagnostic messages, you can simply press one of the hot keys described below.

The QuietBoot Screen stays up until just before the operating system loads unless:

1. You press <ESC> to display the POST screen.
2. You press <Del> to enter Setup.
3. POST issues an error message.
4. The BIOS or an option ROM requests keyboard input.

The following explains each of these situations.

4.2.1.1 Press <ESC>

1. Pressing <ESC> switches the POST screen and The boot process continues with the text-based POST screen until the end of POST, and then displays the BootFirst Menu, with these options:
   a. Load the operating system from a boot device of your choice.
   b. Enter Setup.
   c. Exit the Boot First Menu (with <ESC>) and load the operating system from the boot devices in the order specified in Setup.

4.2.1.2 Press <Del>

Pressing < Del > at any time during POST enter Setup. (after keyboard initialization)

4.2.1.3 POST Error

Whenever POST detects a non-fatal error, QuietBoot switches to the POST screen and displays the errors. It then displays this message:

Press <F1> to resume, <Del> to Setup

Press <F1> to continue with the boot. Press <Del> if you want to correct the error in Setup.

4.2.1.4 Keyboard Input Request

If the BIOS or an Option ROM (add-on card) requests keyboard input, QuietBoot switches over to the POST screen and the Option ROM displays prompts for entering the information. POST continues from there with the regular POST screen.

4.2.2 Phoenix Multiboot

Phoenix Multiboot expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, or CDROM. You can select your boot device in Setup, or you can choose a different device each time you boot during POST by selecting your boot device in **The Boot First Menu**.
Multiboot consists of:

The Setup Boot Menu
The Boot First Menu

4.3 Installing Drivers

4.3.1 Video Drivers

Various drivers are provided for different operating systems and software. To install a driver, refer to the Setup program located on the CD-ROM (provided with your board).

4.3.2 Ethernet Drivers

Various drivers are provided for different operating systems and software. To install a driver, use the Setup program and the ReadMe.bat file located on the CD-ROM (provided with your board).

4.3.3 Other Drivers

For other operating system drivers and installation instructions or for more information, contact Kontron's Technical Support department.

4.4 Console Redirection (VT100 Mode)

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

4.4.1 Requirements

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix© or Procom© can also be used.

4.4.2 Setup & Configuration

Follow these steps to set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the "Advanced" page, "Console Redirection" menu.
3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable as shown in the next page.

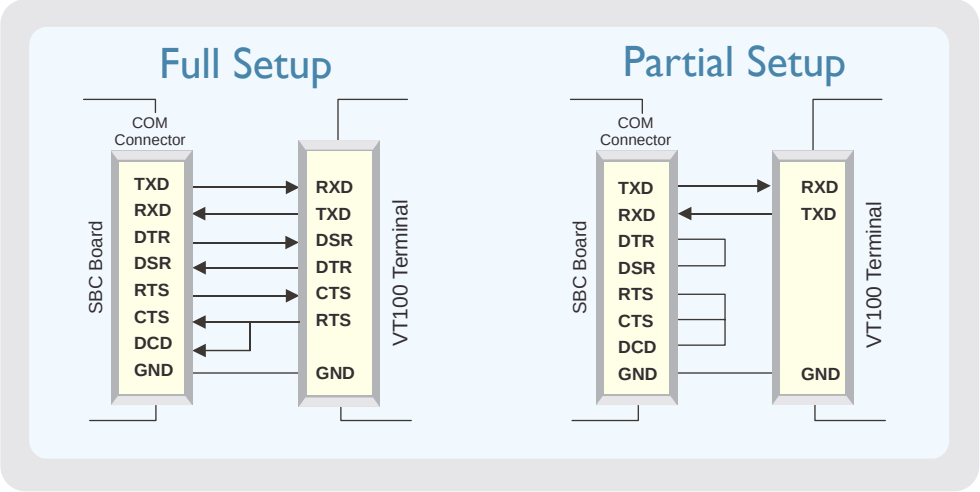
NOTE

If you do not require a full cable for your terminal, you can set up a partial cable by using only the TxD and RxD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

5. Configure your terminal to communicate using the same parameters as in CMOS Setup.
6. Install the VT100 jumper. Reboot the board.
7. Use the remote keyboard and display to setup the BIOS.

Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.

Console Redirection is done by refreshing the Video address @ B8000h at the selected BAUD rate. This means that a low baud rate refreshes the screen slowly, but the CPU time is maximized for the applications. A high BAUD rate refreshes the screen rapidly but the CPU is frequently interrupted by the Serial Port.



Console Redirection provided by Phoenix based BIOS offers various escape sequences to emulate keyboard function keys. The following table lists the escape sequences available.

Escape sequence	Function		Escape sequence	Function
Esc Del	Warm Reset		Esc [6 4 ~	(Ctrl-F1)
Esc O P	F1		Esc [6 5 ~	(Ctrl-F2)
Esc O Q	F2		Esc [6 6 ~	(Ctrl-F3)
Esc O R	F3		Esc [6 7 ~	(Ctrl-F4)
Esc O S	F4		Esc [6 8 ~	(Ctrl-F5)
Esc O w	F3		Esc [6 9 ~	(Ctrl-F6)
Esc O x	F4		Esc [7 0 ~	(Ctrl-F7)
Esc O t	F5		Esc [7 1 ~	(Ctrl-F8)
Esc O u	F6		Esc [7 2 ~	(Ctrl-F9)
Esc O q	F7		Esc [7 3 ~	(Ctrl-F10)
Esc O r	F8		Esc [7 4 ~	(Ctrl-F11)
Esc O p	F10		Esc [7 5 ~	(Ctrl-F12)

PART 5

5 Troubleshooting

1. POWER AND BOOT PROBLEMS
2. SHB IS TOO SLOW
3. OFF-BOARD PCI PROBLEMS
4. ON-BOARD VIDEO PROBLEMS
5. IDE PROBLEMS

5.1 Power and Boot Problems

This section describes common problems. Read it carefully before calling Kontron technical support.

5.1.1 Power Supply Doesn't Start

A simple visual test for supply voltage is done by checking the fan operation. Once the power is applied to the board, the power supply fan must be running.

If a backplane is used, it might provide visible indications of the power supply. When OFF, only auxiliary supplies (+5Vaux and +3.3Vaux if any) should be ON. When ON, all supplies LEDs should be ON and the "PowerGood" LED (if any) should be ON.

If all LEDs are off, this is an indication that the power supply has detected an overcurrent. Remove all loads from the power supply with the exception of the SHB. Do not try to power an empty system; power supplies also have a minimum load requirement.

5.1.1.1 SHB Used in Stand-Alone Without ATX Control

Even if the SHB is normally used in a backplane, it might be a good idea to try it in stand-alone to make sure that the power supply and the SHB are both functional.

Put the SHB flat on a non-conductive surface. Plug the 20-pin and 4-pin cables from the power supply into the SHB J25 and J20 connectors and don't connect any other cable.

Put jumper W4 on the SHB. This jumper overrides the ATX circuit of the SHB and asserts the PS-ON# turn-on signal of the power supply.

Plug the power supply in an AC outlet and turn on the mechanical "ON" switch (if any) of the power supply.

If the power supply does not start, try another one.

If it still does not start, contact Kontron technical support.

5.1.1.2 SHB Used in Stand-Alone With ATX Control

First, try the board in the non-ATX configuration to make sure that the SHB and power supply are functional.

Remove W4 and connect a momentary pushbutton between pin #1 and #2 of the hardware monitor connector J10.

5.1.1.3 SHB Used in a Backplane Without ATX Control

First, try the board in the stand-alone non-ATX configuration (see section 5.1.1.1) to make sure that the SHB and power supply are functional.

When ATX control is not used, the power supply is turnedON either by its mechanical ON/OFF switch or a latching pushbutton used to fake an ATX control.

In all case, the backplane should provide some jumper setting to bypass the SHB ATX circuit. Consult your backplane documentation.

If no pushbutton is used, set the backplane jumpers for “Always ON” configuration. If there is no such setting on the backplane, put W4 on the SHB and set the backplane jumpers so that the SHB will control the power supply. If no jumpers are present on the backplane, this should be the default configuration.

If it does not work, contact your backplane vendor's technical support.

With the latching pushbutton configuration, the control signals do not go through the SHB. If it does not work, it is a backplane configuration problem. Consult your backplane documentation.

5.1.1.4 SHB Used in a Backplane With ATX Control

In doubt, try the SHB and backplane in stand-alone non-ATX configuration (see section 5.1.1.1) to make sure they are both functional.

Set any backplane ATX configuration jumpers to "Controlled by SHB".

Put jumper W4 on the SHB. This should turn-on the power supply. It will confirm that the PS-ON# signal is properly routed to the power supply. Remove W4 after confirmation.

If it does not start, try to connect the pushbutton to pin #1 & #2 of the hardware monitor connector (J10) on the SHB. This will bypass the backplane pushbutton routing. If it does not work, consult Kontron Technical support.

Next, remove the pushbutton from the SHB and connect it to the appropriate connector on the backplane. If it doesn't work, contact your backplane vendor's technical support.

5.1.2 Power Supply Doesn't Stop (Softoff doesn't work)

First, make sure that jumper W4 is not present on the SHB.

When you turn-off the board, you have to press the ATX pushbutton for a minimum of 4 seconds. Press the pushbutton for 10 seconds to be sure.

5.1.3 Bad Behavior Following an AC loss

Following an AC loss, you can choose to leave the board off or put it in the state is was before the AC loss (i.e. mimic a non-ATX power supply behavior).

This is a BIOS setup option in the "power" menu.

5.1.4 SHB Stuck in Reset

When the SHB is stuck in reset, the bi-color debug LED light is orange (red and green LEDs on) and does not blink.

The following table gives possible causes that can keep the board in reset.

Possible Cause	Things to try
Missing 4-wire cable to power the CPU. Very common.	Take a voltmeter and measure the voltage between the connector pins on the SHB. You should get +12V. If not, check cables.
4-Wire cable is plugged into the backplane but the power supply 4-wire cable is not connected to the backplane.	
Power supply doesn't assert its “PowerGood” signal	Check pin P1-B2 (second finger of first connector on primary component side). You should see a voltage above 2.4V. If not, try another power supply.
One or more supply is too low.	Take a voltmeter and measure the following voltages on the backside of the SHB, in the pins of its stand-alone power connector: +3.3V, +5V, +12V, +5Vsb. Those supplies should be within 5%.
Incompatible backplane keying on bus B.	Check pin P3-B1 (first finger of third connector on primary component side. You must have 3.3V.
Shorted reset switch.	Make sure pin #13 of multi-function connector (J11) is not grounded. Unplug any cable on J11 to be sure.

5.1.5 SHB Hang During Boot

First, you want to read the last postcode on the debug LED. Consult the BIOS postcode listing. This might give you a clue on what the problem is. If you call Kontron technical support, the first thing they will ask you is to read the postcode.

Possible Cause	**Things to try**
Insufficient power	Try a bigger power supply or remove external PCI cards to reduce the load..
PCI device conflict on bus A	See section on *off-board* PCI problems.
PCI problem on bus B.	See section on *off-board* PCI problems.
Bad setting on CPU power.	Make sure the CPU type jumper (W15) match the CPU used. If not, the CPU can be over or under powered and this can lead to strange behaviors.
Unsupported CPU.	Make sure that the CPU is in the list of approved CPU types. You might need to download the latest BIOS update to provide the appropriate micro-code fixes for this CPU. Also, some older CPUs (pre-Northwood) requires a higher core voltage. If the voltage requirement of the CPU is higher than 1.6V, it will not be powered at the right voltage.
Memory problems.	Make sure the memory type is in the approved list and is properly inserted.
Cable problems.	Remove all non-essential cables and check pin #1 alignment on the remaining cables.

5.2 SHB is Too Slow

First, look on the backside of the SHB. If the red LED is ON, than it is an overheat condition that causes the CPU to slow down. Possible causes are an insufficient heatsink on the CPU, a heatsink not properly installed or insufficient system airflow.

If a mobile CPU is used, look in the BIOS setup under the advanced CPU options. You can set the CPU to operate in “battery optimized mode” (BOM). This is a low power and low speed mode. Unless you have very tight thermal requirement, you should set the CPU in “performance optimized mode” (POM).

If a 533MHz front side bus CPU is used, make sure jumper W14 is removed. This jumper forces the CPU front side bus to 400MHz.

5.3 Off-board PCI Problems

First, remove all PCI card in the system. If it works, the problem is probably related to external PCI cards. If it still does not work and the backplane has a PCI bridge on bus A, you might have a conflict between the chipset and the bridge. See section on bus A problems. Otherwise, populate the PCI cards on bus A only to see if its works, then bus B to find which bus causes the problem. Go to the appropriate section.

5.3.1 Bus A Problems

Bus A being a conventional 33MHz PCI bus, it's unlikely that it's a timing or protocol problem.

One known problem is a device conflict between the chipset and an external PCI device that has an IDSEL set to AD31. This IDSEL should be on the first slot next to the SHB or on a backplane bridge if any.

Kontron backplanes have a jumper to change the IDSEL of the first slot to AD27 instead of AD31. Consult the backplane documentation to make sure that the jumper is set to AD27.

If the backplane comes from a different vendor, avoid using the slot next to the SHB if you can. If you cannot or if the backplane has a bridge, consult your backplane vendor's technical support for a possible workaround.

5.3.2 Bus B Problems

5.3.2.1 Bus B is Not Working Properly

Expected problems on bus B are timing, protocol and mode/frequency detection problems.

First, set the bus to conventional 33MHz PCI by setting the backplane jumpers, if any, or the SHB jumpers. The PCI-X addendum required PCI-X devices to be able to operate in 33MHz PCI. If it still does not work, than it's a faulty PCI device on the bus. Otherwise, crank up bus speed until you find the fastest possible speed/mode allowed.

The SHB being limited by its chipset to a memory address space of 4GByte, PCI cards that requires huge amount of memory space will not work. Consult Kontron technical support if it's the case.

5.3.2.2 Bus B Mode/Speed is Too Slow

The PCI mode and speed are indicated in the BIOS summary screen.

Make sure all downclocking jumpers on the SHB are removed.
Also, check your backplane for any downclocking jumpers.

The actual mode and speed of PCI bus B is set to the fastest supported mode of all PCI cards or devices attached to the bus. Avoid mixing PCI-X cards and conventional PCI cards on a bus segment. This segment would automatically fall down to conventional PCI.

The PCI specification does not provide any way to distinguish between 100MHz and 133MHz PCI-X capability. This has to be done manually. Kontron ship the SHB configured for 100MHz (safe configuration). For 133MHz operation, put jumper W10 on the SHB.

5.3.3 On-board Video Problems

With Windows 2000, DirectX 8.1 or higher must be installed before the ATI driver installation.
The second CRT does not have a DDC link, Windows cannot detect the monitor type on the secondary CRT. You must enter your monitor type manually in the display properties.

5.3.4 IDE Problems

When only one drive is present on an IDE channel, it must be configured as the master device, otherwise it will not be detected.

When a drive is present on the primary channel and a CompactFlash is also present, the channel speed is restricted by the CompactFlash. Use a 40-wire cable for the external drive or the CompactFlash will not be detected.

6

APPENDICES

A. MEMORY & I/O MAPS

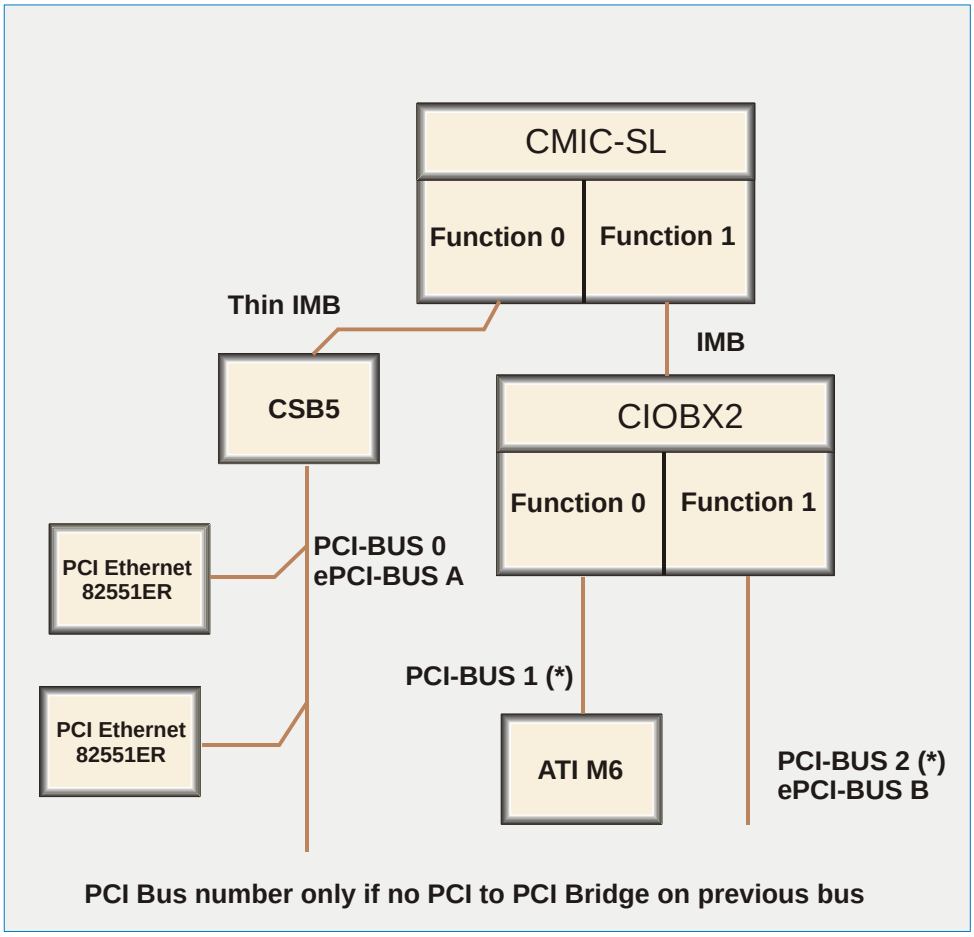
A.1 MEMORY MAPPING

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CFFFF	Video BIOS ATI M6 64KB (size can be change if other primary display)
D0000-DFFFF	Optional ROM (Free)
	LAN BIOS around 30KB if activated, address may vary
	External SCSI BIOS 18KB-64KB , address may vary
	USB BIOS Legacy Support, 16K at DC000h if not disabled
E0000-FFFFF	System BIOS
100000-PCI Memory	DRAM available
PCI memory-4GB	Hole for PCI memory and BIOS flash device

A.2 I/O MAPPING

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
190-1CF				Kontron Control Port
1F0-1F7, 3F6				Primary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	2787-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)
400-0FFF				Chipset Reserved

A.3 PCI BUS DIAGRAM



B. KONTRON EXTENSION REGISTERS

B.1 REGISTERS SUMMARY

Offset	Function
00h	Serial Ports Mode and Buffers Control
01h	Reset history and CpuFault
02h	Lock and History Clear
03h	Hardware Monitor, ID Chip
04-05h	Reserved
06h	Watchdog Control
07-09h	Reserved
0Ah	Debug LED Control
0B-0Ch	Reserved
0Dh	SpeedStep Control
0E-0Fh	Reserved
10h	FPGA Interrupt Number
11h	FPGA Interrupt Enables
12h	FPGA Interrupt Requests
13-17h	Reserved
18h	I2C Controller: Address register
19h	I2C Controller: Transmit buffer
1Ah	I2C Controller: Receive buffer
1Bh	I2C Controller: Flags
1Ch	I2C Controller Hub
1D-1Fh	Reserved

B.2 SERIAL PORTS MODE AND BUFFERS CONTROL

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x190	Read	NU	Break1	Break0	RS485	RS232	ST1	NU	NU
	Write	NU	Break1	Break0	RS485	RS232	ST1	NU	NU
	Reset	X	0	0	0	1	0	X	X

Break[1..0] Reset on a serial port break (locked when bit LOCK=1):
00: never reset from serial port
01: reset from break on serial port 1
10: reset from break on serial port 2
11: prohibited

RS485 Serial port buffer control, see table below

RS232 Serial port buffer control, see table below

ST1 Serial port buffer control, see table below

RS485	RS232	ST1	Description
0	1	X	RS232 mode (default)
1	0	0	RS485/422 point-to-point mode. - RX is always enable: - TX enabled when COM2 RTS is asserted.
1	0	1	RS485 party line mode: - RX enabled when COM2 RTS is deasserted, - TX enabled when COM2 RTS is asserted.
1	1	X	Illegal. This puts the buffers in RS232 mode.
0	0	X	Illegal. This puts the buffers in RS232 mode. This is the condition on power up. Value is changed by the BIOS.

B.3 RESET HISTORY AND CPUFAULT

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x191	Read	PBRST	COM	WDO	CpuFlt	NU	NU	NU	NU
	Write	NU	NU	NU	CpuFlt	NU	NU	NU	NU
	Reset	PBRST	COM	WDO	1	X	X	X	X

PBRST A pushbutton reset was trapped by the reset history circuit.

COM A com port reset was trapped by the reset history circuit.

WDO A watchdog reset was trapped by the reset history circuit.

CpuFlt CPU Fault: a "1" indicate a fault by pulling pin CPUFAULT# to GND on the hardware monitor connector. Set on reset by the hardware and cleared by the BIOS.

B.4 LOCK AND HISTORY CLEAR

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x192	Read	NU	NU	NU	NU	NU	Lock	NU	ClrHis#
	Write	NU	NU	NU	NU	NU	Lock	NU	ClrHis#
	Reset	X	X	X	X	X	1	X	1

Lock — When “1”, prohibit modification of some critical control bits (watchdog enable, reset from serial port,etc.).

ClrHis# — Clear and bring back to 1 to clear the reset history.

B.5 HARDWARE MONITOR & ID CHIP

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x193	Read	AppFlt	GPIO2	GPIO1	FanFlt#	IDChip	ExtFlt#	NU	NU
	Write	AppFlt	GPIO2	GPIO1	NU	IDChip	NU	NU	NU
	Reset	1	1	1	X	1	X	X	X

AppFlt — Application Fault: inverted state of pin APPFAULT# on the hardware monitor connector. Set on reset by the hardware and normally cleared by the application software.

GPIO[2..1] — General purpose I/O pins on the hardware monitor connector.

FanFlt# — Return the state of pin FanFlt# in the hardware monitor connector.

ExtFlt# — Return the state of pin ExtFlt# in the hardware monitor connector.

IDChip — ID Chip (DS2401 serial number) control. Open-drain output with pin readback.

B.6 WATCHDOG CONTROL

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x196	Read	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
	Write	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
	Reset	0	1	1	1	X	X	X	X

WDEN Enable watchdog. Lockable with bit LOCK.
WDD[2..0] Timeout selection. A write to this register triggers the watchdog. Timeout as follow:
000: 0.016s
001: 0.065s
010: 0.262s
011: 1.048s
100: 4.194s
101: 16.78s
110: 67.11s
111: 268.4s

B.7 DEBUG LED CONTROL

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x19A	Read	NU	NU	NU	EnPost	HD_Act	Red	Green	NU
	Write	NU	NU	NU	EnPost	HD_Act	Red	Green	NU
	Reset	X	X	X	1	0	0	0	X

EnPost Enable usage of the debug LED to display the last post code of the boot.
HD_Act Setting this bit will tie IDE_ACT to the debug red LED
Red Set this bit to turn on the debug red LED.
Green Set this bit to turn on the debug green LED.

About debug LED: The idea is that the LED will light red when in reset (this is hardware). As soon as the FPGA is programmed, the LED lights yellow and is enabled for post-code display (see bellow). If the BIOS fail, it is possible to read the post-code. If the BIOS succeed, it will disable the post-code and enable HD activity on the green LED. If needed, the application software can then disable hard disk activity reporting and directly control the bi-color LED for status reporting.

How to read the 8-bit post-code:

- Yellow: start of post sequence
- Red blink: This is the high nibble. 0 to 15 blinks represent hexadecimal 0 to F.
- Green blink: This is the low nibble. 0 to 15 blinks represent hexadecimal 0 to F.

B.8 SPEEDSTEP CONTROL

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x19D	Read	X	X	X	X	X	X	X	X
	Write	X	X	X	X	X	X	X	BOM
	Reset	X	X	X	X	X	X	X	X

BOM 1: Battery Optimized Mode (low power, low frequency).
0: Performance optimized mode (high power, high frequency).
X Don't care.

This register is used by the BIOS to change the CPU mode. Don't use this register.

B.9 FPGA INTERRUPT NUMBER

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A0	Read	NU	NU	NU	NU	Legacy ISA Interrupt number			
	Write	NU	NU	NU	NU	Legacy ISA Interrupt number			
	Reset	X	X	X	X	0000b			

During the boot process, the BIOS assign a legacy interrupt to the FPGA and writes the interrupt number in this register. A driver that needs to use the interrupt read this register to find out what interrupt is used.

B.10 FPGA INTERRUPT ENABLES

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A1	Read	NU	NU	I2CEn	FanFlt	ExtFlt	NU	WD	NU
	Write	NU	NU	I2CEn	FanFlt	ExtFlt	NU	WD	NU
	Reset	X	X	0	0	0	X	0	X

I2C Enable interrupt by the I2C controller.
FanFlt Enable an interrupt by signal FanFlt# on the hardware monitor connector.
ExtFlt Enable an interrupt by signal ExtFlt# on the hardware monitor connector.
WD Put the watchdog in dual-stage mode an enable an interrupt on first stage time-out.

B.11 FPGA INTERRUPT REQUESTS

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A2	Read	NU	NU	I2C	FanFlt	ExtFlt	NU	WD	NU
	Write	NU	NU	I2C	FanFlt	ExtFlt	NU	WD	NU
	Reset	X	X	0	X	X	X	X	X

I2C	Set when bit BUSY in the I2C controller switche from 1 to 0 (i.e. task completion).
FanFlt	Set when the harware monitor signal FANFLT# changes state.
ExtFlt	Set when the harware monitor signal EXTFLT# changes state.
WD	Set when the first stage of the watchdog times out.

Interrupt requests are generated regardless of the state of the interrupt enable bits.
To clear a request bit, write a "1" at this bit location. Following a reset, a false request can occurs. Always clear a pending request before enabling an interrupt source.

Request bits use an edge detection circuit. The are set when the interrupt condition is detected (transition of the monitored signal). For example, when the signal FanFlt# in the hardware monitor connecter is asserted (i.e. fall to GND) the correspondig request is set. If the request is clear, the circuit will wait for a transition on FanFlt# to assert the request again. The interrupt service can read register 0x193 to find the actual state of the signal.

B.12 I^2C CONTROLLER: ADDRESS REGISTER

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A8	Read	NU	NU	NU	NU	NU	NU	NU	NU
	Write	A6	A5	A4	A3	A2	A1	A0	Read
	Reset	X	X	X	X	X	X	X	X

A[6..0]	I^2C device address.
READ	1: to read from the I^2C device, 0: to write to the I^2C device.

Writing to this register triggers the generation of a START sequence and will transmit the address and READ bit. Bit OPEN and BUSY in the flags register will turn to 1. When the sequence is completed, bit BUSY will return to 0 but bit OPEN will stay to 1. At this moment, bit RXACK in the flags register will indicate the I2C device acknowledge.

B.13 I²C CONTROLLER: TRANSMIT BUFFER

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A9	Read	NU	NU	NU	NU	NU	NU	NU	NU
	Write	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
	Reset	X	X	X	X	X	X	X	X

Writing to this register trigger a data-transmit operation.

B.14 I²C CONTROLLER: RECEIVE BUFFER

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1AA	Read	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
	Write	Write anything to trigger reception							
	Reset	X	X	X	X	X	X	X	X

Write anything at this location to start clocking a byte out of the I²C device.

This register hold the last received data. Since the receiver operates all the time, including during address or data transmission, a pin readback of the last transmission is available at the end of any transmission.

B.15 I²C CONTROLLER: FLAGS

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1AB	Read	V1	V0	BUSY	OPEN	TXACK	RXACK	SCL	SDA
	Write	NU	NU	NU	OPEN	TXACK	NU	SCL	SDA
	Reset	V1	V0	0	0	0	X	1	1

V[1..0]	Version/capability. 00 for now.
BUSY	Operation in progress. Don't write any I2C register when this bit is set.
OPEN	Connection open. Set to “1” when opening the connection. Clearing this bit will send a STOP condition on the I2C bus.
TXACK	Acknowledge to transmit on I2C byte reception. Should always be 1 at the exception of the last byte to be received.
RXACK	Acknowledge received from device on the last I2C byte transmission. Should be 0 if an I2C device acknowledged the transfer.
SCL & SDA	Direct reading and control of SCL and SDA lines. Allow software control of the lines when the controller doesn't use them. For debugging purpose only. When not in use, leave to 1. Those bit are forced to 1 when bit OPEN is set. On read, give the pin status.

B.16 I²C HUB CONFIGURATION

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1AC	Read	NU	NU	NU	NU	NU	I2C2	I2C1	I2C0
	Write	NU	NU	NU	NU	NU	I2C2	I2C1	I2C0
	Reset	X	X	X	X	X	0	0	0

I2C[2..0]
- 000: I2C controller not connected to any bus, default.
- 001: I2C controller connected to on-board PROM
- 010: I2C controller connected to hardware monitor connector
- 100: I2C controller connected to ePCI-X SMBus
- 011: I2C controller connected to on-board PROM and hardware monitor
- 101: I2C controller connected to on-board PROM and ePCI-X
- 110: I2C controller connected to hardware monitor and ePCI-X
- 111: I2C controller connected to on-board PROM, hardware monitor and ePCI-X

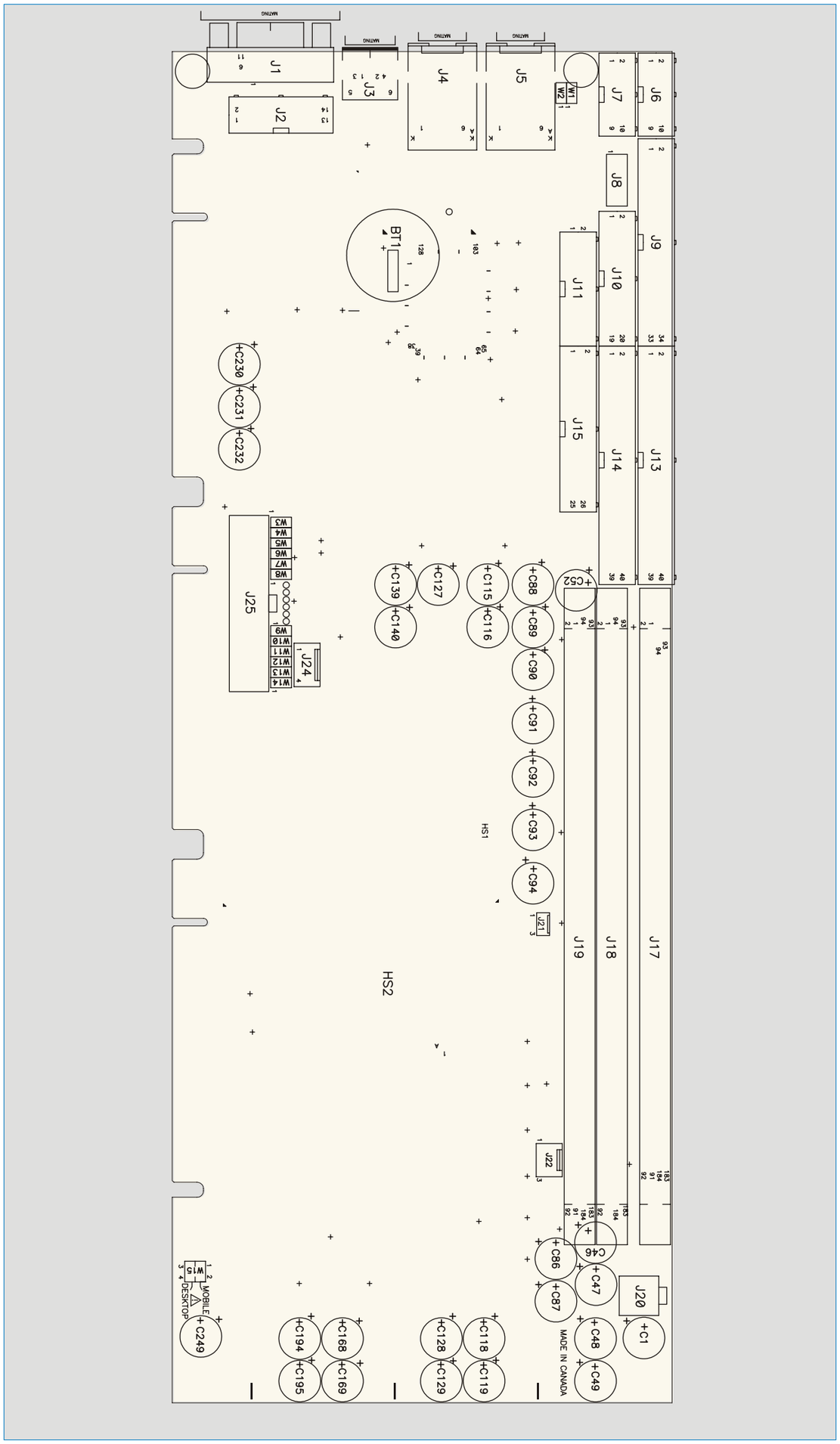
I2C bus routing is used mostly in case of conflictual I2C addresses. In absence of addresses conflicts, connect the controller to all busses. It will act like a hub: every data transmitted is sent to all busses and data received is "ored" from all the busses.

When connected to the hardware monitor connector, the I2C link connect as follow:

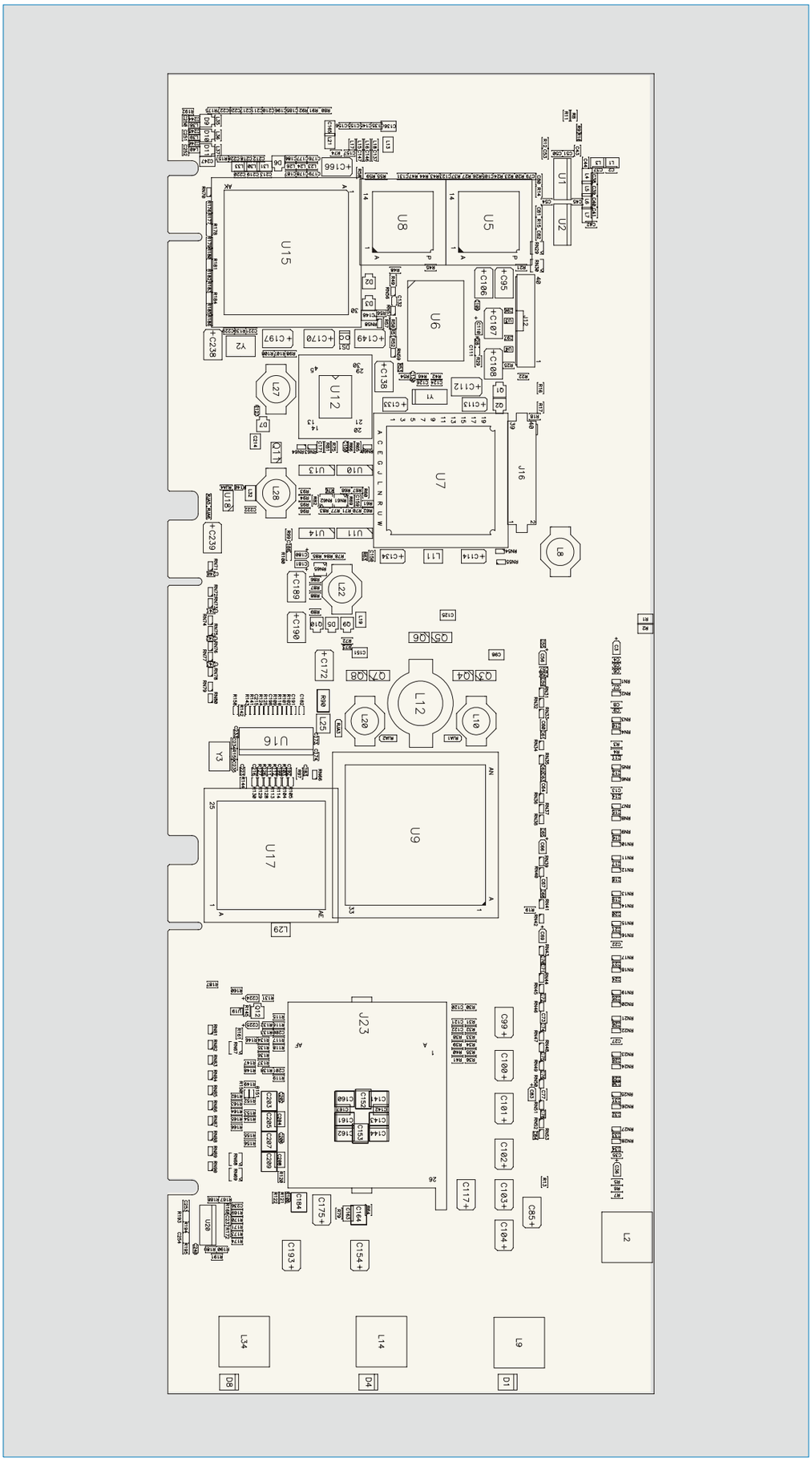
- SDA connect to GPIO1
- SCL connect to GPIO2

C. BOARD DIAGRAMS

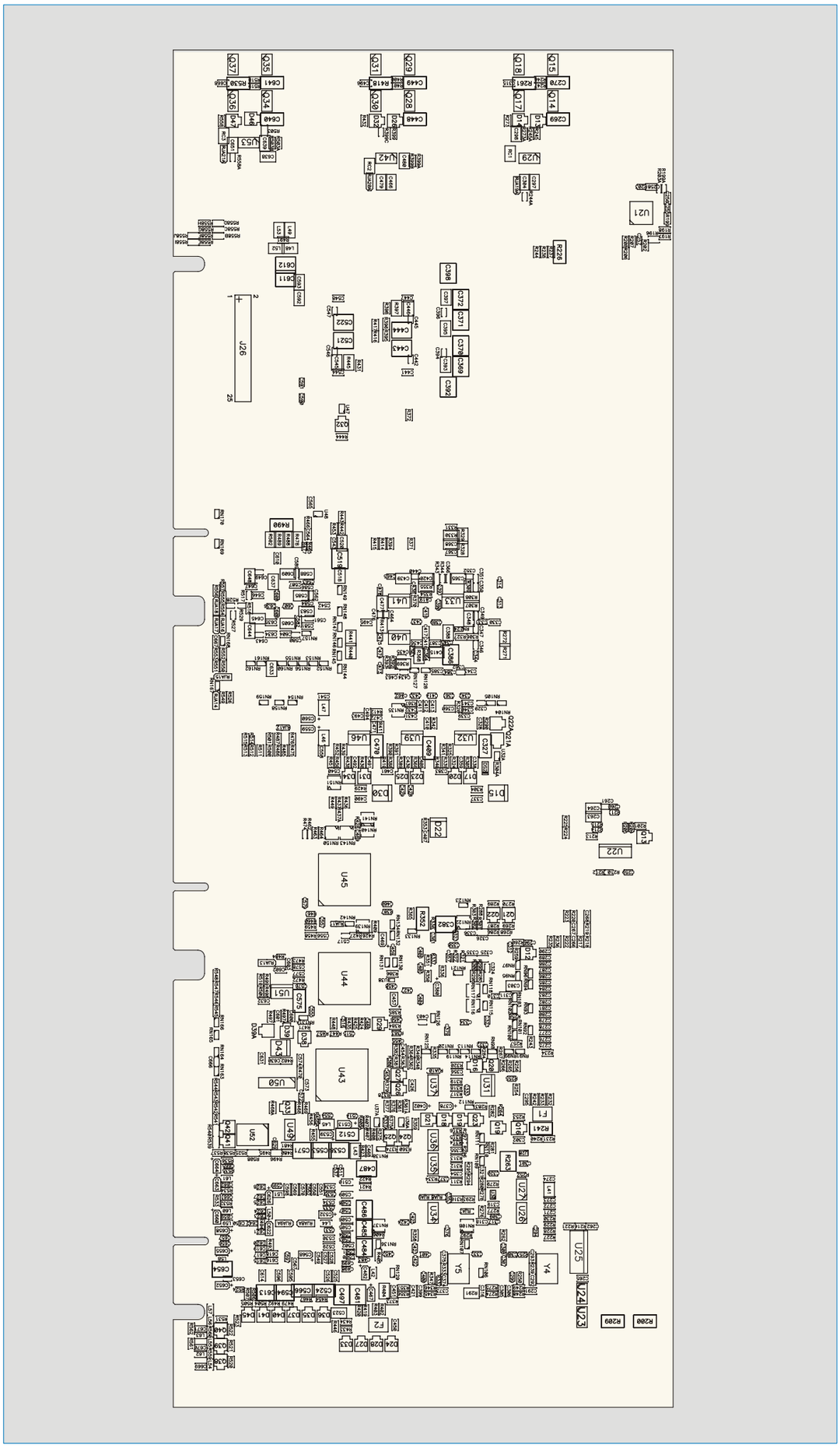
C.1 ASSEMBLY DEVICE T.H. TOP SIDE



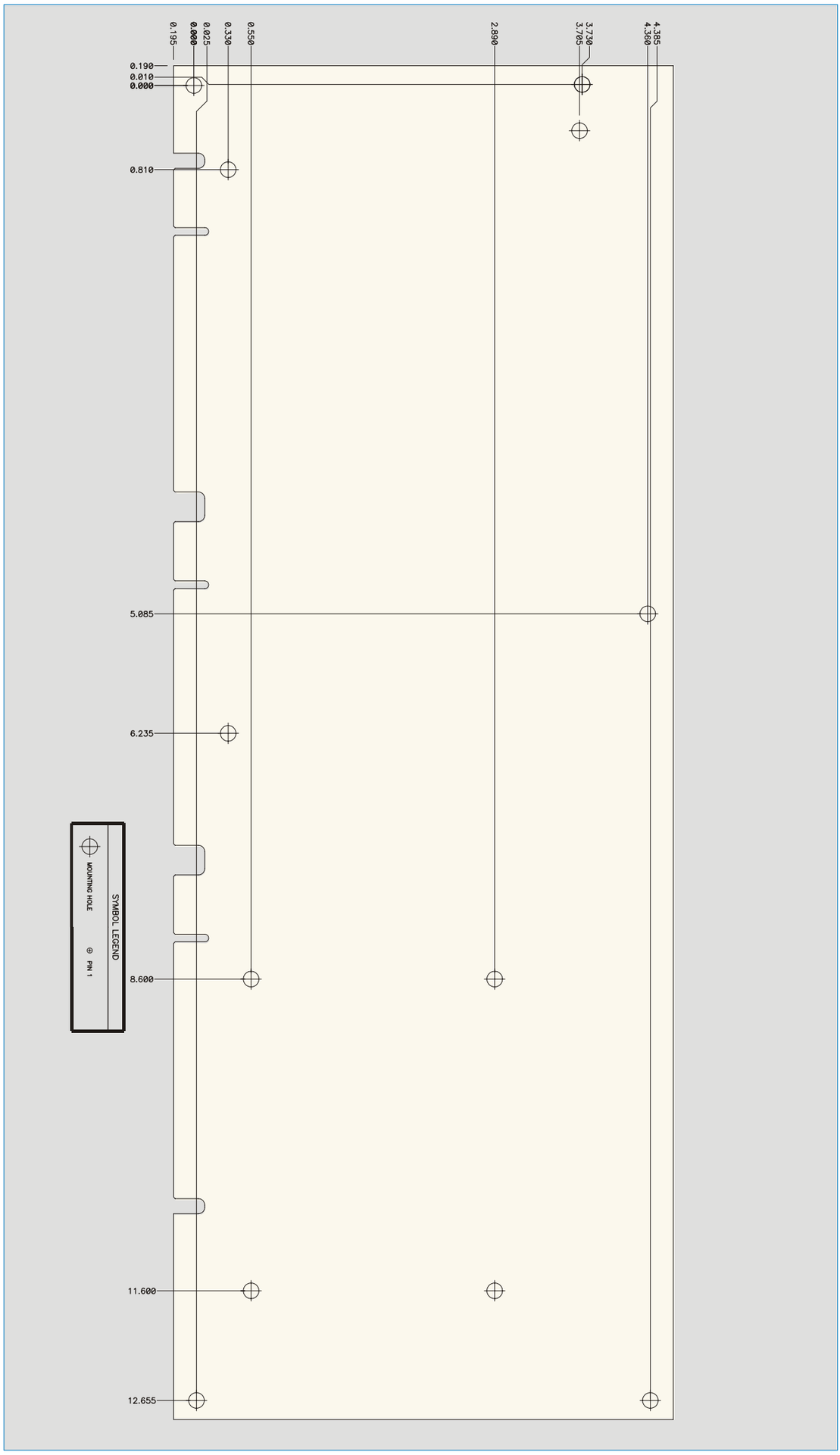
C.2 TOP DEVICE SURFACE MOUNT



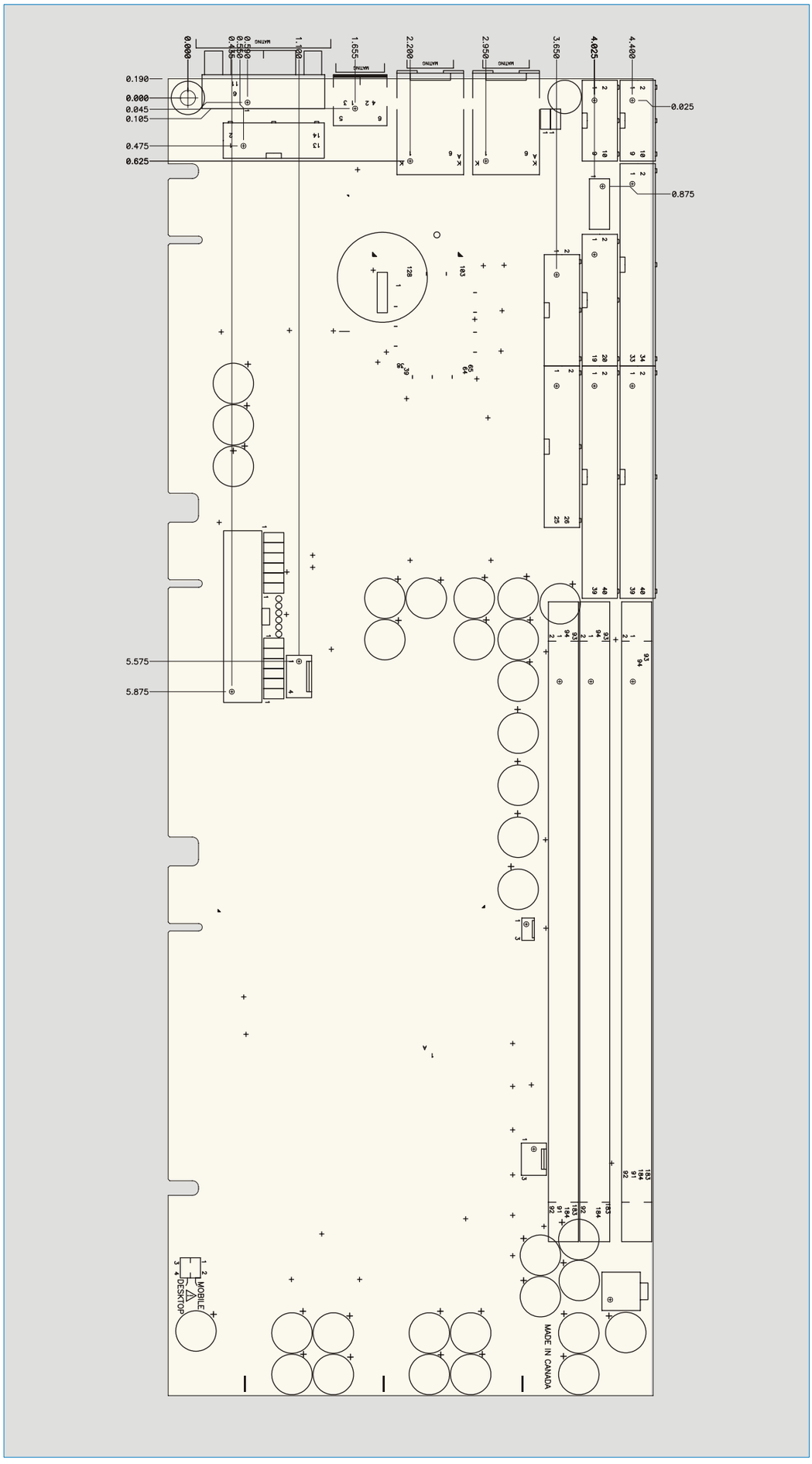
C.3 BOTTOM DEVICE SURFACE MOUNT



C.4 MOUNTING HOLES



C.5 CONNECTOR LOCATION TOP SIDE



D. CONNECTOR PINOUTS

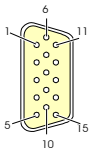
D.1 CONNECTORS AND HEADERS SUMMARY

Connector	Description
J1	Primary Video
J2	Secondary Video and TV-OUT
J3	PS/2 Keyboard / Mouse
J4	Ethernet LAN2
J5	Ethernet LAN1
J6	Serial Port 1 (header)
J7	Serial Port 2 (header)
J8	USB 0 / USB 1 (header)
J9	Floppy
J10	Hardware monitor
J11	Multifunction
J12	JILI Interface
J13, J14	IDE0 / IDE1
J15	Parallel Port
J16	CompactFlash disk
J17-J19	DIMM Socket
J20	CPU Power
J21	CMIC Fan
J22	CPU Fan
J23	CPU Socket
J24	POST Codes
J25	ATX Power Supply

D.2 CRT VGA INTERFACE (J1)

Signal		Signal		Signal	
RED	1	Analog GND	6	N.C.	11
GREEN	2	Analog GND	7	SDATA	12
BLUE	3	Analog GND	8	HSYNC	13
N.C.	4	N.C.	9	VSYNC	14
GND	5	GND	10	SCLK	15

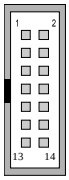
Front View



D.3 TV-OUT/SECONDARY VIDEO (J2)

Pin Number	Signal
(TV-Out composite out) COMP	1
(TV-Out S-Video chroma) C	3
GND	5
GND	7
GND	9
GND	11
GND	13

Top View

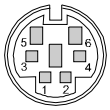


Pin Number	Signal
2	GND
4	Y (TV-Out S-Video luma)
6	RED (Secondary CRT)
8	GREEN (Secondary CRT)
10	BLUE (Secondary CRT)
12	HSYNC (Secondary CRT)
14	VSYNC (Secondary CRT)

D.4 PS/2 KEYBOARD/MOUSE (J3)

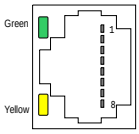
Signal	
KB:DATA	1
MOUSE:DATA	2
GND	3
VCC	4
KB:CLK	5
MOUSE:CLK	6

Front View



D.5 ETHERNET 10BASE-T/100BASE-TX (J4 & J5)

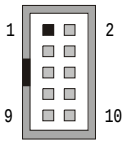
TX+	1
TX-	2
RX+	3
N.C.	4
N.C.	5
RX-	6
N.C.	7
N.C.	8



D.6 SERIAL PORT 2 & 1 - (J6 & J7) RS-232

Pin Number	Signal
1	DCD
3	RXD
5	TXD
7	DTR
9	GND

Top View

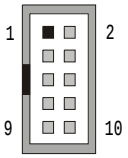


Pin Number	Signal
2	DSR
4	RTS
6	CTS
8	RI
10	N.C.

D.7 USB HEADER (J8)

Pin Number	Signal
1	USB0:VCC
3	USB0:DATA-
5	USB0:DATA+
7	USB0:GND
9	GND

Top View

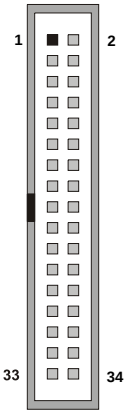


Pin Number	Signal
2	USB1:VCC
4	USB1:DATA-
6	USB1:DATA+
8	USB1:GND
10	GND

D.8 FLOPPY DRIVE (J9)

Pin Number	Signal
1	GND
3	GND
5	GND
7	GND
9	GND
11	GND
13	GND
15	GND
17	N.C.
19	GND
21	GND
23	GND
25	GND
27	N.C.
29	FDETECT
31	GND
33	N.C.

Top View



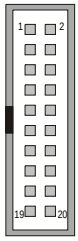
Pin Number	Signal
2	DENSEL#
4	N.C.
6	N. C.
8	INDEX#
10	MTR0#
12	DSEL1#
14	DSEL0#
16	MTR1#
18	DIR#
20	STEP#
22	WDATA#
24	WGATE#
26	TRK0#
28	WRPROT#
30	RDATA#
32	HDSEL#
34	DSKCHG#

Active Low Signal

D.9 SYSTEM MONITOR (J10)

Pin Number	Signal
1	GND
3	Reserved
5	GPIO1/SDA
7	APPFLT#
9	EXTFLT#
11	FANFLT#
13	CHASINT#
15	FANTACH1
17	FANTACH3
19	FANTACH5

Top View



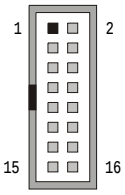
Pin Number	Signal
2	POWER BUTTON#
4	GND
6	GPIO2/SCL
8	CPUFLT#
10	GND
12	GND
14	GND
16	FANTACH2
18	FANTACH4
20	FANTACH6

Active Low Signal

D.10 MULTI-FUNCTION (J11)

Pin Number	Signal
1	KB:CLK
3	KB:DATA
5	VCC
7	SPEAKER
9	MOUSE:CLK
11	MOUSE:DATA
13	PBRES#
15	IDE:ACT#

Top View



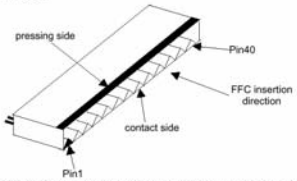
Pin Number	Signal
2	GND
4	GND
6	VCC
8	VCC
10	GND
12	GND
14	GND
16	VCC

Active Low Signal

D.11 JUMPTEC INTELLIGENT LVDS INTERFACE (J12)

Signal	Pin Number
LCDFLM	1
LVD0-/oddLVD0-	2
LVD0+/oddLVD0+	3
ENAVDD	4
LVD1-/oddLVD1-	5
LVD1+/oddLVD1+	6
Not connected	7
LVD2-/oddLVD2-	8
LVD2+/oddLVD2+	9
GND	10
LVC-/oddLVC-	11
LVC+/oddLVC+	12
GND	13
LVD3-/oddLVD3-	14
LVD3+/oddLVD3+	15
DDC_Data	16
evenLVD0-	17
evenLVD0+	18
DDC_Clock	19
evenLVD1-	20
evenLVD1+	21
Not connected	22
evenLVD2-	23
evenLVD2+	24
GND	25
evenLVDC-	26
evenLVDC+	27
GND	28
evenLVD3-	29
evenLVD3+	30
+5V	31
+5V	32
+5V	33
+5V	34
EnableBacklight	35
GND	36
GND	37
+12V	38
+12V	39
+12V	40

The various connector manufacturers may use different pin1 definitions for their devices. Please use the following diagram instead:



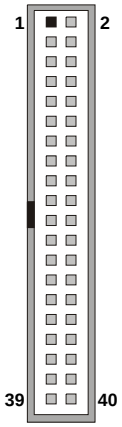
IMPORTANT NOTE: Since the same pin1 definition is valid for transmitter- and receiver-side, only FlatFoil cables (FFC) with opposite contact ends have to be used !

side view of FFC:

For more information, consult Jumptec JILI specification.

D.12 PRIMARY & SECONDARY EIDE (J13 & J14)

Signal				Signal
RST#	1		2	GND
D7	3		4	D8
D6	5		6	D9
D5	7		8	D10
D4	9		10	D11
D3	11		12	D12
D2	13		14	D13
D1	15		16	D14
D0	17		18	D15
GND	19		20	N.C. (KEY)
DMARQ	21		22	GND
IOW#	23		24	GND
IOR#	25		26	GND
IORDY	27		28	GND (CSEL)
DMACK#	29		30	GND
IRQ	31		32	N.C. (IOCS16#)
A1	33		34	N.C. (PDIAG#)
A0	35		36	A2
CS0#	37		38	CS1#
ACT#	39		40	GND



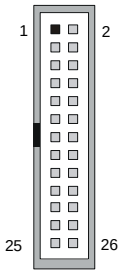
Active Low Signal

D.13 PARALLEL PORT (J15)

Standard Mode

Pin Number	Signal
1	STB#
3	D0
5	D1
7	D2
9	D3
11	D4
13	D5
15	D6
17	D7
19	ACK#
21	BUSY
23	PE
25	SLCT

Top View



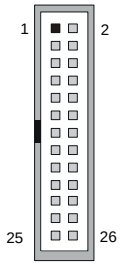
Pin Number	Signal
2	ALF#
4	ERR#
6	INIT#
8	SLCTIN#
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND

Active Low Signal

EPP Mode

Pin Number	Signal
1	WRITE#
3	D0
5	D1
7	D2
9	D3
11	D4
13	D5
15	D6
17	D7
19	INTR
21	WAIT#
23	N.C.
25	N.C.

Top View



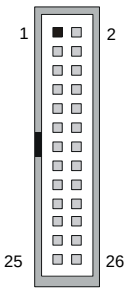
Pin Number	Signal
2	DATASTB#
4	N.C.
6	N.C.
8	ADDRSTRB#
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND

Active Low Signal

ECP Mode

Pin Number	Signal
1	STROBE#
3	D0
5	D1
7	D2
9	D3
11	D4
13	D5
15	D6
17	D7
19	ACK#
21	BUSY, PERIPHACK
23	PERROR, ACKREVERSE
25	SELECT

Top View



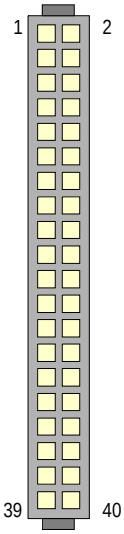
Pin Number	Signal	
	Compatible Mode	High Speed Mode
2	AUTOFD	HOSTACK
4	FAULT	PERIPHRQST
6	INIT	REVERSERQST
8	SELECTIN	SELECTIN
10	GND	
12	GND	
14	GND	
16	GND	
18	GND	
20	GND	
22	GND	
24	GND	
26	GND	

Active Low Signal,

D.14 COMPACTFLASH™ (J16)

Signal	Pin Number
D11	1
D12	3
D13	5
D14	7
D15	9
CS1#	11
DMACK#	13
DMARQ	15
PDIAG#	17
IRQ15	19
VCC	21
GND	23
RESET#	25
CSEL	27
A1	29
A0	31
D0	33
D1	35
D2	37
IOCS16#	39

Top View



Pin Number	Signal
2	GND
4	D3
6	D4
8	D5
10	D6
12	D7
14	CS0#
16	IOR#
18	IOW#
20	VCC
22	VCC
24	GND
26	GND
28	A2
30	DASP#
32	IORDY
34	D8
36	D9
38	D10
40	GND

D.15 CPU POWER (J20)

Signal	
+12V	4
GND	2

	Signal
3	+12V
1	GND

Active Low Signal

D.16 CHIPSET AND CPU FAN HEADERS (J21 AND J22)

Signal	
SENSE	1
+12V fused	2
GND	3

Front View

D.17 POST CODE DEBUG (J24)

Signal	
+3.3V	1
POST:DATA	2
POST:CLOCK	3
GND	4

Front View

D.17.1 ATX-Type BOARD Power (J25)

Pin Number		Top View	Pin Number	
Signal				Signal
VCC3	11	11 1	1	VCC3
-12V	12	12 2	2	VCC3
GND	13	13 3	3	GND
PS_ON#	14	14 4	4	VCC
GND	15	15 5	5	GND
GND	16	16 6	6	VCC
GND	17	17 7	7	GND
N.C.	18	18 8	8	PWROK
VCC	19	19 9	9	5VSB
VCC	20	20 10	10	+12V

Active Low Signal

E. EPCI-X REFERENCE

This appendix gives an overview of ePCI-X. For more information on the ePCI-X specification, go to www.picmg.org and look for PICMG 1.2 specification.

For more information on PCI and PCI-X bus signals and protocol, go to www.pcisig.com . The following figures show a full-size and half-size SHB with connector naming and pins numbering.

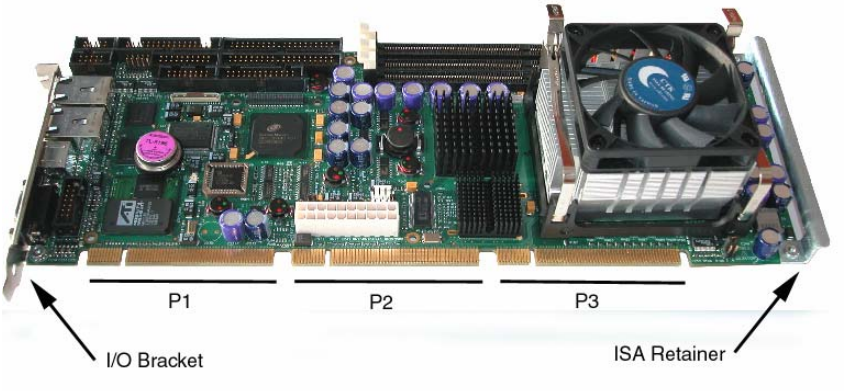


Figure 1: Full-Size Dual-Bus SHB (view from side B)

The dual-bus SHB has all three edge connectors while the single-bus implementation only has P1 and P2. Signals related to bus B are left unconnected in a dual-bus SHB.

Figure 2: Half-Size Single-Bus SHB (view from side B)

E.1 EPCI-X EDGE CONNECTOR

	P1 Connector			P2 Connector			P3 Connector (optional)	
	Side B (front)	Side A (back)		Side B (front)	Side A (back)		Side B (front)	Side A (back)
1	-12V	+12V	1	GND	a_AD04	1	b_VIO	b_AD22
2	PWRGD	PWRBT#	2	a_AD05	+3.3V	2	b_C/BE3#	GND
3	PSON#	+5Vaux	3	a_AD03	a_AD02	3	b_AD23	b_AD21
4	TRST#	GND	4	GND	a_AD00	4	+5V	b_AD20
5	TMS	TCK	5	a_AD01	GND	5	b_AD19	GND
6	TDO	TDI	6	Reserved	a_REQ64#	6	b_AD17	b_AD18
7	Reserved	a_PRSNT#	7	+5V	a_ACK64#	7	GND	b_AD16
8	+5V	Reserved	8	Reserved	+5V	8	b_C/BE2#	+3.3V
9	a_INTB#	+5V	9	a_VIO	a_C/BE7#	9	b_IRDY#	b_FRAME#
10	a_INTD#	a_INTA#	10	GND	a_C/BE6#	10	GND	b_TRDY#
11	+5V	a_INTC#	11	a_C/BE5#	GND	11	b_DEVSEL#	GND
12	Key	Key	12	Key	Key	12	Key	Key
13	Key	Key	13	Key	Key	13	Key	Key
14	+3.3Vaux	+5V	14	a_C/BE4#	a_PAR64	14	+5V	b_PCIXCAP
15	GND	Reserved	15	+5V	a_AD62	15	b_LOCK#	b_STOP#
16	Reserved	a_GNT3#	16	a_AD63	GND	16	b_PERR#	GND
17	+3.3V	GND	17	a_AD61	a_AD60	17	GND	b_PAR
18	a_REQ3#	a_GNT2#	18	GND	a_AD58	18	b_SERR#	b_AD15
19	a_REQ2#	a_GNT1#	19	a_AD59	+3.3V	19	b_C/BE1#	+3.3V
20	GND	+3.3V	20	a_AD57	a_AD56	20	GND	b_AD13
21	a_REQ1#	a_RST#	21	GND	a_AD54	21	b_AD14	b_AD11
22	a_REQ0#	a_GNT0#	22	a_AD55	GND	22	b_AD12	GND
23	+3.3V	GND	23	a_AD53	a_AD52	23	+5V	b_AD09
24	a_CLKFO	a_CLKFI	24	+5V	a_AD50	24	b_AD10	b_M66EN
25	GND	+3.3V	25	a_AD51	GND	25	b_AD08	GND
26	a_CLKC	a_CLKD	26	a_AD49	a_AD48	26	GND	b_C/BE0#
27	+3.3V	GND	27	GND	a_AD46	27	b_AD07	b_AD06
28	a_CLKA	a_CLKB	28	a_AD47	+3.3V	28	b_AD05	+3.3V
29	GND	+3.3V	29	a_AD45	a_AD44	29	GND	b_AD04
30	a_AD31	PME#	30	GND	a_AD42	30	b_AD03	b_AD02
31	a_AD29	GND	31	a_AD43	GND	31	b_AD01	GND
32	+5V	a_AD30	32	a_AD41	a_AD40	32	+5V	b_AD00
33	a_AD27	a_AD28	33	+5V	a_AD38	33	b_ACK64#	b_REQ64#
34	a_AD25	GND	34	a_AD39	GND	34	b_C/BE7#	GND
35	GND	a_AD26	35	a_AD37	a_AD36	35	GND	b_C/BE6#
36	a_C/BE3#	a_AD24	36	GND	a_AD34	36	b_C/BE5#	b_PAR64
37	a_AD23	+3.3V	37	a_AD35	+3.3V	37	b_C/BE4#	+3.3V
38	GND	a_AD22	38	a_AD33	a_AD32	38	GND	b_AD62
39	a_AD21	a_AD20	39	GND	GND	39	b_AD63	b_AD60
40	a_AD19	GND	40	b_CLKD	b_CLKC	40	b_AD61	GND
41	+5V	a_AD18	41	+3.3V	GND	41	+5V	b_AD58
42	a_AD17	a_AD16	42	b_CLKB	b_CLKA	42	b_AD59	b_AD56
43	a_C/BE2#	GND	43	GND	+3.3V	43	b_AD57	GND
44	GND	a_FRAME#	44	b_CLKFO	b_CLKFI	44	GND	b_AD54
45	a_IRDY#	a_TRDY#	45	GND	GND	45	b_AD55	b_AD52
46	a_DEVSEL#	+5V	46	b_INTB#	b_INTA#	46	b_AD53	+3.3V
47	+3.3V	a_PCIXCAP	47	b_INTD#	b_INTC#	47	GND	b_AD50
48	a_LOCK#	a_STOP#	48	+5V	GND	48	b_AD51	b_AD48
49	a_PERR#	GND	49	b_GNT3#	b_GNT2#	49	b_AD49	GND
50	+5V	SER_SDA	50	b_REQ3#	b_REQ2#	50	+5V	b_AD46

	P1 Connector			P2 Connector			P3 Connector (optional)	
51	a_SERR#	SER_SCL	51	GND	+5V	51	b_AD47	b_AD44
52	a_PAR	GND	52	b_GNT1#	b_GNT0#	52	b_AD45	GND
53	GND	a_C/BE1#	53	b_REQ1#	b_REQ0#	53	GND	b_AD42
54	a_AD15	a_AD14	54	+5V	GND	54	b_AD43	b_AD40
55	a_AD13	+3.3V	55	b_RST#	b_PRSNT#	55	b_AD41	+3.3V
56	GND	a_AD12	56	+5V	b_AD30	56	GND	b_AD38
57	a_AD11	a_AD10	57	b_AD31	GND	57	b_AD39	b_AD36
58	a_AD08	GND	58	b_AD29	b_AD28	58	b_AD37	GND
59	+5V	a_AD09	59	GND	b_AD26	59	+5V	b_AD34
60	a_AD07	a_C/BE0#	60	b_AD27	+3.3V	60	b_AD35	b_AD32
61	a_M66EN	GND	61	b_AD25	b_AD24	61	b_AD33	GND
62	Reserved	a_AD06	62	GND	Reserved	62	GND	Reserved

E.2 BUS DEDICATED SIGNALS

Bus A	Bus B	Description
a_REQ[0..3]# a_GNT[0..3]#	b_REQ[0..3]# b_GNT[0..3]#	PCI arbitration signals
a_AD[0..31] a_C/BE[0..3]# a_DEVSEL# a_FRAME# a_IRDY# a_LOCK# a_PAR a_PERR# a_RST# a_SERR# a_STOP# a_TRDY#	b_AD[0..31] b_C/BE[0..3]# b_DEVSEL# b_FRAME# b_IRDY# b_LOCK# b_PAR b_PERR# b_RST# b_SERR# b_STOP# b_TRDY#	PCI 32-bit bussed signals
a_AD[32..63] a_C/BE[4..7]# a_PAR64 a_REQ64# a_ACK64#	b_AD[32..63] b_C/BE[4..7]# b_PAR64 b_REQ64# b_ACK64#	PCI 64-bit bussed signals
a_INTA# a_INTB# a_INTC# a_INTD#	b_INTA# b_INTB# b_INTC# b_INTD#	PCI interrupts
a_CLKA a_CLKB a_CLKC a_CLKD	b_CLKA b_CLKB b_CLKC b_CLKD	PCI bus clocks
a_CLKFI a_CLKFO	b_CLKFI b_CLKFO	Clock feedback trace match in length with bus clocks
a_VIO	b_VIO	PCI bus electrical keying and I/O power: 3.3V, 5V or open
a_M66EN	b_M66EN	PCI bus mode detection for conventional PCI: gnd or open
a_PCIXCAP	b_PCIXCAP	PCI bus mode detection for PCI-X: gnd, pull-down or open
a_PRSNT#	b_PRSNT#	PCI bus presence: 0 if bus is present, open otherwise

E.3 COMMON SIGNALS AND POWERS

Signal	Description
PME#	PCI busses power management event
SER_SCL	PCI busses and backplane I^2C/SMBus clock
SER_SDA	PCI busses and backplane I^2C/SMBus data
PSON#	ATX control: direct connection to an ATX power supply
PWRGD	ATX control: direct connection to an ATX power supply
PWRBT#	ATX control: connect to the system ON/OFF pushbutton
TCK TDI TDO TMS TRST#	SHB JTAG, for manufacturing use
+3.3V (22)	Power
+5V (25)	Power
GND (75)	Power
+12V	Power
-12V	Power
+3.3Vaux	PCI standby power
+5Vaux	ATX Standby power
Reserved	Reserved

F. BIOS SETUP ERROR CODES

F.1 POST BEEP

POST beep codes are defined in the BIOS to provide low level tone indication when an error occurs during the BIOS initialization.

Beep codes consist of a combination of long and short beeps. They are described as follows

Code Beeps POST Routine Description

Code	Beeps	POST Routine Description
02h		Verify Real Mode
03h		Disable Non-Maskable Interrupt (NMI)
04h		Get CPU type
06h		Initialize system hardware
08h		Initialize chipset with initial POST values
09h		Set IN POST flag
0Ah		Initialize CPU registers
0Bh		Enable CPU cache
0Ch		Initialize caches to initial POST values
0Eh		Initialize I/ O component
0Fh		Initialize the local bus IDE
10h		Initialize Power Management
11h		Load alternate registers with initial POST values
12h		Restore CPU control word during warm boot
13h		Initialize PCI Bus Mastering devices
14h		Initialize keyboard controller
16h	1- 2- 2- 3	BIOS ROM checksum
17h		Initialize cache before memory autosize
18h		8254 timer initialization
1Ah		8237 DMA controller initialization
1Ch		Reset Programmable Interrupt Controller
20h	1- 3- 1- 1	Test DRAM refresh
22h	1- 3- 1- 3	Test 8742 Keyboard Controller
24h		Set ES segment register to 4 GB
26h		Enable A20 line
28h		Autosize DRAM
29h		Initialize POST Memory Manager
2Ah		Clear 512 KB base RAM
2Bh		Enhanced COMS init
2Ch	1- 3- 4- 1	RAM failure on address line ***xxxx*** *
2Eh	1- 3- 4- 3	RAM failure on data bits ***xxxx*** * of low byte of memorybus
2Fh		Enable cache before system BIOS shadow

Code Beeps POST Routine Description (cont'd)

30h	1- 4- 1- 1	RAM failure on data bits ***xxxx*** * of high byte of memory bus
32h		Test CPU bus- clock frequency
33h		Initialize Phoenix Dispatch Manager
34h		CMOS test
35h		Register re-initialization
36h		Warm start shut down
38h		Shadow system BIOS ROM
39h		Cache re-initialization
3Ah		Autosize cache
3Ch		Advanced configuration of chipset registers
3Dh		Load alternate registers with CMOS values
42h		Initialize interrupt vectors
45h		POST device initialization
46h	2- 1- 2- 3	Check ROM copyright notice
48h		Check video configuration against CMOS
49h		Initialize PCI bus and devices
4Ah		Initialize all video adapters in system
4Bh		QuietBoot start (optional)
4Ch		Shadow video BIOS ROM
4Eh		Display BIOS copyright notice
4Fh		Multi-Boot Initialization
50h		Display CPU type and speed
51h		Initialize EISA board
52h		Test keyboard
54h		Set key click if enabled
55h		USB initialization
56h		Enable Keyboard
58h	2- 2- 3- 1	Test for unexpected interrupts
59h		Initialize POST display service
5Ah		Display prompt "Press DEL to enter SETUP"
5Bh		Disable CPU cache
5Ch		Test RAM between 512 and 640 KB
60h		Test extended memory
62h		Test extended memory address lines
64h		Jump to UserPatch1
66h		Configure advanced cache registers
67h		Initialize Multi Processor APIC
68h		Enable external and CPU caches
69h		Setup System Management Mode (SMM) area
6Ah		Display external L2 cache size

Code Beeps POST Routine Description (cont'd)

6Bh		Load custom defaults (optional)
6Ch		Display shadow- area message
6Eh		Clear Memory
70h		Display error messages
74h		Test RTC
76h		Check for keyboard errors
7Ch		Set up hardware interrupt vectors
7Dh		ISM initialization
7Eh		Initialize coprocessor if present
80h		Disable onboard Super I/ O ports and IRQs
81h		Late POST device initialization
82h		Detect and install external RS232 ports
83h		Configure non-MCD IDE controllers
84h		Detect and install external parallel ports
85h		Initialize PC-compatible PnP ISA devices
86h		Re- initializes onboard I/ O ports.
87h		Configure Motheboard Configurable Devices (optional)
88h		Initialize BIOS Data Area
89h		Enable Non-Maskable Interrupts (NMIs)
8Ah		Initialize Extended BIOS Data Area
8Bh		Test and initialize PS/ 2 mouse
8Ch		Initialize floppy controller
8Fh		Determine number of ATA drives (optional)
90h		Initialize hard-disk controllers
91h		Initialize local-bus hard-disk controllers
92h		Jump to UserPatch2
93h		Build MPTABLE for multi-processor boards
95h		Install CD ROM for boot
96h		Clear huge ES segment register
97h		Fixup Multi Processor table
98h	1- 2	Search for option ROMs. One long, two short beeps on checksum failure
99h		Check for SMART Drive (optional)
9Ah		Shadow option ROMs
9Ch		Set up Power Management
9Dh		Initialize security engine (optional)
9Eh		Enable hardware interrupts
9Fh		Determine number of ATA and SCSI drives
A0h		Set time of day

Code Beeps POST Routine Description (cont'd)

A4h		Initialize Typematic rate
A8h		Erase DEL prompt
AAh		Scan for DEL key stroke
ACh		Enter SETUP
AEh		Clear Boot flag
B0h		Check for errors
B2h		POST done - prepare to boot operating system
B4h	1	One short beep before boot
B5h		Terminate QuietBoot (optional)
B6h		Check password (optional)
B7h		ACPI initialization
B9h		Prepare Boot
BAh		Initialize DMI parameters
BCh		Clear parity checkers
BDh		Display MultiBoot menu
BEh		Clear screen (optional)
C0h		Try to boot with INT 19
C1h		Initialize POST Error Manager (PEM)
C2h		Initialize error logging
C3h		Initialize error display function
C4h		Initialize system error handler
C5h		PnPnd dual CMOS (optional)
C8h		Force check (optional)
C9h		Extended checksum (optional)
CFh		Extended BIOS data Fail
D1h		BIOS stack initialization
D2h		Unknown interrupt
D3h		Setup WAD
D4h		Get CPU string

Code Beeps POST Routine Description (cont'd)

Code	Beeps	For Boot Block in Flash ROM
80h		Initialize the chipset
81h		Initialize the bridge
82h		Initialize the CPU
83h		Initialize system timer
84h		Initialize system I/ O
85h		Check force recovery boot
86h		Checksum BIOS ROM
87h		Go to BIOS
88h		Set Huge Segment
89h		Initialize Multi Processor
8Ah		Initialize OEM special code
8Bh		Initialize PIC and DMA
8Ch		Initialize Memory type
8Dh		Initialize Memory size
8Eh		Shadow Boot Block
8Fh		System memory test
90h		Initialize interrupt vectors
91h		Initialize Run Time Clock
92h		Initialize video
93h		Initialize System Management Mode
94h	1	Output one beep before boot
95h		Boot to Mini DOS
96h		Clear Huge Segment
97h		Boot to Full DOS

F.2 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

F.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

1. If it's the first boot, check for the onboard battery jumper W3. The board is shipped with W3 jumper set to OFF (onboard battery disconnected). This jumper must be shorted (ON) for proper battery operation.
2. CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This indicates that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

Operating System not found

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Floppy Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

Expansion ROM not initialized

Cannot initialize the PCI expansion ROM. You not have free conventional memory for expension ROM (C0000h to DFFFFh). You must be disable not used expansion ROM.

G. BIOS UPDATE & EMERGENCY PROCEDURE

BIOS UPDATE PROCEDURE

The BIOS update procedure is detailed in a ReadMe file included with the BIOS package as well as the update utility. This package can be downloaded from our website www.kontron.com or from our FTP site ftp://ftp.kontron.ca/Support

EMERGENCY PROCEDURE

Symptoms:

- No POST code on a power up (when using a POST card).
- Board does not boot, even after usual hardware and connection verifications.
- At power up, there is floppy disk led activity, which is one sign that the BIOS as detected a corrupted BIOS CRC prior POST and fallen back automatically to Emergency Recovery Mode looking for the floppy Emergency disk.

The Emergency Recovery procedure is detailed in a ReadMe file included with the Emergency BIOS package as well as the update utility. This package can be downloaded from our website www.kontron.com or from our FTP site ftp://ftp.kontron.ca/Support

H. GETTING HELP

At Kontron, we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Kontron, our products or services, you may reach us at the above numbers or by writing to :

Kontron Inc..
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

LIMITED WARRANTY

Kontron Inc, ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

Returning Defective Merchandise

If your Kontron product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand:

- The Kontron Invoice number
- Your purchase order number
- The serial number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make certain you receive an RMA number from Kontron's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:

- Make a copy of the request form on the following page.
- Fill out the form and be as specific as you can about the board's problem.
- Fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.

6) When returning a Kontron board:

   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured, since incoming units are insured by Kontron):

Kontron Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

RETURN TO MANUFACTURER AUTHORIZATION REQUEST

Contact Name : _____

Company Name : _____

Street Address : _____

City : _____ Province/State: _____

Country : _____ Postal/Zip Code: _____

Phone Number : _____ Extension : _____

Fax Number : _____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Fax this form to Kontron's Technical Support department in Canada at (450) 437-8053