
# ENDURA EMB-1 User's Guide

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# Before you begin

This guide provides detailed hardware reference information about the EMB-1. It also explains how to configure the BIOS and the board configuration options.

This guide assumes that you are familiar with PC systems based on the Intel x86 architecture.

Be sure to read and save all instructions contained in this guide.

## About this guide

## Guide contents

This guide describes the EMB-1..

| Chapter | | Description |
|---|---|---|
| 1 | Overview | Introduces the EMB-1, briefly describes its features, and lists specifications. |
| 2 | Installation | Explains how to install, remove or replace EMB-1's components. |
| 3 | BIOS configuration | Explains how to configure the BIOS using the built-in BIOS setup menus. |
| 4 | Theory of operations | Describes EMB-1's components. |

### Appendices

The appendices provide additional information about the EMB-1.

| Appendix | | Description |
|---|---|---|
| A | Chipset and I/O map | Lists the I/O port addresses for the address-mapped devices in the EMB-1. |
| B | Interrupts | Lists DMA channel and IRQ assignments to the peripherals supported by the EMB-1. |
| C | Connectors | Details the connectors on the EMB-1 and gives the signal pinout of each connector. |
| D | Installing and configuring RomPilot | Describes how to install, configure, and enable a RomPilot image on a server (EMB-1) and the Management Workstation Application software on a client.. |
| E | BIOS update and recovery | Details how to update and recover your system BIOS and the flash boot device (FBD). |

| Appendix | | Description |
|---|---|---|
| F | Error messages | Explains common error messages and beep codes. |
| | Glossary | Defines terms used in this manual. |

## Notational conventions

This manual uses the following conventions:

- `Screen text and syntax strings appear in this font.`
- All numbers are decimal unless otherwise stated.
- Bit 0 is the low-order bit. If a bit is set to 1, the associated description is true unless otherwise stated.


Notes indicate important information about the product.


Cautions indicate situations that may result in damage to data or the hardware.


Tips indicate alternate techniques or procedures that you can use to save time or better understand the product.


ESD cautions indicate situations that may cause damage to hardware via electro-static discharge.


The globe indicates a World Wide Web address.


Warnings indicate situations that may result in physical harm to you or the hardware.

# Where to get more information

## About EMB-1

You can find out more about EMB-1 from these sources:

- **World Wide Web**: RadiSys maintains an active site on the World Wide Web. The site contains current information about the company and locations of sales offices, new and existing products, contacts for sales, service, and technical support information. You can also send e-mail to RadiSys using the web site.

  
  When sending e-mail for technical support, please include information about both the hardware and software, plus a detailed description of the problem, including how to reproduce it.

  
  To access the RadiSys web site, enter this URL in your web browser:
  `http://www.radisys.com`

  Requests for sales, service, and technical support information receive prompt response.

- **Other**: If you purchased your RadiSys product from a third-party vendor, you can contact that vendor for service and support.

# Contents

# Figures

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# 1 Overview

The EMB-1 is a standard Intel† Celeron-based, PC-compatible motherboard. It fits into a standard ATX form-factor chassis and requires an ATX power supply.

The EMB-1 supports the 366 and 433MHz versions of the Celeron processor. Both versions contain 128KB of L2 cache. The processor connects to the motherboard through a Plastic Pin Grid Array (PPGA) 370-pin socket.

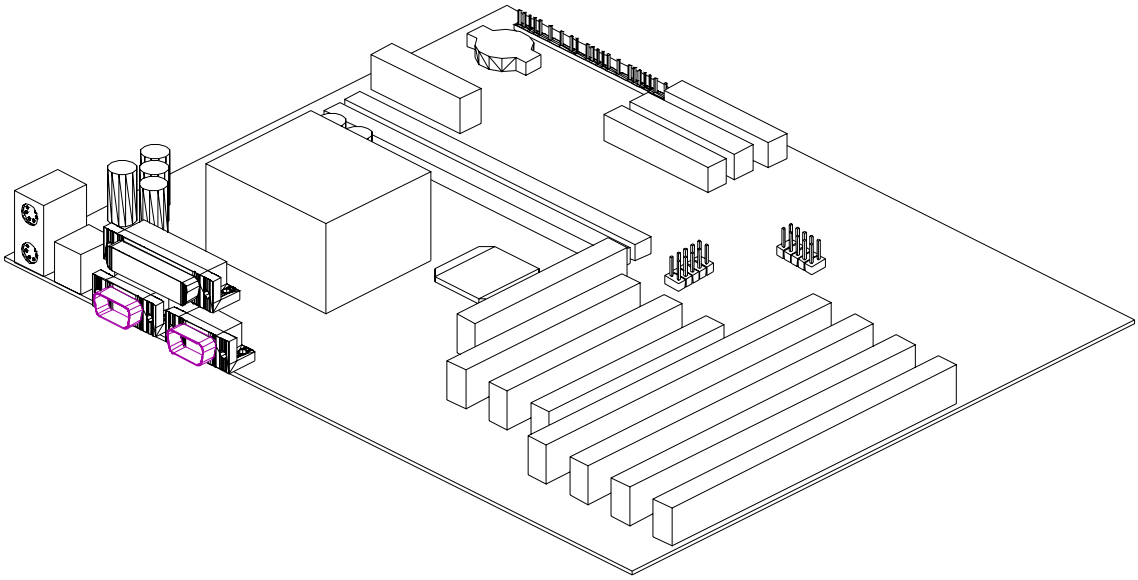


**Figure 1-1. The EMB-1**

## Feature summary

- **Processor**
  - 370-pin PPGA socket
  - 366 or 433 MHz Intel Celeron
- **Main memory**
  - Two 168-pin Dual Inline Memory Module (DIMM) sockets
  - Supports up to 512 MB synchronous DRAM (SDRAM)
  - Supports Error Checking and Correcting (ECC) and non-ECC memory

- **Intel North Bridge 82443BX**
  - Host Bus to 32 bit, 33 MHz PCI bridge
  - SDRAM support with or without ECC
- **Intel South Bridge 82371EB PCI ISA IDE Xcelerator (PIIX4E)**
  - PCI to ISA bridge
  - Two independent EIDE channels
  - Dual channel USB support
  - Integrated RTC with external battery backup
- **National PC87309-ICK-VLJ Super I/O**
- **Expansion Slots**
  - One AGP slot
  - Three ISA slots
  - Two PCI slots
  - One shared PCI/ISA slot
- **Video graphics (Optional)**
  - Chips and Technology 69000 64-bit GUI and video-accelerated controller
  - 2 MB of video memory integrated into the video controller
- **Peripheral interfaces**
  - Two serial ports (one via cable)
  - One parallel port
  - One PS/2 keyboard port
  - One PS/2 mouse port
  - Two floppy drives
  - Two USB ports
  - Standard ATX I/O shield
- **Other features**
  - PhoenixBIOS†
  - Plug and Play Compatible
  - Support for Advanced Power Management (APM) - APM 1.2
  - Custom boot logo

# Specifications

## Environmental specifications

**Table 1-1. EMB-1 environmental specifications**

| Characteristic | State | Value |
|---|---|---|
| Temperature (Ambient) | Operating | 0°C to 55°C |
| | Storage | –40°C to 70°C |
| Humidity | Operating/storage | 5% to 95% RH noncondensing 25°C – 45°C |
| Vibration | Operating | 0.04$g^2$/Hz from 5-1000Hz random, 10 min. per sweep cycle<br>Sine wave cycle: 0.075mm displacement from 10–57Hz<br>Sine wave cycle: 1G from 57-150Hz |
| | Storage | 0.06$g^2$/Hz from 5-1000Hz random, 10 min. per sweep cycle |
| Shock (un-packaged) | Operating | 30 G, 11 ms duration, half-sine shock pulse |
| | Storage | 50 G, 11 ms duration, half-sine shock pulse |
| Altitude | Operating | To 15,000 ft (4,500 m) |
| | Storage | To 40,000 ft (12,000 m) |
| ESD | Operating | 4KV direct contact, 8KV air |

These are system-level tests. The EMB-1's conformance to these specifications may be affected by the rest of the system's ability to conform.

## Additional specifications

**Table 1-2. Additional EMB-1 specifications**

| Characteristic | Value | Description |
|---|---|---|
| Current | +5V | Measurement at DOS prompt with no onboard video is 3.04A. |
| | | Measurement at DOS prompt with onboard video is 3.36A. |
| | +3.3V | Measurement at DOS prompt with no onboard video is 0.73A. |
| | | Measurement at DOS prompt with onboard video is 0.91A. |
| Power consumption[1] | 25W | Typical measurement for the EMB-1. |
| | 25W | Maximum total for all I/O cards inserted in PCI/ISA slots. |
| | 75W | Approximate worst-case EMB-1 power consumption with RAM and without I/O cards. |
| Mechanical dimensions | 12 x 9.6 inches | |
| Safety | UL Listed<br>CB Report | |
| EMC | CISPR 22:1997 / EN 55022:1998—Class B | |
| | CISPR 24:1997 / EN 55024:1998 | |
| | FCC Class B | |

1 The power supply rating required for your system depends on a variety of factors, including the processor installed on the EMB-1, amount of installed RAM, and the number and type of installed I/O cards and peripherals.

For detailed information about cooling and proper ventilation of ATX systems, see *Performance ATX Desktop System Thermal Design Suggestions.* You can download this document at the following web address:

`http://www.teleport.com/~ffsupprt/`

# 2 Installation

This chapter explains how to install, remove or replace components of the EMB-1.

When reading this file online, you can immediately view information about any installation topic by placing the mouse cursor over a topic name and clicking.



Avoid causing ESD (electrostatic discharge) damage:

- Remove modules from their antistatic bags only in a static-free environment.
- Perform the installation process (described later in this chapter) only in a static-free environment.
- During external cable installation, ensure that the cables are not active. The EMB-1 is not designed for hot insertion of any interface, except USB.

The EMB-1 modules, like most other electronic devices, are susceptible to ESD damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

Other setup is done by configuring BIOS options as described in *Chapter 3, BIOS configuration*.

# Setting jumpers and headers

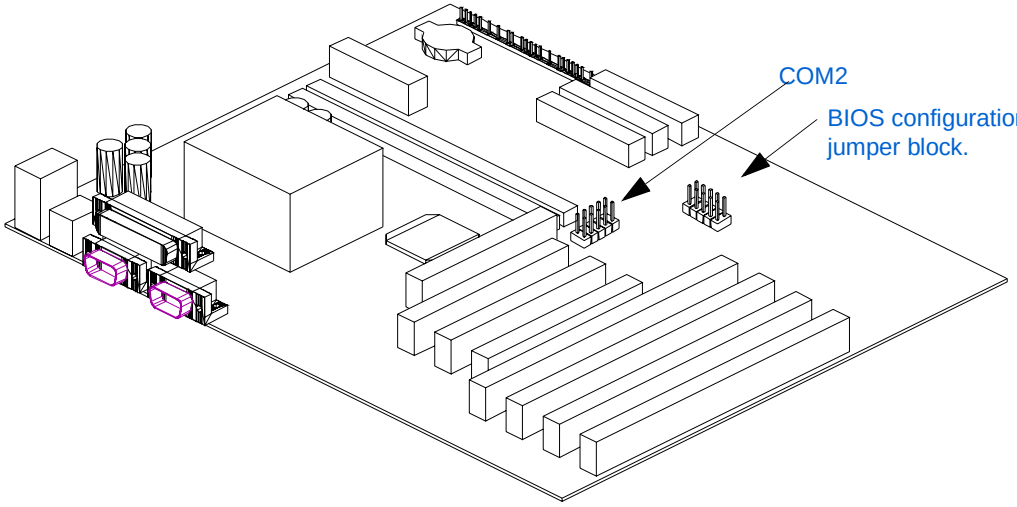


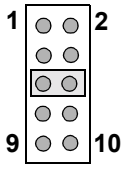

**Figure 2-1. EMB-1 jumper and COM2 location**

### BIOS configuration jumper block.

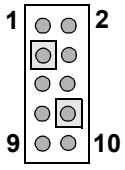
The BIOS configuration jumper block does not contain any user-configurable jumpers for normal operation.

Use extreme caution when updating the boot block. A BIOS boot block rarely changes and should not require updating.

Jumper settings on the BIOS configuration jumper block are typically used during manufacturing for reprogramming the BIOS in the flash boot device (FBD). You use these jumpers mainly for BIOS updates. For specific instructions, see *Appendix E, BIOS update and recovery*.




Pins 5 and 6:
Force BIOS recovery




Pins 3 and 8:
Boot block write enable

**Figure 2-2. BIOS configuration jumper block settings**

| Function | Pins | Description |
|---|---|---|
| Force BIOS Recovery | 5, 6 | Connect pin 5 (~FRC_RCVR) to pin 6 (GND) to force BIOS recovery. This signal is connected to GPI 20 of the PIIX4E. It is readable by the boot block BIOS code and forces the boot block to initiate a recovery sequence at power-up. |
| Boot-block write enable | 3, 8 | Connect pin 8 (BBEN) to pin 3 (VCC) to enable programming of the boot block. The pins are separated to prevent accidental connections of these pins. |

# Installing and removing the EMB-1

For detailed instructions on installing and removing the EMB-1, see your chassis manual.

The procedures in this chapter assume familiarity with the general terminology associated with personal computers and with the safety practices and regulatory compliance required for using and modifying electronic equipment.

Disconnect the EMB-1 from its power source and from any telecommunications links, networks or modems before doing any of the procedures described in this chapter. Failure to disconnect power, telecommunications links, networks or modems before you open the system or do any procedures can result in personal injury or equipment damage.

Some circuitry on the system board may continue to operate even though the front panel power button is off.

## Before you begin

Before you begin an installation into a new system, have the following equipment ready to use:

- Video device (VGA or better monitor or flat panel display)
- Video graphics adapter card, if your EMB-1 does not contain an embedded graphics controller
- PS/2 keyboard to enter BIOS setup information
- A minimum of one SIMM module
- A Phillips screwdriver (#2 bit)
- A jumper removal tool.
- An antistatic wrist strap and a conductive foam pad to use when working on the system.

Optionally, you'll need one of the following mass storage devices to boot from:

- IDE hard disk drive with cable
- Floppy disk drive with cable

Complete these steps before you begin the installation.

1. Set up an equipment log and record the new system model and serial numbers, all installed options, and the old system configuration. This provides the information necessary to complete a full recovery, if needed.

   Note that you may be completely replacing a system I/O board that contains serial and parallel ports plus the hard disk drive and floppy disk drive controller. When you need this information, it is easier to consult the log than to open up and examine the system.

2. Inspect the board, noting the location of the connectors and major components.
3. Check and record the jumper settings to make sure they are correct. In most cases the jumper defaults should be adequate for your needs. For more information about the jumper settings, see *Setting jumpers and headers* on page 6.
4. Consider backing up your hard disk drive.

## Unpack and inspect the EMB-1

Unpack and visually inspect the board for damage which may have occurred in shipment. Retain all packing material and shipping documentation.

If damage occurred during shipment, notify the carrier at once to initiate a damage claim. Contact your dealer or RadiSys customer service for replacement of damaged products.

Make sure you take great care in providing protection from Electro-Static Discharge (ESD). Do not flex or scrape a printed circuit board when handling.

If you are working with a new system, skip ahead to the appropriate section of this chapter.

# Removing the old motherboard

1. Observe the precautions at the beginning of this chapter.
2. Disconnect cables, connectors, and so on, from the system.
3. Remove any add-in boards. (For detailed information, see *Removing an Add-in Board*.)
4. Label and remove and peripherals that prevent extraction of the existing motherboard.
5. Label and disconnect the all cables connected to the motherboard.
6. Remove the metal screws that secure the motherboard to the chassis as shown in Figure 2-3. Carefully lift the board up and out of the system.

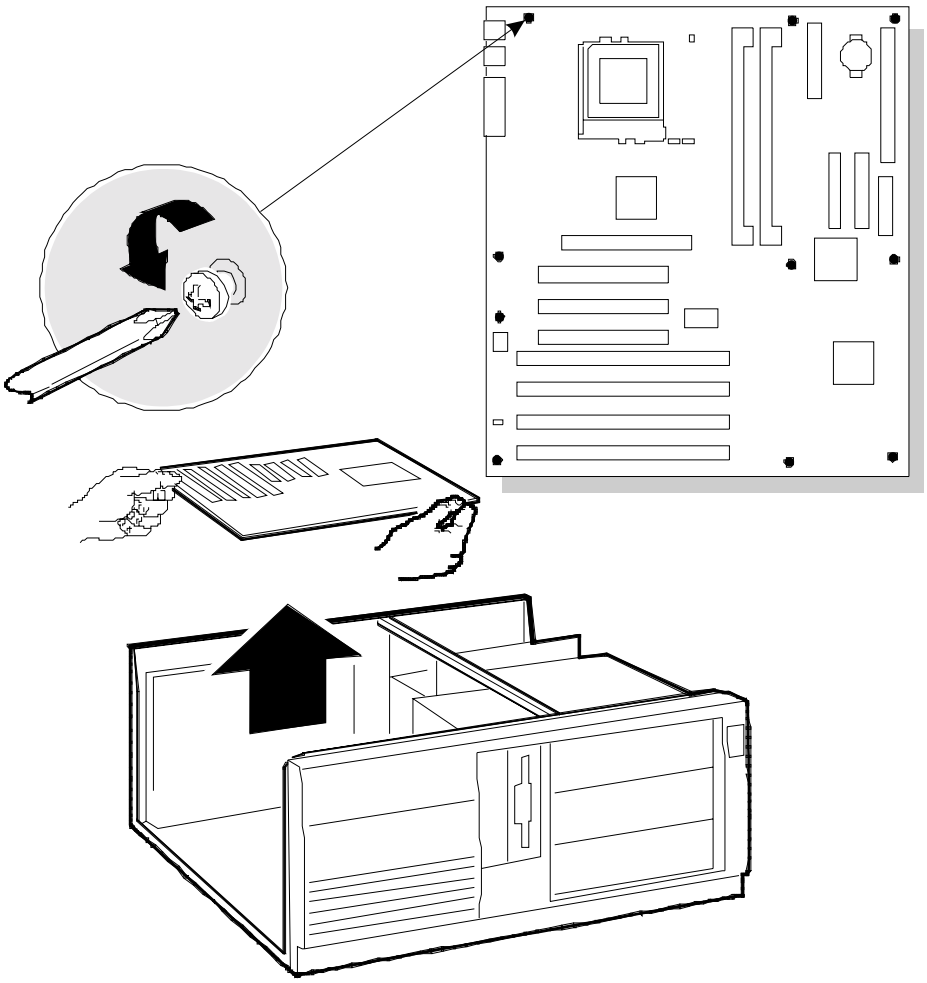


**Figure 2-3. Removing the old motherboard**

## Installing the EMB-1

Do not flex any printed circuit board or scrape any board components.

1. Align the board over the chassis with the expansion slot connectors toward the back of the system.

   Some systems allow access by removing a side panel or even a bottom panel. The EMB-1 installs in any standard ATX system chassis.

2. Place the I/O shield that came with the EMB-1 over the I/O connectors.

   The I/O shield should fit snuggly into chassis cut out. Once installed, the motherboard holds the shield in place.

3. Move the EMB-1 into place over the mounting screw standoffs until the holes line up.

4. Make sure the I/O connectors and I/O shield line up with the insertion hole in the back of the system.

   The I/O shield should fit snugly into chassis cutout. Once installed, the EMB-1 holds the shield in place.

5. Secure the board to the chassis.

   When installing the motherboard be careful to slide the USB connector *under* the USB connector tab on the I/O panel.

6. Install the motherboard with 10 screws.

7. Connect the front panel reset and LED wires to the motherboard as follows:

| LED wire | J19 header |
|---|---|
| Reset SW | 4–5 |
| PWR ON LED | 7–9 |
| HD LED | 11–12 |
| PWR SW | 15–16 |
| SPEAKER | 26–29 |

8. If necessary, reinstall any peripherals removed prior to extraction of the existing motherboard.

9. Attach the floppy cable, floppy power, motherboard power and the fan power cables. If you have a COM2 punchout, install the COM2 cable from J13 to the rear panel punchout.

   Route wiring away from sharp edges and heat sources such as the CPU. Ensure that wiring harnesses do not block cooling intake and exit paths.

10. Replace the chassis cover.

## Creating a custom boot logo

The custom boot logo is a standard OS/2 or Microsoft† Windows† bitmap file in RLE format. The EMB-1 supports both 16 and 256 color images. The maximum logo image size for 16-color images is 640 x 480. The maximum logo image size for 256-color images is 320 x 200. Smaller images are automatically centered on the screen. The screen's background color is the color of the logo image's lower left corner pixel. The EMB-1 ignores invalid images, such as wrong file formats or oversized images. As a result, the EMB-1 displays the default blank screen.

The maximum size of the logo binary file is 64K (65536) bytes. The logo is programmed into the EMB-1 just like any other User BIOS Extension (UBE).

To create and enable a custom boot logo, do the following:

1. Generate a standard .bmp file in RLE format using a graphics software product.

2. Obtain the REFLASH.EXE utility from the RadiSys web site. For information about assessing the RadiSys web site, see Where to get more information on page iv.

3. Flash the .bmp file into the flash boot device. The file is located in the 128K block starting at offset 512K (80000H).

   ```
   reflash  /F=yourlogo.bmp  /O=80000
   ```

4. Enable the custom boot logo.

   A. Enter BIOS setup. See *Chapter 3, BIOS configuration*.

   B. Select Disabled in the Boot-time Diagnostic field of the Optional Features sub-menu

5. To disable the custom boot logo, do one of the following:

   A. Press the ESC key at any time during BIOS POST.

   B. Select Enabled in the Boot-time Diagnostic field of the Optional Features sub-menu.

# Installing the COM2 cable

The EMB-1 supports COM2 through a a 9-conductor ribbon cable. One end of the cable has a 9 pin D-sub connector that connects to the chassis. The other end has a 10-pin header connector that connects to the COM2 connector located on the EMB-1. For COM2's pinout information, see *Appendix C, Connectors*. For cable pinout information, see the following table

- J1 refers to the 9 pin D-sub connector.
- P1 refers to the 10 pin header connector.
- Pin 1 of P1 is not connected.

**Figure 2-4. Cable pinout**

| Pin Number J1 | Pin Number P1 |
|---|---|
| 5 | 2 |
| 9 | 3 |
| 4 | 4 |
| 8 | 5 |
| 3 | 6 |
| 7 | 7 |
| 2 | 8 |
| 6 | 9 |
| 1 | 10 |

To install the COM2 cable:

1. Turn off all peripheral devices connected to the computer.
2. Turn off the computer.
3. Remove the computer cover and locate the COM2 connector. shown in Figure 2-1.
4. Connect the 10-pin header to the COM2 connector

   Ensure that pin 1 of the cable joins pin 1 of the COM2 connector located on the EMB-1.

5. Connect the 9 pin D-sub connector to the chassis.
6. Replace the computer cover.
7. Turn on the computer.

# Maintaining and upgrading the EMB-1

## Upgrading memory

The EMB-1 has two DIMM sockets, as shown in this figure.

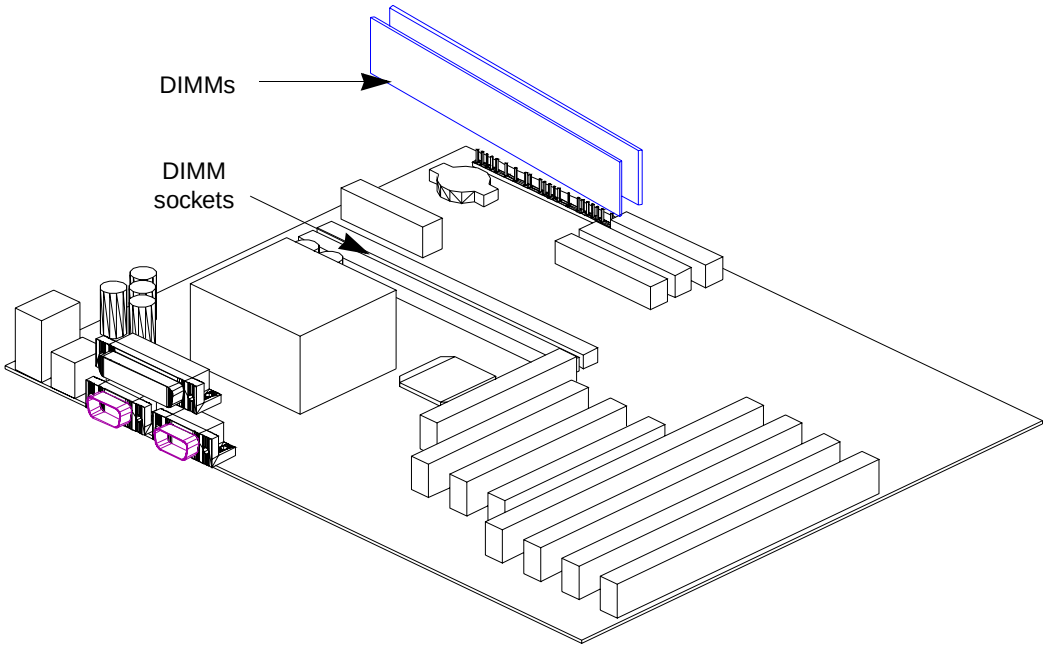



**Figure 2-5. DIMM socket locations**

Minimum memory size is 16 MB; maximum memory size is 512 MB. The EMB-1 supports single- or double-sided DIMMs in the following sizes:

| DIMM Size | Non-ECC Configuration | ECC Configuration |
|---|---|---|
| 16 MB | 2 Mbit x 64 | 2 Mbit x 72 |
| 32 MB | 4 Mbit x 64 | 4 Mbit x 72 |
| 64 MB | 8 Mbit x 64 | 8 Mbit x 72 |
| 128 MB | 16 Mbit x 64 | 16 Mbit x 72 |
| 256 MB | 32 Mbit x 64 | 32 Mbit x 72 |

- You can install memory in one or both sockets.
- You can vary memory size between sockets.
- The BIOS automatically detects memory type, size, and speed.
- For ECC operation, all installed memory must be ECC.

1. If memory upgrade involves removal of existing DIMMs, do the following:
   A. Turn off all peripheral devices connected to the computer. Turn off the computer.
   B. Remove the computer cover and locate the DIMM sockets. shown in Figure 2-5.

C. Push the clips at either end of the DIMM socket away from the socket. The DIMM pops out of the socket.

Avoid using excessive force as the DIMM sockets are fragile.

D. Hold the DIMM by its edges, lift it away from the socket, and place it in an antistatic package.

E. Replace the computer cover.

2. To install DIMMs, do the following**:**

Perform these steps only in a static-free environment.

A. Turn off all peripheral devices connected to the computer. Turn off the computer.

B. Remove the computer cover and locate the DIMM sockets, shown in Figure 2-5.

C. Remove the DIMM from its antistatic package.

Hold the DIMM by the edges.

D. Insert the DIMM.

i. Push the clips at either end of the DIMM socket away from the socket.

Avoid using excessive force as the DIMM sockets are fragile.

ii. Position the DIMM above the socket and align the two small notches in the bottom edge of the DIMM with the keys in the socket.

iii. Insert the bottom edge of the DIMM into the socket.

iv. Push down on the top edges of the DIMM until the retaining clips snap into place. Make sure that the clips are firmly in place.

E. Replace the computer cover.

F. Turn on the computer.

If you installed a DIMM with ECC memory, you must enable ECC Configuration in BIOS setup (see *Chapter 3, BIOS configuration* for specific instructions).

## Replacing the battery

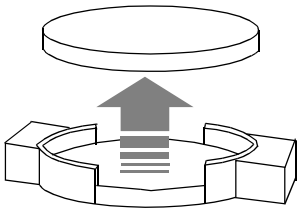
Replace the battery with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to manufacturer's instructions.

Perform these steps only in a static-free environment.

1. Before you begin, write down all the BIOS setup parameters while the battery is still good, or save them, using the CMOS save and restore feature of the BIOS configuration Exit Menu.
2. Turn off the power.

   If you leave the power on when removing the battery, setup values return to default conditions.

3. Locate the battery on the EMB-1, then lift the battery out.



4. Press the new battery into place, positive (+) side up.

   Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to manufacturer's instructions.

5. Restore the CMOS settings as described in the CMOS Save and Restore Sub-Menu on page 34

   After replacing the battery, you may need to reset the system clock.

# 3 BIOS configuration

The EMB-1 uses the PhoenixBIOS to configure and select various system options. This chapter details the various menus and sub-menus used to configure the system.

This chapter is written as though you are setting up each field in sequence and for the first time. Your system may be correctly pre-configured and require very little setup.

You may see some error messages during the execution of the BIOS initialization sequence. If errors occur during the power-on self-test (POST), the BIOS displays the error on the appropriate line of the screen display and, depending on how your system is configured, either pauses or attempts to continue. For information about error messages, see *Appendix F, Error messages*.

## BIOS setup screens

The EMB-1's BIOS includes a setup program that displays and modifies the system configuration. This information is maintained in the EMB-1's nonvolatile CMOS RAM and is used by the BIOS to initialize the EMB-1 hardware.

You can enter the BIOS Setup only during the system reset process, following a power-up, front panel reset, or equivalent. To enter Setup, press the F2 key when prompted.

To revert to the original BIOS settings, do one of the following:

- Select Get Default Values from the Exit menu on page 44.
- Press the F9 key.

Select from the menus shown in the next table to set up the BIOS.

When reading this file online, you can immediately view information about any menu by placing the mouse cursor over menu name and clicking.

| Menu | Sub-menu |
|---|---|
| Main setup menu | Primary/Secondary Master/Slave sub-menus<br>Optional Features sub-menu<br>UBE Shadow Control sub-menu |
| Advanced menu | Advanced Chipset Control sub-menu<br>PCI Configuration sub-menu<br>PCI/PNP ISA UMB Region Exclusion sub-menu<br>PCI/PNP ISA IRQ Resource Exclusion sub-menu<br>Cache Memory sub-menu<br>I/O Device Configuration sub-menu |
| Security menu | None |
| Power menu | None |
| Boot menu | None |
| Exit menu | CMOS Save and Restore sub-menu |

Press the up and down cursor (arrow) keys to move from field to field. Press the right and left arrow keys to move between the menus as shown in the menu bar at the top of the screen. If you use the arrow keys to leave a menu and then return, your active field is always at the beginning of the menu. If you select a sub-menu and then return to the main menu, you return to that sub-menu heading.

Fields with a triangle to the left are actually sub-menu headings; press the Enter key when the cursor rests on one of these headings to reach that sub-menu. For most fields, position the cursor at the field and from the numeric keypad, press the + and – keys to rotate through the available choices. You can also use the Enter key to display choices. Certain numeric fields can also be entered via the keyboard. Once the entry has been changed to appear as desired, use the up and down arrow to move to the next field.

Additional help information is available in the help area on the Setup screen for each menu.

## Main setup menu

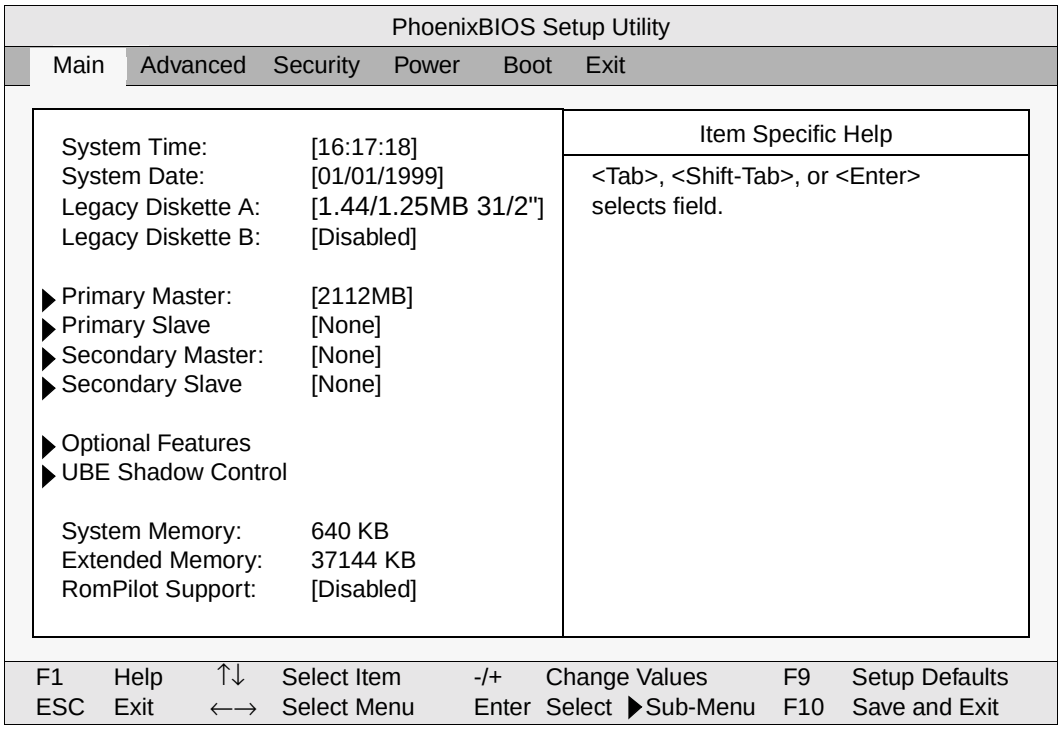



**Figure 3-1. BIOS Setup Main menu**

The far right menu in the menu bar is the Exit menu. Use the options in the Exit menu to save your changes, reload default BIOS settings, and so on. Press the ESC key to go immediately to the Exit menu.

The fields in each menu and sub-menu are explained below. Additional help information is available in the help area on the BIOS setup screen.

| Field | Description |
|---|---|
| System Time/System Date | Sets the system time and date. To change these values, go to each field and enter the desired value. Press the tab key to move from hour to minute to second, or from month to day to year. There is no default value. |
| Legacy Diskette A:<br>Legacy Diskette B: | Identifies the type of floppy disk drive installed as the A: or B: drive. Possible settings include:<br>• **Disabled (default for drive B:)**<br>• **360 KB, 5¼"**<br>• **1.2MB, 5¼"**<br>• **720 KB, 3½"**<br>• **1.44, 31/2" (default for drive A:)**<br>• **2.88 MB, 3½"** |
| Primary Master sub-menu | Displays a menu that you use to enter information for the master IDE drive connected to the primary IDE controller. Once you enter the information, the drive shows as selected on this menu. For more information, see Primary/Secondary Master/Slave sub-menus on page 20. |
| Primary Slave sub-menu | Displays a menu that you use to enter information for the slave IDE drive connected to the primary IDE controller. Once you enter the information, the drive shows as selected on this menu. For more information, see Primary/Secondary Master/Slave sub-menus on page 20. |
| Secondary Master sub-menu | Displays a menu that you use to enter information for the secondary IDE drive connected to the primary IDE controller. Once you enter the information, the drive shows as selected on this menu. For more information, see Primary/Secondary Master/Slave sub-menus on page 20. |
| Secondary Slave sub-menu | Displays a menu that you use to enter information for the secondary IDE drive connected to the primary IDE controller. Once you enter the information, the drive shows as selected on this menu. For more information, see Primary/Secondary Master/Slave sub-menus on page 20. |
| Optional Features sub-menu | Displays a menu that you can use to set and change the keyboard settings and boot-up feature options. For more information, see Optional Features sub-menu on page 24. |
| UBE Shadow Control sub-menu | Displays a menu that you use to control copying information from ROM into RAM and accessing it in the shadow (alternate) memory location. For more information, see UBE Shadow Control sub-menu on page 25. |
| System memory | Displays the amount of conventional memory (below 1MB). This field is not editable; no user interaction is required. |
| Extended memory | Displays the amount of extended memory (above 1MB). This field is not editable; no user interaction is required. |
| RomPilot support | Displays the status of RomPilot. The options are:<br>• **Disabled (default)**<br>• **Enabled** |

## Primary/Secondary Master/Slave sub-menus

There are a total of four IDE adapter sub-menus for the primary and secondary hard disk controllers, each having a master and slave drive menu.

Access this screen to:

- See or reconfigure the detailed characteristics of the primary hard disk (select the IDE Adapter 0 Master item from the Main BIOS Setup).
- Set up new disks and allow the Setup program to determine the proper settings based on information on the disk. Note that the Setup program can detect these settings only on drives that comply with ANSI specifications.
- Set up existing (formatted) disks. Note that you must use the same parameters used when the disk originally was formatted. You must select an option for the Type field, then enter the specific cylinder, head, and sector information listed on the label attached to the drive at the factory.

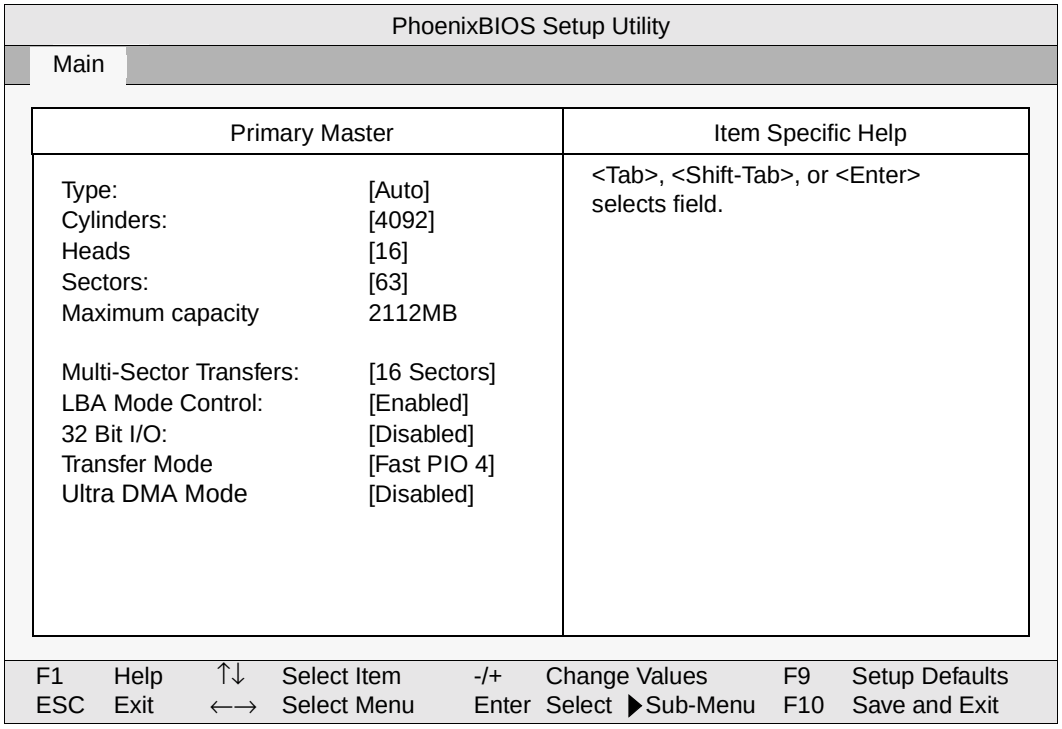



**Figure 3-2. Master/Slave sub-menu**

| Field | Description |
|---|---|
| Type | Identifies the disk type.You can select one of these:<br>• **Auto (default)**: Select this option when you want the POST to query the hard disk for its parameters whenever the POST runs. If a hard disk type is set to “Auto”, but no hard disk is actually present, the BIOS queries the (non-existent) hard disk until it times out, adding a number of seconds to the duration of the POST.<br>• **None**: Select this option if this adapter does not have an IDE hard disk drive.<br>• **CD-ROM**: Select this option if this adapter has a CD-ROM drive.<br>• **IDE Removable:** Provides support for high-capacity disks that can be formatted as floppy or hard disks. This option may be used for compact flash cards.<br>• **ATAPI Removable**: Select this option if this adapter has a removable disk drive.<br>• **Other ATAPI**: Select this option if the adapter has an ATAPI device that is not a CD-ROM or hard drive.<br>• **User**: Select this option if you have an IDE disk but cannot use the “Autotype” feature. Then enter the correct drive values for cylinders, heads, sectors/track, and write precompensation.<br>**Note**: For disks not supplied, consult the product’s documentation.<br>Once you complete setup for the IDE Master, you can choose the IDE Adapter 0 Slave Sub-menu to configure your second drive. When finished, press the ESC key to return to the Main setup menu. |
| Cylinders | Displays the number of cylinders on this system.<br>This field is only editable when you select User in the Type field. |
| Heads | Displays the number of heads on this system.<br>This field is only editable when you select User in the Type field. |
| Sectors | Displays the number of sectors on this system.<br>This field is only editable when you select User in the Type field. |
| Maximum Capacity | Displays the amount of disk space available on this system.<br>This field is only editable when you select User in the Type field. |

| Field | Description |
|---|---|
| Multi-Sector Transfers | Allows the System BIOS to read ahead by the specified number of sectors whenever a disk access is performed. This has the effect of reading more data at once to reduce the absolute number of discrete disk reads performed by the operating system, which may increase system performance.<br>You can select one of these:<br>• **Disabled (default if no drive is installed)**<br>• **2 sectors**<br>• **4 sectors**<br>• **8 sectors**<br>• **16 sectors (default if a drive is installed)**<br>Note that autotyping may change this value if the hard disk reports that it supports block accesses. |
| LBA Mode Control | Determines how the System BIOS references hard disk data. You can use this option only if both the hard disk being configured and the operating system support Logical Block Addressing (LBA). Autotyping may change this value if the hard disk reports that it supports LBA.<br>This field is only editable when you select User in the Type field.<br>You can select one of these:<br>• **Disabled**: Reference hard disk data using the Cylinders/ Heads/Sectors (CHS) method.<br>• **Enabled**: Reference hard disk data as logical blocks.<br>**Note**: You can select this option only if both the hard disk being configured and the OS support LBA. If you enable this option and LBA is not supported, then CHS mode is used. Autotyping may change this value if the hard disk reports that it supports LBA. |
| 32-bit I/O | Determines how the System BIOS accesses the hard disk controller. Autotyping does not affect this option.<br>You can select one of these:<br>• **Enabled**: Accesses with 32-bit I/O accesses. Select this option to maximize system performance when the onboard PCI IDE controller is used if drive supports 32-bit I/O.<br>• **Disabled (default)**: Select this option if an ISA Bus IDE controller is installed in the system. |

| Field | Description |
|---|---|
| Transfer Mode | Selects the mode that the System BIOS uses to access the hard disk.<br>This field is only editable when you select User in the Type field.<br>You can select one of these:<br>• **Standard**<br>• **Fast PIO 1**<br>• **Fast PIO 2**<br>• **Fast PIO 3**<br>• **Fast PIO 4**<br>• **Fast PIO 3 / DMA 1**<br>• **Fast PIO 4 / DMA 2**<br>Older hard disks only support “Standard”. Newer hard disks adhering to “Fast ATA” or “Enhanced IDE” specifications may support the fast programmed I/O or DMA modes. Autotyping may change this value depending on the transfer modes that the hard disk reports it supports.<br>The fast DMA modes take full advantage of the onboard bus mastering hard disk controller and should yield the highest performance when used in conjunction with multitasking operating systems that support it. |
| Ultra DMA Mode | Selects the Ultra DMA Mode that the System BIOS uses to access the hard disk. DMA modes take full advantage of the onboard bus mastering hard disk controller and should yield the highest performance when used in conjunction with multitasking OSs that support it.<br>This field is only editable when you select User in the Type field.<br>You can select one of these:<br>• **Disabled**<br>• **Mode 0**<br>• **Mode 1**<br>• **Mode 2**<br>• **Mode 3**<br>• **Mode 4** |

## Optional Features sub-menu

The Optional Features Sub-menu allows the user to set and change keyboard settings.

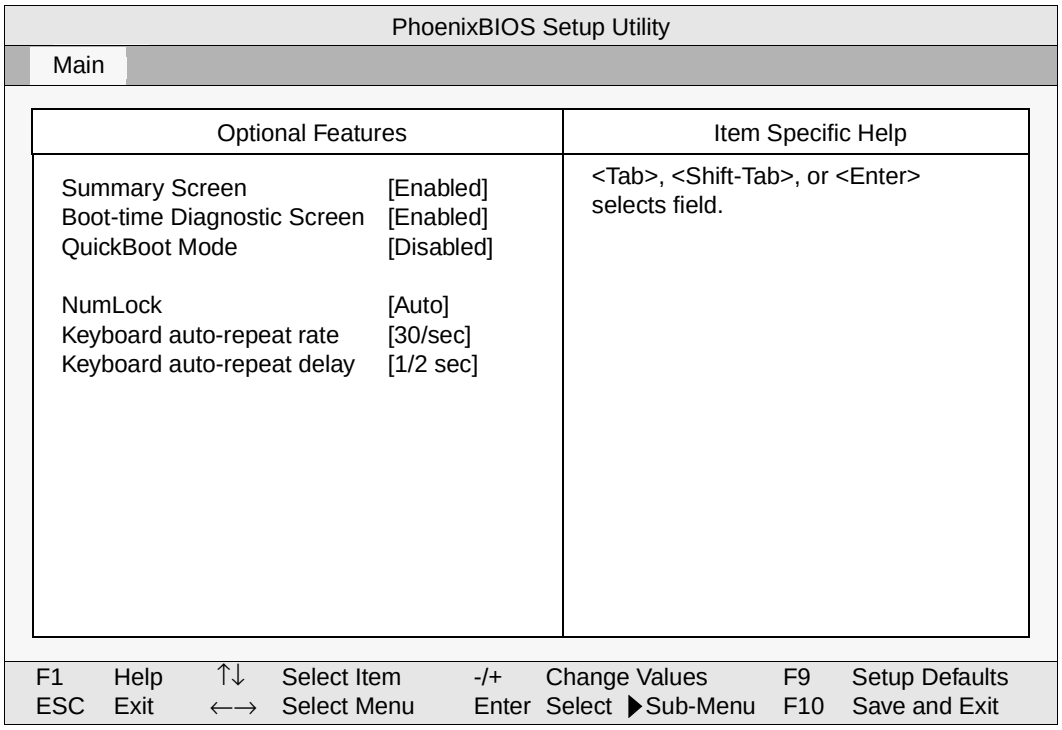



**Figure 3-3. Optional Features sub-menu**

| Field | Description |
|---|---|
| Summary Screen | Determines whether the system configuration displays prior to loading the operating system.<br>You can select one of these:<br>• **Enabled (default)**: Displays a summary of the system configuration before the operating system starts to load<br>• **Disabled**: Does not display a summary of the system configuration before the operating system starts to load. Selecting this option speeds up the boot process. |
| Boot-time Diagnostic Screen | Determines whether the system displays a custom boot logo or the boot time diagnostic screen.<br>You select one of these:<br>• **Disabled**: Displays a custom boot logo.<br>• **Enabled (default)**: Displays the boot time diagnostic screen. |
| QuickBoot Mode | Determines whether the system runs selected tests during boot-up.<br>You can select one of these:<br>• **Disabled (default)**: Does not run certain tests during boot. Selecting this option speeds up the boot process.<br>• **Enabled**: Runs tests during boot. |

| Field | Description |
|---|---|
| Numlock | Determines whether the keyboard numbers (the Numlock feature) operates.<br>You can select one of these:<br>• **Auto (default)**:<br>• **On**: Engages the Numlock key at boot.<br>• **Off** Disengages the Numlock key at boot. |
| Keyboard Auto-repeat Rate | Sets the auto-repeat rate if holding a key down on the keyboard.<br>You can select one of these:<br>• **30/second (default)**<br>• **26.7/second**<br>• **21.8/second**<br>• **18.5/second**<br>• **13.3/second**<br>• **10/second**<br>• **6/second**<br>• **2/second** |
| Keyboard Auto-repeat Delay | Sets the delay between when a key is pressed and when the auto-repeat feature begins.<br>You can select one of these:<br>• **½ second (default)**<br>• **¼ second**<br>• **¾ second**<br>• **1 second** |

## UBE Shadow Control sub-menu

*Shadowing* refers to the technique of copying BIOS extensions from ROM into DRAM and accessing them from DRAM. This allows the CPU to access the BIOS extensions much more quickly and generally increases system performance if many calls to the BIOS extensions are made.

### About shadow memory regions

There is no effect on the system if a region is shadowed that does not contain a BIOS extension. Note that each shadow region in the setup menu is 16KB in size. Multiple shadow regions may have to be enabled if the BIOS extension to be shadowed is larger than 16KB.

For example, if you select a source offset of 18000h, a destination of D4000h, and a size of 16KB, the BIOS will shadow the contents of 98000h–A0000h in the FBD (as measured from the base of the FBD) to D4000h–DC000h in memory.

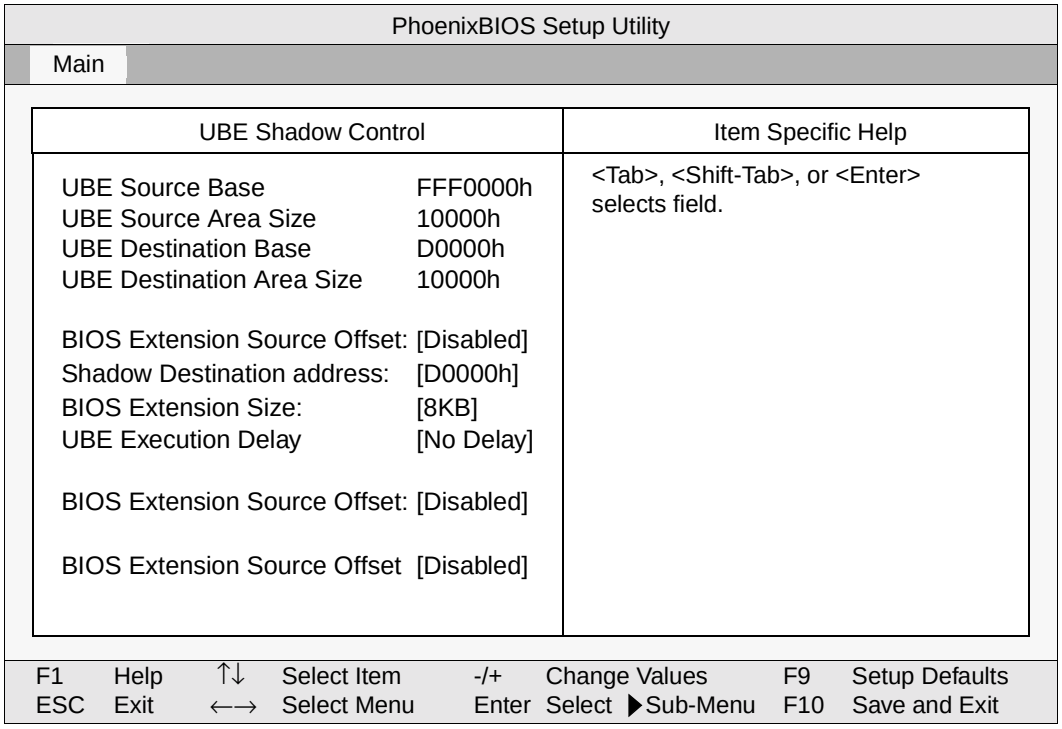



**Figure 3-4. UBE Shadow Control sub-menu**

| Field | Description |
|---|---|
| BIOS Extension Source Offset | Specifies the location of the BIOS extension from the base address of main block #5 of the FBD.<br>You can select one of these:<br>• **Disabled (default)** • **8000h•**<br>• **0000h** • **A000h**<br>• **2000h** • **C000h**<br>• **4000h** • **E000h**<br>• **6000h** |
| Shadow Destination Address | Specifies the destination address of the BIOS extension in shadow memory.<br>You can select one of these:<br>• **0000h (default)** • **8000h**<br>• **2000h** • **A000h**<br>• **4000h** • **C000h**<br>• **6000h** • **E000h**<br>**Note**: This field displays only if the BIOS Extension Source field contains a value other than [Disabled]. |

| Field | Description |
|---|---|
| BIOS Extension Size | Identifies the BIOS extension's size.<br>You can select one of these:<br>• **8KBytes (default)** • **40KBytes**<br>• **16KBytes** • **48KBytes**<br>• **24KBytes** • **56KBytes**<br>• **32KBytes** • **64KBytes**<br>**Note**: This field displays only if the BIOS Extension Source field contains a value other than [Disabled]. |
| UBE Execution Delay | Specifies the amount of execution delay. The options are:<br>• **No delay (default)**<br>• **1 sec**<br>• **2 sec**<br>• **3 sec**<br>• **4 sec**<br>• **5 sec**<br>• **6 sec**<br>• **7 sec** |

# Advanced menu

This menu contains settings for integrated peripherals, memory shadow, cache, and large disk access mode. You access this menu by selecting Advanced from the Main BIOS Setup menu.

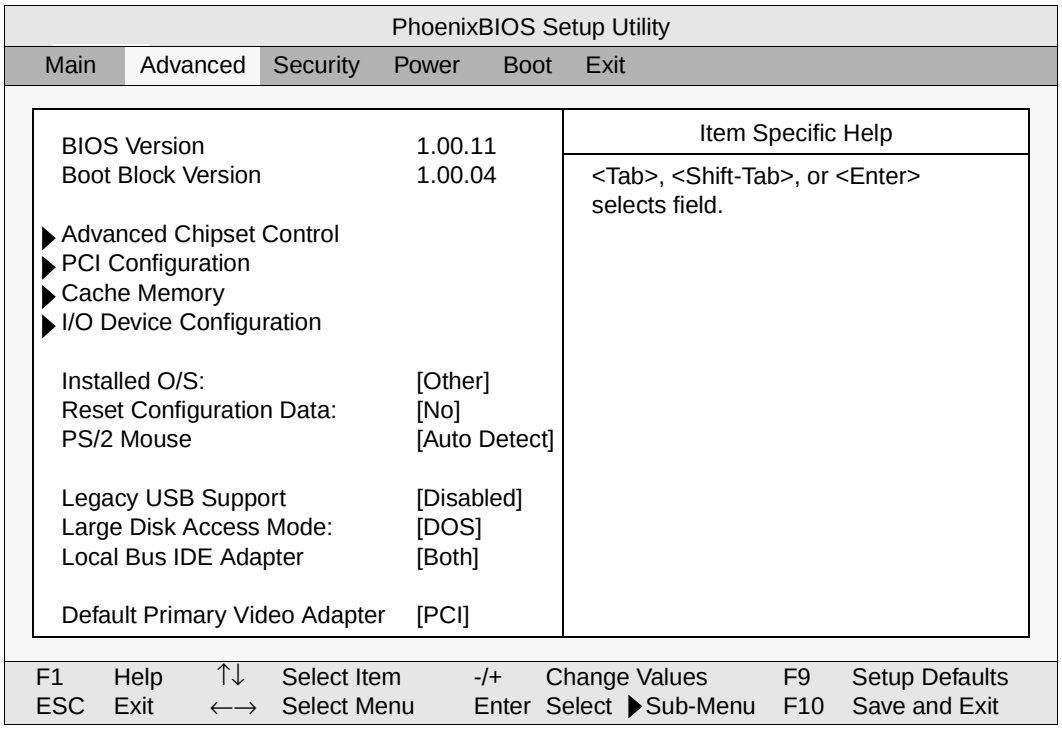



**Figure 3-5. Advanced menu**

| Field | Description |
|---|---|
| Advanced Chipset Control sub-menu | Displays a menu that you use to configure the PCI-chipset. For more information, see Advanced Chipset Control sub-menu on page 31 |
| PCI Configuration sub-menu | Displays a menu that you use to enter configuration information for PCI devices. For more information, see PCI Configuration sub-menu on page 32. |
| Cache Memory sub-menu | Displays a menu that you use to control the use of CPU cache. For more information, see Cache Memory sub-menu on page 35 |
| I/O Device Configuration sub-menu | Displays a menu that you use to configure peripheral devices. For more information, see I/O Device Configuration sub-menu on page 38. |

| Field | Description |
|---|---|
| Installed OS | Identifies the operating system (OS) you plan to use on this system.<br>You can select one of these:<br>• **Other (default)**: Select this option when you plan to use an OS other than Windows 95, Windows 98, and Windows NT.<br>• **PnP OS**: Select this option when you plan to use any PnP OS.<br>**Note**: Setting this to the incorrect value may produce unexpected results. |
| Reset Configuration Data | Determines whether to clear the Extended System Configuration Data (ESCD) block that resides in the Flash Boot Device (FBD) parameter block #2.<br>You can select one of these:<br>• **No (default)**: Does not clear the ESCD block.<br>• **Yes**: Clears the ESCD block. You must clear the block the first time a system is turned on or if the ESCD becomes corrupted. This option automatically resets to “No” after the block is cleared. |
| PS/2 Mouse | Determines whether a PS/2 mouse functions on this system.<br>• **Auto Detect (default)**: Allows the system BIOS to determine whether a PS/2 mouse functions on this system.<br>• **Disabled**: Prevents any installed PS/2 mouse from functioning and frees IRQ 12.<br>• **Enabled**: Sets the system to use a PS/2 mouse, if installed. |
| Legacy USB Support | Determines whether the system supports the Legacy Universal Serial Bus (USB).<br>You can select one of these:<br>• **Disabled (default)**: The system does not support the Legacy USB<br>• **Enabled**: The system supports the Legacy USB. |

| Field | Description |
|---|---|
| Large Disk Access Mode | Specifies whether MS-DOS systems can use hard disks up to 8GB (1024C x 255H x 63S) without special drivers or LBA.<br>If the drive fails while installing new software, change this setting and try again.<br>You can select one of these:<br>• **DOS (default)**: Causes the System BIOS to perform cylinder/head translation, if the drive is configured in Setup to have more than 1024 cylinders. Select this option if your system uses a drive larger than 528 MB and runs DOS or MS-DOS†.<br>• **Other**: Select this option if your system uses a drive larger than 528 MB and runs an OS other than DOS or MS-DOS. |
| Local Bus IDE adapter | Determines which, if any, onboard PCI Bus IDE hard disk controllers are enabled.<br>You can select one of these:<br>• **Both (default)**: Enables both the primary and secondary controllers.<br>• **Disabled**: Select this option if the system contains a PCI hard disk controller.<br>• **Primary**: Enables only the primary controller.<br>• **Secondary**: Enables only the secondary controller. |
| Default Primary Video Adapter | Specifies the type of video card used for the boot display device. The options are:<br>• **PCI (default if a PCI card is installed or if onboard video is used)**<br>• **AGP (default if an AGP card is installed)** |

## Advanced Chipset Control sub-menu

Use the options in this sub-menu to configure the PCI chipset.

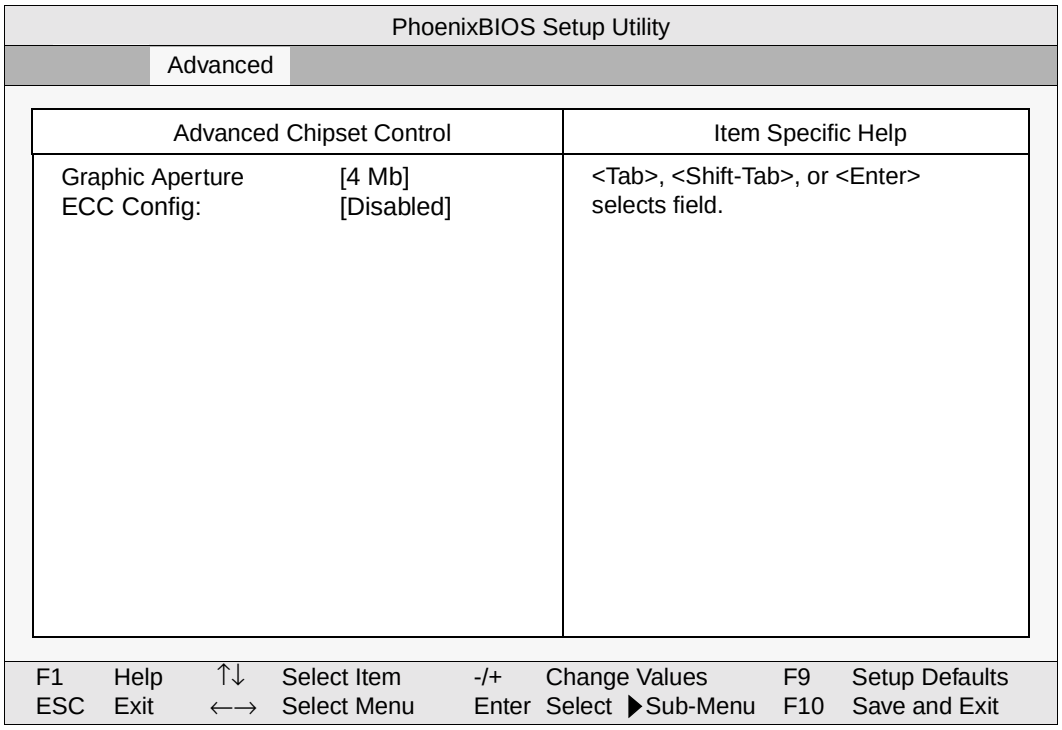



**Figure 3-6. Advanced Chipset Control sub-menu**

| Field | Description |
|---|---|
| Graphic Aperture | Determines the size of the Graphics Aperture for the AGP video device.<br>• **4 Mb (default if onboard video is installed)**<br>• **8 Mb**<br>• **16 Mb**<br>• **32 Mb**<br>• **64 Mb**<br>• **128 Mb**<br>• **256 Mb** |
| ECC Config | • **Disabled (default)**<br>• **EC**<br>• **ECC**<br>• **ECC Scrub** |

## PCI Configuration sub-menu

Use the options in this sub-menu to control the exclusion of the UMB region for PCI or ISA and the exclusion of the IRQs for PCI or ISA

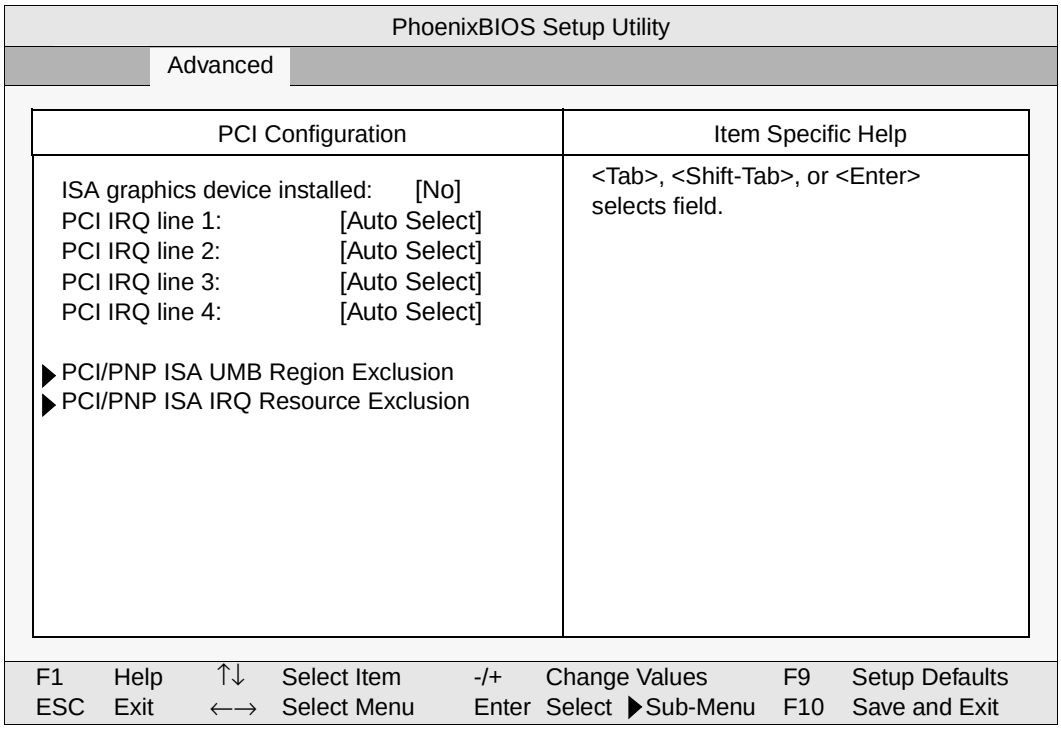



**Figure 3-7. PCI Configuration sub-menu**

| Field | Description |
|---|---|
| ISA graphics device installed | Specifies whether an ISA graphics device is installed in the system.<br>• **No (default)**: No ISA graphics device exists in this system.<br>• **Yes**: An ISA graphics device exists in this system. |
| PCI IRQ lines | Determines which IRQ the PCI IRQ (PIRQ) lines (1–4) use.<br>You can select one of these:<br>• **Auto Select (default)**<br>• **3**<br>• **4**<br>• **5**<br>• **7**<br>• **9**<br>• **10**<br>• **11**<br>• **12**<br>• **14**<br>• **15**<br>• **Disabled** |
| PCI/PNP ISA UMB Region Exclusion sub-menu | Displays a menu that you use to reserve specific upper memory blocks for ISA devices. For more information, see PCI/PNP ISA UMB Region Exclusion sub-menu on page 33. |
| PCI/PNP ISA IRQ Resource Exclusion sub-menu | Displays a menu that you use to control the ISA interrupt resources. For more information, see PCI/PNP ISA IRQ Resource Exclusion sub-menu on page 34. |

### PCI/PNP ISA UMB Region Exclusion sub-menu

The PCI/PNP ISA UMB Region Exclusion sub-menu control upper memory blocks for use of Legacy ISA devices.

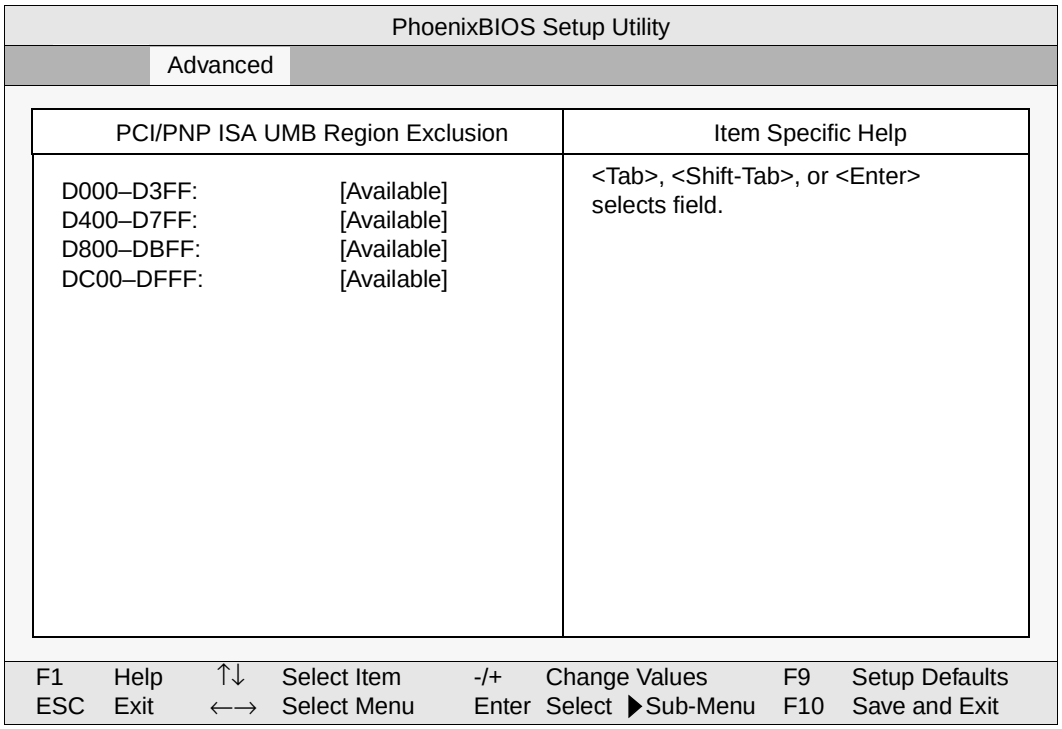



**Figure 3-8. PCI/PNP ISA UMB Region Exclusion sub-menu**

| Field | Description |
|---|---|
| Memory Regions | Determines the use of each UMB region.<br>You can select one of these:<br>• **Available (default)**: Makes the regions available for PCI use.<br>• **Reserved**: Reserves the specified block of upper memory regions for ISA use. |

### PCI/PNP ISA IRQ Resource Exclusion sub-menu

The PCI/PNP ISA IRQ Resource Exclusion Sub-Menu controls the exclusion of PCI and ISA interrupt regions.

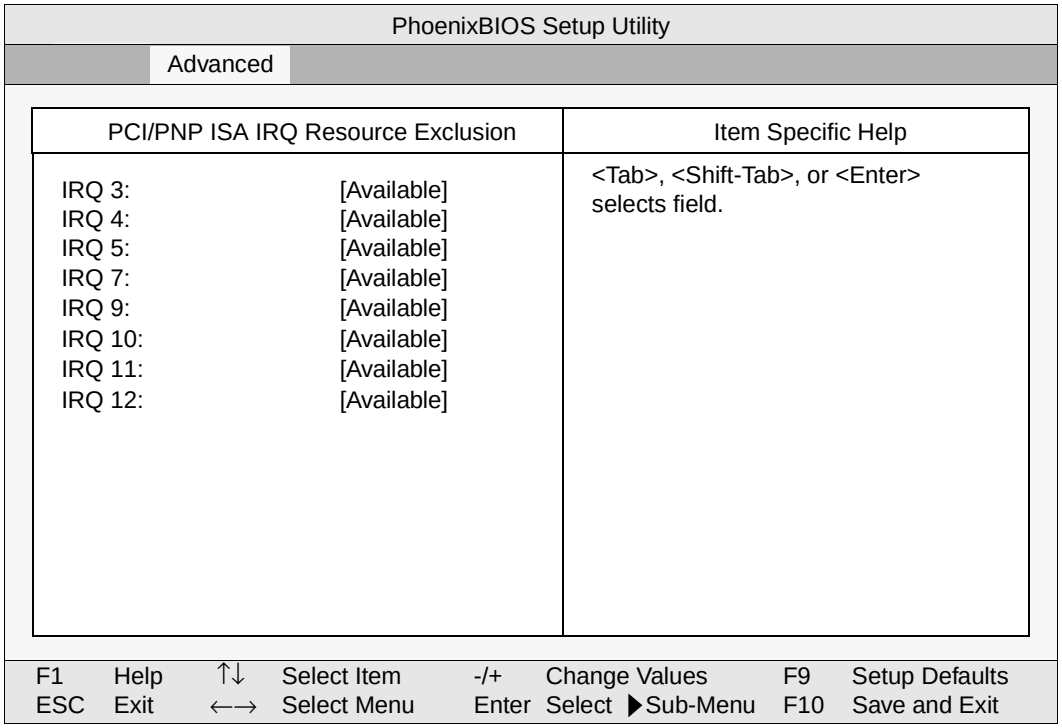



**Figure 3-9. PCI/PNP ISA IRQ Resource Exclusion sub-menu**

| Field | Description |
|---|---|
| Interrupts | Determines the use of each interrupt.<br>You can select one of these:<br>• **Available (default)**: Makes the specified ISA IRQs available for PCI use.<br>• **Reserved**: Reserves the interrupt for ISA use. |

## Cache Memory sub-menu

The options in this screen control the cacheability of certain memory regions and also the settings of the Level 2 (L2) cache.

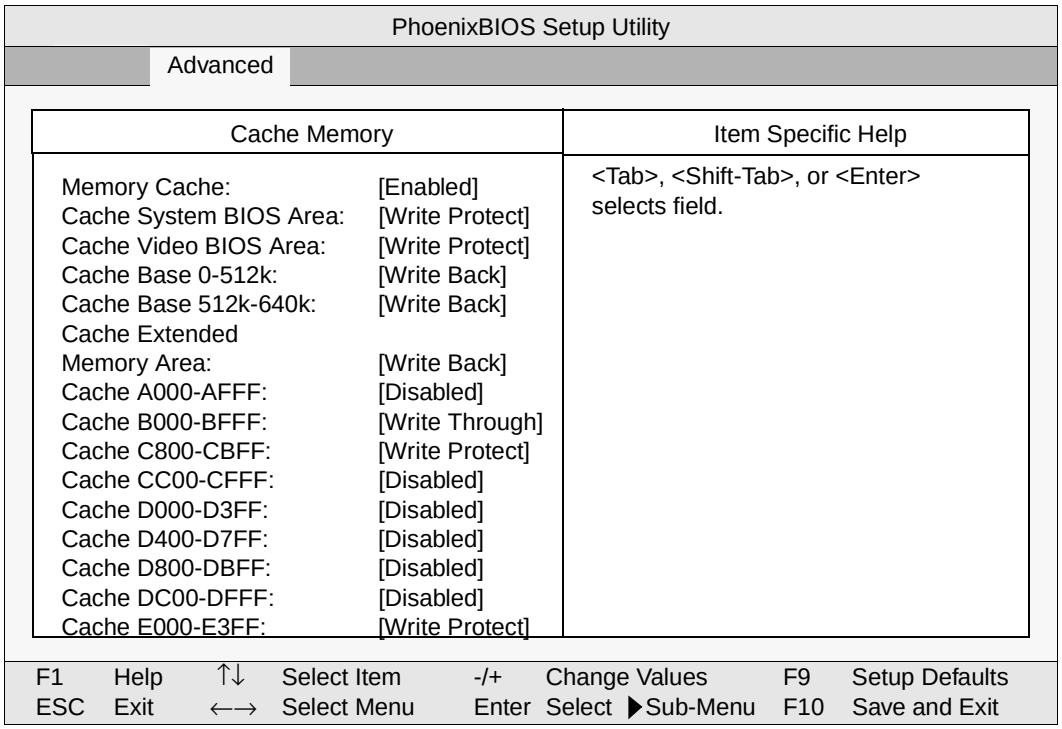



**Figure 3-10. Cache memory sub-menu**

| Field | Description |
|---|---|
| Memory Cache | Enables (default) or disables memory caching. |
| Cache System BIOS Area | Determines whether the System BIOS is cached in DRAM.<br>You can select one of these:<br>• **Write Protect (default)**: caches the System BIOS in the 0E0000h through 0FFFFFh DRAM area<br>• **uncached**: Does not cache the system BIOS. |
| Cache Video BIOS Area | Determines whether the VGA BIOS is cached in a region.<br>You can select one of these:<br>• **Write Protect (default)**: caches the VGA BIOS in the 0C0000h through 0C7FFFh region<br>• **uncached**: Does not cache the VGA BIOS. |

| Field | Description |
|---|---|
| Cache Bases | Determines how the system caches base memory. You can select one of these:<br>• **Write Back (default)**: Writes and reads to and from system memory are cached, then written to system memory when you perform a write-back operation.<br>Select this option to reduce bus traffic by eliminating unnecessary writes to system memory.<br>This option provides the best performance, but requires that all devices that access system memory on the system bus be able to snoop memory accesses to ensure system memory and cache coherency.<br>• **Write Through**: Writes and reads to and from system memory are cached.<br>Select this option for frame buffers or when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses.<br>• **Write Protect**: Reads come from cache lines when possible, and read misses cause cache fills. Writes are propagated to the system bus and cause corresponding cache lines on all processors on the bus to be invalidated. Speculative reads are allowed.<br>• **uncached**: The system does not cache memory. |
| Cache Extended Memory Area | Determines how the system caches extended memory. You can select one of these:<br>• **Write Back (default)**: Writes and reads to and from system memory are cached, then written to system memory when you perform a write-back operation.<br>Select this option to reduce bus traffic by eliminating unnecessary writes to system memory.<br>This option provides the best performance, but requires that all devices that access system memory on the system bus be able to snoop memory accesses to ensure system memory and cache coherency.<br>• **Write Through**: Writes and reads to and from system memory are cached.<br>Select this option for frame buffers or when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses.<br>• **Write Protect**: Reads come from cache lines when possible, and read misses cause cache fills. Writes are propagated to the system bus and cause corresponding cache lines on all processors on the bus to be invalidated. Speculative reads are allowed.<br>• **uncached**: The system does not cache memory. |

| Field | Description |
|---|---|
| Cache Memory Regions<br>Cache A000-AFFF<br>Cache B000-BFFF<br>Cache C800-CBFF<br>Cache CC00-CFFF<br>Cache D000-D3FF<br>Cache D400-D7FF<br>Cache D800-DBFF<br>Cache DC00-DFFF<br>Cache E000-E3FF<br>Cache E400-E7FF<br>Cache E800-E8FF<br>Cache EC00-EFFF | Determines how the system deals with specified memory blocks or shadow[1] memory. You can select one of these:<br>• **Disabled (default)**: The system does not cache memory.<br>• **USWC Caching**: System memory locations are not cached (as with uncacheable memory) and coherency is not enforced by the processor's bus coherency protocol. Speculative reads are allowed. Writes may be delayed and combined in the write buffer to reduce memory accesses.<br>Select this option for video frame buffers, where the order of writes is unimportant as long as the writes update memory so they can be seen on the graphics display.<br>• **Write Back**: Writes and reads to and from system memory are cached, then written to system memory when you perform a write-back operation.<br>Select this option to reduce bus traffic by eliminating unnecessary writes to system memory.<br>This option provides the best performance, but requires that all devices that access system memory on the system bus be able to snoop memory accesses to ensure system memory and cache coherency.<br>• **Write Through**: Writes and reads to and from system memory are cached.<br>Select this option for frame buffers or when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses.<br>• **Write Protect**: Reads come from cache lines when possible, and read misses cause cache fills. Writes propagate to the system bus and cause corresponding cache lines on all processors on the bus to be invalidated. Speculative reads are allowed.<br>When BIOS extensions are present in these regions, enabling caching for that region increases performance |

## I/O Device Configuration sub-menu

Use the options in this sub-menu to configure the onboard serial and parallel port and disk controllers.

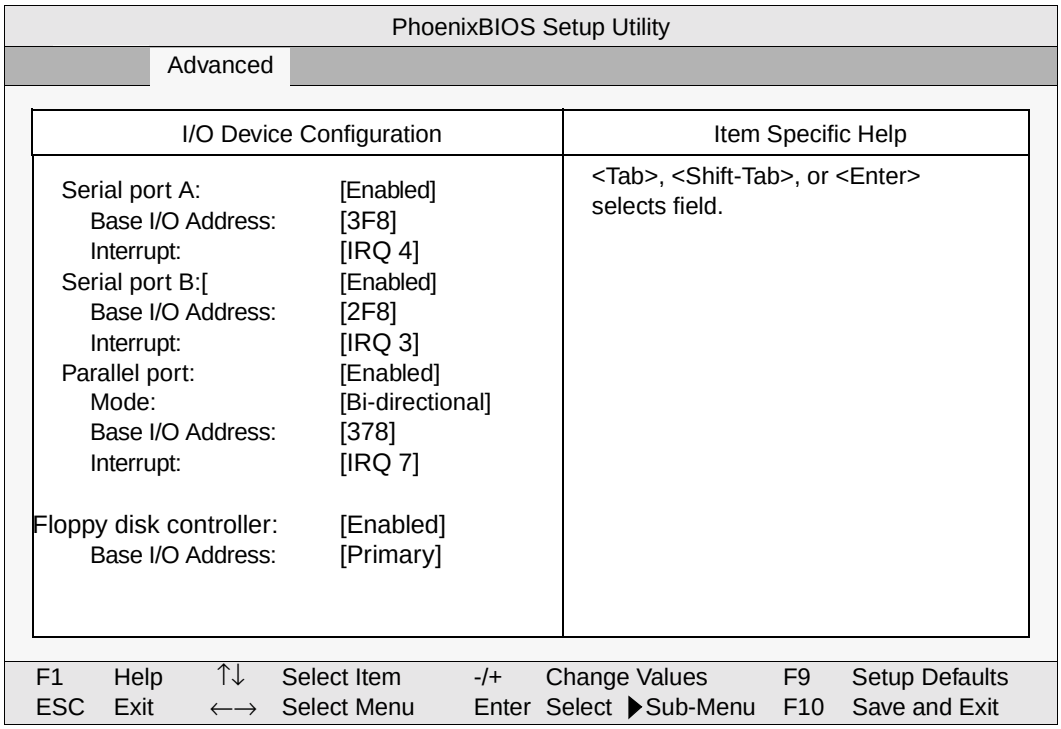



**Figure 3-11. I/O Device Configuration sub-menu**

| Field | Description |
|---|---|
| Serial Port A/Serial Port B | Configures the selected serial port, labelled COM 1 or COM 2.<br>You can select one of these:<br>• **Enabled (default)**: The serial port is configured.<br>• **Auto**: Either the BIOS or OS configures the serial port.<br>• **Disabled**: The serial port is not configured. |
| Base I/O Address | Configures the base address for the selected serial port. If you select a value already used by another serial port, an asterisk displays at the left side of the screen.<br>You can select one of these:<br>• **3F8 (default, Port A)**<br>• **2F8 (default, Port B)**<br>• **3E8**<br>• **2E8**<br>**Note**: This field displays only if the Serial Port field contains a value of [Enabled]. |

| Field | Description |
|---|---|
| Interrupt | Specifies which interrupt line the serial port uses.<br>• **IRQ 3 (default, Port B)**<br>• **IRQ 4 (default, Port A)**<br>**Note**: This field displays only if the Serial Port field contains a value of [Enabled]. |
| Parallel Port | Configures the parallel port, labelled LPT.<br>You can select one of these:<br>• **Enabled (default)**: The parallel port is configured.<br>• **Disabled**: The parallel port is not configured.<br>• **Auto**: Either the BIOS or OS configures the parallel port. |
| Mode | Configures the mode for the parallel port.<br>You can select one of these:<br>• **Bi-directional (default)**<br>• **Output only**<br>• **EPP**<br>• **ECP**<br>**Note**: This field displays only if the Parallel Port field contains a value of [Enabled], [OS Controlled], or [Auto]. |
| Base I/O Address | Configures the I/O base address for the parallel port.<br>You can select one of these:<br>• **378 (default)**<br>• **278**<br>• **3BC**<br>**Note**: This field displays only if the Parallel Port field contains a value of [Enabled]. |
| Interrupt | Specifies which interrupt line the parallel port uses.<br>• **IRQ 5**<br>• **IRQ 7 (default)**<br>**Note**: This field displays only if the Parallel Port field contains a value of [Enabled]. |
| Floppy Disk Controller | Determines whether the floppy disk controller is available for use.<br>You can select one of these:<br>• **Enabled (default)**: User configuration.<br>• **Disabled**: No configuration.<br>• **Auto** Either the BIOS or OS configures the floppy disk controller. |
| Base I/O Address | Configures the base I/O address for the floppy disk controller. You can select one of these:<br>• **Primary (default)**<br>• **Secondary** |

# Security menu

The Security menu sets and changes passwords and security features. The supervisor password gives unrestricted access to view and change all setup options. The user password restricts who can view and change setup options.

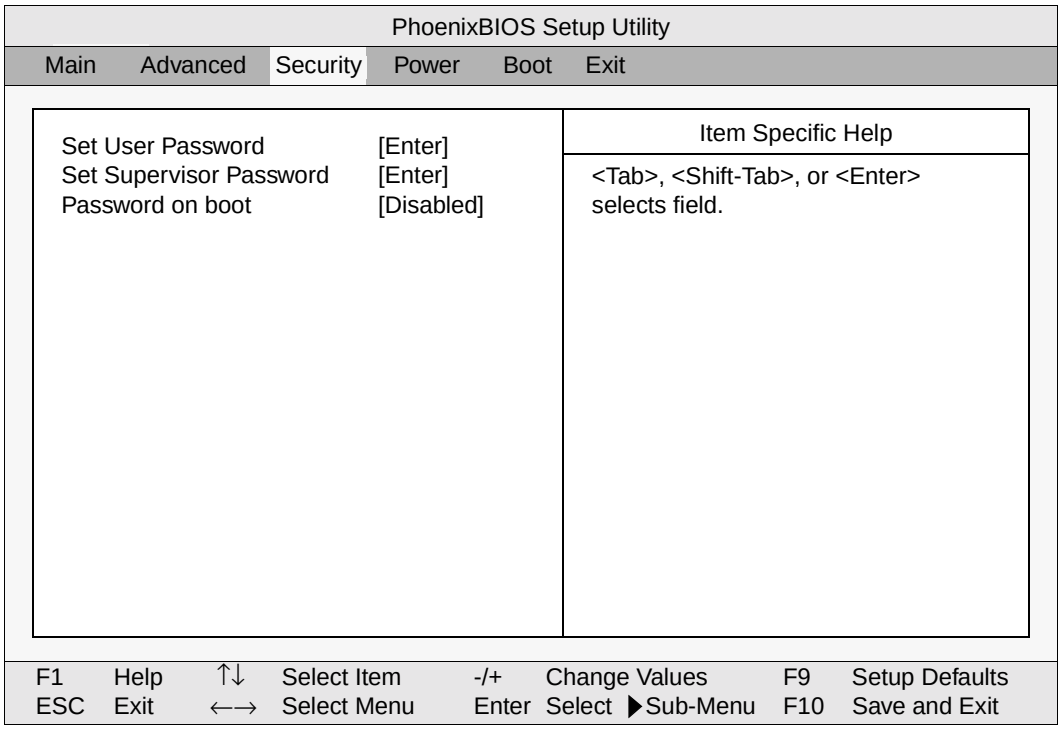



**Figure 3-12. Security menu**

| Field | Description |
|---|---|
| Set User Password | Sets the user password. |
| Set Supervisor Password | Sets supervisor's password. Supervisor's password controls access to the setup utility. |
| Password on Boot | Determines whether the user must enter a password before the system boots.<br>You can select one of these:<br>• **Disabled (default)** Password is not required.<br>• **Enabled** Password is required. |

# Power menu

Options in this menu control power facilities.

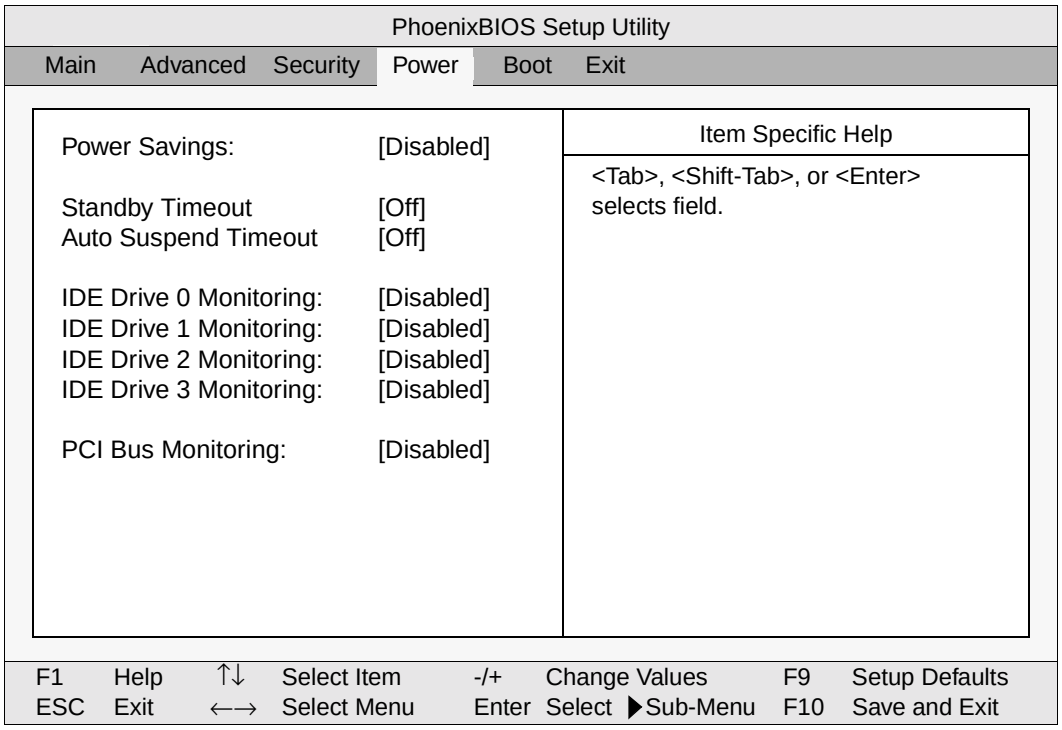



**Figure 3-13. Power menu**

| Field | Description |
|---|---|
| Power Savings | Determines the type, if any, of power management.<br>You can select one of these:<br>• **Disabled (default)**<br>• **Customized**<br>• **Maximum Power Savings**<br>• **Maximum Performance** |
| Standby Timeout | Determines the inactivity duration, if any, required to elapse before the system is placed in Standby Mode.<br>You can select one of these:<br>• **Off (default)**<br>• **1 min (default if Power Savings is set to Maximum Power Savings)**<br>• **2 min**<br>• **4 min**<br>• **6 min**<br>• **8 min**<br>• **12 min**<br>• **16 min (default if Power Savings is set to Maximum Performance)**<br>**Note**: You can edit this field only if Power Savings is set to Customized. |

| Field | Description |
|---|---|
| Auto Suspend Timeout | Sets the inactivity duration, if any, required to elapse before the system goes into Suspend Mode from Standby Mode.<br>You can select one of these:<br>• **Off (default)**<br>• **5 Minutes (default if Power Savings is set to Maximum Battery Life)**<br>• **10 Minutes**<br>• **15 Minutes**<br>• **20 Minutes**<br>• **30 Minutes**<br>• **40 Minutes**<br>• **60 Minutes (default if Power Savings is set to Maximum Performance)**<br>**Note**: You can edit this field only if Power Savings is set to Customized. |
| IDE Drive 0–3 Monitoring | Determines whether activity is generated on the IDE device (required to keep the system awake).<br>You can select one of these:<br>• **Disabled (default)**<br>• **Enabled** |
| PCI Bus Monitoring | Determines whether activity is generated on the PCI Bus (required to keep the system awake).<br>You can select one of these:<br>• **Disabled (default)**<br>• **Enabled** |

# Boot menu

The Boot menu changes boot sequence options.

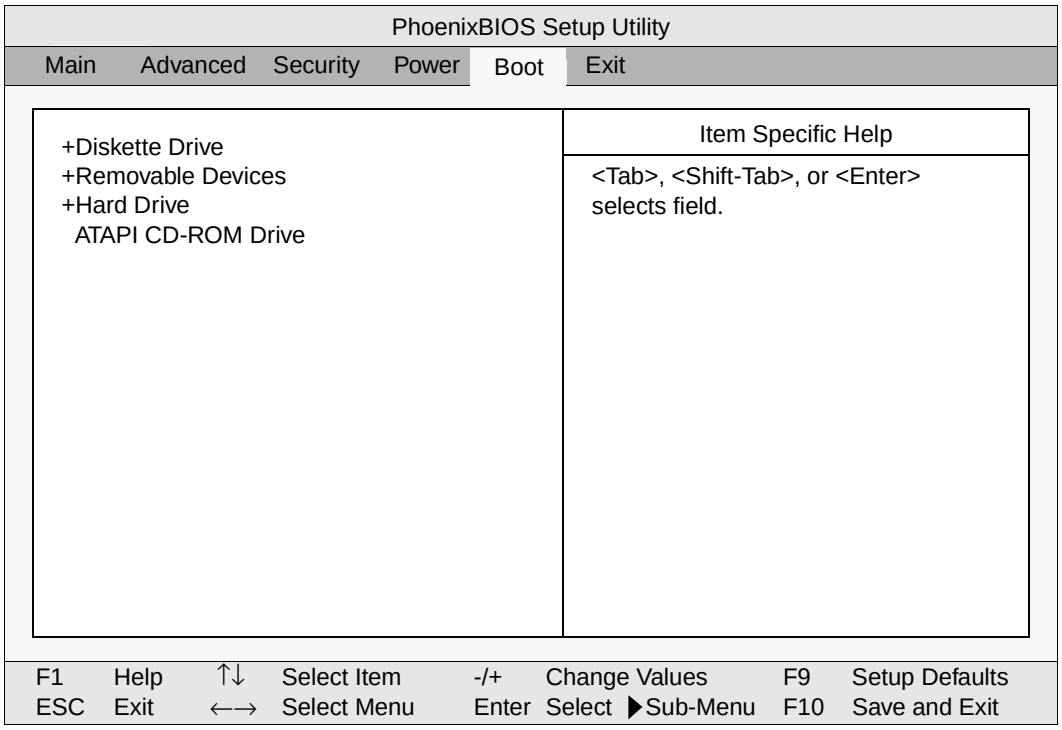



**Figure 3-14. Boot menu**

To move an item to a higher level in the list, highlight the item and then press the “+” key. To move an item to a lower level in the list, highlight the item and then press the “–” key.

To display all boot device sub-menus under all respective device types, press the Ctrl and Enter keys at the same time.

To display a sub-menu that lists all devices of a specified type available on the system, highlight the device type and press the Enter key. If more than one device of that type exists, use the “+” and “–” keys to change the boot order within the given device type.

# Exit menu

Use the options in this menu to save and exit, or abandon your changes and exit to the system.

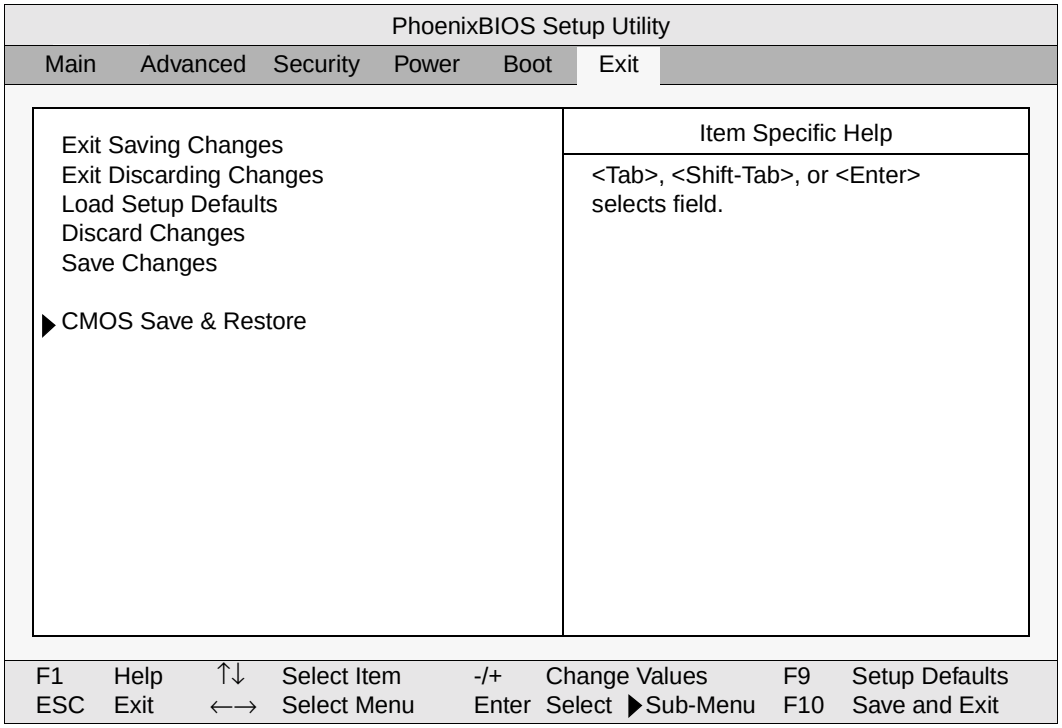



**Figure 3-15. Exit menu**

| Field | Description |
|---|---|
| Exit Saving Changes | Saves the values you just entered and exits to load the operating system. The new values are loaded, and you exit and reboot. |
| Exit Discarding Changes | Discards the changes you just made and revert to the BIOS as it was before you entered the BIOS Setup program. The system boots with the old values. |
| Load Setup Values | Resets the BIOS values to the original, default values set at the factory, before any suppliers or other end users made changes. |
| Discard Changes | Loads the system with the previous values before this editing session started. You do not exit. |
| Save Changes | Saves the edits you made during this session but does not exit. |
| CMOS Save & Restore | Displays a menu that controls how the system handles CMOS values. For more information, see *CMOS Save and Restore sub-menu* on 45. |

## CMOS Save and Restore sub-menu

Options in this menu specify how the system handles CMOS values.

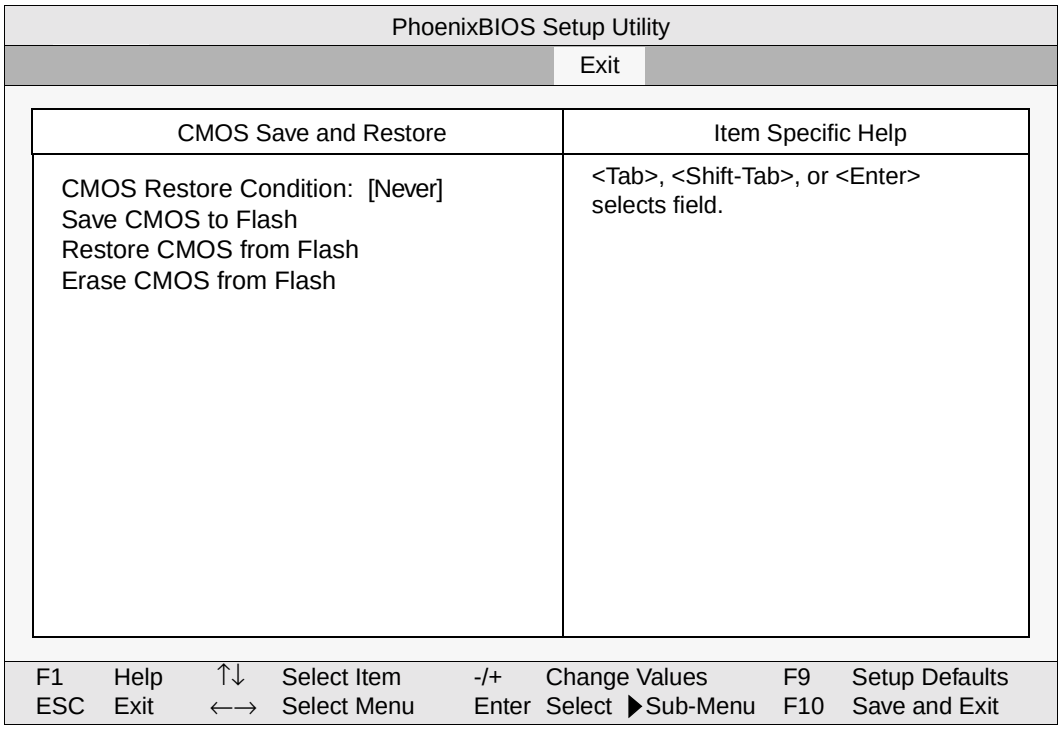



**Figure 3-16. CMOS Save and Restore sub-menu**

| Field | Description |
|---|---|
| CMOS Restore Condition | Determines the conditions under which the BIOS restores CMOS RAM from FBD Parameter Block #1 when booting.<br>You can select one of these:<br>• **Never (default)**<br>• **Always**<br>• CMOS Corruption |
| Save CMOS to Flash | Immediately saves current settings in the Setup utility to CMOS RAM and into FBD Parameter Block #1. This process may take several seconds to complete.<br>**Note**: Always select this option *before* restoring CMOS from Flash. |
| Restore CMOS from Flash | Immediately restores CMOS RAM and current settings in the Setup utility from FBD Parameter Block #1.<br>**Note**: This option is available only if the CMOS was previously saved to Flash. |
| Erase CMOS from Flash | Immediately erases the CMOS image stored in the flash device. |

# 4 Theory of operations

## Overview

The EMB-1 is a standard Celeron-based, PC-compatible motherboard. It fits into a standard ATX form-factor chassis and it requires an ATX power supply.

When reading this file online, you can immediately view information about any topic by placing the mouse cursor over a task and clicking.

# Organization

## Block diagram

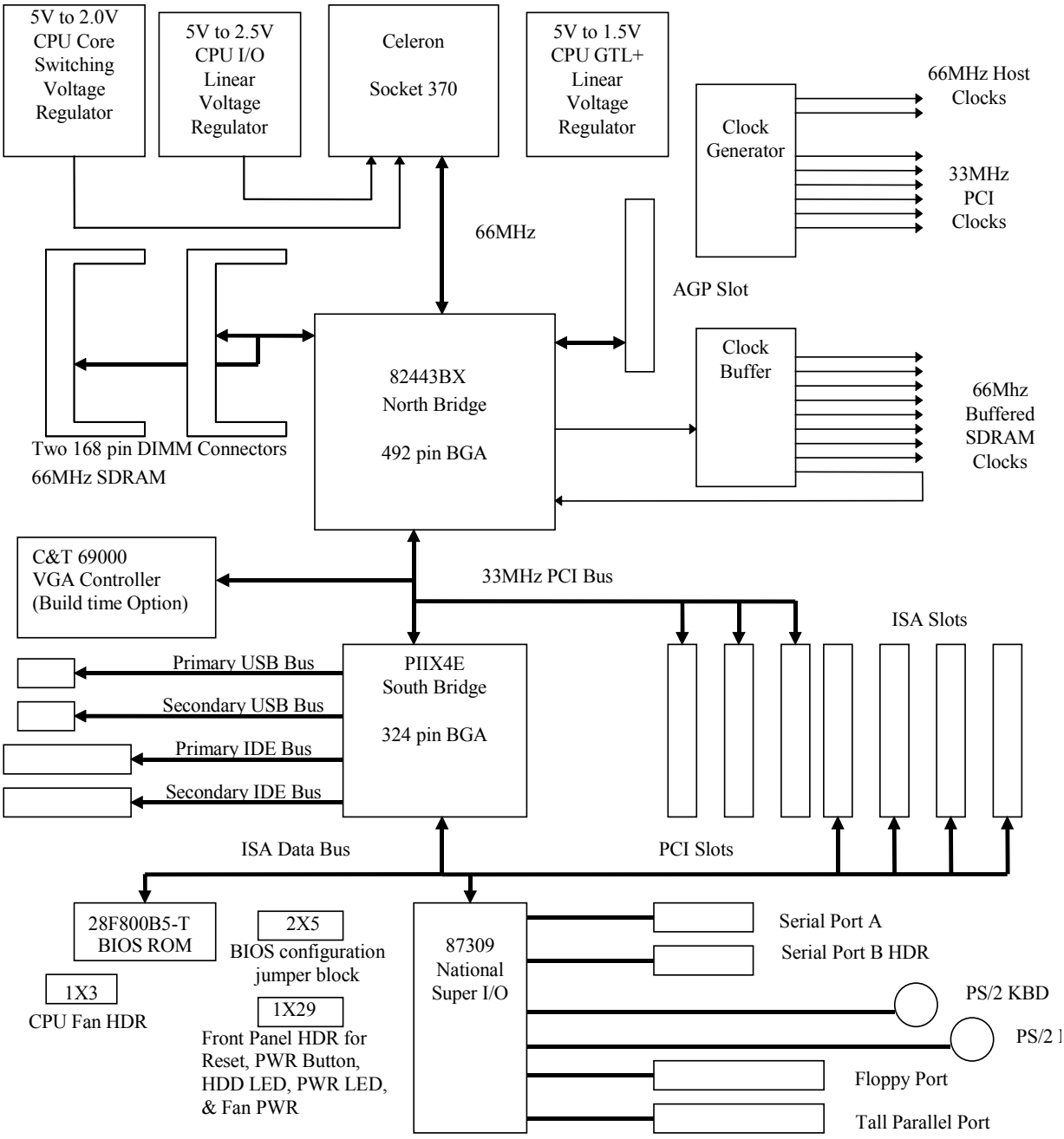



**Figure 4-1. EMB-1 block diagram**

# Features

## Processor

The EMB-1 supports the 366 and 433MHz versions of the Intel Celeron processor. Both versions contain 128KB of L2 cache. The processor connects to the EMB-1 through a Plastic Pin Grid Array (PPGA) 370-pin socket.

## Memory

The EMB-1 has two DIMM sockets. Minimum memory size is 16 MB; maximum memory size is 512 MB.

The EMB-1 supports the following memory features:

- 168-pin DIMMs
- 66 and 100 MHz (matching host bus speed) unbuffered SDRAM only
- Non-ECC (64-bit) and ECC (72-bit) memory
- 100 MHz memory shall be Serial Presence Detect (SPD) memory; 66 MHz may be either SPD or non-SPD
- 3.3 V memory only

Single- or double-sided DIMMs in the following sizes:

| DIMM Size | Non-ECC Configuration | ECC Configuration |
|---|---|---|
| 16 MB | 2 Mbit x 64 | 2 Mbit x 72 |
| 32 MB | 4 Mbit x 64 | 4 Mbit x 72 |
| 64 MB | 8 Mbit x 64 | 8 Mbit x 72 |
| 128 MB | 16 Mbit x 64 | 16 Mbit x 72 |
| 256 MB | 32 Mbit x 64 | 32 Mbit x 72 |

- You can install memory in one or both sockets.
- You can vary memory size between sockets.
- The BIOS automatically detects memory type, size, and speed.

SDRAM improves memory performance through memory access that is synchronous with the memory clock. This simplifies the timing design and increases memory speed because all timing is dependent on the number of memory clock cycles.

To install or remove memory, see Chapter 2, Installation.

### ECC memory

ECC memory detects multiple-bit errors and corrects single-bit errors. When you install ECC memory, the BIOS supports both ECC and non-ECC mode. The BIOS automatically detects if ECC memory is installed and provides the Setup option for selecting ECC mode. If non-ECC memory is installed, the Setup option for ECC mode does not appear. To enable ECC mode, see Chapter 3, BIOS configuration.

The following table describes the effect of using Setup to put each memory type in each supported mode. Whenever you select ECC mode in Setup, some performance loss occurs.

**Table 4-1. Memory error detection mode established in setup program**

| | ECC Disabled | ECC Enabled |
|---|---|---|
| Non-ECC DIMM | No error detection | N/A |
| ECC DIMM | No error detection | Single-bit error correction, multiple-bit error detection |

### Second-level cache

The EMB-1 includes 128KB of L2 write-back cache.

## Memory map

After BIOS POST, the physical addresses from the CPU are mapped into memory according to the following table. All shadowed BIOS addresses are write protected by the BIOS.

Some devices that may claim PCI Bus memory space are listed in this section. The system BIOS and/or operating system drivers dynamically allocate these devices.

| Range | Content | Cacheable |
|---|---|---|
| 00000000–0009FFFF | First 640 KB of DRAM (DOS memory) | Yes |
| 000A0000–000BFFFF | VGA video DRAM, mapped to the Video Module | No |
| 000C0000–000CBFFF | Shadowed VGA BIOS | Yes |
| 000CC000–000CFFFF | USB Buffer Area | Yes |
| 000D0000–000DFFFF | ISA Bus or UBE | Yes |
| 000E0000–000E3000 | SM BIOS Data Area | Yes |
| 000E4000–000FFFFF | System BIOS Shadow | Yes |
| 00100000-00FFFFFF | DRAM or<br>PCI or ISA | Yes<br>No |
| 01000000–03FFFFFF | DRAM or<br>PCI | Yes<br>No |
| 04000000–07FFFFFF | DRAM or<br>PCI | No<br>No |
| FFF00000–FFFFFFFF | System ROM BIOS | No |

## Interrupt usage

For details about EMB-1 PC-compatible interrupt usage, see Appendix B, Interrupts.

## Flash boot device

The EMB-1 uses the Intel E28F800B5-T as a flash boot device (FBD). The FBD contains the boot, main, and parameter blocks shown in Figure 4-2 and shadowed at the top of 32-bit address space. Using the FBD allows reprogramming of the main and parameter blocks of the BIOS.

The Plug and Play ESCD is also stored in the FBD in the block addressed from FFFFA000h–FFFFBFFFh. This block is always accessible for re-programming.

The Flash BIOS device is memory addressed and resides in the last 1MB of system memory at address FFF00000h–FFFFFFFFh.

### FBD and system BIOS update

You can update the FBD or just the system BIOS by either booting to MS-DOS or installing the force recovery jumper. To update the FBD, you must also install the boot block write enable jumper. For additional information, see *Appendix E, BIOS update and recovery*.

Use extreme caution when updating the boot block. A BIOS boot block rarely changes and should not require updating.

### FBD and system BIOS recovery

Some types of failure can corrupt the FBD and the system BIOS. To recover the system BIOS, you must install the force recovery jumper. To recover the FBD (which also recovers the system BIOS), you must install the boot block write enable jumper as well as the force recovery jumper. For additional information, see *Appendix E, BIOS update and recovery*.

If the boot block is corrupt and not executable (for example, force recovery does not work), return the EMB-1 to the factory for repair. For information about returning items to RadiSys, see the RadiSys web site.

### BIOS ROM and ROM shadowing

The EMB-1 utilizes a FBD as its BIOS ROM. The BIOS ROM is mapped into the top of the processor's 32-bit address space. The BIOS consists of the 16 KByte boot block and the system BIOS in the main blocks 5 - 8 and both 8KB parameter blocks. The layout is described in the next figure.

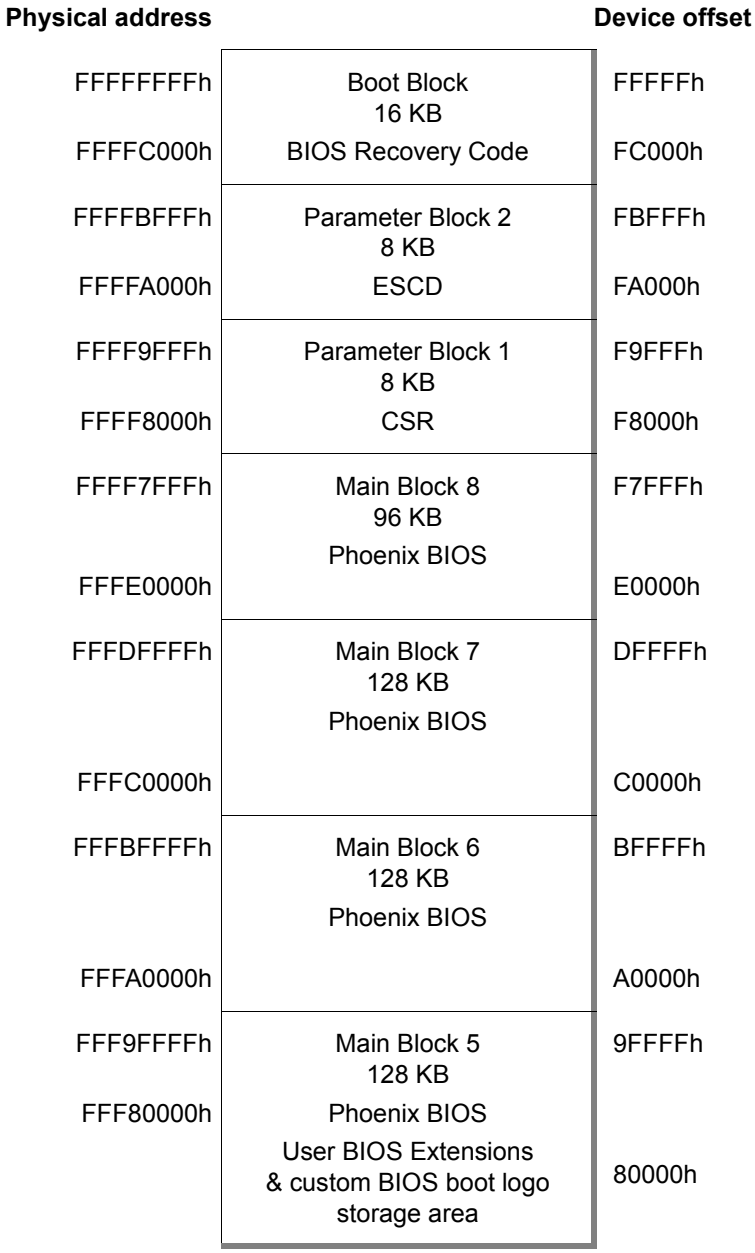



**Figure 4-2. Flash boot device memory: upper 512 KB**

The BIOS initialization software copies the ROM contents into DRAM (a process called *shadowing*) at addresses 0E0000h–0FFFFFh. The VGA BIOS is copied into 0C0000h–0C7FFFh of DRAM. After copying into these areas, the BIOS write-protects them. Subsequent writes to these areas complete successfully but do not alter the data in DRAM.

There are two parameter blocks, each 8 KB in size, used for BIOS code.

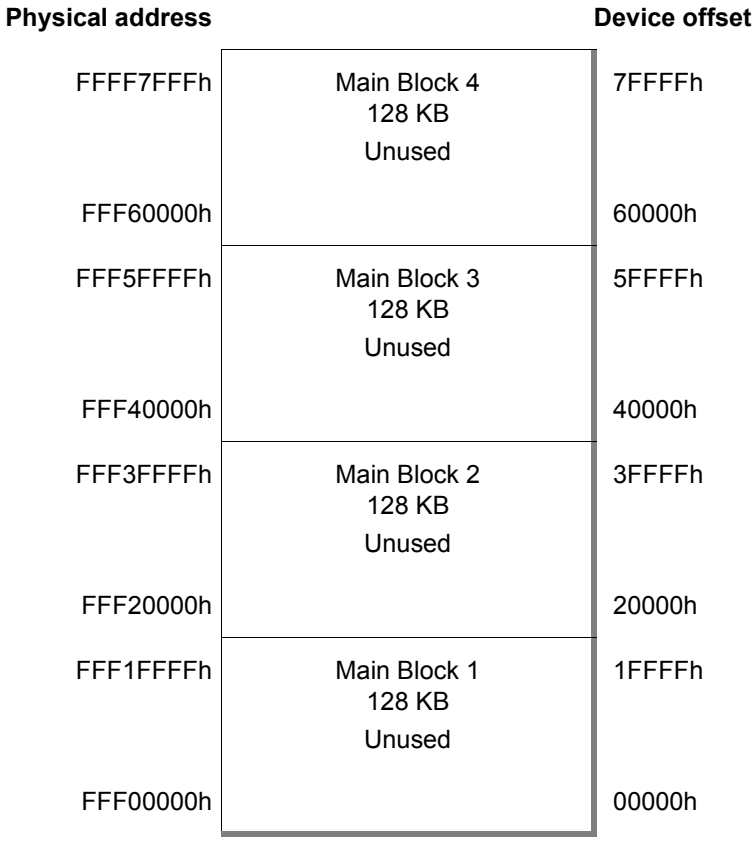



**Figure 4-3. Flash boot device memory: lower 512 KB**

## Custom boot logo

You can create a custom boot logo which displays throughout POST. The EMB-1's BIOS uses a standard OS/2 or Microsoft† Windows† bitmap in RLE format. For additional information about the custom boot logo, see Chapter 2, Installation.

## 82443BX host bridge

The Intel 82443BX is a 492 pin BGA running on 3.3V with mixed +5V, 3.3V, and GTL+ termination voltages. The 82443BX provides bus-control signals, address paths, and data paths for transfers between the processor's host bus, PCI bus, the AGP, and main memory. As implemented on the EMB-1, the 82443BX features:

- Processor interface control
  - Support for processor host bus frequencies of 66 MHz
  - 32-bit addressing

- Integrated DRAM controller, with support for
  - +3.3 V only SDRAM configurations
  - Up to two double-sided DIMMs
  - 100-MHz or 66-MHz SDRAM
  - DIMM serial presence detect via SMBus interface
  - SDRAM 64-bit data interface with ECC support
  - Symmetrical and asymmetrical DRAM addressing
- AGP interface
- PCI bus interface

### AGP

The integrated AGP is a high-performance bus for graphics-intensive applications, such as 3D applications. AGP, while based on the *PCI Local Bus Specificatio*n, Rev. 2.1, is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amount of graphics data with the following features

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent bus efficiency

### 82443BX PCI bus

The Intel 82443BX supports processor-to-PCI cycles. The 82443BX PCI CLK runs at 33 MHz. PCI Bus features include:

- Fully synchronous, minimum latency 33 MHz PCI bus interface
- Zero wait state CPU-to-PCI write timings (no IRDY stall) for superior graphics performance
- PCI 2.1 compliant
- Data streaming support from PCI to DRAM (approximately 120MB/s for writes, approximately 100MB/s for reads)
- Supports five PCI bus masters in addition to the Host and PCI to ISA bridge

## PIIX4E PCI-ISA bridge

The Intel PIIX4E is a 324 pin BGA that runs on 3.3V with a reference voltage tied to +5V for +5V signal compatibility. The PIIX4E supports a PCI-to-ISA bridge, an IDE controller, compatibility devices, a dual USB controller, and a real time clock (RTC). A detailed description of each of these follows.

### PCI-ISA bridge

The PIIX4E is PCI 2.1 and IEEE996 compatible (ISA, AT bus). On PCI, the PIIX4E operates as a bus master for various internal modules, such as the USB controller, DMA controller, IDE bus master controller, distributed DMA masters, and on behalf of ISA

masters. Internal registers or cycles passed to the ISA or EIO buses make the PIIX4E operate as a target. All internal registers are positively decoded.

The PIIX4E chip drives most of the ISA bus directly. The PIIX4E incorporates an ISA bus compatible master and slave interface, and directly drives five ISA slots without external data buffers. The ISA interface also provides byte swap logic, I/O recovery support, wait state generation, and SYSCLK generation. There are four devices on the EMB-1 connected to the ISA bus, the SuperI/O, and the Flash ROM BIOS.

### IDE controller

The PIIX4E fast IDE interface supports up to four IDE devices through two independent IDE signal channels. The IDE interface supports PIO IDE transfers up to 14 MB/s and Bus Master IDE transfers up to 33 MB/s. It does not consume any ISA DMA resources and integrates eight 32-bit buffers for optimal transfers.

The PIIX4E chip supports Modes 1, 2, 3, and 4 as well as Bus Master (DMA) Modes 0, 1, and 2. There is no support for the obsolete IDE register at I/O address 0x3F7. The PIIX4E supports “Ultra DMA/33” Synchronous DMA Mode Transfers.

Only PCI Masters have access to the IDE port. ISA Bus masters cannot access the IDE I/O port addresses. The IDE data transfer command strobes, DMA request and grant signals, and IORDY signals interface directly to the chipset.

### Compatibility devices

The PIIX4E contains three compatibility devices, a DMA controller, a timer/counters, and an interrupt controller. The DMA controller incorporates the logic of two 82C37 DMA controllers. The timer/counter block contains three counters that are equivalent in function to those found in one 82C54 programmable interval timer. The ISA compatible interrupt controller incorporates the functionality of two 82C59 interrupt controllers.

The DMA controller has seven independently programmable channels. Channels [3:0] are hardwired to 8 bit, count-by-byte transfers. Channels [7:5] are hardwired to 16-bit, count by word transfers. Any two of the seven DMA channels can provide support for fast Type-F transfers. The DMA controller also generates the ISA refresh cycles.

The timer/counter block provides the system timer function, refresh request, and speaker tone. The 14.31818 MHz oscillator input provides the clock source for these three counters.

Cascading of the interrupt controllers provides 14 external and two internal interrupts. Additionally, PIIX4E supports a serial interrupt scheme.

All of the registers in these modules can be read and restored. This allows saving and restoring the system state after removing power and restoring it to the circuit.

### Enhanced USB controller

The PIIX4E USB controller provides enhanced support for the Universal Host Controller Interface. This includes support allowing legacy software to use a USB based keyboard and mouse.

### RTC

The PIIX4E RTC is Motorola MC146818A compatible with 256 bytes battery backed RAM. The RTC performs two key functions:

- Monitoring time of day
- Storing system data including during a system power-down.

The RTC operates on a 32.768 kHz crystal and a separate battery. The RTC also supports two lockable memory ranges. Configuration space allows locking two 8 byte ranges to read and write accesses by setting specific bits. This prevents unauthorized reading of passwords or other system security information.

In addition, the RTC supports a date alarm, that allows for scheduling a wake-up event up to 30 days rather than just 24 hours, in advance.

The RTC (as supported by the BIOS) is Y2K ready.

## Battery

The 3.0V lithium battery mounted on the EMB-1 is a Renata CR2032 "coin cell" or equivalent. Should the battery fail, you may obtain and install a replacement. For information about replacing the battery, see *Replacing the battery on page 14*.

Write down all CMOS setup parameters while the battery is still good, or save them using the options available on the BIOS configuration'sCMOS Save and Restore sub-menu on page 45.

The battery powers the CMOS RAM and TOD clock when system power is not present. If system power is present, the +5V voltage also powers the CMOS RAM and TOD clock. This is done with the +3.3V isolation diodes, so that either the onboard battery or the +3.3V power supply voltage can supply power and neither power source affects the other.

The battery has an expected battery life of 2 years on continuous battery power. In a system that is powered on much of the time and where the ambient power-off temperature is less than 60°C, the battery is estimated to have a life of 10 years.

## National PC87309VLJ Super I/O controller

The National PC87309VLJ Super I/O controller provides floppy controller, parallel port, serial ports, and PS/2 keyboard/mouse interface.

### Floppy disk

The floppy signals connect to a header on the EMB-1 allowing ribbon cable connection of a floppy disk drive. The device is accessed at the standard PC I/O addresses of 3F0h–3F7h and interrupts are signaled on IRQ6.

### Parallel port

One IEEE1284 parallel port is provided. The port can be configured to run in standard, enhanced (EPP), or Microsoft high speed mode (ECP) modes. MS-DOS and Windows recognize this port as LPT1. LPT1 is compliant with the IEC1000-4-2 specification.

### Serial ports

Two serial ports that are RS-232 compatible are provided. The Super I/O chip includes 16C550 compatible UARTs with separate send and receive 16-byte FIFOs. The COM1 port is configured at I/O addresses 3F8–3FFh and uses IRQ4. The COM2 port is configured at I/O addresses 2F8–2FFh and uses IRQ3. The Super I/O chip allows relocation of these ports to the COM3 and/or COM4 standard I/O addresses, respectively. If so configured, COM3 and COM4 use I/O addresses 3E8–3EFh and 2E8–2Efh respectively. If not needed, these serial ports can be disabled in the BIOS setup screen to free the I/O address and interrupt for usage by other expansion products. COM1 connects to a 9-pin D-Sub serial port connector located in the I/O shield. COM2 is connected to a 2X5 pin header on the EMB-1. External access to COM2 can be achieved through a cable connected to the 2X5 pin header and a serial connector mounted in one of the EMB-1's expansion slot openings. For additional information about COM2, see Installing the COM2 cable on page 12

### Keyboard and mouse controller

A keyboard port and mouse port are provided. The Super I/O keyboard controller is functionally equivalent to the industry standard 8042A controller. It is located at I/O locations 60–64h. The keyboard interrupt connects to IRQ1. If enabled, the mouse interrupt uses IRQ12.

## Video graphics (optional)

A Chips and Technology 69000 64-bit GUI and video-accelerated controller is used to implement a high performance CRT video interface via the P2 connector.

The controller supports the following non-interlaced video resolutions on the CRT.

| Screen format (pixels) | No. of colors | Refresh rates (Hz) | Memory required |
|---|---|---|---|
| 640x480 | 256 | 60, 75, 85 | 300KB |
| 640x480 | 65,535 | 60, 75, 85 | 600KB |
| 640x480 | 16.8 Million | 60, 75, 85 | 900KB |
| 800x600 | 65,535 | 60, 75, 85 | 960KB |
| 800x600 | 16.8 Million | 60, 75, 85 | 1.44MB |
| 1024x768 | 256 | 60, 75, 85 | 786KB |
| 1024x768 | 65,535 | 60, 75, 85 | 1.57MB |
| 1280x1024 | 256 | 60, 75 | 1.31MB |
| 1600x1200 | 256 | 60 | 1.92MB |

### Video DRAM

The EMB-1 hardware includes a VGA graphics controller implemented using the Chips and Technologies CT69000 GUI-Accelerated SVGA/XGA. This is connected to the local PCI bus to give the best possible graphics performance and controls an SVGA/XGA monitor connected to the VGA front panel connector. The CT69000 is located as device 8 (IDSEL = AD19) for host PCI bus configuration space accesses. The CT69000 has on-chip frame buffer memory, providing 2MBytes of video memory which results in these resolutions:

| Dimensions | Resolution | Refresh rates (Hz) |
|---|---|---|
| 640 x 480 | 8-, 16-, or 24-bit colors | 60, 75, 85 |
| 800 x 600 | 8-, 16-, or 24-bit colors | 60, 75, 85 |
| 1024 x 768 | 8- or 16-bit colors | 60, 75, 85 |
| 1280 x 1024 | 8-bit colors | 60 |

# A Chipset and I/O map

This appendix contains the I/O port addresses for the address-mapped devices in the EMB-1. As is standard for the ISA bus, the A[15:0] bits are decoded for the 0200h–03FFh range and A[15] and A[9:0] are decoded for addresses above 8000h.

This appendix also contains the PCI device assignments.

**Table A-1. First (8-bit) DMA controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 0000 | DMA Controller 1 | R/W | DMA 1 Channel 0 address |
| 0001 | | R/W | DMA 1 Channel 0 count |
| 0002 | | R/W | DMA 1 Channel 1 address |
| 0003 | | R/W | DMA 1 Channel 1 count |
| 0004 | | R/W | DMA 1 Channel 2 address |
| 0005 | | R/W | DMA 1 Channel 2 count |
| 0006 | | R/W | DMA 1 Channel 3 address |
| 0007 | | R/W | DMA 1 Channel 3 count |
| 0008 | | R<br>W | DMA 1 Command<br>DMA 1 Status |
| 0009 | | W | DMA 1 Write request |
| 000A | | W | DMA 1 Single Mask Bit |
| 000B | | W | DMA 1 Write Mode |
| 000C | | W | DMA 1 Clear byte pointer |
| 000D | | W | DMA 1 Master clear |
| 000E | | W | DMA 1 Clear mask |
| 000F | | R/W | DMA 1 Read/write all mask register bits |

**Table A-2. First interrupt controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 0020 | Interrupt Controller 1 | R/W | INT 1 Control |
| 0021 | | R/W | INT 1 Mask |

**Table A-3. Time/counter functions**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 0040 | Timer/counter | R/W | Counter 0 Count |
| 0041 | | R/W | Counter 1 Count |
| 0042 | | R/W | Counter 2 Count |

**Table A-3. Time/counter functions**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 0043 | | W | Command mode |

**Table A-4. Keyboard controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 0060 | Keyboard Controller | R/W<br>R | Data I/O register<br>Reset Xbus IRQ12/M and IRQ1 |
| 0061 | NMI status and control | R<br>W | NMI status<br>NMI control |
| 0064 | Keyboard controller | R<br>W | Status register<br>Command register |

**Table A-5. Real-time clock**

| I/O Addr | Functional group | R/W | Usage | |
|---|---|---|---|---|
| 0070 | Real-time clock, NMI | W | RTC index register = bits 6–0<br>NMI enable = bit 7 | |
| 0071 | | R/W | RTC data register | |
| | | | 0 | seconds |
| | | | 1 | seconds alarm |
| | | | 2 | minutes |
| | | | 3 | minutes alarm |
| | | | 4 | hours |
| | | | 5 | hours alarm |
| | | | 6 | day of week |
| | | | 7 | date of month |
| | | | 8 | month |
| | | | 9 | year |
| | | | A | status A |
| | | | B | status B |
| | | | C | status C |
| | | | D | status D |
| | | | E...3F | NVRAM |

**Table A-6. DMA page registers: Intel EX 82371EB of PC/AT**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 0080 | DMA controller 1 | R/W | DMA page (reserved) |
| 0081 | | R/W | DMA Channel 2 page register |
| 0082 | | R/W | DMA Channel 3 page register |
| 0083 | | R/W | DMA Channel 1 page register |
| 0084 | | R/W | DMA page (reserved) |
| 0085 | | R/W | DMA page (reserved) |

**Table A-6. DMA page registers: Intel EX 82371EB of PC/AT**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 0086 | | R/W | DMA page (reserved) |
| 0087 | | R/W | DMA Channel 0 page register |
| 0088 | DMA controller 2 | R/W | DMA page (reserved) |
| 0089 | | R/W | DMA Channel 6 page register |
| 008A | | R/W | DMA Channel 7 page register |
| 008B | | R/W | DMA Channel 5 page register |
| 008C | | R/W | DMA page (reserved) |
| 008D | | R/W | DMA page (reserved) |
| 008E | | R/W | DMA page (reserved) |
| 008F | | R/W | DMA low page register refresh |

**Table A-7. Port 92**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 0092 | Port 92 | R/W | Port 92 |

**Table A-8. VGA controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| x094 | VGA controller | R/W | POS102 access control |

**Table A-9. Second interrupt controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 00A0 | Interrupt controller 2 | R/W | INT 2 control |
| 00A1 | | R/W | INT 2 mask |

**Table A-10. Advanced Power management controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 00B2 | Advanced power management | R/W | Control |
| 00B3 | | R/W | Status |

**Table A-11. Second (16-bit) DMA controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 00C0 | DMA controller 2 | R/W | DMA 2 Channel 4 address |
| 00C2 | | R/W | DMA 2 Channel 4 count |
| 00C4 | | R/W | DMA 2 Channel 5 address |
| 00C6 | | R/W | DMA 2 Channel 5 count |
| 00C8 | | R/W | DMA 2 Channel 6 address |

**Table A-11. Second (16-bit) DMA controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 00CA | | R/W | DMA 2 Channel 6 count |
| 00CC | | R/W | DMA 2 Channel 7 address |
| 00CE | | R/W | DMA 2 Channel 7 count |
| 00D0 | | R<br>W | DMA 2 Status<br>DMA 2 Command |
| 00D2 | | W | DMA 2 Write request |
| 00D4 | | W | DMA 2 Write single mask bit |
| 00D6 | | W | DMA 2 Write mode |
| 00D8 | | W | DMA 2 Clear byte pointer |
| 00DA | | W | DMA 2 Master clear |
| 00DC | | W | DMA 2 Clear mask |
| 00DE | | R/W | DMA 2 Read/write all register mask bits |

**Table A-12. Coprocessor interface**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 00F0 | Coprocessor | W | Coprocessor error |

**Table A-13. VGA controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| x102 | VGA controller | R/W | POS102 register |

**Table A-14. Super I/O controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| x15C | Super I/O controller | R/W | Index register |
| x15D | | R/W | Data register |

**Table A-15. Secondary IDE**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 0170 | Secondary IDE | R/W | Data |
| 0171 | | R/W | Error/features |
| 0172 | | R/W | Sector count |
| 0173 | | R/W | Sector number |
| 0174 | | R/W | Cylinder low |
| 0175 | | R/W | Cylinder high |
| 0176 | | R/W | Drive/head |
| 0177 | | R/W | Status/command |

**Table A-16. Primary IDE**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 01F0 | Primary IDE | R/W | Data |
| 01F1 | | R/W | Error/features |
| 01F2 | | R/W | Sector count |
| 01F3 | | R/W | Sector number |
| 01F4 | | R/W | Cylinder Low |
| 01F5 | | R/W | Cylinder high |
| 01F6 | | R/W | Drive/head |
| 01F7 | | R/W | Status/command |

**Table A-17. Serial I/O (COM 2) port**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| x2F8 | COM 2 serial port | R | Receiver buffer |
| | | W | Transmitter buffer |
| | | R/W | Baud rate divisor latch (LSB) |
| x2F9 | | R/W | Interrupt enable register |
| | | R/W | Baud rate divisor latch (MSB) |
| x2FA | | R | Interrupt ID register |
| | | W | FIFO control register |
| x2FB | | R/W | Line control register |
| x2FC | | R/W | Modem control register |
| x2FD | | R | Line status register |
| x2FE | | R/W | Modem status register |
| x2FE | | R/W | Scratch pad |

**Table A-18. Secondary IDE**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 0374 | Secondary IDE | | Reserved |
| 0375 | | | Reserved |
| 0376 | | R/W | Alt status/device control |

**Table A-19. Parallel I/O (LPT1) port**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| x378 | LPT1 parallel port | R/W | Printer data register |
| x379 | | R | Printer status register |
| | | W | Printer status register (EPP only) |
| x37A | | R/W | Printer control register |
| x37B | | R/W | EPP Address Port |
| x37C | | R/W | EPP Data port 0 |
| x37D | | R/W | EPP Data port 1 |
| x37E | | R/W | EPP Data port 2 |

**Table A-19. Parallel I/O (LPT1) port**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| x37F | | R/W | EPP Data port 3 |

**Table A-20. VGA controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| x3B4 | VGA controller | R/W | CRT Controller index (mono) |
| x3B5 | | R/W | CRT Controller data (mono) |
| x3BA | | R<br>W | Input status (mono)<br>Feature control output (mono) |

**Table A-21. EGA controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| x3C0 | EGA controller | W | Attribute controller index/data |
| x3C1 | | R | Attribute controller index/data |
| x3C2 | | R<br>W | Input status register 0 Miscellaneous output |
| x3C3 | | R/W | Motherboard sleep |
| x3C4 | | R/W | Sequencer index |
| x3C5 | | R/W | Sequencer data |
| x3C6 | | R/W<br>R/W | Video DAC pixel mask<br>Hidden DAC register |
| x3C7 | | R<br>W | DAC state<br>Pixel address read mode |
| x3C8 | | R/W | Pixel mask write mode |
| x3C9 | | R/W | Pixel data |
| x3CA | | R | Feature control readback |
| x3CC | | R | Miscellaneous output readback |
| x3CE | | R/W | Graphics controller index |
| x3CF | | R/W | Graphics controller data |

**Table A-22. CGA controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| x3D4 | CGA controller | R/W | CRT controller index (color) |
| x3D5 | | R/W | CRT controller data (color) |
| x3DA | | R/W | Feature control, input status |

**Table A-23. Floppy disk controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| x3F0 | Floppy disk controller | R | Status register A |
| x3F1 | | R | Status register B |
| x3F2 | | R/W | Digital output register |
| x3F3 | | R/W | Tape driver register |
| x3F4 | | R<br>W | Main status register<br>data rate select register |

**Table A-23. Floppy disk controller**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| x3F5 | | R/W | Data register |

**Table A-24. Primary IDE**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| x3F6 | Primary IDE | R/W | Alternate status/device control |
| x3F7 | | R<br>W | Digital input register<br>configuration control register |

**Table A-25. Serial I/O (COM 1) port**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 3F8 | COM 1 serial port | R<br>W | Receiver buffer<br>Transmitter buffer |
| | | R/W | Baud rate divisor latch (LSB) |
| 3F9 | | R/W | Interrupt enable register |
| | | R/W | Baud rate divisor latch (MSB) |
| 3FA | | R<br>W | Interrupt ID register<br>FIFO control register |
| 3FB | | R/W | Line control register |
| 3FC | | R/W | Modem control register |
| 3FD | | R | Line status register |
| 3FE | | R/W | Modem status register |
| x3FF | | R/W | Scratch pad |

**Table A-26. Interrupts**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 04D0 | Interrupt controller 1 | R/W | INTC-1 Edge/level control |
| 04D1 | Interrupt controller 2 | R/W | INTC-2 Edge/level control |

**Table A-27. ECP registers**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| x778 | ECP | R/W | FIFO |
| x779 | | R/W | Configuration Register B |
| x77A | | R/W | Extended Control Register |

**Table A-28. PCI configuration**

| I/O Addr | Functional group | R/W | Usage |
|---|---|---|---|
| 0CF8–0CFB (Dword only) | PCI configuration | R/W | Configuration address register |
| 0CFC–0CFF | | R/W | Configuration data register |

**Table A-29. PCI device assignments**

| Peripheral | IDSEL number | Device number | Function number | INTx number | Arbitration Signals REQ number/ GNT number |
|---|---|---|---|---|---|
| Intel 82BX443 North Bridge PCI | AD11 | 0 | 0 | - | - |
| Intel 82BX443 North Bridge AGP | AD12 | 1 | 0 | - | - |
| PCI/ISA Bus bridge (PIIX4E)<br>PCI/ISA bridge<br>IDE interface<br>USB<br>PM | AD18 | 7 | <br>0<br>1<br>2<br>3 | D | PHLD# / PHLDA# directly from the 82BX443 |
| Chips and Technology 69000 | AD19 | 8 | 0 | B | - |
| PCI Expansion Slot #1 | AD20 | 9 | 0 | B,C,D,A | 0 |
| PCI Expansion Slot #2 | AD21 | 10 | 0 | C,D,A,B | 1 |
| PCI Expansion Slot #3 | AD22 | 11 | 0 | D,A,B,C | 2 |

# B Interrupts

The following table shows interrupt assignments for the EMB-1.

**Table B-1. Interrupts**

| Interrupt | Description |
|---|---|
| IRQ0 | System timer |
| IRQ1 | Keyboard controller |
| IRQ2 | Cascade interrupt input |
| IRQ3 | COM2, COM1, or unassigned |
| IRQ4 | COM1, COM2, or unassigned |
| IRQ5 | Unassigned |
| IRQ6 | Floppy or unassigned |
| IRQ7 | LPT1 or unassigned |
| IRQ8 | Real time clock |
| IRQ9 | Unassigned |
| IRQ10 | Unassigned |
| IRQ11 | Unassigned |
| IRQ12 | Mouse |
| IRQ13 | Numeric coprocessor |
| IRQ14 | Primary IDE |
| IRQ15 | Secondary IDE or unassigned |
| NMI | Memory Parity (disabled) |

# C Connectors

This appendix details the connectors on the EMB-1 and gives the signal pinout of each conncector. Pins are labeled from the point of view of looking into the front of the connector on the EMB-1.

When reading this file online, you can immediately view information about any connector by placing the mouse cursor over a connector name and clicking.

# Connector Locations

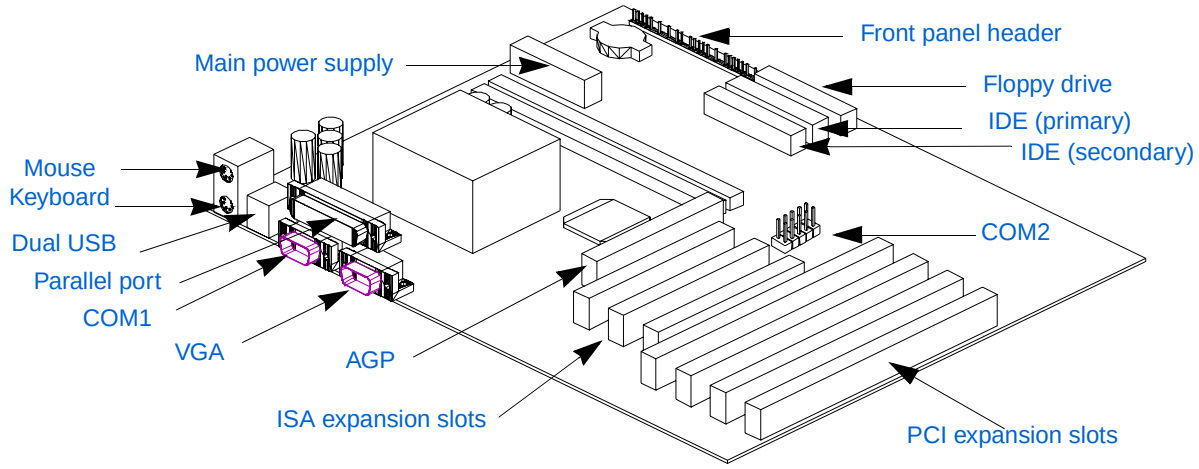



**Figure C-1. EMB-1 connectors**

- For information about jumper settings, see Setting jumpers and headers on page 6.
- For additional information about COM2, see Installing the COM2 cable on page 12.

# Connector Descriptions

## AGP

**Table C-1. AGP connector**

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| A1 | 12V | B1 | ~OVERCNT | A34 | VDDQ3.3 | B34 | VDDQ3.3 |
| A2 | ~TYPEDET | B2 | 5V | A35 | AD22 | B35 | AD21 |
| A3 | RESERVED | B3 | 5V | A36 | AD20 | B36 | AD19 |
| A4 | USB- | B4 | USB+ | A37 | GND | B37 | GND |
| A5 | GND | B5 | GND | A38 | AD18 | B38 | AD17 |
| A6 | ~INTA | B6 | INTB~ | A39 | AD16 | B39 | ~C/BE2 |
| A7 | ~RST | B7 | CLK | A40 | VDDQ3.3 | B40 | VDDQ3.3 |
| A8 | ~GNT | B8 | ~REQ | A41 | ~FRAME | B41 | ~IRDY |
| A9 | 3.3V | B9 | 3.3V | A42 | RESERVED | B42 | 3.3Vaux |
| A10 | ST1 | B10 | ST0 | A43 | GND | B43 | GND |
| A11 | RESERVED | B11 | ST2 | A44 | RESERVED | B44 | RESERVED |
| A12 | ~PIPE | B12 | ~RBF | A45 | 3.3V | B45 | 3.3V |
| A13 | GND | B13 | GND | A46 | ~TRDY | B46 | ~DEVSEL |
| A14 | RESERVED | B14 | RESERVED | A47 | ~STOP | B47 | VDDQ3.3 |
| A15 | SBA1 | B15 | SBA0 | A48 | ~PME | B48 | ~PERR |
| A16 | 3.3V | B16 | 3.3V | A49 | GND | B49 | GND |
| A17 | SBA3 | B17 | SBA2 | A50 | PAR | B50 | ~SERR |
| A18 | RESERVED | B18 | SB_STB | A51 | AD15 | B51 | ~C/BE1 |
| A19 | GND | B19 | GND | A52 | VDDQ3.3 | B52 | VDDQ3.3 |
| A20 | SBA5 | B20 | SBA4 | A53 | AD13 | B53 | AD14 |
| A21 | SBA7 | B21 | SBA6 | A54 | AD11 | B54 | AD12 |
| A22 | KEY | B22 | KEY | A55 | GND | B55 | GND |
| A23 | KEY | B23 | KEY | A56 | AD9 | B56 | AD10 |
| A24 | KEY | B24 | KEY | A57 | ~C/BE0 | B57 | AD8 |
| A25 | KEY | B25 | KEY | A58 | VDDQ3.3 | B58 | VDDQ3.3 |
| A26 | AD30 | B26 | AD31 | A59 | RESERVED | B59 | AD_STB0 |
| A27 | AD28 | B27 | AD29 | A60 | AD6 | B60 | AD7 |
| A28 | 3.3V | B28 | 3.3V | A61 | GND | B61 | GND |
| A29 | AD26 | B29 | AD27 | A62 | AD4 | B62 | AD5 |
| A30 | AD24 | B30 | AD25 | A63 | AD2 | B63 | AD3 |
| A31 | GND | B31 | GND | A64 | VDDQ3.3 | B64 | VDDQ3.3 |
| A32 | RESERVED | B32 | AD_STB1 | A65 | AD0 | B65 | AD1 |
| A33 | C/BE3~ | B33 | AD23 | A66 | RESERVED | B66 | RESERVED |

## COM1

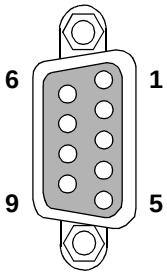



**Table C-2. COM1 connector**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Carrier detect | 6 | Data set ready |
| 2 | Receive data | 7 | Request to send |
| 3 | Transmit data | 8 | Clear to send |
| 4 | Data terminal ready | 9 | Ring indicator |
| 5 | Signal ground | | |

## COM2

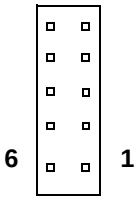



**Table C-3. COM2 connector**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Carrier detect | 6 | Data set ready |
| 2 | Receive data | 7 | Request to send |
| 3 | Transmit data | 8 | Clear to send |
| 4 | Data terminal ready | 9 | Ring indicator |
| 5 | Signal ground | | |

## Dual USB

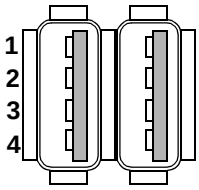



**Table C-4. Dual USB connector**

| Pin | Signal |
|---|---|
| Mechanical Solder Lug | Shield Ground |
| 1 | VCC (1Amp Fused) |
| 2 | DATA– |
| 3 | DATA+ |
| 4 | Signal Ground |
| Mechanical Solder Lug | Shield Ground |

## Floppy drive

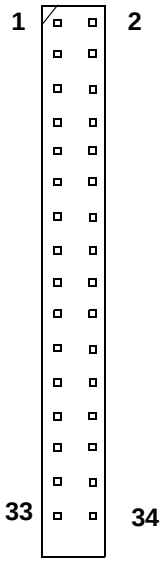



**Table C-5. Floppy Drive Connector**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | GND | 2 | FD:DENSEL |
| 3 | GND | 4 | NC |
| 5 | NC | 6 | FD:DRATE0 |
| 7 | GND | 8 | FD:~INDEX |
| 9 | GND | 10 | FD:~MTR1 |
| 11 | GND | 12 | FD:~DS1 |
| 13 | GND | 14 | FD:~DS0 |
| 15 | GND | 16 | FD:~MTR0 |
| 17 | NC | 18 | FD:~DIR |
| 19 | GND | 20 | FD:~STEP |
| 21 | GND | 22 | FD:~WDATA |
| 23 | GND | 24 | FD:~WGATE |
| 25 | GND | 26 | FD:~TRK0 |
| 27 | NC | 28 | FD:~WP |
| 29 | GND | 30 | FD:~RDATA |
| 31 | GND | 32 | FD:~HDSEL |
| 33 | GND | 34 | FD:~DSKCHG |

# Front panel header

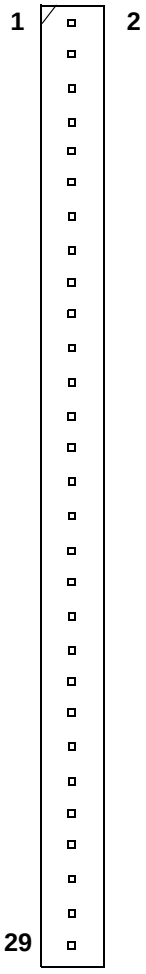



**Table C-6. Front panel header**

| Pin | Signal | Function |
|---|---|---|
| 1 | GND | |
| 2 | +12VDC | Chassis Fan |
| 3 | GND | |
| 4 | GND | System Reset |
| 5 | Reset Signal | |
| 6 | Key | |
| 7 | System On LED PWR | |
| 8 | Key | System On LED |
| 9 | GND | |
| 10 | Key | |
| 11 | HD LED PWR | |
| 12 | ~HD ACT | HD Activity LED |
| 13 | Key | |
| 14 | HD LED PWR | |
| 15 | SW_ON | System On Switch |
| 16 | GND | |
| 17 | NC | |
| 18 | NC | |
| 19 | Key | |
| 20 | NC | |
| 21 | Key | |
| 22 | NC | |
| 23 | NC | |
| 24 | NC | |
| 25 | NC | |
| 26 | SPKR_DAT | |
| 27 | SPKR_DAT | External Speaker |
| 28 | Key | |
| 29 | GND | |

# IDE (primary)

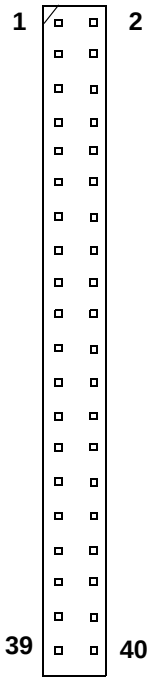



**Table C-7. IDE connector (primary)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | IDEP:RST | 2 | GND |
| 3 | PIDE:D7 | 4 | PIDE:D8 |
| 5 | PIDE:D6 | 6 | PIDE:D9 |
| 7 | PIDE:D5 | 8 | PIDE:D10 |
| 9 | PIDE:D4 | 10 | PIDE:D11 |
| 11 | PIDE:D3 | 12 | PIDE:D12 |
| 13 | PIDE:D3 | 14 | PIDE:D13 |
| 15 | PIDE:D2 | 16 | PIDE:D14 |
| 17 | PIDE:D0 | 18 | PIDE:D15 |
| 19 | GND | 20 | NC |
| 21 | PIDE:DRQ | 22 | GND |
| 23 | PIDE:IOW | 24 | GND |
| 25 | PIDE:IOR | 26 | GND |
| 27 | PIDE:IORDY | 28 | Cable Select |
| 29 | PIDE:~DAK | 30 | GND |
| 31 | AT:IRQ14 | 32 | NC |
| 33 | PIDE:A1 | 34 | NC |
| 35 | PIDE:A0 | 36 | PIDE:A2 |
| 37 | PIDE:~CS1 | 38 | PIDE:~CS3 |
| 39 | ~HDACT | 40 | GND |

## IDE (secondary)

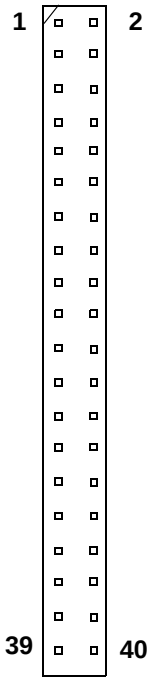



**Table C-8. IDE connector (secondary)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | IDES:RST | 2 | GND |
| 3 | SIDE:D7 | 4 | SIDE:D8 |
| 5 | SIDE:D6 | 6 | SIDE:D9 |
| 7 | SIDE:D5 | 8 | SIDE:D10 |
| 9 | SIDE:D4 | 10 | SIDE:D11 |
| 11 | SIDE:D3 | 12 | SIDE:D12 |
| 13 | SIDE:D2 | 14 | SIDE:D13 |
| 15 | SIDE:D1 | 16 | SIDE:D14 |
| 17 | SIDE:D0 | 18 | SIDE:D15 |
| 19 | GND | 20 | NC |
| 21 | SIDE:DRQ | 22 | GND |
| 23 | SIDE:~IOW | 24 | GND |
| 25 | SIDE:~IOR | 26 | GND |
| 27 | SIDE:IORDY | 28 | Cable Select |
| 29 | SIDE:~DAK | 30 | GND |
| 31 | AT:IRQ15 | 32 | NC |
| 33 | SIDE:A1 | 34 | NC |
| 35 | SIDE:A0 | 36 | SIDE:A2 |
| 37 | SIDE:~CS1 | 38 | SIDE:~CS3 |
| 39 | ~HDACT | 40 | GND |

## ISA expansion slot

**Table C-9. ISA expansion slot**

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| A1 | ~IOCHK | B1 | GND | C1 | SBHE# | D1 | ~MEMCS16 |
| A2 | SD7 | B2 | RESET | C2 | LA23 | D2 | ~IOCS16 |
| A3 | SD6 | B3 | +5V | C3 | LA22 | D3 | IRQ10 |
| A4 | SD5 | B4 | IRQ9 | C4 | LA21 | D4 | IRQ11 |
| A5 | SD4 | B5 | -5V | C5 | LA20 | D5 | IRQ12 |
| A6 | SD3 | B6 | DRQ2 | C6 | LA19 | D6 | IRQ15 |
| A7 | SD2 | B7 | -12V | C7 | LA18 | D7 | IRQ14 |
| A8 | SD1 | B8 | ~SRDY | C8 | LA17 | D8 | ~DACK0 |
| A9 | SD0 | B9 | +12V | C9 | ~MEMR | D9 | DRQ0 |
| A10 | IOCHRDY | B10 | GND | C10 | ~MEMW | D10 | ~DACK5 |
| A11 | AEN | B11 | ~SMEMW | C11 | SD8 | D11 | DRQ5 |
| A12 | SA19 | B12 | ~SMEMR | C12 | SD9 | D12 | ~DACK6 |
| A13 | SA18 | B13 | ~IOW | C13 | SD10 | D13 | DRQ6 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| A14 | SA17 | B14 | ~IOR | C14 | SD11 | D14 | ~DACK7 |
| A15 | SA16 | B15 | ~DACK3 | C15 | SD12 | D15 | DRQ7 |
| A16 | SA15 | B16 | DRQ3 | C16 | SD13 | D16 | +5V |
| A17 | SA14 | B17 | ~DACK1 | C17 | SD14 | D17 | ~MASTER |
| A18 | SA13 | B18 | DRQ1 | C18 | SD15 | D18 | GND |
| A19 | SA12 | B19 | ~REFRESH | | | | |
| A20 | SA11 | B20 | BCLK | | | | |
| A21 | SA10 | B21 | IRQ7 | | | | |
| A22 | SA9 | B22 | IRQ6 | | | | |
| A23 | SA8 | B23 | IRQ5 | | | | |
| A24 | SA7 | B24 | IRQ4 | | | | |
| A25 | SA6 | B25 | IRQ3 | | | | |
| A26 | SA5 | B26 | ~DACK2 | | | | |
| A27 | SA4 | B27 | TC | | | | |
| A28 | SA3 | B28 | BALE | | | | |
| A29 | SA2 | B29 | +5V | | | | |
| A30 | SA1 | B30 | OSC | | | | |
| A31 | SA0 | B31 | GND | | | | |
| KEY | | KEY | | | | | |

## Keyboard

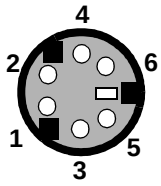



**Table C-10. Keyboard pin-out**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Data | 4 | +5V |
| 2 | Not used | 5 | Clock |
| 3 | Ground | 6 | Not used |

## Main power supply

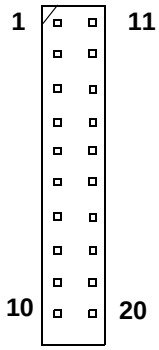



**Table C-11. Main power connector**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +3.3VDC | 11 | +3.3VDC/sense |
| 2 | +3.3VDC | 12 | -12VDC |
| 3 | GND | 13 | GND |
| 4 | +5VDC | 14 | PS_ON# |
| 5 | GND | 15 | GND |
| 6 | +5VDC | 16 | GND |
| 7 | GND | 17 | GND |
| 8 | PWR_OK | 18 | -5VDC |
| 9 | +5VSB | 19 | +5VDC |
| 10 | +12VDC | 20 | +5VDC |

## Mouse

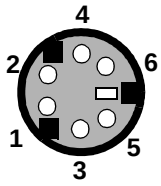



**Table C-12. Mouse pin-out**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Data | 4 | +5V |
| 2 | Not used | 5 | Clock |
| 3 | Ground | 6 | Not used |

## Parallel port

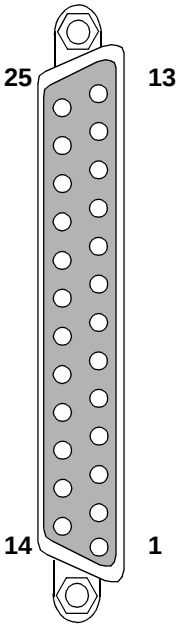



**Table C-13. Parallel Port**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Strobe | 14 | Auto line feed |
| 2 | DB0 | 15 | Error |
| 3 | DB1 | 16 | Initialize printer |
| 4 | DB2 | 17 | Select in |
| 5 | DB3 | 18 | Signal ground |
| 6 | DB4 | 19 | Signal ground |
| 7 | DB5 | 20 | Signal ground |
| 8 | DB6 | 21 | Signal ground |
| 9 | DB7 | 22 | Signal ground |
| 10 | Acknowledge | 23 | Signal ground |
| 11 | Busy | 24 | Signal ground |
| 12 | Paper end | 25 | Signal ground |
| 13 | Select | 26 | |

## PCI expansion slot

**Table C-14. PCI Expansion Slot Connectors**

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| A1 | GND | B1 | -12V | A32 | AD16 | B32 | AD17 |
| A2 | +12V | B2 | GND | A33 | +3.3V | B33 | ~C/BE2 |
| A3 | +5V | B3 | GND | A34 | ~FRAME | B34 | GND |
| A4 | +5V | B4 | NC | A35 | GND | B35 | ~IRDY |
| A5 | +5V | B5 | +5V | A36 | ~TRDY | B36 | +3.3V |
| A6 | ~INTA | B6 | +5V | A37 | GND | B37 | ~DEVSEL |
| A7 | ~INTC | B7 | ~INTB | A38 | ~STOP | B38 | GND |
| A8 | +5V | B8 | ~INTD | A39 | +3.3V | B39 | ~LOCK |
| A9 | RESERVED | B9 | NC | A40 | +5V | B40 | ~PERR |
| A10 | +5V (I/O) | B10 | RESERVED | A41 | +5V | B41 | +3.3V |
| A11 | RESERVED | B11 | NC | A42 | GND | B42 | ~SERR |
| A12 | GND | B12 | GND | A43 | PAR | B43 | +3.3V |
| A13 | GND | B13 | GND | A44 | AD15 | B44 | ~C/BE1 |
| A14 | +3.3V aux | B14 | RESERVED | A45 | +3.3V | B45 | AD14 |
| A15 | ~RST | B15 | GND | A46 | AD13 | B46 | GND |
| A16 | +5V (I/O) | B16 | CLK | A47 | AD11 | B47 | AD12 |
| A17 | ~GNT | B17 | GND | A48 | GND | B48 | AD10 |
| A18 | GND | B18 | ~REQ | A49 | AD9 | B49 | GND |
| A19 | ~PME | B19 | +5V (I/O) | A50 | KEY | B50 | KEY |
| A20 | AD30 | B20 | AD31 | A51 | KEY | B51 | KEY |
| A21 | +3.3V | B21 | AD29 | A52 | ~C/BE0 | B52 | AD8 |
| A22 | AD28 | B22 | GND | A53 | +3.3V | B53 | AD7 |
| A23 | AD26 | B23 | AD27 | A54 | AD6 | B54 | +3.3V |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| A24 | GND | B24 | AD25 | A55 | AD4 | B55 | AD5 |
| A25 | AD24 | B25 | +3.3V | A56 | GND | B56 | AD3 |
| A26 | IDSEL | B26 | ~C/BE3 | A57 | AD2 | B57 | GND |
| A27 | +3.3V | B27 | AD23 | A58 | AD0 | B58 | AD1 |
| A28 | AD22 | B28 | GND | A59 | +5V (I/O) | B59 | +5V (I/O) |
| A29 | AD20 | B29 | AD21 | A60 | ~REQ64C | B60 | ~ACK64C |
| A30 | GND | B30 | AD19 | A61 | +5V | B61 | +5V |
| A31 | AD18 | B31 | +3.3V | A62 | +5V | B62 | +5V |

## Processor fan

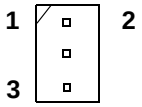



**Table C-15. Processor fan connector**

| Pin | Signal |
|---|---|
| 1 | GND |
| 2 | +12VDC |
| 3 | GND |

## VGA

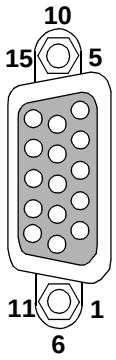



**Table C-16. VGA Pin-out**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Red | 9 | (key) |
| 2 | Green | 10 | Ground |
| 3 | Blue | 11 | (not used) |
| 4 | (not used) | 12 | (not used) |
| 5 | Ground | 13 | Horizontal sync |
| 6 | Ground | 14 | Vertical sync |
| 7 | Ground | 15 | programmable |
| 8 | Ground | | output |

# D Installing and configuring RomPilot

RomPilot provides the tools you need to remotely manage EMB-1's system, including BIOS, configuration and startup. This is done over a network. RomPilot is compatible with many PCI network adapters.

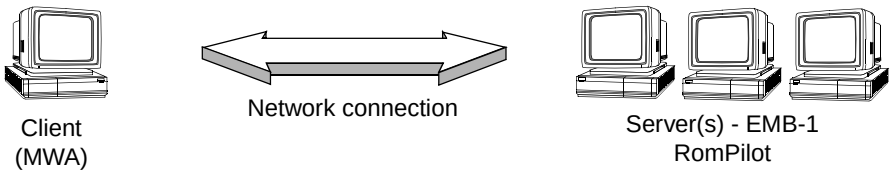



**Figure D-1. Relationship between the client and the server(s)**

| Term | Definition |
|---|---|
| Client | System that remotely manages the server(s). |
| Server | System(s) managed by the client. This is the EMB-1. |
| RomPilot image | Code integrated into server(s) system's BIOS, which you must configure and enable. |
| Management Workstation Application (MWA) | Software application installed on client system. Allows you to remotely manage the server(s). |

After you link the client and the server(s), you can:

- Store information about all server systems.
- Automatically log and monitor server's boot process.
- Pause and step through the server's POST.
- Access the server's DMI, ESCD, CMOS, PCI, and sector level disk information.
- Reboot the server.
- Upload and execute Phoenix Loadable Modules.

This appendix describes how to install, configure, and enable a RomPilot image on a server and the MWA software on a client.

When reading this file online, you can immediately view information about any RomPilot topic by placing the mouse cursor over a topic name and clicking.

**Task** **Page**

# Configuring the server - EMB-1

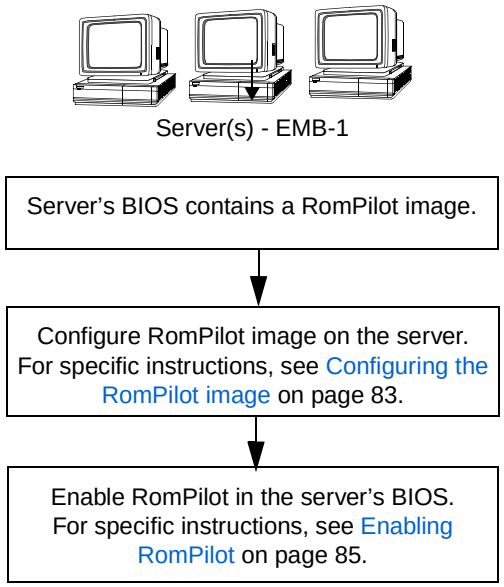



**Figure D-2. Configuring and enabling RomPilot on the server(s)**

## Before you begin

You will need the following during server configuration:

- RomPilot install disk. To obtain the install disk, see the RadiSys web site.
- A PCI network adapter.
- An IP and gateway address to assign to the server. You can also attach a Dynamic Host Configuration Protocol (DHCP) server to a DHCP-capable network. This assigns an IP address at the time of connection.
- The client's IP address.
- The correct network driver. The driver must be a Netware driver ending in "*.LAN." The driver must be smaller than 150,000 bytes.

## Installing the RomPilot image

The RomPilot image is already integrated into the server's BIOS. However, to remotely manage the server(s), you must do the following:

- Configure the RomPilot image to work with a specific network adapter and network.
- Enable the RomPilot image.

RadiSys has validated an Intel 82558-based Ethernet adapter with the EMB-1.

To configure the RomPilot image, see Configuring the RomPilot image on page 83.
To enable the RomPilot image, see Enabling RomPilot on page 85.

## Configuring the RomPilot image

To configure the RomPilot image, you must provide information required to complete a series of configuration windows. The first series of windows specifies network and driver information. The second series specifies server information.

During configuration, you can do the following at any time:

- Press the Esc key to move to the previous window.
- Select Abort to abort the installation.

Until you configure the RomPilot image and the client communicates with a server, the following error message displays during the boot process:

```
RomPilot reports error #26
```

1. Boot the server into MS-DOS.

   Ensure that MS-DOS does not load any memory managers.

2. Insert the RomPilot install disk into the floppy drive.

   The first time you execute the RomPilot image configuration program, the following message displays:

   ```
   RomPilot install data is corrupt. Using defaults.
   ```

   This is normal. Press the Enter key to continue configuration.

3. At the A: prompt, type Install and press the Enter key.
4. Press the Enter key. This displays the Connection Type window.

### Network and driver information

1. Specify the type of connection that the server uses to communicate with the client.
   A. Select Network Adapter (Default).
   B. Press the Enter key twice. This displays the Network Adapter window.
2. Specify the network adapter you want to use with RomPilot.
   A. Select Network Adapter.
   B. Press Enter twice. This displays the Network Driver Window.
3. Specify the driver you want to use with the server's network adapter. You can enter a path into the top field. You can use Refresh to show the potential drivers.
   A. Select the appropriate driver.
   B. Press the Enter key twice. This displays the Driver Load String Window.
4. Modify the default load string for the network driver. In most cases, the default settings should be sufficient.
   A. Select the appropriate driver load string.
   B. Press the Tab key.

C. Press the Enter key. This displays the Information/Verification window.

5. Confirm your selections for the network adapter and driver.

   A. To accept the selections, do the following:

      i. Press the Tab key to select Okay.

      ii. Press the Enter key. This links the network adapter with the server. The DHCP window displays.

   B. To change any selection, do the following:

      i. Navigate to the window(s) that need editing.

      ii. Change the appropriate setting(s).

      iii. Navigate back to the Information/Verification window.

      iv. Press the Tab key to select Okay.

      v. Press the Enter key to link the network adapter with the server. The DHCP window displays.

### Server information

1. Select how you want to specify the server's IP address. If you select DHCP, you will not need a specific IP address for the server.

   A. If you want to use a DHCP server, do the following:

      i. Select DHCP.

      ii. Press the Enter key. This displays the Drivers Parameters window.

      iii. Proceed to step 4.

2. If you do not select a DHCP server in step 1, the Machine Details window displays.

3. Specify the server's IP address, Subnet mask, and Gateway address.

   A. Enter the correct information into the fields. Press the Tab key to move between fields.

   B. Select Okay. This displays the Driver Parameters window.

4. Specify the network adapter's buffer details. The default settings should be sufficient for most situations.

   The buffer size must be at least 2100.

   A. Press the Tab key to move between fields.

   B. Select Okay and press the Enter key. This displays the Machine Name window.

5. Assign a unique name to the RomPilot server. The client uses the server name to distinguish between different servers.

   A. Press the Tab key to select Okay.

   B. Press the Enter key. This displays the Management Machines window.

6. Complete the IP Address, Application Type, and Timeout fields. Press the Tab key to move between fields.

   Use a maximum of three client machines to manage the servers on a network. Only one client can communicate with one specific server at one specific time. Using a Timeout prioritizes the clients.

   A. Press the Tab key to select Okay.

   B. Press the Enter key. This displays the Reset Traps window.

7. In the Reset Traps, Error Traps, Boot Traps, and 2nd SNMP port windows, do the following:

   A. Select the defaults setting.

   B. Press the Tab key to select Okay.

   C. Press the Enter key.

8. Type in a pass-phrase in the Pass Phrase window.

   The pass-phrase must be 1 to 64 characters long. You will use the same pass-phrase to link the the server to the client.

   A. Press the Enter key.

      As soon as you confirm the pass-phrase, the configuration program reads the BIOS into a file. It then inserts the driver and the configuration information into the BIOS. The customized BIOS automatically reflashes into the server.

      If you execute the install from a floppy disk, this may take a couple of minutes.

      During this process, a series of messages displays:

      ```
      Reading BIOS from ROM into a file.
      Inserting driver into BIOS file.
      Writing BIOS from file to ROM.
      ```

      After BIOS reflash, the final information window displays.

   B. Turn the server's power off and on to reboot the server.

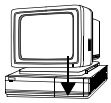
## Enabling RomPilot

To enable RomPilot:

1. Reboot the server.
2. During the boot process, press F2 to enter BIOS Setup.
3. Navigate to the BIOS main menu setup screen. See Main setup menu on page 18, for specific instructions.
4. Select RomPilot.
5. Change setting to Enabled.

6. Exit BIOS setup and continue the Boot process. The server is now ready to communicate with the client.

# Configuring the client



Client system

Install MWA software on a client system. For specific instructions, see Installing MWA on page 86.

Link the client with the server(s). For specific instructions, see Linking the client with the server(s) - EMB-1 on page 87.

**Figure D-3. Configuring a client system**

## Before you begin

### System requirements

The client machine requires:

- Windows 95, Windows 98 or Windows NT.
- A minimum 5 MB of free disk space.

### Installation and configuration requirements

During MWA installation and client configuration, you will need:

- The client's IP address.
- The server's name.
- The server's Pass-Phrase.

The client must be connected to the same network as the server.

## Installing MWA

### Installing the Setup wizard

1. Insert the MWA install disk into the client's floppy drive. To obtain the install disk, see the RadiSys web site.
2. Double-click on Setup.exe.

3. Follow the prompts provided by the setup wizard. Once setup is complete, a window containing several icons displays.

### Installing the MWA software

1. Double-click on the RomPilot MWA icon.
2. Enter a full directory path.
3. Click OK. This displays the following message:

   ```
   Do you want to create a new User Verification Phrase?
   ```

4. Click OK. This displays a window that prompts you to enter a Pass-Phrase.
5. Type in the pass-phrase you created during server configuration.
6. Type in the same pass-phrase to verify it.
7. Press the Enter key. This displays the Management Workstation Application window.

## Linking the client with the server(s) - EMB-1

1. Select New from the File menu.
   A. Enter the server's IP address.

   If you selected a DHCP server during server configuration, you do not have a fixed IP address for this server. To complete this field, enter a "dummy" IP address, such as "10.10.100.1".

   B. Press the Enter key. The Server Properties screen displays.
2. Enter the server's name. Use the name you created during server configuration.
3. Select Enter Pass Phrase.
   A. Type in a pass-phrase. Use the same pass-phrase you created during server configuration.
   B. Type in the pass-phrase again to verify it.
   C. Press OK. The Server Properties window displays.
4. Press OK to accept this server's information and to add this server to the client's database.
5. Repeat steps 1-4 for each server.

# Using the MWA software

For information about using the MWA software, see the online help.

# E BIOS update and recovery

This appendix details how to update and recover your system BIOS and the flash boot device (FBD).

When reading this file online, you can immediately view information about any topic by placing the mouse cursor over a task and clicking.



## Before you begin

To update or recover a system BIOS or the FBD, you must first create a flash diskette. There are two types of flash diskettes.

- The BIOS flash diskette, which only updates or recovers the system BIOS.
- The FBD flash diskette, which updates and recovers the FBD and the system BIOS.

### Creating a BIOS flash diskette

1. Obtain the BIOSREC.ZIP file from the RadiSys web site.
2. Unzip the contents to a directory on your hard drive.
3. To create the flash diskette within a Windows 95, Windows 98 or Windows NT operating system, do the following:
   A. Double-click on WINCRIS.EXE from the directory created in step 2.
   B. Insert a blank diskette into the floppy drive.
   C. Follow the steps as directed by WINCRIS.EXE.
4. To create the flash diskette within MS-DOS, do the following:
   A. Select CRISDISK.BAT from the directory created in step 2.
   B. Insert a blank diskette into the floppy drive.
   C. Follow the steps as directed by CRISDISK.BAT.

## Creating a FBD flash diskette

1. Obtain the FBDREC.ZIP file from the RadiSys web site.
2. Unzip the contents to a directory on your hard drive.
3. To create the flash diskette within a Windows 95, Windows 98 or Windows NT operating system, do the following:
   A. Double-click on WINCRIS.EXE from the directory created in Step 2.
   B. Insert a blank diskette into the floppy drive.
   C. Follow the steps as directed by WINCRIS.EXE.
4. If you are creating the flash diskette within MS-DOS, do the following:
   A. Select CRISDISK.BAT from the directory created in step 2.
   B. Insert a blank diskette into the floppy drive.
   C. Follow the steps as directed by CRISDISK.BAT.

# Updating the system BIOS

## Using a flash diskette

1. Create a flash diskette. See Creating a BIOS flash diskette on page 89.
2. Boot system into MS-DOS without memory managers.
3. Insert the flash diskette into the floppy drive.
4. Change MS-DOS directory to match the floppy drive's directory.
5. Type PHLASH and press Enter. This starts the update. When finished, the following message appears:

```
Flash memory has been successfully programmed
PRESS ANY KEY TO RESTART THE SYSTEM
If the system does not restart
TURN THE POWER OFF, THEN ON
```

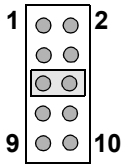
6. Turn off system power and re-boot.

## Using the force recovery jumper

1. Install the force recovery jumper:
   A. Turn off power.
   B. Remove the computer cover.

C. Find the BIOS configuration jumper block, located at J15.

D. Connect pins 5 and 6, as shown below.




Pins 5 and 6:
Force BIOS recovery

2. Insert the flash diskette into the floppy drive.
3. Power up the EMB-1.

   You will hear the following audio signals:

| Beep code | Definition |
|---|---|
| One long beep followed by two short beeps | BIOS update begins. |
| One steady single beep | BIOS update continues. |
| One long beep | BIOS update finishes. |

If there is an error, the speaker emits three beeps.

4. Remove the force recovery jumper:

   A. Turn off power.

   B. Find the BIOS configuration jumper block, located at J15.

   C. Disconnect pins 5 and 6.

5. Replace the computer cover.
6. Power up the EMB-1.

# Recovering the system BIOS

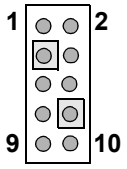
To recover a corrupted system BIOS, you must use the force recovery jumper. See Using the force recovery jumper on page 90 for detailed instructions.

# Updating the FBD

Updating the FBD also updates the system BIOS.

## Using a flash diskette

1. Create a flash diskette. See Creating a FBD flash diskette on page 90.
2. Install the boot block write enable jumper:
   A. Turn off power.
   B. Remove the computer cover.
   C. Find the BIOS configuration jumper block, located at J15.
   D. Connect pins 3 and 8, as shown below.




Pins 3 and 8:
Boot block write enable

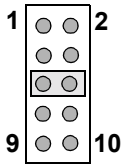
3. Replace the computer cover.
4. Boot system into MS-DOS without memory managers.
5. Insert the flash diskette into the floppy drive.
6. Change MS-DOS directory to match the floppy drive's directory.
7. Type PHLASH and press Enter. This starts the update. When finished, the following message appears:

```
Flash memory has been successfully programmed
PRESS ANY KEY TO RESTART THE SYSTEM
If the system does not restart
TURN THE POWER OFF, THEN ON
```

8. Turn off system power.
9. Remove the boot block write enable jumper:
   A. Turn off power.
   B. Remove the computer cover.
   C. Find the BIOS configuration jumper block, located at J15.
   D. Disconnect pins 3 and 8.
10. Replace the computer cover.
11. Power up the EMB-1.

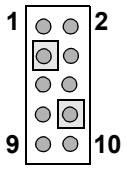
## Using the force recovery jumper

1. Install the force recovery and the boot block write enable jumpers:
   A. Turn off power.
   B. Remove the computer cover.
   C. Find the BIOS configuration jumper block, located at J15.
      a. Connect pins 5 and 6 to install the force recovery jumper, as shown below.




Pins 5 and 6:
Force BIOS recovery

      b. Connect pins 3 and 8 to install the boot block write enable jumper, as shown below.




Pins 3 and 8:
Boot block write enable

2. Insert the flash diskette into the floppy drive.
3. Power up the EMB-1.

   You will hear the following audio signals:

| Beep code | Definition |
|---|---|
| One long beep followed by two short beeps | BIOS update begins. |
| One steady single beep | BIOS update continues. |
| One long beep | BIOS update finishes. |

   If there is an error, the speaker emits three beeps.

4. Remove the force recovery and boot block write enable jumpers:
   A. Turn off power.
   B. Remove the computer cover.
   C. Find the BIOS configuration jumper block, located at J15.
      a. Disconnect pins 5 and 6.
      b. Disconnect pins 3 and 8.

5. Replace the computer cover.
6. Power up the EMB-1.

## Recovering the FBD.

If the boot block is corrupt and not executable, return the EMB-1 to the factory for repair. For information about returning items to RadiSys, see the RadiSys web site.

Use extreme caution when updating the boot block. A BIOS boot block rarely changes and should not require updating.

To recover a corrupted FBD, you must use the force recovery jumper. See Using the force recovery jumper on page 93 for detailed instructions.

# F Error messages

## Boot failures

The System BIOS halts and attempts to display an error message on the VGA monitor when it encounters the following conditions:

| Condition number | Warning message |
|---|---|
| 0200 | Failure fixed disk |
| 0210 | Stuck key |
| 0212 | Keyboard controller failed |
| 0213 | Keyboard locked - unlock key switch |
| 0220 | Monitor type does not match CMOS - run setup |
| 0230 | System RAM failed at offset: |
| 0231 | Shadow RAM failed at offset: |
| 0232 | Extended RAM failed at offset: |
| 0250 | System battery is dead. Replace and run setup. |
| 0251 | System CMOS checksum bad - Default configuration used |
| 0260 | System timer error |
| 0270 | Real time clock error |
| 0271 | Check date and time settings |
| 0280 | Previous boot incomplete - Default configuration used |
| 0281 | Memory size found by POST differed from EISA CMOS |
| 02B0 | Diskette Drive A error |
| 02B1 | Diskette Drive B error |
| 02B2 | Incorrect Drive A type - run setup |
| 02B3 | Incorrect Drive B type - run setup |
| 02D0 | System cache error - cache disabled |
| 02F0 | CPU ID: |
| 02F4 | EISA CMOS not writeable |
| 02F5 | DMA rest failed |
| 02F6 | Software NMI failed |
| 02F7 | Fail-Safe Timer NMI |

# Beep codes

| Code | Beeps | POST routine description |
|---|---|---|
| 16h | 1-2-2-3 | BIOS ROM checksum |
| 20h | 1-3-1-1 | Test DRAM refresh |
| 22h | 1-3-1-3 | Test 8742 keyboard controller |
| 2Ch | 1-3-4-1 | RAM failure on address line xxxx |
| 2Eh | 1-3-4-3 | RAM failure on address line xxxx of low byte of memory bus |
| 30h | 1-4-1-1 | RAM failure on data bits xxxx of high byte of memory bus |
| 46h | 2-1-2-3 | Check ROM copyright notice |
| 58h | 2-2-3-1 | Test for unexpected interrupts |
| 98h | 1-2 | Search for option ROMs. One long, two short beeps on checksum failure |
| B4h | 1 | One short beep before boot |

# Glossary

**Access Time:** A factor in measurement of a memory storage device's operating speed. It is the amount of time required to perform a read operation. More specifically, it is the period of time between which the memory receives a read command signal and the time when the requested data becomes available to the system data bus.

**Address:** A number that identifies the location of a word in memory. Each word in a memory storage device or system has a unique address. Addresses are always specified as a binary number, although octal, hexadecimal, and decimal numbers are often used for convenience.

**APM:** Advanced Power Management. A software interface specification that allows operating system device drivers to control the power management functionality of a PC.

**ANSI:** American National Standards Institute. An organization dedicated to advancement of national standards related to product manufacturing.

**ATA:** AT Bus Attachment. An interface definition for PC peripherals. See IDE.

**Autotype:** A convenient method of IDE device detection whereby the system BIOS queries the IDE device to obtain operational parameters. If the device supports autotype, this information is passed to the BIOS where it is used to automatically configure the drive controller.

**BIOS:** Basic Input/Output System. Firmware in a PC-compatible computer that runs when the computer is powered up. The BIOS initializes the computer hardware, allows the user to configure the hardware, boots the operating system, and provides standard mechanisms that the operating system can use to access the PC's peripheral devices.

**BDA:** BIOS Data Area. BIOS Data Area. A 256 byte block of DRAM starting at address 400H that contains data initialized and used by the System BIOS detailing the system configuration and errors encountered during POST.

**BIOS Extension:** An object code module that is typically integrated into the FBD or placed into a ROM that is accessible on the peripheral bus (PCI, ISA, etc.) in the address range 0C0000h through 0DFFFFh. BIOS extensions have a pre-defined header format and contain code that is used to extend the capabilities of the System BIOS.

**BIOS Image:** Information contained in the flash boot device in binary file format consisting of initialzation data, setup configuration data, diagnostic sequences, and other instructions necessary to start up a computer and prepare it to load an operating system.

**BIOS Recovery:** A process whereby an existing, corrupt BIOS image in the flash boot device is overwritten with a new image. Also referred to as a flash recovery.

**BIOS Update:** A process whereby an existing, uncorrupted BIOS image in the flash boot device is overwritten with a new image. Also referred to as a flash update.

**Bit:** A binary digit.

**Boot:** The process of starting a computer and loading the operating system from a powered down state (cold boot) or after a computer reset (warm boot). Before the operating system loads, the computer performs a general hardware initialization and resets internal registers.

**Boot Block:** A write-protected 16KB section of the flash boot device located at physical address FFFFC000h to FFFFFFFFh which contains code to perform rudimentary hardware intitialization at system power up. The boot block also contains code to recover the BIOS via floppy disk.

**Boot Device:** The storage device from which the computer boots the operating system.

**Boot Sequence:** The order in which a computer searches external storage devices for an operating system to boot. The boot device must be the first in the boot sequence.

**Byte:** A group of 8 bits.

**CPU:** Central Processing Unit. A semiconductor device which performs the processing of data in a computer. The CPU, also referred to as the microprocessor, consists of an arithmetic/logic unit to perform the data processing, and a control unit which provides timing and control signals necessary to execute instructions in a program.

**Chipset:** One or more integrated circuits that, along with a CPU, memory, and other peripherals, implements an IBM PC-AT compatible computer. The chipset typically implements a DRAM controller, bus, interface logic, and PC peripheral devices.

**CAS:** Column Address Strobe. An input signal from the DRAM controller to an internal DRAM latch register specifying the column at which to read or write data. The DRAM requires a column address and a row address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of column addresses and row addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.

**COM Port:** A bi-directional serial communication port which implements the RS-232 specification.

**CMOS:** Complimentary Metal Oxide Semiconductor. A fast, low power semiconductor RAM used to store system configuration data.

**Conventional Memory :** The first 640 KB of a computer's total memory capacity. If a computer has no extended memory, conventional memory equals the total memory capacity. In typical computer systems, conventional memory can contain BIOS data, the operating system, applications, application data, and terminate and stay resident (TSR) programs. Also called system memory.

**CSR:** CMOS Save and Restore. A System BIOS feature that allows the user to backup the contents of CMOS RAM (contained within the real time clock) to the BIOS Flash device to be restored later if necessary (such as when the real time clock battery dies).

**CHS:** Cylinders/Heads/Sectors. A specification of disk drive operating parameters consisting of the number of disk cylinders, disk drive read/write heads, and disk sectors.

**Default:** The state of all user-changeable hardware and software settings as they are originally configured before any changes are made.

**DOS:** Disk Operating System. One or more programs which allow a computer to use a disk drive as an external storage device. These programs manage storage and retrieval of data to and from the disk and interpret commands from the computer operator.

**Driver:** A software component of the operating system which directs the computer interface with a hardware device. The software interface to the driver is standardized such that application software calling the driver requires no specific operational information about the hardware device.

**DRAM.:** Dynamic Random Access Memory. Semiconductor RAM memory devices in which the stored data does not remain permanently stored, even with the power applied, unless the data are periodically rewritten into memory during a refresh operation.

**EEPROM:** Electrically Erasable Programmable ROM. Specifically, those EPROMs which may be erased electrically as compared to other erasing methods.

**Error Checking and Correction:** A feature of the T2 chipset that enables it to detect single or multi-bit errors in DRAM reads and correct single bit errors. This feature requires that all banks of DRAM use x36 (parity) SO DIMMs.

**ECP:** Extended Capabilities Port. An enhancement of the standard PC parallel port that allows high speed bi-directional data transfers and other features.

**EDO:** Extended Data Out. A type of DRAM that allows higher memory system performance since the data pins are still driven when CAS# is de-asserted. This allows the next DRAM address to be presented to the device sooner than with Fast Page Mode DRAM.

**Extended Memory:** The RAM address space, in a computer so equipped, above the 1 MB level.

**ESCD:** Extended System Configuration Data. A block of nonvolatile memory that stores information on the devices found and configured by the Plug and Play BIOS.

**External Device:** A peripheral or other device connected to the computer from an external location via an interface cable.

**Fixed Disk:** A hard disk drive or other data storage device having no removable storage medium. Fixed disk storage devices use inflexible disk media and are sealed to prevent data loss due to media surface contamination. Fixed disks generally provide the most storage space for a given cost when compared to semiconductor, tape, and other popular mass storage technologies.

**FBD:** Flash Boot Device. A flash memory device containing the computer's BIOS. In the NY1210, a 1 MByte Intel 28F800B5 semiconductor flash memory containing the system and video BIOS images, the BIOS initializing code and the recovery code which allows self hosted reflashing.

**Flash Memory:** A fast EEPROM semiconductor memory typically used to store firmware such as the computer BIOS. Flash memory also finds general application where a semiconductor non-volatile storage device is required.

**Flash Recovery:** See BIOS Recovery.

**Flash Update:** See BIOS Update.

**Force Update:** See BIOS Recovery.

**GB or GByte:** Gigabyte. Approximately one billion (US) or one thousand million (Great Britain) bytes. 2^30 = 1,073,741,824 bytes exactly.

**Hang:** A condition where the system microprocessor suspends processing operations due to an anomaly in the data or an illegal instruction.

**Header:** A mechanical pin and sleeve style connector on a circuit board. The header may exist in either a male or female configuration. For example, a male header has a number and pattern of pins which corresponds to the number and pattern of sleeves on a female header plug.

**h:** Hexadecimal. A base 16 numbering system using numeric symbols 0 through 9 plus alpha characters A, B, C, D, E, and F as the 16 digit symbols. Digits A through F are equivalent to the decimal values 10 through 15.

**Host Bus:** The address/data bus that connects the CPU and the chipset.

**ISA:** Industry Standard Architecture. A popular microcomputer expansion bus architecture standard. The ISA standard originated with the IBM PC when the system bus was expanded to accept peripheral cards.

**I/O:** Input/Output. The communication interface between system components and between the system and connected peripherals.

**IDE:** Integrated Drive Electronics. A hard disk drive/controller interface standard. IDE drives contain the controller circuitry at the drive itself, as compared to the location of this circuitry on the computer motherboard in non-IDE systems. IDE drives typically connect to the system bus with a simple adapter card containing a minimum of on-board logic.

**INT:** Interrupt Request. A software-generated interrupt request.

**IRQ:** Interrupt Request. In ISAbus systems, a microprocessor input from the control bus used by I/O devices to interrupt execution of the current program and cause the microprocessor to jump to a special program called the interrupt service routine. The microprocessor executes this special program, which normally involves servicing the interrupting device. When the interrupt service routine is completed, the microprocessor resumes execution of the program it was working on before the interruption occurred.

**ISR:** Interrupt Service Routine. A program executed by the microprocessor upon receipt of an interrupt request from an I/O device and containing instructions for servicing of the device.

**Jumper:** A set of male connector pins on a circuit board over which can be placed coupling devices to electrically connect pairs of the pins. By electrically connecting different pins, a circuit board can be configured to function in predictable ways to suit different applications.

**KB or KByte:** Kilobyte. Approximately one thousand bytes. $2^{10} = 1024$ bytes exactly.

**Logical Address:** The memory-mapped location of a segment after application of the address offset to the physical address.

**LBA:** Logical Block Addressing. A method the system BIOS uses to reference hard disk data as logical blocks, with each block having a specific location on the disk. LBA differs from the CHS reference method in that the BIOS requires no information relating to disk cylinders, heads, or sectors. LBA can be used only on hard disk drives designed to support it.

**MB or MByte:** Megabyte. Approximately one million bytes. 2^20 = 1,048,576 bytes exactly.

**Memory:** A designated system area to which data can be stored and from which data can be retrieved. A typical computer system has more than one memory area. See Conventional Memory and Extended Memory.

**Memory shadowing:** Copying information from an extension ROM into DRAM and accessing it in this alternate memory location.

**Offset:** The difference in location of memory-mapped data between the physical address and the logical address.

**Operating System:** See DOS.

**PCI:** Peripheral Connect Interface. A popular microcomputer bus architecture standard.

**Peripheral Device:** An external device connected to the system for the purpose of transferring data into or out of the system.

**PC/AT:** Personal Computer/Advanced Technology. A popular computer design first introduced by IBM in the early 1980s.

**PS/2:** Personal System 2. Computers designed with IBM's proprietary bus architecture known as Micro Channel.

**Physical Address:** The address or location in memory where data is stored before it is moved as memory remapping occurs. The physical address is that which appears on the computer's address bus when the CPU requests data from a memory address. When remapping occurs, the data can be moved to a different memory location or logical address.

**Pinout:** A diagram or table describing the location and function of pins on an electrical connector.

**POST:** Power On Self Test. A diagnostic routine which a computer runs at power up. Along with other testing functions, this comprehensive test initializes the system chipset and hardware, resets registers and flags, performs ROM checksums, and checks disk drive devices and the keyboard interface.

**Program:** A set of instructions a computer follows to perform specific functions relative to user need or system requirements. In a broad sense, a program is also

| | |
|---|---|
| | referred to as a software application, which can actually contain many related, individual programs. |
| **RAM:** | Random Access Memory. Memory in which the actual physical location of a memory word has no effect on how long it takes to read from or write to that location. In other words, the access time is the same for any address in memory. Most semiconductor memories are RAM. |
| **ROM:** | Read Only Memory. A broad class of semiconductor memories designed for applications where the ratio of read operations to write operations is very high. Technically, a ROM can be written to (programmed) only once, and this operation is normally performed at the factory. Thereafter, information can be read from the memory indefinitely. |
| **Real Mode:** | The operational mode of Intelx86 CPUs that uses a segmented, offset memory addressing method. These CPUs can address 1 MB of memory using real mode. |
| **Real Mode Address:** | A memory address composed of two 16-bit values: a segment address and an offset quantity. A real mode address is constructed by shifting a segment address 4 bits to the left and then adding the offset value. A real mode address is a physical address. |
| **RTC:** | Real Time Clock. Peripheral circuitry on a computer motherboard which provides a nonvolatile time-of-day clock, an alarm, calendar, programmable interrupt, square wave generator, and a small amount of SRAM. In the NY1210, the RTC operates independently of the system PLL which generates the internal system clocks. The RTC is typically receives power from a small battery to retain the current time of day when the computer is powered down. |
| **Reflashing:** | The process of replacing a BIOS image, in binary format, in the flash boot device. |
| **Register:** | An area typically inside the microprocessor where data, addresses, instruction codes, and information on the status on various microprocessor operations are stored. Different types of registers store different types of information. |
| **Reset:** | A signal delivered to the microprocessor by the control bus, which causes a halt to internal processing and resets most CPU registers to 0. The CPU then jumps to a starting address vector to begin the boot process. |
| **RFA:** | Resident Flash Array. The RFA represents flash memory that is resident on the hardware platform that is utilized for OS or application purposes. |
| **RS-232:** | A popular asynchronous bi-directional serial communication protocol. Among other things, the RS-232 standard defines the interface cabling and electrical characteristics, and the pin arrangement for cable connectors. |
| **RAS:** | Row Address Strobe. An input signal to an internal DRAM latch register specifying the row at which to read or write data. The DRAM requires a row address and a column address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of row addresses and column addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required. |
| **Segment:** | A section or portion of addressable memory serving to hold code, data, stack, or other information allowing more efficient memory usage in a computer |

system. A segment is the portion of a real mode address which specifies the fixed base address to which the offset is applied.

**Serial Port:** A physical connection with a computer for the purpose of serial data exchange with a peripheral device. The port requires an I/O address, a dedicated IRQ line, and a name to identify the physical connection and establish serial communication between the computer and a connected hardware device. A serial port is often referred to as a COM port.

**Shadow Memory:** RAM in the address range 0xC000h through 0xFFFFFh used for shadowing. Shadowing is the process of copying BIOS extensions from ROM into DRAM for the purpose of faster CPU access to the extensions when the system requires frequent BIOS calls. Typically, system and video BIOS extensions are shadowed in DRAM to increase system performance.

**Standoff:** A mechanical device, typically constructed of an electrically non-conductive material, used to fasten a circuit board to the bottom, top, or side of a protective enclosure.

**SRAM:** Static Random Access Memory. A semiconductor RAM device in which the data remains permanently stored as long as power is applied, without the need for periodically rewriting the data into memory.

**SYSCLK:** ISAbus System Clock. The ~8.33MHz clock signal present on the ISAbus to which all bus transactions are synchronized.

**System Memory:** See Conventional Memory.

**USB:** Universal Serial Bus. A new serial data bus that is intended to eliminate the need for separate serial, parallel, mouse, keyboard, joystick, etc. ports on a PC-compatible. These ports can be conceivably replaced by a few, daisy-chained USB ports, all with identical connectors but capable of much higher throughput, upwards of 12Mbs.

**UED:** User Editable Drive. A feature of the NY1210's Phoenix NuBIOS. When a "User" type hard disk drive setting shows in the IDE Adapter Sub-Menu the BIOS queries the hard disk drive for the purpose of retrieving disk geometry. If the hard disk drive is capable of providing this information, the BIOS uses it to automatically set up the drive for use with the system.

**VESA:** Video Electronics Standards Association. A group of hardware and software vendors that define specifications for hardware and software interfaces for a variety of devices.

**VGA:** Video Graphics Adapter. A popular PC graphics controller and display adapter standard developed by IBM. The standard specifies, among other things, the resolution capabilities of the display device. Display devices meeting the VGA standard must be capable of displaying a minimum resolution of 640 horizontal pixels by 480 vertical pixels with at least 16 screen colors.

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