RadiSys®

Endura EM440 & EM440V

Product Development Specification

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1. Revision History.

Revision 00	10th March 2000	Initial update from EMB1 Rev 02.
Revision 01	27th April 2000	Update for Rev01 to add riser and auto on/off power on.
Revision 02	15th May 2000	Added PCI/ISA slot number clarification
Revision 03	23rd August 2000	Update for Rev02 changes and connector descriptions
Revision 10	25th September 2000	First Customer Release

2. Reference Materials

2.1. Intel Documents

Document Title	Intel Order #
82371AB PCI-to-ISA / IDE Xcelerator (PIIX4); April 1997	290562-001
Intel 82371EB (PIIX4E) Specification Update; Rev 0.3; November 1997	290635-007
PIIX4 BIOS Specification Update; Revision 0.9, December 1997	
82371AB (PIIX4) PCI ISA IDE Xcelerator Timing Specification; September 1997	290548-001
Intel 440BX AGPset: 82443BX Host Bridge/Controller Datasheet; April 1998	290633-001
82443BX Specification Update; Rev 2.0; June 1998	
440BX/440GX BIOS Specification Update; Rev 2.7; June 30th 1998	
Intel Celeron Processor Datasheet; January 1999	243658-006
370-Pin Socket (PGA370) Design Guidelines; November 1998	244410-001
Intel ® Celeron ™ Processor (PPGA)/440ZX AGPset Recommended Design & Debug Practices; Rev 1.0; Sept 1998	FM-1335 (yellow cover)
Intel ® Celeron ™ Processor, 300A, 333, 366 MHz, PPGA, Electrical, Mechanical, and Thermal Specifications (EMTS); Rev 1.0; August 4th 1998	FM-1276 (yellow cover)
Intel ® Coppermine-256K Processor, 600E, 700 MHz, FC-PGA, Electrical, Mechanical, and Thermal Specifications (EMTS); Rev 1.5; Sept 1999	FM-1685 (yellow cover)
Intel ® Celeron ™ Processor/440ZX AGPset Uniprocessor Customer Reference Schematics; Rev 1.0; August 1998	FM-1294 (yellow cover)
ATX Riser Specification Revision 1.0 December 1999	
5 Volt Boot Block Flash Memory; April 1999	290599-006

Table 1. Reference Materials - Intel Documents

2.2. RadiSys Documents

Title	Author
BX System BIOS Base Specification (Rev 1.1, 6/10/99)	Bob McGregor
Product-Specific Embedded Motherboard (EMB1) System BIOS Specification (Rev 1.1, 6/10/99)	Bob McGregor

Table 2. Reference Materials - RadiSys Documents

2.3. Other Documents

Title	Publisher
PC87309 Super I/O Plug and Play Compatible Chip in Compact 100-Pin VLJ Packaging; April 1998	National Semiconductor

Table 3. Reference Materials - Other Documents

3. Project Overview

This motherboard is a standard product designed to fit into an ATX desktop computer chassis. This product uses components that have been selected from the Intel Embedded Roadmap and are available from Intel for a minimum of 5 years from their date of introduction. This motherboard will be available from RadiSys for 5 years from the date of its introduction.

3.1. Functional Overview

This ATX long life, embedded motherboard consists of the following components:

CPU	370-PPGA 300/66,433/66,566/66,733/66:370FC-PGA 600/100,700/100,850/100
Socket 370	RadiSys P/N 97-0002-00 or equivalent
North Bridge	Intel FW82443BX; RadiSys P/N 97-3201-00 or equivalent
South Bridge	Intel FW82371EB PIIX4E; RadiSys P/N 97-3202-00 or equivalent
Memory	Two 168 pin DIMM connectors; RadiSys P/N 97-0006-00 or equivalent
2X AGP Conn.	RadiSys P/N 97-1801-00 or equivalent
PCI slots	Two and one shared; RadiSys P/N 97-0183-00 or equivalent
PCI Riser	Radisys P/N 97-1806-00 or equivalent
ISA slots	Three and one shared; RadiSys P/N 97-0184-00 or equivalent
Clock Generator	Pericom PI6C103; RadiSys P/N 97-3204-00 or equivalent
Clock Buffer	Pericom PI6C182HX; RadiSys P/N 97-0255-00 or equivalent
Power	5V to 2.0V CPU core voltage regulator; Fairchild FAN5061M; RadiSys P/N 97-0012-00 or equivalent
Flash Boot Device (FBD)	Micron 28F400B5-T, 512KB; RadiSys P/N 97-xxxx-00 or equivalent
Super I/O	National PC87309; RadiSys P/N 97-3203-00 or equivalent
Parallel Port VGA Connector Serial Port COM1	RadiSys P/N 97-0107-00 or equivalent (Combination connector) OR 97-1803-00 for parallel and 97-1804-00 for serial if non video board.
Serial Port COM2	RadiSys P/N 97-0239-00 or equivalent
Floppy	RadiSys P/N 97-0176-00 or equivalent
IDE	Two RadiSys P/N 97-0188-00 or equivalent
ATX PWR Conn.	RadiSys P/N 97-0196-00 or equivalent
USB	Dual, Stacked connector; RadiSys P/N 97-0151-00 or equivalent
PS/2	Stacked Keyboard/Mouse PS/2 connector; RadiSys P/N 97-0203-00 or equivalent
CPU Fan Header	RadiSys P/N 97-0162-00 or equivalent
RTC Battery Socket	RadiSys P/N 97-2500-00 or equivalent
RTC Battery Cell	Sony CR2032; RadiSys P/N 17-0025-00 or equivalent
1X29 Header	For: fan, PWR button, reset button, PWR LED, HD LED, PC Speaker; RadiSys P/N 97-1800-00 or equivalent
2X3 Hard/Soft PSU	Radisys P/N 97-259-00 or equivalent
2X5 Manufacturing Header	RadiSys P/N 97-0119-00 or equivalent
Operating System Support	Win 98,Win2000, WinNT 4.0, QNX & VX Works

Table 4. EM440 Components

3.2. Schematic Block Diagram

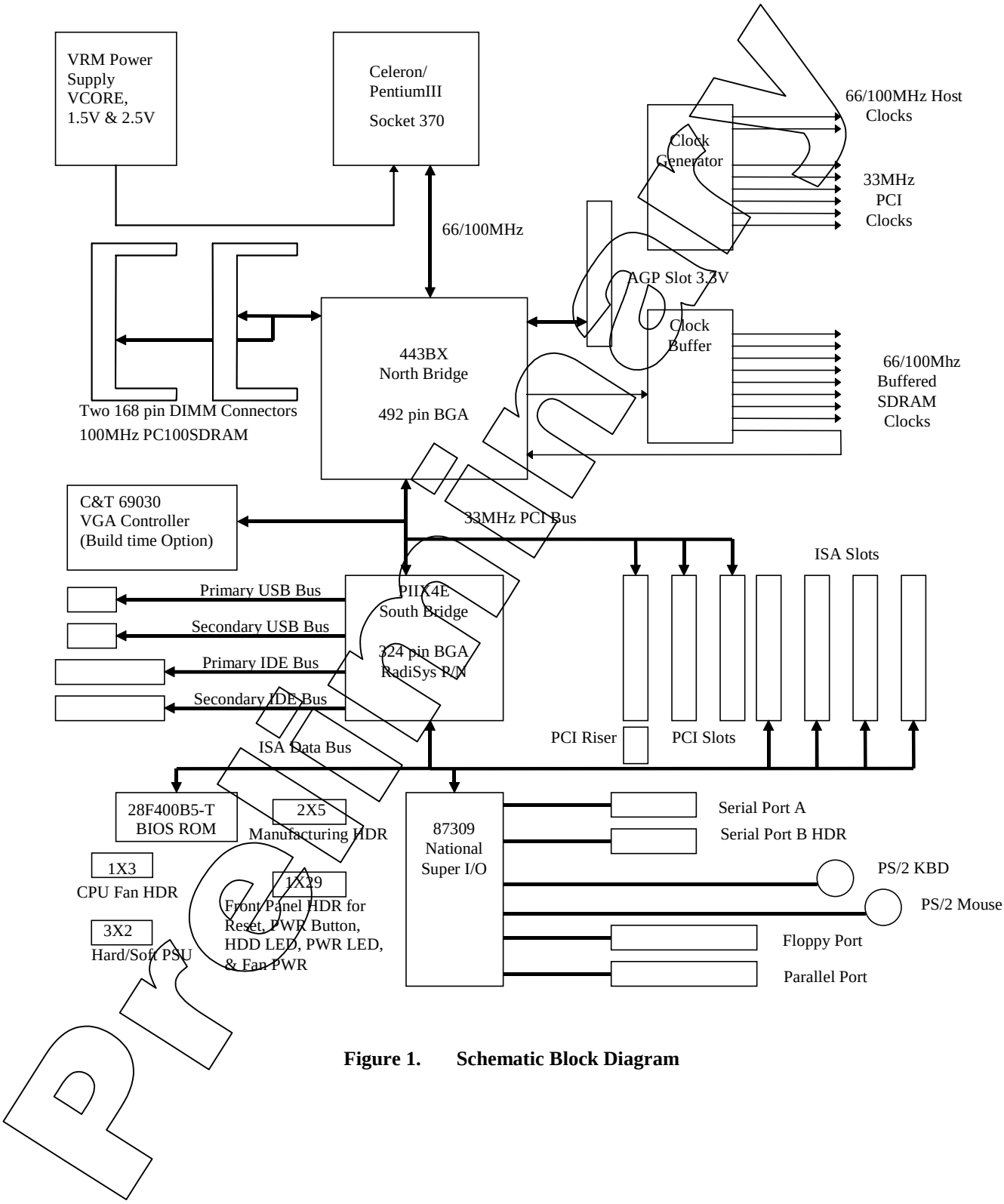

Figure 1. Schematic Block Diagram

3.2. Celeron/Pentium III CPU

This ATX motherboard supports a Socket 370, Intel Celeron® and Pentium III Processors. It uses the GTL+ system bus used by the Pentium II/III processors with support limited to single processor based systems. The 366, 433 & 566MHz versions of the Intel (Mendacino) Celeron® Processor in a Plastic Pin Grid Array (PPGA) or FC_PGA and the 600, 700 & 850MHz versions of the Coppermine Pentium III processors in the FC_PGA will be supported. All three versions of Celeron contain 128KB of L2 cache and 16KB Code and 16KB Data L1 cache. The Coppermine Pentium III processors contain 256KB of L2 enhanced cache.

Power and voltage specifications are as follows:

Power:	300/66MHz:	21.4W maximum
	433/66MHz:	25.4W maximum
	566/66MHz:	TBDW maximum
	733/66MHz:	TBDW maximum
	600/100MHz:	19.3W maximum
	700/100MHz:	22.5W maximum
	850/100MHz:	27.3W maximum

85^0 C maximum case temperature

The thermal solution is discussed in the mechanical section of this specification.

3.3. 82443BX North Bridge

The Intel 82443BX system controller provides an integrated solution for the socket 370 processors and data path components. The 82443BX is a 492 pin BGA running on 3.3V with mixed +5V, 3.3V, and GTL+ termination voltages and dissipates a maximum of 5W. The 82443BX contains support for a CPU to PCI bridge, a CPU to AGP bridge, a DRAM/SDRAM memory controller, and the central arbitration functions for the PCI bus. The 82443BX supports concurrent CPU, AGP, and PCI transactions to main memory.

3.3.1 82443BX PCI Bus

The Intel 82443BX supports CPU-to-PCI cycles. The 82443BX and the PCI CLK run at 33 MHz. When acting as a PCI target, the 82443BX does not respond to the cycles listed in Table 4. When acting as a bus master on behalf of the CPU, the 82443BX does not issue PCI commands for the host bus commands listed in Table 5.

The PCI Bus features are:

- Fully synchronous, minimum latency 33 MHz PCI bus interface
- Zero wait state CPU-to-PCI write timings (no IRDY stall)
- PCI 2.1 compliant
- Data streaming support from PCI to DRAM (~120MB/s for writes, ~100MB/s for reads)
- Supports five PCI bus masters in addition to the Host and PCI to ISA bridge

PCI Command
Interrupt Acknowledge
Special Cycle
I/O Read
I/O Write
Configuration Read
Configuration Write
Dual Address Cycle
Reserved Commands

Table 5. 82443BX Unsupported PCI Target Commands

Host Bus Command
Deferred Reply
Branch Trace Message
Memory Read of 16 Bytes
Memory Write of 16 Bytes

Host Bus Command
EA Memory Access

Table 6. 82443BX Unsupported Commands as PCI Master

3.3.2. AGP Bus

The 82443BX Host Bridge provides a AGP bus interface that is compliant with the A.G.P. Interface Specification, Revision 1.0. The 82443BX supports AGP/PCI interface referred to as AGP for PCI transactions and AGP for PCI transactions using the AGP enhanced protocols. The AGP is a high performance bus intended for graphical display devices. It provided the following features:

- Pipelined memory read and write operations.
- De-multiplexing of address and data on the bus.
- Real data throughput over 500 MB/sec.

The AGP connector supports the AGP retention mechanism clip using the right handed level version.

3.3.3. DRAM/SDRAM Memory Controller

The 82443BX supports EDO, 66 MHz & 100MHz SDRAM memory at densities up to 512MB. The EM440 will only have two 168 pin DIMM sockets and has not been validated using EDO. Presently, 256MB per SDRAM DIMMs are readily available. The BX does not support Fast Page Mode memory devices.
The 82443BX and the EM440 also support ECC.

3.4. PIIX4E South Bridge

The Intel PIIX4E is a 324 pin BGA running on 3.3V with a reference voltage tied to +5V for +5V signal compatibility. It dissipates a maximum of 1W. The PIIX4E provides support for a PCI to ISA bridge, an IDE controller, compatibility devices, a dual USB controller, an SMBus interface, a real time clock (RTC), and system power management. A detailed description of each of these follows.

3.4.1. PCI - ISA Bridge

The PIIX4E is fully PCI 2.1 compatible as well as IEEE 996 compatible (ISA, AT bus). On PCI, the PIIX4E operates as a bus master for various internal modules, such as the USB controller, DMA controller, IDE bus master controller, distributed DMA masters, and on behalf of ISA masters. Internal registers or cycles passed to the ISA or EIO buses make the PIIX4E operate as a target. All internal registers are positively decoded.

The PIIX4E chip drives most of the ISA bus directly. The PIIX4E incorporates an ISA bus compatible master and slave interface, and directly drives five ISA slots without external data buffers. The ISA interface also provides byte swap logic, I/O recovery support, wait state generation, and SYSCLK generation. There are two devices on the EM440 connected to the ISA bus, the Super I/O and the Flash ROM BIOS.

3.4.2. IDE Controller

The PIIX4E fast IDE interface supports up to four IDE devices through two independent IDE signal channels. The IDE interface supports PIO IDE transfers up to 14 MB/s and Bus Master IDE transfers up to 33 MB/s. It does not consume any ISA DMA resources and integrates eight, 32-bit buffers for optimal transfers.

The PIIX4E chip supports Modes 1, 2, 3 & 4 as well as Bus Master (DMA) Modes 0, 1 and 2. There is no support for the obsolete IDE register at I/O address 0x3F7. The PIIX4E supports “Ultra DMA/33” Synchronous DMA Mode Transfers.

Only PCI Masters have access to the IDE port. ISA Bus masters cannot access the IDE I/O port addresses. The IDE data transfer command strobes, DMA request and grant signals, and IORDY signals interface directly to the chip-set.

3.4.3. Compatibility Devices

The PIIX4E contains three compatibility devices, a DMA controller, a timer/counters, and an interrupt controller. The DMA controller incorporates the logic of two 82C37 DMA controllers. The timer/counter block contains three counters that are equivalent in function to those found in one 82C54 programmable interval timer. The ISA compatible interrupt controller incorporates the functionality of two 82C59 interrupt controllers.

The DMA controller has seven independently programmable channels. Channels [3:0] are hardwired to 8 bit, count-by-byte transfers. Channels [7:5] are hardwired to 16-bit, count by word transfers. Any two of the seven DMA channels can provide support for fast Type-F transfers. The DMA controller also generates the ISA refresh cycles.

The DMA controller supports two separate methods for handling legacy DMA via the PCI bus. The PC/PCI protocol allows PCI-based peripherals to initiate DMA cycles by encoding requests and grants via three PC/PCI REQ#/GNT# pairs. The second method, Distributed DMA, allows PCI devices to receive reads and writes to 82C37 registers. The DMA controller also provides support for the serial interrupt scheme typically associated with Distributed DMA. The EM440 does not support using either of these protocols.

The timer/counter block provides the system timer function, refresh request, and speaker tone. The 14.31818 MHz oscillator input provides the clock source for these three counters.

Cascading of the interrupt controllers provides 14 external and two internal interrupts. Additionally, PIIX4E supports a serial interrupt scheme. The EM440 does not support using this protocol.

All of the registers in these modules are able to be read and restored. This allows saving and restoring the system state after removing power and restoring it to the circuit.

3.4.4. Enhanced USB Controller

The PIIX4E USB controller provides enhanced support for the Universal Host Controller Interface (UHCI). This includes support allowing legacy software to use a USB based keyboard and mouse. The following are characteristics of the USB controller and its implementation on the EM440:

- supports serial transfers at 12 or 1.5Mbit/sec
- supports legacy keyboard and mouse software with USB-based keyboard and mouse
- supports Universal Host Controller Interface (UHCI) design guide
- all of the termination components for the USB signals will be included on the EM440 Baseboard. Standard termination techniques are as follows: A 47pF cap to GND, a 27 ohm series resistor, a 15K ohm resistor to GND, and a series ferrite bead before connecting to the USB connector on each of the USB signals.

3.4.5. SMBus Interface

The PIIX4E SMBus interface allows the CPU to communicate via SMBus to other peripherals. This bus will be used to read the Serial Present Detect (SPD) information from the memory module when configuring the memory controller. It can also be used to disable the unused clock outputs on the clock buffer. The SMBus is a subset of the I2C protocol.

3.4.6. Real-Time Clock (RTC)

The PIIX4E contains an internal Real-Time Clock. The battery voltage needed to maintain the RTC and CMOS RAM is supplied by the EM440.

The PIIX4E Real-Time Clock has the following characteristics:

- 2.0V to 3.6V is the required voltage range for the RTC battery input to the PIIX4E
- date-and-time keeping with alarm features and battery backed up information
- three interrupt features including time of day alarm
- 256 bytes of battery-backed static RAM in two banks: the standard bank and the extended bank
- requires an external oscillating source of 32.768KHz that is provided on board; this clock is divided down to a 1Hz signal
- two 8-byte lockable RAM ranges that, when locked, cannot be read or written
- Y2K compliant
- 6uA typical; 8uA maximum current drawn on RTC power supply

3.4.7. Power Management Logic

The PIIX4E power management function provides a wide range of capabilities and configuration options. The EM440 will support basic power management functionality by putting the system in "Standby". This includes spinning down the hard disk, shutting down the VGA display, and throttling back the CPU. It also supports wake up events from the PS/2 keyboard and mouse. **Note:** ACPI is not currently supported.

The EM440 supports automatic power on/off control when used with a standard ATX power supply. This allows the user to configure the board to always power on or to wait for the power button to be pressed. Configuration is set through the BIOS setup "power" tab screen. The EM440 will retain the configuration as long as the onboard button cell battery is functional.

If the onboard battery is not fitted then the board will always power on.

3.5. PCI Bus Implementation And Devices

The EM440 Baseboard implements a 3.3V, 32 bit primary PCI bus & supports 5V add in PCI cards. The bus runs at 33 MHz and has the 82443BX as the central resource. The primary PCI bus will have at most seven peripherals connected to it: a host/PCI-AGP bus bridge, a PCI/ISA bridge, a VGA controller, and three expansion slots (one shared with ISA slot) for PCI add-in cards. The VGA controller will be a build time option for EM440 Baseboard. One of the PCI slots has support for an ATX Riser card which can have 1 to 3 PCI slots.
A previous section describes the host/PCI bus and the PCI/ISA bridge components.
A description of the on-board devices and their PCI configuration space appears in Table 14 on page 17. The IDSEL pin on each of the devices connect to the listed PCI address pin. In order to select the configuration registers of a given device, a PCI Configuration Space access must be made with the device's corresponding IDSEL address bit set.

3.5.1 PCI ATX Riser Card Slots

PCI Slot 3 (next to the AGP connector) has the capability to have an ATX Riser card inserted. This can support up to 3 PCI card slots mounting the PCI cards horizontally. These slots are mutually exclusive with the onboard PCI and ISA slots.

Slot No.	IDSEL	PIRQ0	PIRQ1	PIRQ2	PIRQ3
Board 2	20	D	A	B	C
Board 3	21	C	D	A	B
Board 4	22	B	C	D	A
Riser 1	27	B	C	D	A
Riser 2	29	C	D	A	B
Riser 3	31	D	A	B	C

Table 7. ATX RISER SLOT ASSIGNMENTS

The ATX Riser connector specification has two Riser identification pins. These are connected to the PIIX4E GPI15 & GPI16 inputs. The following table shows the riser card type as indicated by the ID pins.

RISER_ID2	RISER_ID1	RISER TYPE
0	0	3 Slot Riser
0	1	2 Slot Riser
1	0	Other
1	1	No Riser Fitted

Table 8. ATX Riser ID type

3.5.2 VGA controller

A Chips and Technology B69030 64-bit GUI and video-accelerated controller is used to implement a high performance CRT video interface via the P2 connector.
The controller will support the following non-interlaced video resolutions on the CRT.

SCREEN FORMAT (PIXELS)	NO. OF COLORS	REFRESH RATES (HZ)	MEMORY REQUIRED
640x480	256	60, 75, 85	300KB
640x480	65,535	60, 75, 85	600KB
640x480	16.8 Million	60, 75, 85	900KB
800x600	65,535	60, 75, 85	960KB
800x600	16.8 Million	60, 75, 85	1.44MB
1024x768	256	60, 75, 85	786KB
1024x768	65,535	60, 75, 85	1.57MB
1024x768	16.8 Million	60, 75	2.36MB
1280x1024	256	60, 75	1.31MB
1280x1024	65,535	60, 75	1.62MB
1600x1200	256	60	1.92MB
1600x1200	65,535	60	3.84MB

Table 9. Available Video Resolutions

3.5.2.1 Video DRAM

The 69030 comes integrated with 4MB of high performance SDRAM onboard the video controller. This eliminates the need for any external video memory modules. A 4 MB DRAM frame buffer is implemented which allows 16-bit color at 1600 x 1200 resolutions.

3.5.3 PCI Expansion Slots

Three standard PCI card edge connectors (one shared) will be on the EM440 for installing PCI add-in boards. Slot 2 has support for ATX Riser card expansion.

The slot references are described here are for compatibility with the EMB1 product. The table following shows how the slot are numbered compared to the standard numbering schemes.

CPU nr slot1	1-AGP	2-PCIw/Riser	3-PCI	4-PCI/ISA	5-ISA	6-ISA	7-ISA
CPU nr slot7	7-AGP	6-PCIw/Riser	5-PCI	4-PCI/ISA	3-ISA	2-ISA	1-ISA
EM440 slots	1-AGP	2-PCIw/Riser	3-PCI	4-PCI/ISA	5-ISA	6-ISA	7-ISA
EMB1 slots	AGP	3-PCIw/Riser	2-PCI	1-PCI/4-ISA	3-ISA	2-ISA	1-ISA

Table 10. Slot Assignment Clarification

3.6. ISA Bus Implementation And Devices

The PIIX4E chip drives most of the ISA bus directly. The BIOS ROM, National 87309 Super I/O and four expansion slots (one shared) for ISA add-in cards are connected to the ISA bus. The 82371EB PIIX4E chip incorporates a fully ISA bus compatible master and slave interface, and is capable of directly driving the four ISA slots without external data buffers. The ISA interface also provides byte swap logic, I/O recovery support, wait state generation and SYSCLK generation.

3.6.1 FLASH Boot Device

The EM440 uses a Micron 28F400B5-T part for the BIOS ROM. The following are characteristics of this component and its implementation:

- Smart 5 Boot Block Flash memory device
- 4 Mbit part (512Kbyte)
- 48 pin TSOP package
- A jumper on the EM440 will allow (when installed) the 16KB Boot Block region of the Flash device to be written
- A jumper on the EM440 will allow (when installed) the FBD to be Crisis Recovered from the serial port.

The PIIX4E provides the control signals to the 28F400B5-T.

3.6.2 Super I/O

The National PC87309VLJ Super I/O controller provides floppy controller, parallel port, serial port, and PS/2 keyboard/mouse interface.

3.6.2.1 Floppy Disk

The floppy signals connect to a header on the EM440 allowing ribbon cable connection of a floppy disk drive. The device is accessed at the standard PC I/O addresses of 3F0h-3F7h and interrupts are signaled on IRQ6.

3.6.2.2 Parallel Port

One IEEE1284 parallel port is provided. The port can be configured to run in standard mode, enhanced mode (EPP) or Microsoft high speed mode (ECP). MSDOS and Windows recognizes this port as LPT1. LPT1 is compliant with the IEC1000-4-2 specification.

3.6.2.3 Serial Ports

Two serial ports that are RS-232 compatible are provided. The Super I/O chip includes 16C550 compatible UARTs with separate send and receive 16-byte FIFOs. The COM1 port is configured at I/O addresses 3F8-3FFh and uses IRQ4. The COM2 port is configured at I/O addresses 2F8-2FFh and uses IRQ3. The Super I/O chip allows relocation of these ports to the COM3 and/or COM4 standard I/O addresses, respectively. If so configured, COM3 and COM4 use I/O addresses 3E8-3EFh and 2E8-2Efh respectively. If not needed, these serial ports can be disabled in the BIOS setup screen to free the I/O address and interrupt for usage by other expansion products. COM1 is connected to a 9-pin D-Sub serial port connector located in the I/O shield. COM2 is connected to a 2X5 pin header on the EM440. External access to COM2 can be achieved through a cable connected to the 2X5 pin header and a serial connector mounted in one of the EM440's expansion slot openings.

3.6.2.4 Keyboard and Mouse controller

A keyboard port and mouse port are provided. The Super I/O keyboard controller is functionally equivalent to the industry standard 8042A controller . It is located at I/O locations 60-64h. The keyboard interrupt connects to IRQ1. If enabled, the mouse interrupt utilizes IRQ12.

3.6.3 ISA Expansion Slots

Four standard ISA card edge connectors (one shared) will be on the EM440 for installing ISA add-in boards. The slots are numbered as slot1 from the edge of the board.

3.7. Clocks

CPU, PCI and ISA device clock generation will be accomplished using a Pericom PI6C103 clock generator. A Pericom PI6C182 clock buffer will be used for the SDRAM clocks and the AGP clock will be generated by the 82443BX. A description of each is as follows:

3.7.1 Pericom PI6C03 Clock Generator

The Pericom PI6C103 clock generator is a high-speed low-noise device using a 14.31818MHz reference crystal that supports CPU and chipset clock frequencies of 66.6 and 100 MHz. The device outputs multiple clocks of which two have fixed frequencies of 14.31818MHz and one with a fixed frequency of 48MHz. A fourth clock output frequency can be configured as either 24MHz or 48MHz and will be configured as a 48MHz on the EM440.
EM440 clocks being provided by the generator are as follows:

Clock Name	# of lines	Frequency	Voltage
CPUCLK	2	66.66/100MHz	2.5
PCICLK	6	33.33MHz	3.3
48MHz	2	48MHz	3.3
REF	2	14.31818MHz	3.3

Table 11. Clock Frequencies

3.7.2 Pericom PI6C182 Clock Buffer

A 28 pin Pericom PI6C182 clock buffer uses the SDRAM reference clock output from the 82443BX to create the clocks needed to drive the SDRAM modules (4 per DIMM connector) and the 2 feedback clocks to the 82443BX. These feedback clocks allow adjustment of the SDRAM reference clock output of the 82443BX. Disabling unused outputs of the clock buffer is possible, by BIOS, via an I2C interface.

3.7.1 AGP Clock

The 66MHZ AGP clock output of the 82443BX will be used to drive the clock signal to a AGP compliant device attached to the EM440 AGP connector.

3.8. Port 80 Access

Installing a PCI Port 80 card into one of the PCI connectors of the EM440 will provide Port 80 access.

4. System Resource Details

4.1. System Memory Map

After the BIOS POST has been completed, the physical addresses from the CPU are mapped into memory according to the following table. All shadowed BIOSes are write protected by the BIOS.

Some devices that may claim PCIbus memory space are listed in this section. The system BIOS and/or operating system drivers dynamically allocate these devices.

Range	CPU address	Region	Cached
0 to 640K	00000000-0009FFFF	System DRAM	yes
640K to 768K	000A0000-000BFFFF	VGA memory window	no
768K to 816K	000C0000-000CBFFF	Shadowed VGA BIOS	yes
816K to 832K	000CC000-000CFFFF	USB Buffer Area	yes
832K to 896K	000D0000-000DFFFF	ISA bus or UBE	yes
896K to 1M	000E0000-000FFFFF	Shadowed System ROM BIOS	yes
1M to 16M (ISA limit)	00100000-00FFFFFF	DRAM or PCI or ISA	yes no
16M to 64M (cache limit)	01000000-03FFFFFF	DRAM or PCI	yes no
64M to Top of Memory (512M)	04000000-07FFFFFF	DRAM or PCI	no no
4G - 1M to 4G	FFF00000-FFFFFFFF	1MB 28F800B5-T FBD	no

Table 12. Memory Map

4.2. System I/O Map

The following registers are accessible in the I/O space. Some compatibility aliasing of PC compatibility registers exists as well, which is not listed here.

The addresses 0x0279 and 0x0A79 are reserved for ISA Plug and Play compatibility.

Port Address	Functional group	R/W	Usage	Access from	Decode by
0000	DMA Controller 1	R/W	DMA 1 Channel 0 address	PCI	PIIX4E
0001		R/W	DMA 1 Channel 0 count	PCI	PIIX4E
0002		R/W	DMA 1 Channel 1 address	PCI	PIIX4E
0003		R/W	DMA 1 Channel 1 count	PCI	PIIX4E
0004		R/W	DMA 1 Channel 2 address	PCI	PIIX4E
0005		R/W	DMA 1 Channel 2 count	PCI	PIIX4E
0006		R/W	DMA 1 Channel 3 address	PCI	PIIX4E
0007		R/W	DMA 1 Channel 3 count	PCI	PIIX4E
0008		R W	DMA 1 Command DMA 1 Status	PCI PCI	PIIX4E
0009		W	DMA 1 Write Request	PCI	PIIX4E
000A		W	DMA 1 Single Mask Bit	PCI	PIIX4E
000B		W	DMA 1 Write Mode	PCI	PIIX4E
000C		W	DMA 1 Clear byte pointer	PCI	PIIX4E
000D		W	DMA 1 Master clear	PCI	PIIX4E
000E		W	DMA 1 Clear Mask	PCI	PIIX4E
000F		R/W	DMA 1 Read/write all mask register bits	PCI	PIIX4E

Port Address	Functional group	R/W	Usage	Access from	Decode by
0020	Interrupt Controller 1	R/W	INT 1 Control	PCI/ISA	PIIX4E
0021		R/W	INT 1 Mask	PCI/ISA	PIIX4E
0022	PCI Arbiter Control	R/W	PM2 Register Block	CPU	82443BX
0040	Timer/Counter	R/W	Counter 0 Count/Status	PCI/ISA	PIIX4E
0041		R/W	Counter 1 Count/Status	PCI/ISA	PIIX4E
0042		R/W	Counter 2 Count/Status	PCI/ISA	PIIX4E
0043		W	Command Mode	PCI/ISA	PIIX4E
0060	Keyboard Controller	R/W R	Data I/O register Reset Xbus IRQ12/M and IRQ1	PCI/ISA PCI/ISA	87309 PIIX4E
0061	NMI Status and Control	R W	NMI Status NMI Control	PCI PCI	PIIX4E
0064	Keyboard Controller	R W	Status Register Command Register	PCI/ISA PCI/ISA	87309
0070	Real-time clock, NMI	W	RTC Index Register = bits 6-0 NMI Enable = bit 7	PCI/ISA	PIIX4E
0071		R/W	RTC Data Register 0 seconds 1 seconds alarm 2 minutes 3 minutes alarm 4 hours 5 hours alarm 6 day of week 7 date of month 8 month 9 year A status A B status B C status C D status D E … FF NVRAM	PCI/ISA	PIIX4E
0080	DMA Controller 1	R/W	DMA Page (reserved)	PCI/ISA	PIIX4E
0081		R/W	DMA Channel 2 page register	PCI/ISA	PIIX4E
0082		R/W	DMA Channel 3 page register	PCI/ISA	PIIX4E
0083		R/W	DMA Channel 1 page register	PCI/ISA	PIIX4E
0084		R/W	DMA Page (reserved)	PCI/ISA	PIIX4E
0085		R/W	DMA Page (reserved)	PCI/ISA	PIIX4E
0086		R/W	DMA Page (reserved)	PCI/ISA	PIIX4E
0087		R/W	DMA Channel 0 page register	PCI/ISA	PIIX4E
0088	DMA Controller 2	R/W	DMA Page (reserved)	PCI/ISA	PIIX4E
0089		R/W	DMA Channel 6 page register	PCI/ISA	PIIX4E
008A		R/W	DMA Channel 7 page register	PCI/ISA	PIIX4E
008B		R/W	DMA Channel 5 page register	PCI/ISA	PIIX4E
008C		R/W	DMA Page (reserved)	PCI/ISA	PIIX4E
008D		R/W	DMA Page (reserved)	PCI/ISA	PIIX4E
008E		R/W	DMA Page (reserved)	PCI/ISA	PIIX4E
008F		R/W	DMA Low Page Register Refresh	PCI/ISA	PIIX4E
0092	Port 92	R/W	Port 92	PCI/ISA	PIIX4E
X094	VGA Controller	R/W	POS102 Access Control	PCI	PIIX4E
00A0	Interrupt Controller 2	R/W	INT 2 Control	PCI/ISA	PIIX4E
00A1		R/W	INT 2 Mask	PCI/ISA	PIIX4E
00B2	Advanced Power	R/W	Control	PCI	PIIX4E

Port Address	Functional group	R/W	Usage	Access from	Decode by
00B3	Management	R/W	Status	PCI	PIIX4E
00C0	DMA Controller 2	R/W	DMA 2 Channel 4 address	PCI	PIIX4E
00C2		R/W	DMA 2 Channel 4 count	PCI	PIIX4E
00C4		R/W	DMA 2 Channel 5 address	PCI	PIIX4E
00C6		R/W	DMA 2 Channel 5 count	PCI	PIIX4E
00C8		R/W	DMA 2 Channel 6 address	PCI	PIIX4E
00CA		R/W	DMA 2 Channel 6 count	PCI	PIIX4E
00CC		R/W	DMA 2 Channel 7 address	PCI	PIIX4E
00CE		R/W	DMA 2 Channel 7 count	PCI	PIIX4E
00D0		R W	DMA 2 Status DMA 2 Command	PCI	PIIX4E
00D2		W	DMA 2 Write Request	PCI	PIIX4E
00D4		W	DMA 2 Write Single Mask Bit	PCI	PIIX4E
00D6		W	DMA 2 Write Mode	PCI	PIIX4E
00D8		W	DMA 2 Clear Byte Pointer	PCI	PIIX4E
00DA		W	DMA 2 Master Clear	PCI	PIIX4E
00DC		W	DMA 2 Clear Mask	PCI	PIIX4E
00DE		R/W	DMA 2 Read/Write all register mask bits	PCI	PIIX4E
00F0	Coprocessor	W	Coprocessor Error	PCI/ISA	PIIX4E
X102	VGA Controller	R/W	POS102 Register	PCI	PIIX4E
X15C	Super I/O	R/W	Index Register	PCI/ISA	87309
X15D	Configuration	R/W	Data Register	PCI/ISA	87309
0170	Secondary IDE	R/W	Data	PCI	PIIX4E
0171		R/W	Error/Features	PCI	PIIX4E
0172		R/W	Sector Count	PCI	PIIX4E
0173		R/W	Sector Number	PCI	PIIX4E
0174		R/W	Cylinder Low	PCI	PIIX4E
0175		R/W	Cylinder High	PCI	PIIX4E
0176		R/W	Drive/Head	PCI	PIIX4E
0177		R/W	Status/Command	PCI	PIIX4E
01F0	Primary IDE	R/W	Data	PCI	PIIX4E
01F1		R/W	Error/Features	PCI	PIIX4E
01F2		R/W	Sector Count	PCI	PIIX4E
01F3		R/W	Sector Number	PCI	PIIX4E
01F4		R/W	Cylinder Low	PCI	PIIX4E
01F5		R/W	Cylinder High	PCI	PIIX4E
01F6		R/W	Drive/Head	PCI	PIIX4E
01F7		R/W	Status/Command	PCI	PIIX4E
X2F8	COM2 Serial Port	R W	Receiver buffer Transmitter buffer	PCI/ISA	87309
		R/W	Baud rate divisor latch (LSB)	PCI/ISA	87309
X2F9		R/W	Interrupt enable register	PCI/ISA	87309
		R/W	Baud rate divisor latch (MSB)	PCI/ISA	87309
X2FA		R W	Interrupt ID register FIFO Control register	PCI/ISA	87309
X2FB		R/W	Line control register	PCI/ISA	87309
X2FC		R/W	Modem control register	PCI/ISA	87309
X2FD		R	Line status register	PCI/ISA	87309
X2FE		R	Modem status register	PCI/ISA	87309
X2FF		R/W	Scratch Pad	PCI/ISA	87309
0374	Secondary IDE		Reserved	PCI	PIIX4E

Port Address	Functional group	R/W	Usage	Access from	Decode by
0375			Reserved	PCI	PIIX4E
0376		R/W	Alt Status/Device Control	PCI	PIIX4E
x378	LPT1 Parallel Port	R/W	Printer Data register	PCI/ISA	87309
x379		R W	Printer Status register Printer Status register (EPP only)	PCI/ISA	87309
x37A		R/W	Printer Control register	PCI/ISA	87309
x37B		R/W	EPP Address Port	PCI/ISA	87309
x37C		R/W	EPP Data Port 0	PCI/ISA	87309
x37D		R/W	EPP Data Port 1	PCI/ISA	87309
x37E		R/W	EPP Data Port 2	PCI/ISA	87309
x37F		R/W	EPP Data Port 3	PCI/ISA	87309
x3B4	VGA Controller	R/W	CRT Controller index (mono)	PCI	CT69000
x3B5		R/W	CRT Controller data (mono)	PCI	CT69000
x3BA		R W	Input Status Register 1 (mono) Feature control output (mono)	PCI	CT69000
x3C0	EGA Controller	W	Attribute controller Index/Data	PCI	CT69000
x3C1		R	Attribute controller Index/Data	PCI	CT69000
x3C2		R W	Input Status Register 0 Miscellaneous output	PCI	CT69000
x3C3		R/W	Motherboard Sleep	PCI	CT69000
x3C4		R/W	Sequencer Index	PCI	CT69000
x3C5		R/W	Sequencer Data	PCI	CT69000
x3C6		R/W R/W	Video DAC pixel mask Hidden DAC register	PCI	CT69000
x3C7		R W	DAC State Pixel address read mode	PCI	CT69000
x3C8		R/W	Pixel mask write mode	PCI	CT69000
x3C9		R/W	Pixel data	PCI	CT69000
x3CA		R	Feature control readback	PCI	CT69000
x3CC		R	Miscellaneous output readback	PCI	CT69000
x3CE		R/W	Graphics controller index	PCI	CT69000
x3CF		R/W	Graphics controller data	PCI	CT69000
x3D4	CGA Controller	R/W	CRT controller index (color)	PCI	CT69000
x3D5		R/W	CRT controller data (color)	PCI	CT69000
x3DA		R W	Input Status Register 1 (color) Feature Control (color)	PCI	CT69000
x3F0	Floppy Disk Controller	R	Status Register A	PCI/ISA	87309
x3F1		R	Status Register B	PCI/ISA	87309
x3F2		R/W	Digital Output Register	PCI/ISA	87309
x3F3		R/W	Tape Driver Register	PCI/ISA	87309
x3F4		R W	Main Status Register Data Rate Select Register	PCI/ISA	87309
x3F5		R/W	Data Register	PCI/ISA	87309
x3F6	Primary IDE	R/W	Alternate Status/Device Control	PCI/ISA	87309
x3F7		R W	Digital Input Register Configuration Control Register	PCI/ISA	87309

Port Address	Functional group	R/W	Usage	Access from	Decode by
03F8	COM1 Serial Port	R W	Receiver buffer Transmitter buffer	PCI/ISA	87309
		R/W	Baud rate divisor latch (LSB)	PCI/ISA	87309
03F9		R/W	Interrupt enable register	PCI/ISA	87309
		R/W	Baud rate divisor latch (MSB)	PCI/ISA	87309
03FA		R W	Interrupt ID register FIFO Control register	PCI/ISA	87309
X3FB		R/W	Line control register	PCI/ISA	87309
X3FC		R/W	Modem control register	PCI/ISA	87309
X3FD		R	Line status register	PCI/ISA	87309
X3FE		R	Modem status register	PCI/ISA	87309
X3FF		R/W	Scratch Pad	PCI/ISA	87309
04D0	Interrupt Controller 1	R/W	INTC-1Edge/Level Control	PCI/ISA	PIIX4E
04D1	Interrupt Controller 2	R/W	INTC-2Edge/Level Control	PCI/ISA	PIIX4E
x778	ECP registers	R/W	FIFO	PCI/ISA	87309
x779		R/W	Configuration Register B	PCI/ISA	87309
x77A		R/W	Extended Control Register	PCI/ISA	87309
0CF8 – 0CFB (Dword only)	PCI Configuration	R/W	Configuration Address Register	CPU	82443BX
0CFC – 0CFF		R/W	Configuration Data Register	CPU	82443BX

Table 13. System I/O Map

Note: Other I/O resources such as USB, Bus Master IDE, PM registers, and SM registers are dynamically configured at power on reset (POST).

4.3. PCI IDSEL & REQ#/GNT# Assignments

Peripheral	IDSEL #	Device #	Function #	INTx#	Arbitration Signals REQ#/GNT#
Intel BX443 North Bridge PCI Intel BX443 North Bridge AGP	AD11 AD12	0 1	0 0	- -	- -
PCI/ISA Bus bridge (PIIX4) PCI/ISA bridge IDE interface USB PM	AD18	7	 0 1 2 3	 D	PHLD# / PHLDA# directly from the BX443
Chips and Technology 69030	AD19	8	0	A	-
PCI Expansion Slot #1	AD20	9	0	D,A,B,C	0
PCI Expansion Slot #2	AD21	10	0	C,D,A,B	1
PCI Expansion Slot #3	AD22	11	0	B,C,D,A	2
ATX Riser Slot #1	AD27	16	0	B,C,D,A	2
ATX Riser Slot #2	AD29	18	0	C,D,A,B	1
ATX Riser Slot #3	AD31	20	0	D,A,B,C	0

Table 14. PCI Device Configuration

4.4. System Interrupt Assignments

The following table lists the signals that are connected to the 82C59 compatible Interrupt Controllers. An 'X' denotes a hardware default/typical DOS-compatible allocation. An 'x' denotes other possible connections under software control (i.e. CMOS Configuration, PnP, ACPI, etc). IRQs not allocated to a device are available for add-in cards.

Under some operating systems/drivers, the Serial port interrupts can be shared. Windows 9x does support this, while Windows NT 4.0 does not. Also, PCI interrupts should be able to be routed to the same IRQ, forcing the drivers to chain their interrupt handlers. All other interrupt sources cannot share interrupts with other devices.

	IRQ0	IRQ1	IRQ2	IRQ3	IRQ4	IRQ5	IRQ6	IRQ7	IRQ8	IRQ9	IRQ10	IRQ11	IRQ12	IRQ13	IRQ14	IRQ15	NMI
Timer	X																
Keyboard Controller		X															
Cascade interrupt input			X														
COM2				X	x												
COM1				x	X												
Floppy							X										
LPT1						x		X									
Real time clock									X								
Mouse													X				
Numeric Coprocessor														X			
Primary IDE															X		
Secondary IDE																X	
Memory Parity (Disabled)																	X
PIRQA (input to PIIX4E)				x	x	x	x	x		x	x	x	x		x	x	
PIRQB (input to PIIX4E)				x	x	x	x	x		x	x	x	x		x	x	
PIRQC (input to PIIX4E)				x	x	x	x	x		x	x	x	x		x	x	
PIRQD (input to PIIX4E)				x	x	x	x	x		x	x	x	x		x	x	

Table 15. IRQ Map

5. Electrical Details.

5.1. Reset Timings.

The following timing diagram shows the power up sequence for the EM440:

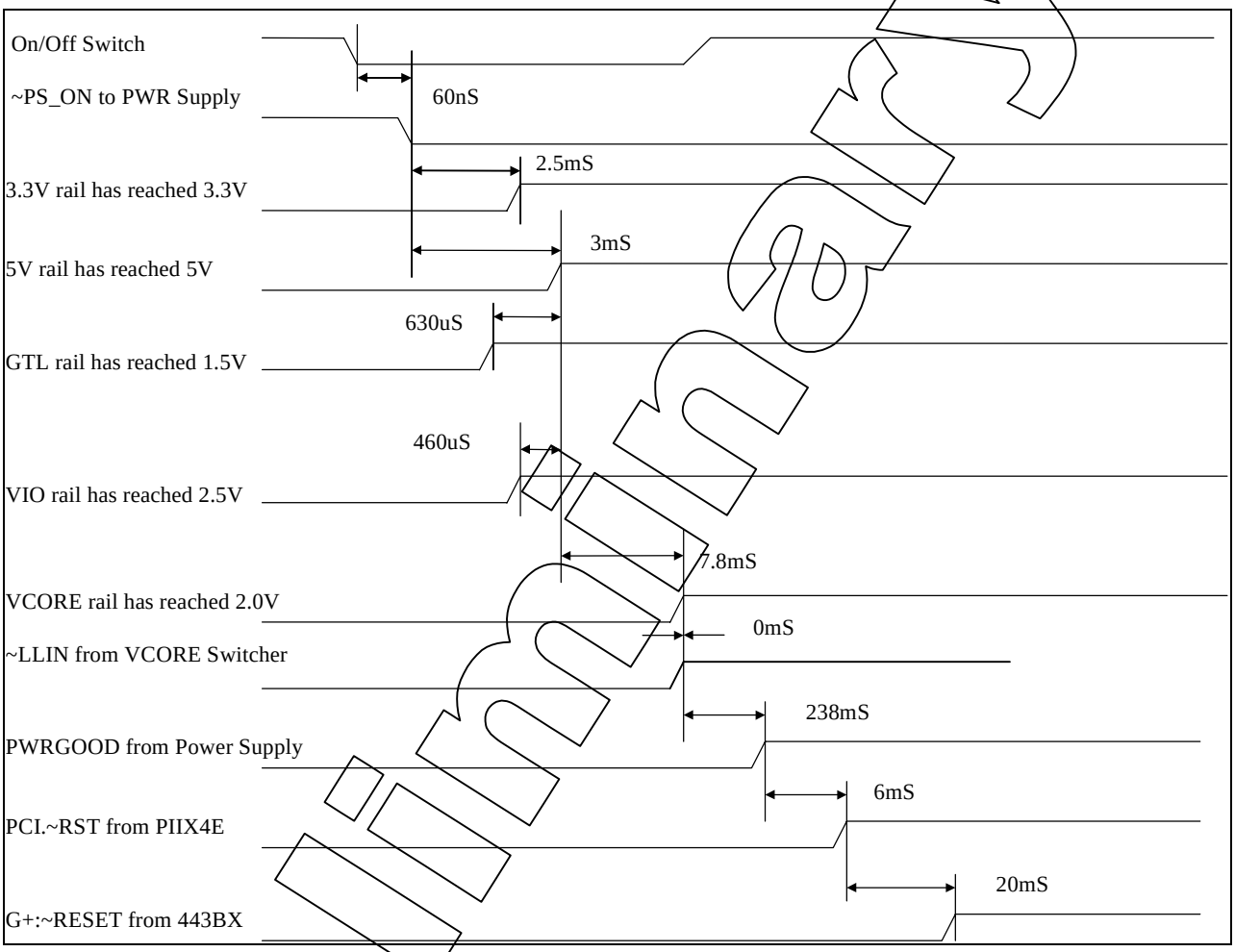

Figure 2. EM440 Reset Timings

5.2. EM440 Clock Trace Lengths

(This section of the specification will be filled in after the prototype PCB has taped out.)

5.2.1. Host Clock Trace Lengths

Series Termination: 22 Ohm series termination should be used for all host clocks. Clock skew between the 82443BX and the CPU can be reduced by tying the clock driver pins together at the clock chip and driving the CPU and 82443BX from this net with a 10 Ohm resistor at the driver for each. Trace lengths still match the specs defined below.

Layout guidelines: Match trace lengths to the longest trace.

Net	Trace length	Min	Max
Clock chip – CPU	H	1.0”	12.0”
Clock chip - 82443BX	H	1.0”	12.0”

5.2.2. PCI Clock Trace Lengths

Series Termination: 33 Ohm series termination are used for all PCI clocks.
Layout guidelines: Match trace lengths to the longest trace.

Net	Trace length	Min	Max
$PCLK:SLOT1..3	H + 4.8”	1.0”	12.5”
$PCLK:SLOT1R..3R	H + 2.3”	1.0”	10.0”
$PCLK:PIIX	H + 7.3”	1.0”	15.0”
$PCLK:BX	H + 7.3”	1.0”	15.0”
$PCLK:VGA	H + 7.3”	1.0”	15.0”

5.2.3. SDRAM Clock Trace Lengths

Series Termination: 33 Ohm series resistors are used for the SDRAM clocks between the CKBF and the DIMMs. For DCLKO (between 82443BX and CKBF), two termination resistors are used: A 43 Ohm series resistor located at the driver, and a 33 Ohm series resistor located at the receiver.
Layout guidelines:

Net	Trace Length	Min	Max	Cap
$DLKO	NA	1.0”	10.0”	NA
$SDRAM:CLK0..7	A	1.0”	3.0”	NA
$DCLKFB	A+2.5”	3.5”	5.5”	20pF

Note: A single clock output from CKBF is used to drive DCLKRD and DCLKWR at the 82443BX. The single clock net should be “T”d as close as possible to the 82443BX. An additional capacitive load of 20pF is also required. The capacitor should also be located as close to the 82443BX as possible.

5.2.4. AGP Clock Trace Lengths

Series Termination: 43 Ohm series termination is used for the AGP clocks.
Layout guidelines: The feedback clock trace length equals the typical clock motherboard trace length plus the card trace length.

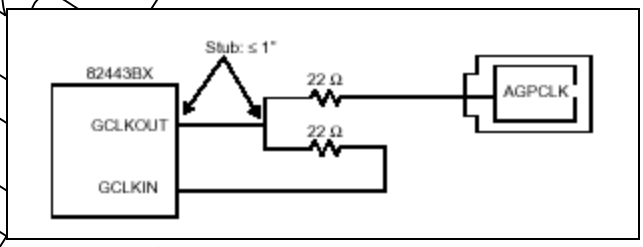

Figure 3. AGP Trace Layout

Net	Trace length	Min	Max	Card Trace Length
43 Ohm resistor - AGP connector	A	0.5”	12”	~3.3”
43 Ohm resistor - 82443BX (feedback)	A + 3.3”	0.5”	15.3”	NA

Note: One driver. The signal splits at the 82443BX, each half of the trace goes through a 43 Ohm resistor, and then to their respective loads. If the graphics chip is down on the motherboard, the trace length to the graphics chip and the feedback trace length to the 82443BX will both be the same length.

5.3. Voltage Supply Requirements

Some of the needed voltages are generated on the EM440 (including the CPU core, I/O voltage, & GTL+). This also has the advantage of closer regulation of the power. Enough capacitance should be installed on the motherboard near the power connector to avoid excessive droop in the power supplies. Capacitors with low ESR should be used near the power input points on the connector.

5.3.1. System Board Power Requirements

For reliable operation, the EM440 power supply will conform to the following specifications:

Voltage	Min	Normal	Max	Units	Tolerance
3.3 Volts	3.14	3.30	3.46	Volts	± 5%
5 Volts	4.75	5.00	5.25	Volts	± 5%
+12 Volts	11.40	12.00	12.60	Volts	± 5%
-12 Volts	-11.40	-12.00	-12.60	Volts	± 5%
-5 Volts	-4.75	-5.00	-5.25	Volts	± 5%

Table 16. Power Supply Tolerances

5.3.2. CPU Core Voltages.

The processors will select their own voltage using the VID0..4 signals from the VRM VCORE voltage.

5.3.3. General +5V Input Requirements.

In *addition* to supplying the processor core and I/O voltage regulators described previously, the EM440 needs +5V for several peripheral components: PC87309, PCI & ISA expansion slots, BIOS ROM, and some logic ICs.

5.3.4. General +3.3V Input Requirements.

The EM440 Baseboard requires +3.3V for the following components: 82443BX, PIIX4E, SDRAM, and 69030 video controller.

5.3.5. EM440 Power Estimate.

The following table contains the estimated power consumption of the EM440. It should be used to determine an appropriate power supply for the ATX system.

	EMB 1 Current (A)					
Device	**-12V**	**+12V**	**+5V**	**+3.3V**	**5VSB**	
Processor (366/66MHz)			6.49			
Processor (600/100MHz)			6.07			
82443BX				0.61		
PIIX4E				0.16		
C&T 69030 Video Ctlr				0.12		
SDRAM (256Meg)(66MHz)				2.34		
SDRAM (256Meg)(100MHz)				2.62		
Baseboard	0.15	0.75	1.47	0.35	0.08	
Total Current A(366/66+Vid)	0.15	0.75	7.96	3.58	0.08	
Total Current A(600/100+Vid)	0.15	0.75	7.54	3.86	0.08	Total
Total Power W(366/66+Vid)	1.80	9.00	39.81	11.80	0.40	62.81 W
Total Power W(600/100+Vid)	1.80	9.00	37.70	12.74	0.40	61.64 W

Table 17. Estimated EM440 Power Usage

Measured:____ ___W

5.4. PIIX4E General Purpose Inputs and Outputs Usage .

The PIIX4E provides a large number of general purpose inputs and outputs. The following table shows those that are used by the EM440 board.

Inputs (GPI's)	EM440 USE	Outputs (GPO's)	EM440 USE
GPI0/~IOCHK	10K PU	GPO0	NC
GPI1	10K PU	GPO1/LA17	**LA17**
GPI2/~REQA	10K PU	GPO2/LA18	**LA18**
GPI3/~REQB	10K PU	GPO3/LA19	**LA19**
GPI4/~REQC	10K PU	GPO4/LA20	**LA20**
GPI5/~APICREQ	10K PU	GPO5/LA21	**LA21**
GPI6/~IRQ8	10K PU	GPO6/LA22	**LA22**
GPI7/SERIRQ	10K PU	GPO7/LA23	**LA23**
GPI8/~THRM	10K PU	GPO8	**IMALIVE**
GPI9~BATLOW	10K PU	GPO9/~GNTA	NC
GPI10/~LID	10K PU	GPO10/~GNTB	NC
GPI11/~SMBALERT	10K PU	GPO11/~GNTC	NC
GPI12/~RI	10K PU	GPO12/~APICACK	NC
GPI13	10K PU	GPO13/~APICCS	**AUTO_ON**
GPI14	**~HARDPWR**	GPO14/IRQ0	**PS_ON**
GPI15	**Riser_ID1**	GPO15/~SUSB	NC
GPI16	**Riser_ID2**	GPO16/~SUSC	NC
GPI17	10K PU	GPO17/~CPU_STP	NC
GPI18	10K PU	GPO18/~PCI_STP	NC
GPI19	10K PU	GPO19/ZZ	NC
GPI20	**~FRCREC**	GPO20/~SUSSTAT1	**~SUSSTAT1**
GPI21	**~LOOPBIOS**	GPO21/~SUSSTAT2	NC
		GPO22/~XDIR	**~XDIR**
		GPO23/~XOE	**~XOE**
		GPO24/~RTCCS	NC
		GPO25/~RTCALE	NC
		GPO26/~KBCCS	NC
		GPO27	NC
		GPO28	NC
		GPO29/IRQ9OUT	NC
		GPO30	NC

Table 18. PIIX4E GPIO Usage

6. Connector Descriptions:

6.1. EM440 Main Power Connector

EM440 Main Power Connector – Foxconn HM20100-P2 (or equivalent) RadiSys PN 97-0196-00			
Pin	**Signal**	**Pin**	**Signal**
1	+3.3VDC	11	+3.3VDC/sense
2	+3.3VDC	12	-12VDC
3	GND	13	GND
4	+5VDC	14	PS_ON#
5	GND	15	GND
6	+5VDC	16	GND
7	GND	17	GND
8	PWR_OK	18	-5VDC
9	+5VSB	19	+5VDC
10	+12VDC	20	+5VDC

Table 19. EM440 Main Power Connector

6.2. Manufacturing Header

Manufacturing Header – Foxconn HC1905G (or equivalent) RadiSys PN 97-0119-00			
Pin	**Signal**	**Pin**	**Signal**
1	IMALIVE	2	GND
3	VCC	4	~LLIN
5	~FRCREC	6	GND
7	GND	8	WE_BB
9	GND	10	~LOOPBIOS

Table 20. Manufacturing Header

6.3. Hard/Soft Switch PSU Header

Manufacturing Header – Foxconn HC1103G (or equivalent) RadiSys PN 97-0259-00			
Pin	**Signal**	**Pin**	**Signal**
1	5VSB	2	5VSB_PS
3	VCC	4	NC
5	~HDSW (GPIx)	6	GND

Table 21. Hard/Soft PSU Header

For Hard switch mode use jumpers 1-3 and 5-6.
For Soft switch mode use jumpers 1-2 and 4-6

Pin 5 can be read by software to determine what type of supply is configured. Currently there is no BIOS support for this.

6.4. Processor Fan Header

Processor Fan Header – Foxconn HF06031 (or equivalent) RadiSys PN 97-0162-00	
Pin	**Signal**
1	GND
2	+12VDC*
3	NC

Table 22. Processor Fan Header

*Pin 2 can be configured to be +5V by changing the location of a resistor. This is a manufacturing build change.

6.5. Front Panel Header

Front Panel Header – Foxconn HB11293-KUB (or equivalent) RadiSys PN 97-1800-00		
Pin	**Signal**	**Function**
1	GND	Chassis Fan
2	+12VDC	
3	GND	
4	GND	System Reset
5	Reset Signal	
6	Key	System On LED
7	System On LED PWR	
8	Key	
9	GND	
10	Key	
11	HD LED PWR	HD Activity LED
12	HD ACT#	
13	Key	
14	HD LED PWR	
15	SW_ON	System On Switch
16	GND	
17	NC	
18	NC	
19	Key	
20	NC	
21	Key	
22	NC	
23	NC	
24	NC	
25	NC	
26	SPKR_DAT	External Speaker
27	SPKR_DAT	
28	Key	
29	GND	

Table 23. Front Panel Header

6.6. IDE HDD Connectors

6.6.1. Primary IDE HDD Connector

Primary IDE HDD Connectors – Foxconn HL07207-D2 (or equivalent) RadiSys PN 97-0188-00			
Pin	**Signal**	**Pin**	**Signal**
1	IDEP:RST	2	GND
3	PIDE:D7	4	PIDE:D8
5	PIDE:D6	6	PIDE:D9
7	PIDE:D5	8	PIDE:D10
9	PIDE:D4	10	PIDE:D11
11	PIDE:D3	12	PIDE:D12
13	PIDE:D2	14	PIDE:D13
15	PIDE:D1	16	PIDE:D14
17	PIDE:D0	18	PIDE:D15
19	GND	20	NC
21	PIDE:DRQ	22	GND
23	PIDE:~IOW	24	GND
25	PIDE:~IOR	26	GND
27	PIDE:IORDY	28	Cable Select
29	PIDE:~DAK	30	GND
31	AT:IRQ14	32	NC
33	PIDE:A1	34	NC
35	PIDE:A0	36	PIDE:A2
37	PIDE:~CS1	38	PIDE:~CS3
39	~HDACT	40	GND

Table 24. Primary IDE HDD Connector

6.6.2. Secondary IDE HDD Connector

Secondary IDE HDD Connectors – Foxconn HL02702-D2 (or equivalent) RadiSys PN 97-0188-00			
Pin	**Signal**	**Pin**	**Signal**
1	IDES:RST	2	GND
3	SIDE:D7	4	SIDE:D8
5	SIDE:D6	6	SIDE:D9
7	SIDE:D5	8	SIDE:D10
9	SIDE:D4	10	SIDE:D11
11	SIDE:D3	12	SIDE:D12
13	SIDE:D2	14	SIDE:D13
15	SIDE:D1	16	SIDE:D14
17	SIDE:D0	18	SIDE:D15
19	GND	20	NC
21	SIDE:DRQ	22	GND
23	SIDE:~IOW	24	GND
25	SIDE:~IOR	26	GND
27	SIDE:IORDY	28	Cable Select
29	SIDE:~DAK	30	GND
31	AT:IRQ15	32	NC
33	SIDE:A1	34	NC
35	SIDE:A0	36	SIDE:A2
37	SIDE:~CS1	38	SIDE:~CS3
39	~HDACT	40	GND

Table 25. Secondary IDE HDD Connector

6.7. Floppy Disk Drive Connector

Floppy Drive Connector – Foxconn HL16176-P0 (or equivalent) RadiSys PN 97-0176-00			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	FD:DENSEL
3	GND	4	NC
5	NC	6	FD:DRATE0
7	GND	8	FD:~INDEX
9	GND	10	FD:~MTR1
11	GND	12	FD:~DS1
13	GND	14	FD:~DS0
15	GND	16	FD:~MTR0
17	NC	18	FD:~DIR
19	GND	20	FD:~STEP
21	GND	22	FD:~WDATA
23	GND	24	FD:~WGATE
25	GND	26	FD:~TRK0
27	NC	28	FD:~WP
29	GND	30	FD:~RDATA
31	GND	32	FD:~HDSEL
33	GND	34	FD:~DSKCHG

Table 26. Floppy Drive Connector

6.8. AGP Connector

AGP Connectors – Foxconn EE06211-TM-3 (or equivalent) RadiSys PN 97-1801-00							
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
A1	12V	B1	OVERCNT#	A34	VDDQ3.3	B34	VDDQ3.3
A2	TYPEDET#	B2	5V	A35	AD22	B35	AD21
A3	RESERVED	B3	5V	A36	AD20	B36	AD19
A4	USB-	B4	USB+	A37	GND	B37	GND
A5	GND	B5	GND	A38	AD18	B38	AD17
A6	INTA#	B6	INTB#	A39	AD16	B39	C/BE2#
A7	RST#	B7	CLK	A40	VDDQ3.3	B40	VDDQ3.3
A8	GNT#	B8	REQ#	A41	FRAME#	B41	IRDY#
A9	3.3V	B9	3.3V	A42	RESERVED	B42	3.3Vaux
A10	ST1	B10	ST0	A43	GND	B43	GND
A11	RESERVED	B11	ST2	A44	RESERVED	B44	RESERVED
A12	PIPE#	B12	RBF#	A45	3.3V	B45	3.3V
A13	GND	B13	GND	A46	TRDY#	B46	DEVSEL#
A14	RESERVED	B14	RESERVED	A47	STOP#	B47	VDDQ3.3
A15	SBA1	B15	SBA0	A48	PME#	B48	PERR#
A16	3.3V	B16	3.3V	A49	GND	B49	GND
A17	SBA3	B17	SBA2	A50	PAR	B50	SERR#
A18	RESERVED	B18	SB_STB	A51	AD15	B51	C/BE1#
A19	GND	B19	GND	A52	VDDQ3.3	B52	VDDQ3.3
A20	SBA5	B20	SBA4	A53	AD13	B53	AD14
A21	SBA7	B21	SBA6	A54	AD11	B54	AD12
A22	KEY	B22	KEY	A55	GND	B55	GND
A23	KEY	B23	KEY	A56	AD9	B56	AD10
A24	KEY	B24	KEY	A57	C/BE0#	B57	AD8
A25	KEY	B25	KEY	A58	VDDQ3.3	B58	VDDQ3.3
A26	AD30	B26	AD31	A59	RESERVED	B59	AD_STB0
A27	AD28	B27	AD29	A60	AD6	B60	AD7
A28	3.3V	B28	3.3V	A61	GND	B61	GND
A29	AD26	B29	AD27	A62	AD4	B62	AD5
A30	AD24	B30	AD25	A63	AD2	B63	AD3
A31	GND	B31	GND	A64	VDDQ3.3	B64	VDDQ3.3
A32	RESERVED	B32	AD_STB1	A65	AD0	B65	AD1
A33	C/BE3#	B33	AD23	A66	RESERVED	B66	RESERVED

Table 27. AGP Connector

6.9. PCI Expansion Slot Connectors

PCI Expansion Slot Connectors – **Foxconn EH06001-GU-V (or equivalent)** RadiSys PN 97-0183-00							
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
A1	GND	B1	-12V	A32	AD16	B32	AD17
A2	+12V	B2	GND	A33	+3.3V	B33	C/BE2#
A3	+5V	B3	GND	A34	FRAME#	B34	GND
A4	+5V	B4	NC	A35	GND	B35	IRDY#
A5	+5V	B5	+5V	A36	TRDY#	B36	+3.3V
A6	INTA#	B6	+5V	A37	GND	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	GND
A8	+5V	B8	INTD#	A39	+3.3V	B39	LOCK#
A9	RESERVED	B9	NC	A40	+5V	B40	PERR#
A10	+5V (I/O)	B10	RESERVED	A41	+5V	B41	+3.3V
A11	RESERVED	B11	NC	A42	GND	B42	SERR#
A12	GND	B12	GND	A43	PAR	B43	+3.3V
A13	GND	B13	GND	A44	AD15	B44	C/BE1#
A14	+3.3V aux	B14	RESERVED	A45	+3.3V	B45	AD14
A15	RST#	B15	GND	A46	AD13	B46	GND
A16	+5V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	GND	A48	GND	B48	AD10
A18	GND	B18	REQ#	A49	AD9	B49	GND
A19	PME#	B19	+5V (I/O)	A50	KEY	B50	KEY
A20	AD30	B20	AD31	A51	KEY	B51	KEY
A21	+3.3V	B21	AD29	A52	C/BE0#	B52	AD8
A22	AD28	B22	GND	A53	+3.3V	B53	AD7
A23	AD26	B23	AD27	A54	AD6	B54	+3.3V
A24	GND	B24	AD25	A55	AD4	B55	AD5
A25	AD24	B25	+3.3V	A56	GND	B56	AD3
A26	IDSEL	B26	C/BE3#	A57	AD2	B57	GND
A27	+3.3V	B27	AD23	A58	AD0	B58	AD1
A28	AD22	B28	GND	A59	+5V (I/O)	B59	+5V (I/O)
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	GND	B30	AD19	A61	+5V	B61	+5V
A31	AD18	B31	+3.3V	A62	+5V	B62	+5V

Table 28. PCI Expansion Slot Connectors

6.9 PCI ATX Riser Connector

Foxconn EH01111-GL-V, Radisys P/N : 97-1806-00

Pin Name	Description	Pin Name	Description
A1	PCI_GNT1#	B1	GND
A2	GND	B2	PCI_CLK1
A3	PCI_GNT2#	B3	GND
A4	GND	B4	PCI_REQ1#
A5	PCI_CLK3	B5	GND
A6	RISER_ID1	B6	PCI_CLK2
A7	RESERVED	B7	GND
A8	RISE_ID2	B8	PCI_REQ2#
A9	NOGO	B9	GND
A10	+12V	B10	PC/PCI_DREQ#
A11	SER_IRQ	B11	PC/PCI_DGNT#

Table 29. ATX Riser Connector

6.10 ISA Expansion Slot Connectors

ISA Expansion Slot Connectors – Foxconn EQ04901-GB-N (or equivalent) RadiSys PN 97-0184-00			
Pin	**Signal**	**Pin**	**Signal**
A1	IOCHK#	B1	GND
A2	SD7	B2	RESET
A3	SD6	B3	+5V
A4	SD5	B4	IRQ9
A5	SD4	B5	-5V
A6	SD3	B6	DRQ2
A7	SD2	B7	-12V
A8	SD1	B8	SRDY#
A9	SD0	B9	+12V
A10	IOCHRDY	B10	GND
A11	AEN	B11	SMEMW#
A12	SA19	B12	SMEMR#
A13	SA18	B13	IOW#
A14	SA17	B14	IOR#
A15	SA16	B15	DACK3#
A16	SA15	B16	DRQ3
A17	SA14	B17	DACK1#
A18	SA13	B18	DRQ1
A19	SA12	B19	REFRESH#
A20	SA11	B20	BCLK
A21	SA10	B21	IRQ7
A22	SA9	B22	IRQ6
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	DACK2#
A27	SA4	B27	TC
A28	SA3	B28	BALE
A29	SA2	B29	+5V
A30	SA1	B30	OSC
A31	SA0	B31	GND
KEY		KEY	
C1	SBHE#	D1	MEMCS16#
C2	LA23	D2	IOCS16#
C3	LA22	D3	IRQ10
C4	LA21	D4	IRQ11
C5	LA20	D5	IRQ12
C6	LA19	D6	IRQ15
C7	LA18	D7	IRQ14
C8	LA17	D8	DACK0#
C9	MEMR#	D9	DRQ0
C10	MEMW#	D10	DACK5#
C11	SD8	D11	DRQ5
C12	SD9	D12	DACK6#
C13	SD10	D13	DRQ6
C14	SD11	D14	DACK7#
C15	SD12	D15	DRQ7
C16	SD13	D16	+5V
C17	SD14	D17	MASTER#
C18	SD15	D18	GND

Table 30. ISA Expansion Slot Connectors

6.11 Serial Port Connectors

6.11.1 COM1 Connector

COM1 Connector – Foxconn DM11353-BV5 (or equivalent) RadiSys PN 97-0107-00	
Pin	**Signal**
1	COM1:DCD
2	COM1:RXD
3	COM1:TXD
4	COM1:DTR
5	COM1:GND
6	COM1:DSR
7	COM1:RTS
8	COM1:CTS
9	COM1:RI

Table 31. COM1 Connector

6.11.2 COM2 Header

COM2 Header – Foxconn HL09051-P5 (or equivalent) RadiSys PN 97-0225-00			
Pin	**Signal**	**Pin**	**Signal**
1	COM2:DCD	2	COM2:DSR
3	COM2:RXD	4	COM2:RTS
5	COM2:TXD	6	COM2:CTS
7	COM2:DTR	8	COM2:RI
9	GND	10	Key (no pin fitted)

Table 32. COM2 Header

6.10. Dual USB Connector

Dual USB Connector – Foxconn UB1112C-81 (or equivalent) RadiSys PN 97-0151-00	
Pin	**Signal**
1	USB1_VCC (Fused)
2	DATA_1-
3	DATA_1+
4	USB1_GND
5	USB2_VCC (Fused)
6	DATA_2-
7	DATA_2+
8	USB2_GND

Table 33. Dual USB Connector

6.11. Parallel Port Connector

Parallel Port Connector – Foxconn DM11353-BV5 (or equivalent) RadiSys PN 97-0107-00	
Pin	**Signal**
1	STROBE#
2	PD0
3	PD1
4	PD2
5	PD3
6	PD4
7	PD5
8	PD6
9	PD7
10	ACK#
11	BUSY
12	PERROR
13	SELECT
14	AUDOFD#
15	FAULT#
16	INIT#
17	SLCTIN#
18-25	GND

Table 34. Parallel Port Connector

6.12. Keyboard/Mouse Connector

Keyboard/Mouse Connector – Foxconn MH11061-D2 (or equivalent) RadiSys PN 97-0203-00			
Keyboard		**Mouse**	
Pin	**Signal**	**Pin**	**Signal**
1	KB:DATA	1 (7)	M:DATA
2	NC	2 (8)	NC
3	KB:GND	3 (9)	M:GND
4	KB:VCC (Fused)	4 (10)	M:VCC (Fused)
5	KB:CLOCK	5 (11)	M:CLOCK
6	NC (GND)	6 (12)	NC (GND)

Table 35. Keyboard/Mouse Connector

6.13. VGA Connector

VGA Connector – Foxconn DM11353-BV5 (or equivalent) RadiSys PN 97-0107-00			
Pin	**Signal**	**Pin**	**Signal**
1	RED	9	NC
2	GREEN	10	GND
3	BLUE	11	NC
4	NC	12	MID1
5	GND	13	HSYNC
6	GND	14	VSYNC
7	GND	15	MID3
8	GND		

Table 36. VGA Connector

7. Mechanical Details

7.1. EM440 Board Dimensions

The EM440 is designed to fit into a standard ATX form-factor chassis. The motherboard's outer dimensions are 12 x 9.6 inches. Figure 4 shows the mechanical form factor, and mounting hole locations. All are in compliance with the ATX Specification - Version 2.03 **Note:** EM440 will have only 3 PCI expansion slots.

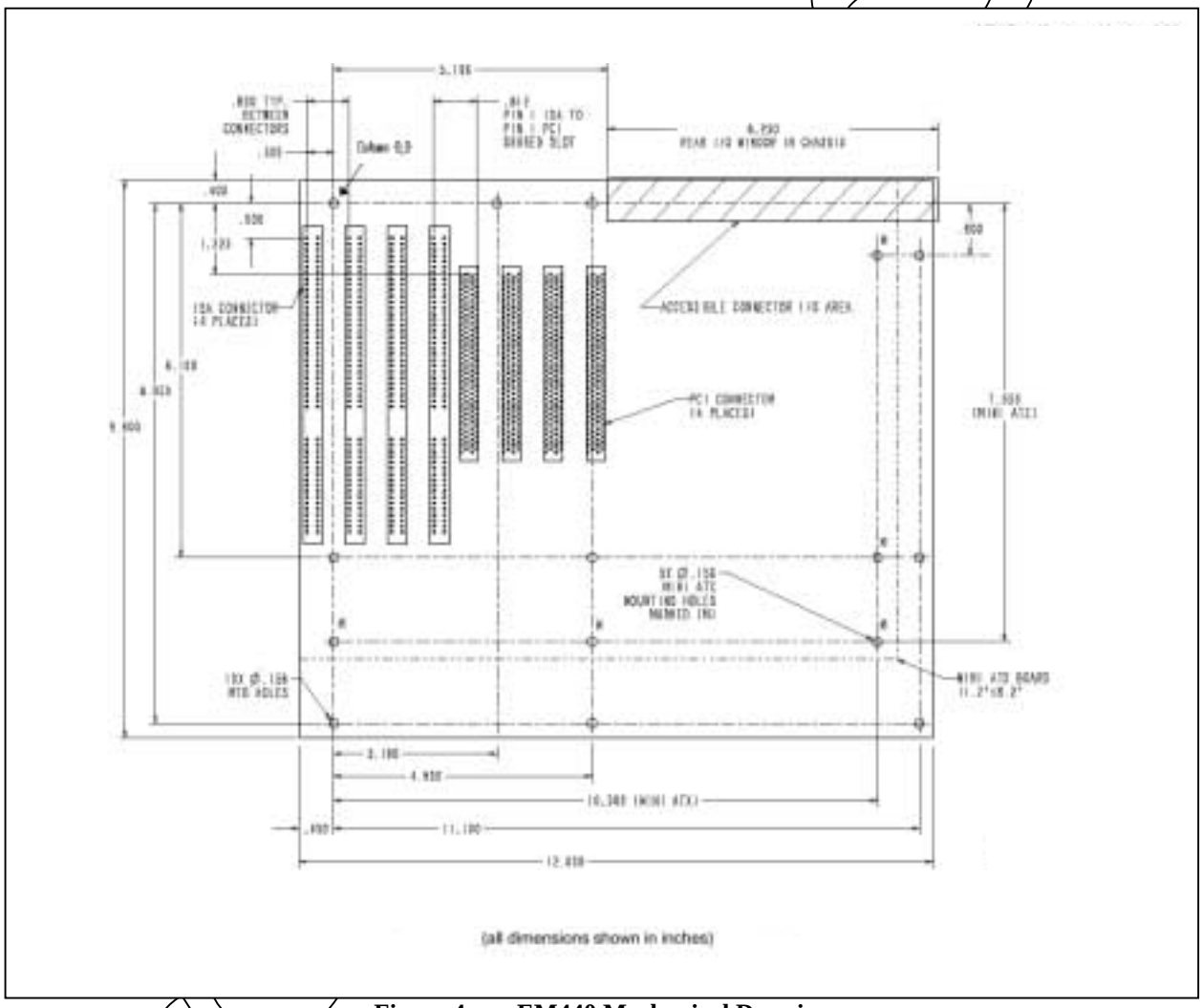

Figure 4. EM440 Mechanical Drawing

7.2. EM440 I/O Shield

The EM440 I/O shield is designed to fit into a standard ATX form-factor chassis. The I/O shields outer dimensions are 6.25 x 1.75 inches. Figure 5 shows the mechanical form factor, and I/O connector locations. There two I/O shields that can be ordered. With video or without video, these are shown below.

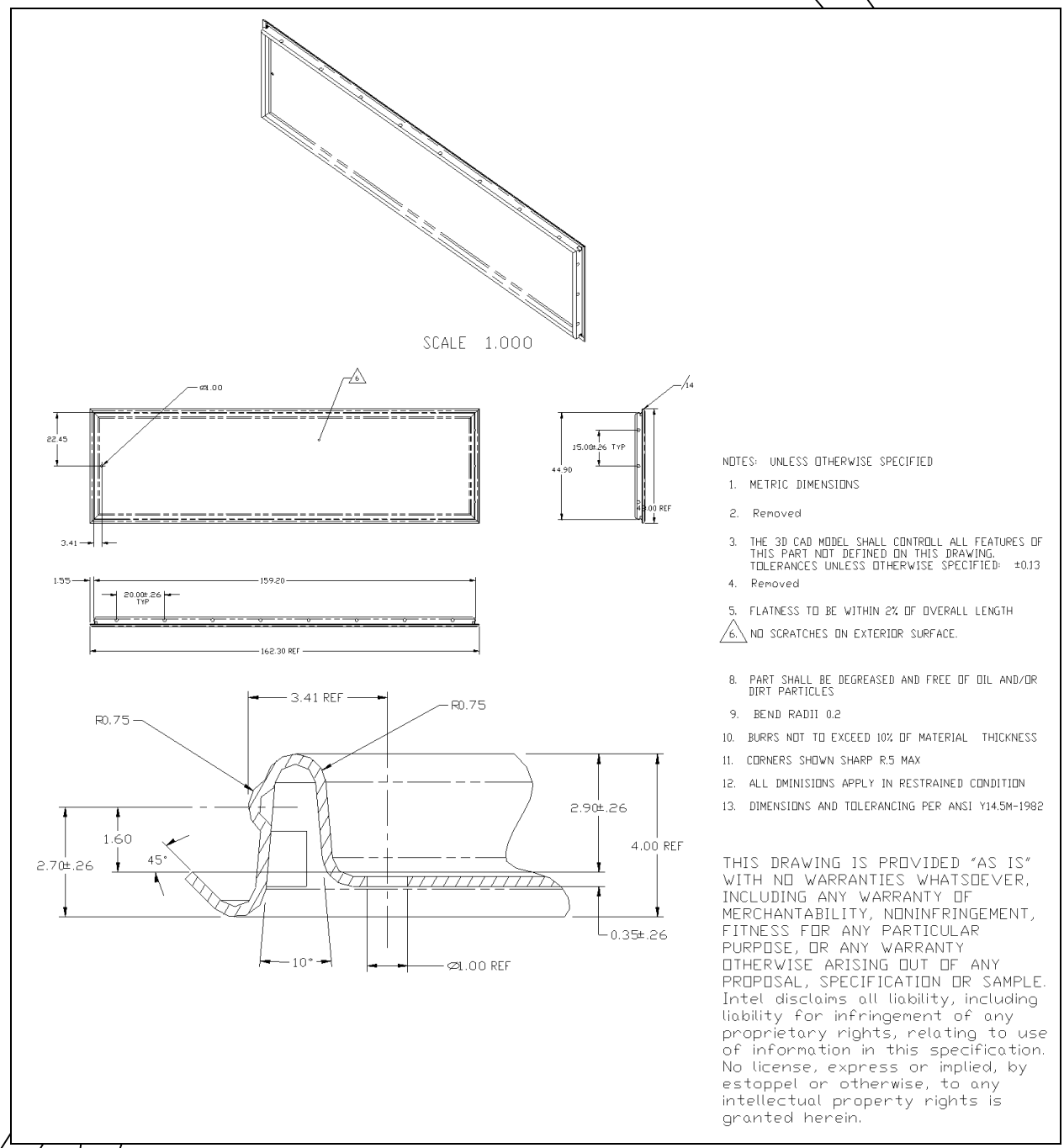

Figure 5. EM440 I/O Shield Drawing

Figure 6. I/O Shield EM440

The I/O shield for the without Video option is part number 97-7716-00

Figure 7. I/O Shield EM440V

The I/O shield for the with Video option is part number 97-7717-00

7.3. Thermal Solution

The thermal solution is an active(fan) heatsink that mounts to the Socket 7 housing. There are numerous manufacturers(AAVID, Wakefield, Thermalloy, etc..) for this heatsink. This heatsink contains a thermal "pad" which interfaces with processor "slug".

For restricted airflow solutions and customers requiring a higher operating environment then the 82443BX and 69030 devices will require heatsinks. These both can use the Radisys part number 97-7713-00 passive heatsink.

8. Environmental and EMC Specifications

Operating and Storage Specifications		
Temperature (Ambient)	Operating	0°C to 55°C with convection cooling 0°C to 70°C with external fan airflow
	Storage	-40°C to 70°C
Humidity	Operating/ storage	5-95% RH non-condensing
Vibration un-packaged	Operating Storage	0.04g²/Hz from 5-1000Hz random, 10 min. per sweep cycle sine wave cycle: 0.075mm displacement from 10-57Hz sine wave cycle: 1G from 57-150Hz 0.06g²/Hz from 5-1000Hz random, 10 min. per sweep cycle
Shock un-packaged	Operating Storage	30g, 11-ms duration, half sine shock pulse 50g, 11-ms duration, half sine shock pulse
Altitude	Operating	to 15,000 ft (4,500 m)
	Storage	to 40,000 ft (12,000 m)
ESD	Operating	EN55024 : 4KV direct contact, 8KV air discharge
EMC Specifications		
FCC Class B		NOTE: When correctly installed into a compatible system.
CISPR 22, 2nd Edition, 1993		NOTE: When correctly installed into a compatible system.

Table 37. EM440 Environmental Specifications