Minitower Pentium Handbuch

P5HX-A

User's Manual (for Award BIOS) V1.0

Table of Contents

Mainboard Description

P5HX-A is a Pentium PCI mainboard using Intel 430HX chipset (TXC, PIIX 3) and SMC 37C669, SMC 37C669FR I/O Chip. There are 4 ISA Bus slots and 4 PCI Bus slots.

1. Processor:

- Intel Pentiumä 75/90/100/120/133/150/166/200 MHz; Intel 125/150/166 MHz (P54CT) ; Intel 150/180/200 MHz (P54CTB) Intel 150/166 MHz (P55C) Cyrix 6X86 120+/133+/150+/166+ MHz

2. Chipset:

- Intel 430HX 82439HX (TXC) / 82371AB (PIIX3) SMC 37C669 / 37C669FR (SUPER I/O)

3. System BIOS:

- Award BIOS

4. L2 On-board Cache:

- Provide Pipleined Burst SRAM 256/512 KB
- On-board cache 256KB / 512KB

5. L2 Cache Module:

- An optional ECS "CM161" or later version of upgrade cache module can be inserted to expand the cache memory size to 256KB or 512KB. An "COAST 2.0" or later cache module can also be used to upgrade the cache memory size.

6. SIMM System Memory Socket:

- Support 72-pin SIMMs of 4MB, 8MB, 16MB ,32MB or 64MB to form a memory size between 8MB to 256MB

7. Expansion Slot:

- 4 ISA Bus Slots.
- 4 PCI Bus Slots. (One ISA-PCI Shared Slot)

8. PS/2 Mouse & Keyboard Set:

- Provide Connectors for PS/2 Keyboards & PS/2 Mouse.

9. Serial / Parallel Port:

- Provide two serial ports and one parallel port.

10. PCI IDE Connector:

- 2 Enhanced PCI IDE up to 4 IDE Device Connectors.

11. FDD Connector:

- Provide an on-board FDD Connector which supports 360KB/720KB/1.2MB/1.44MB/2.88MB type drives.

12. Power Supply Connectors:

- Provide the connectors for standard PC power supply or ATX power supply.

Features

CPU:

- One Socket 7 supports Pentium 75/90/100/120/133/150/166/200 MHz CPU with On-board Regulator and Intel Overdrive CPUs.
- Upgradable to Pentium 125/150/166 MHz (P54CT) and 150/180/200 MHz (P54CTB) CPUs.
- Support Intel 150/166 MHz (P55C)
- Support Cyrix M1 100/110/120/133 MHz CPU.

BIOS:

- Support Award BIOS with flash ROM

- PNP specification V1.0a

Cache:

- Support the CPU’s internal first level (L1) cache and external secondary level (L2) cache.
- > 16KB Level 1 Cache:
- Data Cache: support 8KB Write-Through and Write-Back policy.
- Code Cache: support 8KB Write-Through policy.
- > 256KB /512KB (optional) Pipelined Burst SRAM On Board.
- > 160-pin Cache Module Socket for Level 2:
- Support COAST 2.0 or later Pipelined Burst for 256KB or 512KB.

Memory:

- Support 4 pieces of 72-pin SIMM sockets with memory size from 4MB to 256MB.
- Support 64 MB DRAM Technology.
- Support EDO/ Fast Page Mode DRAM.

Slots:

- 4 16-bit ISA slots with 100% ISA compatible function.
- 4 32-bit PCI slots support PCI master.
- PCI specification version 2.1.
- CPU to PCI memory write posting with 4 word deep buffers.
- Converts Back-to-Back sequential CPU to PCI memory writes to PCI Burst writes.

FDD:

- Two floppy drives support 360KB, 720KB, 1.2MB, 1.44MB, 2.88MB, and 3 Mode floppy drives.

RTC:

- Use Dallas 12B887 compatible RTC module (Internal 128 byte of CMOS RAM).

IDE:

- Build-in Intel 430HX PCIset chip 32-bit PCI IDE interface with 2 IDE channels.
- Support up to PIO mode 4 timing or DMA mode 2 with transfer rate timing up to 22MB/sec.

System Memory

SIMM:

P5HX-A provides tremendous flexibility DRAM configurations. It accepts a maximum of 256MB memory size. The on-board DRAM is installed with SIMM (Single-In-line-Memory Module).

There are two memory banks which support the 4M/8M/16M/32M/64M type, single and/or double-density modules. The DRAM type of SIMM1 /SIMM2 is independent of SIMM3/SIMM4.

The type of SIMM1 and SIMM2 must be same if theyexist at the same time.

Cache Memory Subsystem

Level 1 Cache

- 16 KB Level 1 Cache that builds in Pentium CPU includes Data Cache and Code Cache.
- 1. Data Cache: supports 8KB Write-Through and Write-Back policy.
- 2. Code Cache: supports 8KB Write-Through policy.

Level 2 Cache

If there is an "On-board 256KB L2 Cache" in the motherboard, users may either upgrade to 512KB by inserting an ECS "CM161" or COAST (2.0 or later) upgrade cache module of 256KB. If there is not any "On-board 256KB L2 Cache" in the motherboard, users may either upgrade to 256KB or 512KB by inserting an ECS "CM161" or COAST (2.0 or later) upgrade cache module of 256KB or 512KB.

Slimline Pentium Handbuch

P5HX-A

Jumperbelegungen

Prozessortyp

Pentium 75	JP9, 1-2, 3-4, Short	JP7, 1-2, Short, JP8, 1-2, Short
Pentium 90	JP9, 3-4, Short	JP7, 1-2, Short, JP8, 1-2, Short
Pentium 100	JP9, 1-2, Short	JP7, 1-2, Short, JP8, 1-2, Short
Pentium 120	JP9, 3-4, Short	JP7, 1-2, Short, JP8, 2-3, Short
Pentium 133	JP9, 1-2, Short	JP7, 1-2, Short, JP8, 2-3, Short
Pentium 150	JP9, 3-4, Short	JP7, 2-3, Short, JP8, 2-3, Short
Pentium 166	JP9, 1-2, Short	JP7, 2-3, Short, JP8, 2-3, Short
Pentium 200	JP9, 1-2, Short	JP7, 2-3, Short, JP8, 1-2, Short

Cyrix 120+ (50MHzX2)	JP9, 1-2, 3-4, Short	JP8, 2-3, Short
Cyrix 133+ (55MHzX2)	JP9, Open	JP8, 2-3, Short
Cyrix 150+ (60MHzX2)	JP9, 3-4, Short	JP8, 2-3, Short
Cyrix 166+ (66MHzX2)	JP9, 1-2, Short	JP8, 2-3, Short

JP9	1-2	3-4	JP7	1-2	2-3	JP8	1-2	2-3
50MHz	Short	Short	INTEL X1.5	Short			Short	
60MHz	Open	Short	INTEL X2	Short				Short
66MHz	Short	Open	INTEL X2.5		Short			Short
55MHz	Open	Open	INTEL X3		Short		Short	
			CYRIX X2	Open	Open			Short
			CYRIX X3	Open	Open		Short	

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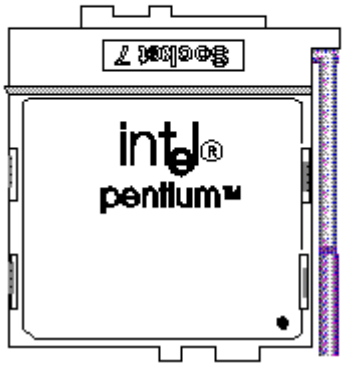
1. Intel Pentium 75MHz (P54C/P54CT/P54CTB) CPU (50MHz Host Clock) installed on board



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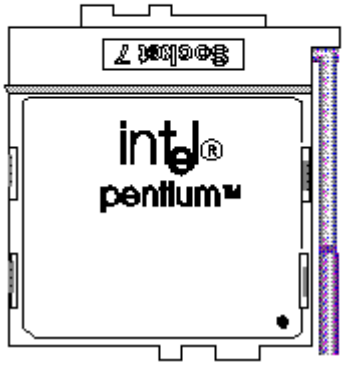
2. Intel Pentium 90MHz (P54C/P54CT/P54CTB) CPU (60MHz Host Clock) installed on board



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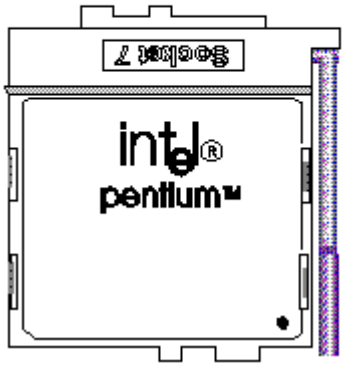
3. Intel Pentium 100MHz (P54C/P54CT/P54CTB) CPU (66MHz Host Clock) installed on board



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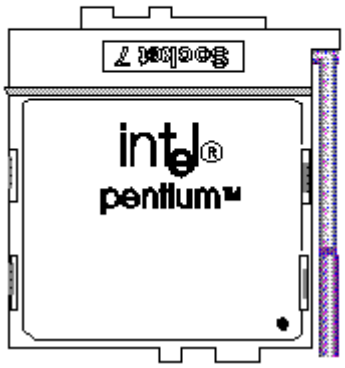
4. Intel Pentium 120MHz (P54C/P54CT/P54CTB) CPU (60MHz Host Clock) installed on board



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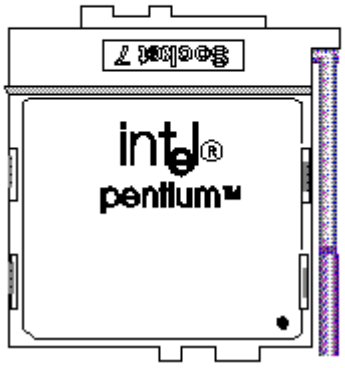
5. Intel Pentium 133MHz (P54C/P54CT/P54CTB) CPU (66MHz Host Clock) installed on board



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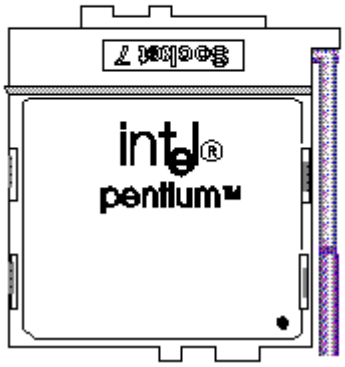
6. Intel Pentium 150MHz (P54C/P54CT/P54CTB) CPU (60MHz Host Clock) installed on board



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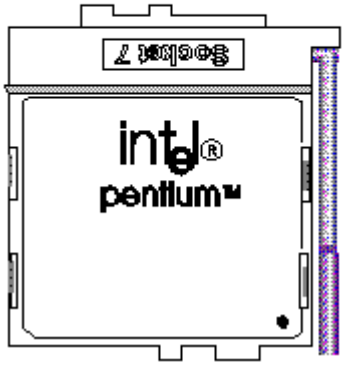
7. Intel Pentium 166MHz (P54C/P54CT/P54CTB) CPU (66MHz Host Clock) installed on board



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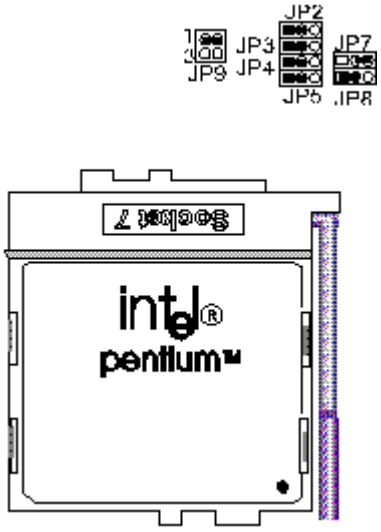
8. Intel Pentium 200MHz (P54C/P54CT/P54CTB) CPU (66MHz Host Clock) installed on board



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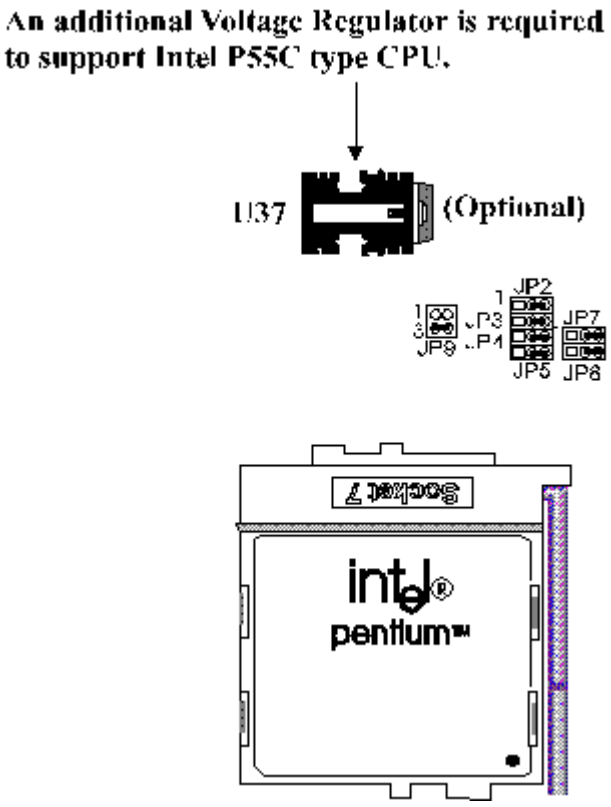
9. Intel Pentium 150MHz (P55C) CPU (60MHz Host Clock) installed on board



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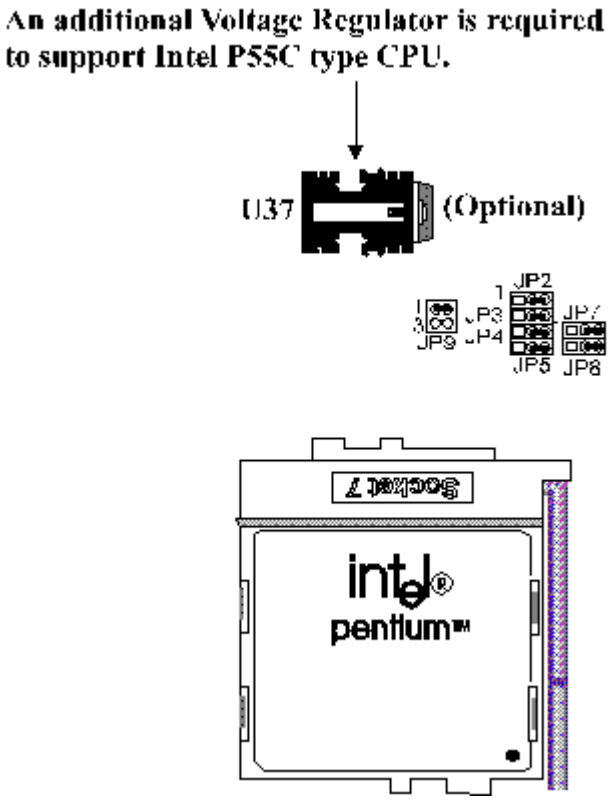
10. Intel Pentium 166MHz (P55C) CPU (66MHz Host Clock) installed on board



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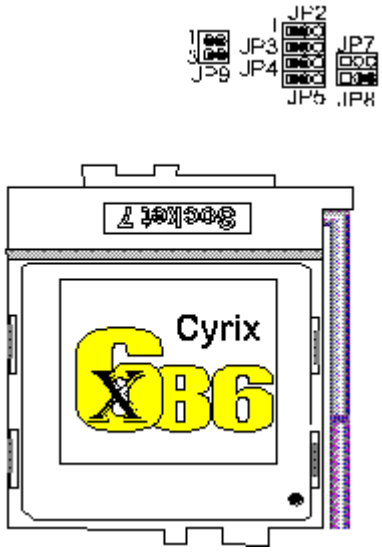
11. Cyrix 6X86 100MHz CPU (50MHz Host Clock) installed on board



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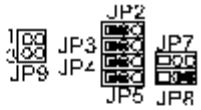
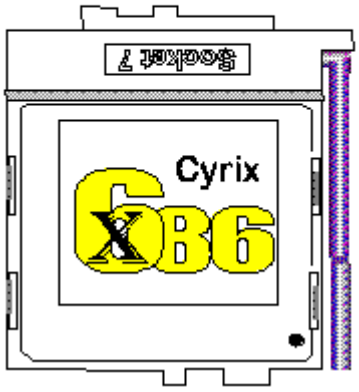
12. Cyrix 6X86 110MHz CPU (55MHz Host Clock) installed on board





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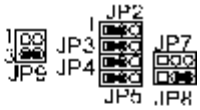
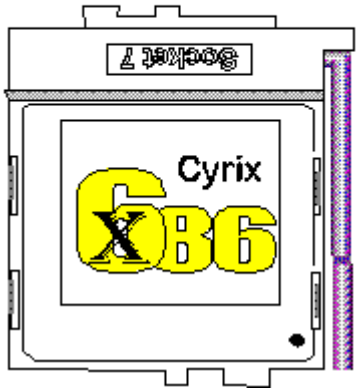
13. Cyrix 6X86 120MHz CPU (60MHz Host Clock) installed on board





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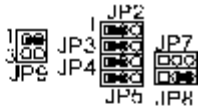
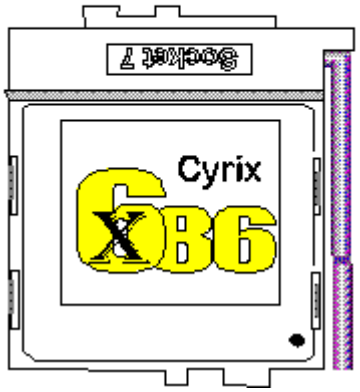
14. Cyrix 6X86 133MHz CPU (66MHz Host Clock) installed on board





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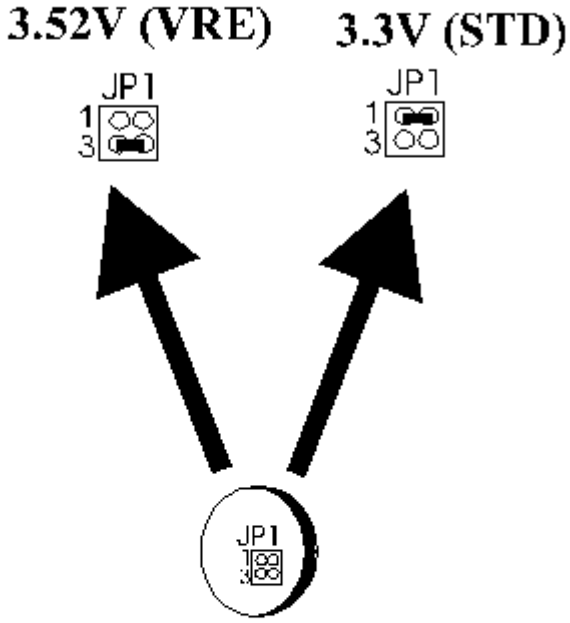
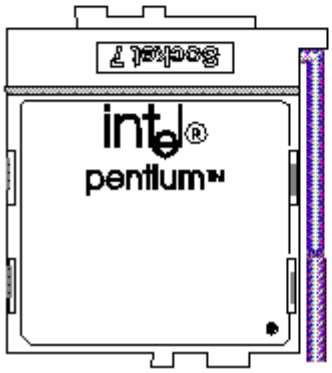
CPU Voltage Selection





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430HX PCIset products

General Asked Questions : Technical

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Q. What kind of CPU can P5HX-B, P5HX-A support?
Answer : P5HX-B and P5HX-A can support the Pentium or compatible processor at host bus 50MHz, 60MHz, and 66MHz for 3.3V technology. They also provide users optional "dual voltage supply circuit" choice of supporting P55C processor or other dual voltage processors.

Q. What kind of chipset do P5HX-B, and P5HX-A use?
Answer : P5HX-B and P5HX-A use Intel 430HX PCIset as main system chipset. It supports the use of EDO DRAM as main memory, and has an enhanced PCI bus to provide a split transaction function and to enable the simultaneous use of the PCI and ISA buses. The computing power of this chipset is 10% greater than its predecessor, the 430FX.

The 430HX PCIset includes the 82439HX, in a 324-lead BGA package, and the 82471SB, in 208-lead QFP package. The 82439HX provides a bridge function for linking the Pentium processor to the PCI bus, and a control function for a main memory and a cache memory. The 82371SB supports a bridge function between the PCI bus and ISA bus, and enhanced IDE controller, and USB controller.

Q. What kind of chip does Intel 430HX PCIset include? What is the main feature of 430HX PCIset?
Answer : Intel 430HX PCIset includes 82439HX(TXC) and 82371SB(PIIX3) chips.
TXC provides the following functions:

- Single 320 pin BGA 439HX (TXC) with integrated Data Paths
- 64-bit Host Bus Interface
- 32-bit PCI Bus Interface
- Integrated DRAM controller
-
    - 64/72-bit Main Memory Interface
    - 4Mbtyes to 512Mbtyes main memory
    - 64Mbit DRAM Technology support
    - 8 Qword Deep Merging DRAM
    - Enhanced EDO/Hyper page mode support (4-clock read leadoff at 50Mhz, 5-2-2-2 read and x-2-2-2 writes at 66Mhz)
    - 8 RAS Lines Available
    - Integrated Programmable-Strength MA Buffers
    - CAS-Before-RAS Refresh
    - Optional DRAM Error Detection/Correction or Parity
- Integrated L2 cache controller
-
    - Optional 512MB DRAM cacheability Limit
    - 64MB standard
- Detects PCI cycles that target DRAM
- PCI Bus Arbiter

PIIX3 provides the following functions:

- PCI-to-ISA bridges
- a fast IDE interface
- Plug-n-Play port
- APIC interface
- PCI 2.1 compliant
- Supports the Universal Serial Bus(USB) at B0 version of PIIX3
- Fully synchronous, Minimum Latency 25/30/33 Mhz PCI interface

Q. When will P5HX-B/P5HX-A support the function of USB?
Answer : Since the USB function of chipset available time is about the end of June, P5HX-B/P5HX-A M/Bs will provide the USB function at the end of July. At that time, P5HX-B/ P5HX-A will offer the pin-headers and flat cable for USB connector jacks.

Q. What is the function of "ECC"?
Answer : The function of "ECC" (error checking and correction) or "EDC" (error detection and correction) provides :

- Superior DRAM data Integrity
- Single Bit error correction, Multi-bit error detection plus Nibble failure detection ECC code
- Single and Multi-bit error reporting
- Virtual swapable bank support
- Merging write buffer eliminates most partial writes cycles

Summary above, ECC can correct DRAM data error with single bit error, and detect DRAM data error with double bits error. Users should use 36-bit SIMM to support the function of ECC. 32-bit SIMM which is no-party SIMM, can not support the function of ECC.

Q. How can users install L2 cache on P5HX-A or P5HX-B?
Answer : P5HX-A or P5HX-B support L2 PBSRAM cache on board or on cache module. The combination of cache size lists as follows:

Total Cache Size	Cache Module with COASt 2.1 or 3.0 Spec.	On board
0	0	0
256KB	0	256KB (32Kx32 2pcs)
256KB	256KB	0
512KB	256KB	256KB (32Kx32 2pcs)
512KB	512KB	0
512KB	0	512KB (64Kx32 2pcs)

Q. What kind of SRAM can be used on P5HX-B or P5HX-A, ASRAM or PBSRAM?
Answer : Due to the trend of PBSRAM(pipeline burst SRAM) being popular, cost being down and performance better than Async. SRAM, P5HX-B and P5HX-A do not provide ASRAM solution. Users can choose either on-board pipeline burst cache or cache module type of P5HX-B or P5HX-A. The cache memory type must be pipelined burst SRAM with the global write enable feature.

Q. Is there any compatible problem of PBSRAM cache module installed on P5HX-B or P5HX-A?
Answer : Yes. P5HX-B and P5HX-A use Intel 430HX PCIset which merely support PBSRAM cache module with COASt 3.0 or COASt 2.1 specification. Some type of Cache module which is only compliant with COASt 1.3 socket may not be installed on P5HX-B or P5HX-A.

Q. Is there any difference between COASt 1.2, COASt 2.1, and COASt 3.0?
Answer : COASt is the specification of PBSRAM cache module. COASt 1.3 can only support Intel 430FX PCIset or compatible chipset M/B. COASt 3.0/2.1 supports Intel 430HX, 430VX, and 430FX PCIset or compatible chipset M/B.

	COASt 1.2	COASt 2.1	COASt 3.0
Chipset support	Intel 430FX PCIset or function compatible chipset	Add Intel 430HX or 430VX PCIset or function compatible chipset	Add Intel 430HX or 430VX PCIset or function compatible chipset
Function difference	Do not support Globe Write	Support Globe Write	Support Globe Write
Others	No Definition of Mechanical Requirements Keying for Proliferations WE# configuration for 82430FX	"Global" PBSRAM functionality Identifies Keying for Proliferations Extended Cacheability Series Resistor Option for non-compliant I/O	Add definition of pin 114 : Interleave burst or linear burst.

Q. What kind of DRAM can be supported on P5HX-B or P5HX-A?
Answer : P5HX-B or P5HX-A support 64/72-bit data path SIMM with FPM(fast page mode) or EDO(Extended Data Out), 1M, 2M, 4M symmetrical or asymmetrical SIMM, or 16MB symmetrical SIMM.

Q. Is 430PCIset PCI 2.1 compliant?

Answer : Yes, the PCI interface is 2.1 compliant and supports up to 4 PCI bus master in addition to the PIIX3 bus master requests. The PCI-to-DRAM interface can reach a 112 MB/sec transfer rate for reads and 121 MB/sec for writes.

Q. The current Windows 95 4.00.950 would not detect PIIX3 correctly. How to correct it?

Answer : The current version of Windows 95 does not recognize the ID of PIIX3. The following steps show how to correct the ID of PIIX3 in Windows 95:

1. Boot up the Windows 95 system.
2. Change the directory to \windows\INF.
3. Edit hidden file Mshdc.inf.
4. Search all lines with "1230" device ID. Copy the lines and replace "1230" with "7010" (device ID for PIIX3)
5. Save the file Mshdc.inf.
6. Restart the computer.