Debug Code Table (Award BIOS)

Code	Description
CPU INIT	CPU Initiation
DET CPU	Test CMOS R/W functionality.
CHIPINIT	Early chipset initialization: -Disable shadow RAM -Disable L2 cache (socket 7 or below) -Program basic chipset registers
DET DRAM	Detect memory -Auto-detection of DRAM size, type and ECC. -Auto-detection of L2 cache (socket 7 or below)
DC FCODE	Expand compressed BIOS code to DRAM
EFSHADOW	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
DC XCODE	Expand the Xgroup codes locating in physical address 1000:0
INIT IO	Initial Superio_Early_Init switch.
CLR SCRN	1. Blank out screen 2. Clear CMOS error flag
INIT8042	1. Clear 8042 interface 2. Initialize 8042 self-test
ENABLEKB	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
DIS MS	1. Disable PS/2 mouse interface (optional). 2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
R/W FSEG	Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
DET FLASH	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
TESTCMOS	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.
PRG CHIP	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.
INIT CLK	Initial Early_Init_Onboard_Generator switch.
CHECKCPU	Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686).
INTRINIT	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
REC MPS	Initial EARLY_PM_INIT switch.
Reserved	Load keyboard matrix (notebook platform)
Reserved	HPM initialization (notebook platform)
SET FDD	1. Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute. 2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead. 3. Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information. 4. Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 5. Early PCI initialization: -Enumerate PCI bus number -Assign memory & I/O resource -Search for a valid VGA device & VGA BIOS, and put it nto C000:0.
INITINT9	Initialize INT 09 buffer

CPUSPEED	1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. Example: onboard IDE controller. 4. Measure CPU speed. 5. Invoke video BIOS.
TESTVRAM	1. Initialize multi-language 2. Put information on screen display, including Award title, CPU type, CPU speed .
RESET KB	Reset keyboard except Winbond 977 series Super I/O chips.
8254TEST	Test 8254
8259MSK1	Test 8259 interrupt mask bits for channel 1.
8259MSK2	Test 8259 interrupt mask bits for channel 2.
8259TEST	Test 8259 functionality.
Reserved	Initialize EISA slot
COUNTMEM	1. Calculate total memory by testing the last double word of each 64K page. 2. Program write allocation for AMD K5 CPU.
MP INIT	1. Program MTRR of M1 CPU 2. Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range. 3. Initialize the APIC for P6 class CPU. 4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.
USB INIT	Initialize USB
TEST MEM	Test all memory (clear all extended memory to 0)
SHOW MP	Display number of processors (multi-processor platform)
PNP LOGO	1. Display PnP logo 2. Early ISA PnP initialization -Assign CSN to every ISA PnP device.
Reserved	Initialize the combined Trend Anti-Virus code.
SHOW EZF	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD (optional)
ONBD IO	1. Initialize Init_Onboard_Super_IO switch. 2. Initialize Init_Onbaord_AUDIO switch.
EN SETUP	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
MSINSTAL	Initialize PS/2 Mouse
CHK ACPI	Prepare memory size information for function call: INT 15h ax=E820h
EN CACHE	Turn on L2 cache
SET CHIP	Program chipset registers according to items described in Setup & Auto-configuration table.
AUTO CFG	1. Assign resources to all ISA PnP devices. 2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to “AUTO”.
INIT FDC	1. Initialize floppy controller 2. Set up floppy related fields in 40:hardware.
CUTIRQ12	(Optional Feature) Enter AWDFLASH.EXE if : -AWDFLASH is found in floppy drive. -ALT+F2 is pressed
DET IDE	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM…..
COM/LPT	Detect serial ports & parallel ports.
DET FPU	Detect & install co-processor

CPU CHG	CPU change
CPR FAIL	CPR error
FAN FAIL	Fan error
UCODEERR	UCODE error
FLOPYERR	Floppy error
KB ERROR	Keyboard error
HD ERR	HDD error
CMOS ERR	CMOS error
MS ERROR	Mouse error
80P ERR	80 port error
BOOT CHG	Boot device change
SMARTERR	HDD smart function error
HM ERROR	Hard monitor error
AINETERR	AI NET error
CASEOPEN	Case open
PASSWORD	Clear EPA or customization logo. 1. Call chipset power management hook. 2. Recover the text fond used by EPA logo (not for full screen logo) 3. If password is set, ask for password.
MEM2CMOS	Save all data in stack back to CMOS
INIT PNP **USB FINAL**	Initialize ISA PnP boot devices 1. USB final Initialization 2. NET PC: Build SYSID structure 3. Switch screen back to text mode 4. Set up ACPI table at top of memory. 5. Invoke ISA adapter ROMs 6. Assign IRQs to PCI devices 7. Initialize APM 8. Clear noise of IRQs.
READ HDD **BOOTMENU**	Read HDD boot sector information for Trend Anti-Virus code 1. Enable L2 cache 2. Program boot up speed 3. Chipset final initialization. 4. Power management final initialization 5. Clear screen & display summary table 6. Program K6 write allocation 7. Program P6 class write combining
NUM LOCK	1. Program daylight saving 2. Update keyboard LED & typematic rate
UPDT DMI	1. Build MP table 2. Build & update ESCD 3. Set CMOS century to 20h or 19h 4. Load CMOS time into DOS timer tick 5. Build MSIRQ routing table.
INT 19H	Boot attempt (INT 19h)