JP1 - CPU frequency jumper 1
default state is connected
pin1=ground/vss
pin2=pin5 of pll, s1 on pll truthtable

JP2 - CPU frequency jumper 2
default state is connected
pin1=ground/vss
pin2=pin4 of pll, s0 on pll truthtable

JP3 - Display mode
default state is connected
pin1=ground
pin2=pin33 of 8042 (p16), CGA (Colour/VGA) display or MDA (Monochrome) display switch.

J4 - RTC battery
default=2&3 connected
pin1=I guess battery +
pin2-3= connect to use onboard RTC battery
pin4=ground

JP4 - Battery type
Positions:
1-2 = lithium cell (not rechargeable)
2-3 = ni-cd
default state with varta battery connected was 1-2 for some reason, which means it doesn't charge

pin1=diode under EEPROM
pin2=pin3 of J4 > positive terminal on battery
pin3=some resistor under EEPROM

JP5 - unknown, connected via solder. Connects to Opti F82C206Q

JP6 - unknown, connected via solder. Looks like it has something to do with ISA bus, goes into LS245 chip next to it

JP7 - Something to do with cache
unable to change, board has max cache & jumper wire is soldered between pins 1&2

JP8 - Something to do with cache
unable to change, board has max cache & jumper wire is soldered between pins 1&2

IMI SC425 is the PLL chip
s0=ground(low/0)
s1=ground(low/0)
s2=open(high/1)
s3=ground(low/0)
That should result in 80mhz on MCLK2 and 40MHz on MCLK1