CALIFORNIA
GRAPHICS
& PERIPHERALS, INC.

CG486VL Green Motherboard

User's Manual

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Preface

Thank you

We at **California Graphics and Peripherals, Inc.** wish to thank you for purchasing this ***CG486VL Green Motherboard.*** We also congratulate you on having chosen a product designed to offer the utmost in dependability and performance. Our products are **designed and built in the USA** to ensure the highest level of quality and sophistication, and we are dedicated to bringing you the compatibility, stability and support necessary to assure that your system will work best in a wide variety of applications and environments.

About This Manual

This manual is written for distributors, PC technicians and knowledgeable PC end users trained in digital circuits, micro-computers, and system programming. It provides information for the installation and use of the ***CG486VL*** **Green Motherboard** from **California Graphics and Peripherals, Inc.**, which supports 486DX™/OverDrive™ 33/25 MHz, and 486DX2™ 66/50 MHz Intel microprocessors, as well as the Intel P23T and P24T CPUs.

Manual Organization

Chapter 1, Introduction, describes the features and performance of the CG486VL Green system board, discusses the importance of using a high quality power supply, and provides detailed information about the Write-back chip set.

Refer to Chapter 2, Installation for a list of the equipment needed to build a system based on the CG486VL motherboard. This chapter provides you with the instructions for handling static sensitive devices, checking or configuring the jumpers for manufacturing, installing on-board memory, and selecting cache size. Read this chapter when you want to install or remove SIMM memory modules, and mount the system board in the chassis. Also refer to this chapter for installing the floppy or hard disk drives, and connecting the cables for the power supply, Turbo Switch, Turbo LED, and Keylock/Power LED, speaker, external battery and keyboard.

Chapter 3, AMI BIOS Setup, provides you with the setup requirements of the AMI BIOS, including instructions to change the password and to use the hard disk utility for hard disk formatting, media analysis, and setting auto interleave values. AMI BIOS beep codes and error messages are also listed in this chapter.

If you encounter any problems, refer to Chapter 4, Troubleshooting, which describes troubleshooting procedures for video, memory, and the setup configuration stored in memory.

Manual Conventions

Keyboard keys listed with hyphens between the key labels should be pressed down together. For example, CTRL-ALT-ESC means press the Control, ALT, and Escape keys down together to achieve the desired result.

Keyboard keys listed without hyphens between the key labels should be pressed down sequentially. For example, ESC F10 means to press the Escape key, release it, and then press the F10 key.

Special Symbols and Notations

The following is a list of the special symbols and notations used in this manual.

Symbol/ Notation	Description
- (Dash)	Used following a capitalized mnemonic or signal name to indicate a "not" (complement) function or an active low signal. Example: -DACK1
h	Used after a number to indicate that the number is a hexadecimal notation. Example: 1Fh

Other Products

California Graphics and Peripherals, Inc. has an ever-growing list of high performance PC products, all designed and built in the USA. We trust that you will enjoy your ***CG486VL*** Green motherboard, and we welcome you to try some of our other products. One such product is our ***SunTracer™*** graphics accelerator card, which was naturally designed for optimum performance with this motherboard. Ask your dealer or distributor for details!

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Chapter 1

Introduction

1-1 Overview

The CG486VL motherboard is a high quality, function-enhanced computer system board, based on the 486DX™, 486DX2™, 486SX™, 487SX™,or OverDrive™Intel micro-processors. Using the same architecture, the CG486VL motherboard can support Intel 486DX 50, 40, 33, 25 MHz, 486DX2- 66, 50 MHz, 486SX/487SX-25 MHz and OverDrive, including Intel P24T technology CPUs .

The board's Industry Standard Architecture (ISA Bus) design has a variety of new features, and its high performance capability provides an ideal, cost-effective system board solution for a wide range of demanding applications such as: CAD, CAM, CAE, networking multi-user environments, database management, desktop publishing, image processing, and artificial intelligence.

This highly integrated system board achieves the highest reliability and yet is small enough for all of its features to be supported in a "Baby-AT size." These features include: a built-in 8 KB internal cache memory, 256 KB/512 KB/1 MB secondary cache memory, 128 MB memory, eight 16-bit AT slots, three VESA VL Local Bus slots, a built-in enhanced math coprocessor, and power saving Green PC Function.

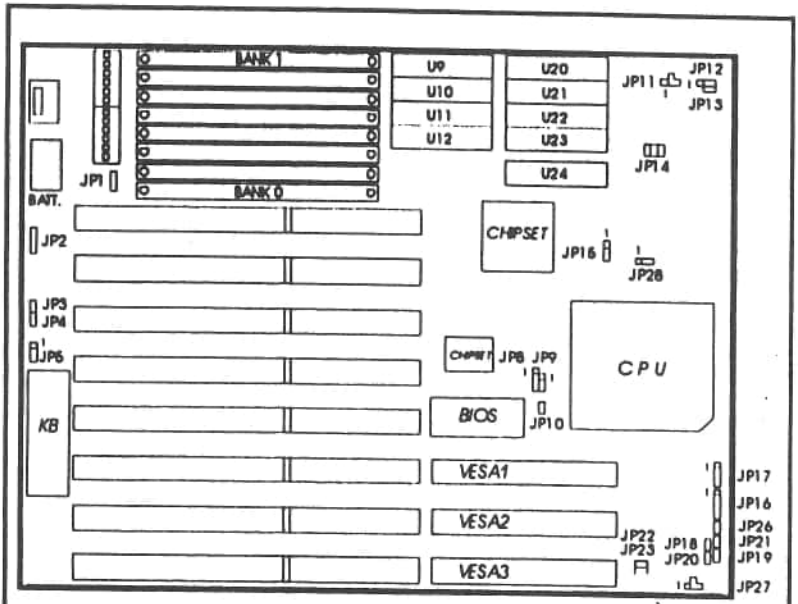
The board supports Write-back cache control for a "0" wait state Intel 80486 microprocessor, with Page and 2 way Page-Interleave memory control. The Write-back technique removes most of the DRAM write penalty with 80 ns or 100 ns DRAM. The DRAM wait

state is BIOS programmable. When Page-Interleave mode is enabled, the performance of 2-way page-interleave is slightly higher than page mode interleave (with one bank of memory).

You can achieve both turbo speed and low speed through the software/BIOS-keyboard by enabling/disabling either the internal or secondary cache, or through the Hardware Turbo Switch control circuitry. Four non-cacheable regions are provided by the system. The system and video ROM BIOS can also be shadowed or cached to enhance performance.

For OS/2 optimization, the system supports Fast Reset. Two Fast Resets are provided: 1) Immediate Reset and 2) Reset right after detecting a HLT instruction (Reset after HLT). Reset after HLT is used by some programs, after they issue the Reset command to the keyboard controller, to "steal" some time for their own use while waiting for the controller's slow response, and before the program's last HLT instruction arrives. This feature improves performance while maintaining compatibility.

Figure 1-1 shows the layout of CG486VL (with 237-pin socket) motherboard. The architecture for the board is illustrated in Figure 1-2.



JUMPER SETTINGS

JP1: 1-2 Battery to 206
2-3 Discharge 206
JP2: External Battery
JP3: Green Power Supply
JP4: IN = COLOR
OUT = MONO
JP5: 1-2 = + 5V VPP to flash memory
2-3 = + 12V VPP to flash memory
JP15: 1-2 = Intel CPU
2-3 = Cyrix CPU
JP16: Keyboard Connector
JP17: Speaker Connector
JP18: Green PC LED
JP19: Turbo Switch
JP20: Hardware switch button for Green PC Mode.
JP21: Turbo LED
JP22: IDE3: IN > 33 MHz
OUT = < 33MHz
JP23: IDE2: IN = 1 WAIT WRITE

CPU TYPE

	486DX/DX2	486SX	487SX	P24T
JP8	1-2, 3-4	2-3	1-2, 3-4	1-2, 3-4
JP9	2-3	Open	Open	1-2
JP10	Open	Open	Open	Short

CPU SPEED

	50MHz	40MHz	33MHz	25MHz
JP15	Open	Open	Open	Short
JP14	1-2, 3-4, 5-6	1-2, 3-4	1-2, 5-6	1-2
JP27	1-2	1-2	2-4	2-4
JP28	1-2	1-2	2-3	2-3

CACHE SIZE

	256K	512K	1MB
JP11	1-2	2-3	2-4
JP12	1-2	2-3	2-3
	8 pieces of 32 K x 8 (U9 U12, U20 24)	4 pieces of 128 K x 8 (U9 U12), and 1 piece of 32 K x 8 (U24)	8 pieces of 32 K x 8 (U9 U12, U20 24)

Figure 1-1 CG486VL Motherboard Layout

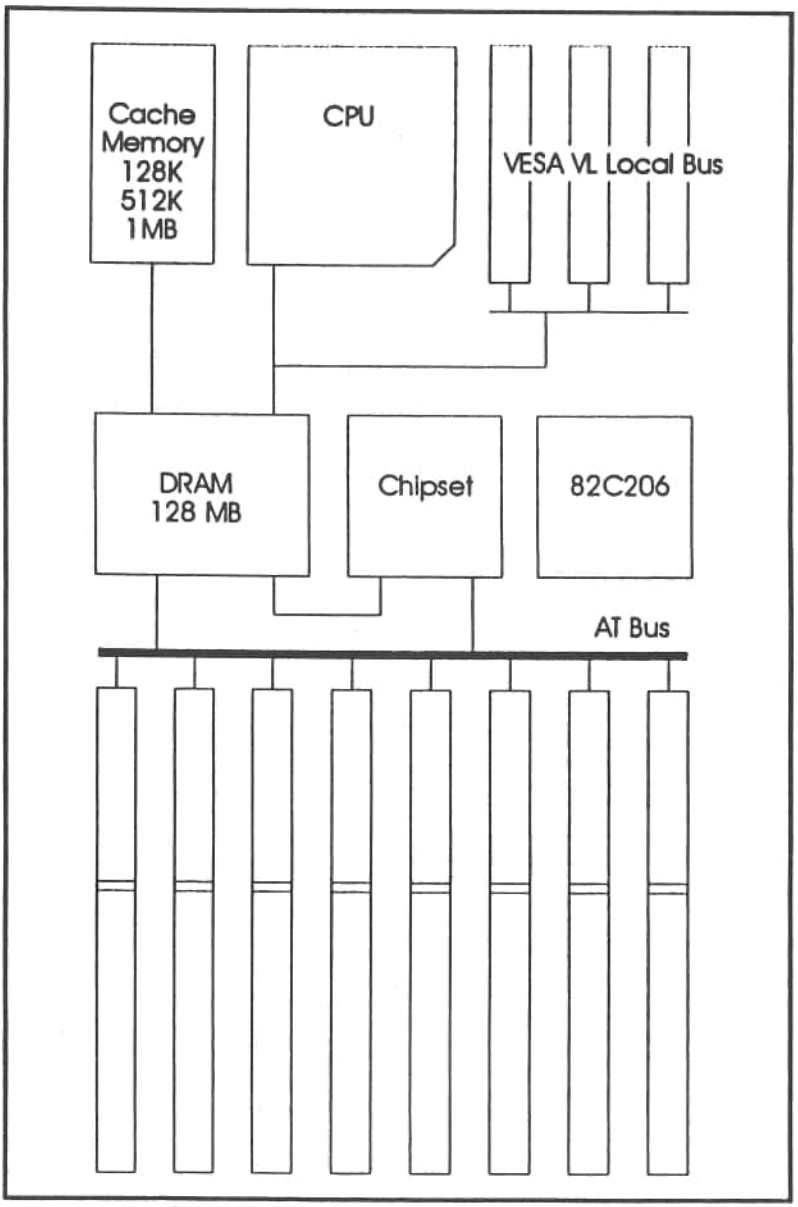


Figure 1-2 System Board Architecture

Features

The following list covers the general features of the CG486VL motherboard.

CPU:

* Intel 32-bit 80486DX, 80486DX2, 80486SX, 80487SX or OverDrive, including Intel P24T OverDrive CPU

Math coprocessor:

* On-chip floating point Math coprocessor for 486DX/DX2, 487SX or OverDrive

Speed:

* Designed to work at 50, 40, 33, 25 MHz on a 486DX-based computer, 66, 50 MHz on a 486DX2-based Computer, 25, MHz on a 486SX or 487SX-based computer, and 50, 40, 33 MHz on a OverDrive-based computer

Cache:

* 8 KB on-chip 4-way set associative internal cache
* Write-back external cache that supports a 256 KB (32 KB x 8), 512 KB (128 KB x 4), or 1 MB (128 KB x 8) secondary cache

Memory:

* 128 MB of memory on the motherboard
* Page and 2 way Page Interleave modes support 256 KB x 9, 1 MB x 9, 4 MB x 9, and 16 MB x 9 (80 ns or 100 ns) for up to 128 MB of on-board memory
* Hidden DRAM refresh

Turbo Switching:

* Hardware Turbo Switch or BIOS Turbo speed selectable by the keyboard
* Turbo Light connector (on and off for High and Low speeds)

Bus:

* Eight 16-bit AT ISA slots
* Three standard VESA VL Local Bus Slots
* Supports 2 Bus Masters and 1 Slave on VESA slots

BIOS:

* AMI BIOS with built-in setup
* Fast Reset and Gate A20 to optimize OS/2

Shadowed/Cached BIOS:

* Shadowed system/video BIOS
* Cached system/video BIOS

Software Compatibility:

* 100% IBM PC/AT compatible
* DOS, OS/2, UNIX, XENIX, and Novell

1-2 Power Supply

As with all computer products, a stable power source is necessary for proper, and reliable operation. It is even more important for high CPU clock rates like 66, 50, 33 MHz for the CG486VL system board.

Although most power supplies generally meet the specifications required by the CPU, some power supplies are not adequate. To obtain the highest system reliability, be certain that your power supply provides +5 VDC with a voltage range between +4.95 VDC (minimum) and +5.25 VDC (maximum).

It is highly recommended that you use a high quality power supply. Additionally, in areas where noisy power transmission is present, you may choose to install a line filter to separate noise from the computer. You can also install a power surge protector to help avoid problems caused by power surges.

1-3 The Write-back Chip Set

The following sections provide detailed information regarding the characteristics of CPU/AT Bus and DRAM controller, as well as Data Buffer.

Bus Arbitration Logic

The CPU will relinquish control of its bus when requested by another device. For DMA and Bus Master cycles, DMAREQ is generated by 206 and a HOLD signal will be sent out to CPU by the chip set. CPU will respond it by asserting HLDA and release the bus to the requesting device. The chip set supports both AT and Hidden Refresh. A Refresh Request is generated every 15.6 sec and CPU will release bus when running in AT Refresh mode. Once the Hidden Refresh is enabled, no HOLD signal will be generated. The CPU will continue its current operation (if it is a cache hit cycle) parallel to AT Bus refresh and, hence, increase system performance.

CPU and AT Bus Interface Logic

The CPU starts a cycle by asserting ADS#. If it is a motherboard DRAM/SRAM cycle, the DRAM/CACHE controller will start access DRAM/SRAM memory. If it is a local bus device cycle, then, the chip set will not respond to it. If it is an AT bus cycle, the chip set will issue an AT bus cycle.

Turbo Speed Control

The chip set supports both hardware and software Turbo speed control. The hardware TURBO switch is controlled by the keyboard controller (Pin 23). When the TURBO pin is high, the system will operate at its full speed. The CPU will enter a HOLD-state every 3 usec out of a 4 usec period if the TURBO pin is tied to low. The chip set controls the arbitration among Refresh, DMA and Non-TURBO hold request.

Cache Controller

The chip set has a built-in burst mode Write-back cache controller in it. It keeps monitoring TAGA7-0 and compares it with CPU TAG address. If cache is enabled and the TAG address matches to the CPU address, it is called a cache "HIT". When a read hit happens, the chip set will burst 4 double words into CPU by alternating CRD0# and CRD1#.

In the case of write hit, the CPU data will be written to the cache RAM by asserting CWE0# (1-bank SRAM or 2-bank SRAM with A2=0) or CWE1# (2-bank SRAM with A2=1). At the same time, an "1" will be written back to DIRTY bit. "DIRTY bit=1" means that the data in SRAM is the only valid data. DRAM data is not updated.

If read miss happens, the DIRTY bit will be checked first before moving in new data. If DIRTY=1, we must remove the only valid data from SRAM to DRAM; then move in the requested data from DRAM to SRAM and CPU. In case of WRITE MISS, data will be written to DRAM.

The advantage of Write-back cache over Write-through cache will show up during write hit cycle. A Write-through cache must write data to both SRAM and DRAM. Usually, DRAM access is slower than SRAM access. If DRAM Write-page miss happens, the penalty will be fairly large (4,5,6..wait states) compared to Write-back cache which only needs to write data to SRAM and it can always be done in 0 wait state.

When DMA/Master memory read hit happens, data will be supplied from SRAM instead of DRAM. A DMA/Master memory read miss will get data from DRAM. In the case of DMA/Master memory write cycle, data will be written into DRAM and SRAM if it is a hit cycle. The DMA/Master write miss cycle will only write data into DRAM.

Tag RAM / Data RAM Configurations

The chip set supports 256 KB, 512 KB, 1 MB cache size for 486. The Tag RAM and Data RAM requirements are listed in Table 2.2.

The chip set combines the DIRTY RAM with TAG RAM. The dirty bit can also be replaced by a tag address in order to increase the cacheable range.

DRAM Controller

As we have mentioned, a Write-through cache needs a fancy DRAM design (for example: Page Interleave mode DRAM controller) to help write cycle, since all write cycles have to go to DRAM. But Write-back Cache does not have such DRAM dependency. All write hit cycles will go to 0 wait SRAM. Therefore, DRAM access is no longer critical since we can almost finish all read/write cycles in "0" wait state.

Pure Page mode DRAM controller is used in this design. No Interleave is needed. It can support mixed type of DRAM. The starting address of each DRAM bank is calculated by internal hardware. You can configure DRAM size from 1 M-byte to 32 M-byte anyway you want as long as no previous bank is empty.

Wait State / DRAM Speeds

The Table below is based on Page mode DRAM which is the most popular type of DRAM now.

CPU Speed	DRAM Speed	DRAM Wait States (READ,WRITE)
25 MHz	100ns	R1WT,W0WT
	80ns	R1WT,W0WT
33 MHz	100ns	R2WT,W0WT
	80ns	R2WT,W0WT
40 MHz	100ns	R2WT,W1WT
	80ns	R2WT,W1WT
50 MHz	100ns	R3WT,W1WT
	80ns	R3WT,W1WT

Shadow RAM

It is much faster to access code from DRAM than from ROM or EPROM. The chip set provides shadow RAM capability to speed up system ROM and adapter ROM access time. By moving those codes from ROM to DRAM, performance can be improved quite dramatically. All shadow RAM will be write protected. Shadow RAM on block C and F can also be cacheable/non-cacheable. It is default to non-cacheable.

DMA / MASTER Access DRAM Logic

DMA and MASTER cycles are very similar. Once the internal arbitration logic grants a DMA/MASTER cycle, this logic will monitor internal cache hit signal and MEMR#, MEMW#. If it is a memory read hit cycle, this logic will provide data from SRAM. A memory read miss cycle will access data from DRAM. In the case of memory write hit cycle, data will be written into both DRAM and SRAM. For write Miss cycle, data will be written into DRAM only.

Refresh Logic

The chip set has an internal counter to generate refresh request signal every 15.6 usec. Once the internal refresh request signal becomes active, the refresh logic will check to see if it is an AT refresh or a Hidden refresh. In the case of an AT refresh, a CPU HOLD signal will be sent to CPU. After receiving HLDA from CPU, DMA/REFRESH arbitration logic will grant refresh cycle to refresh logic. Refresh logic will start cycle by sending refresh address and 2 staggered RAS#. If hidden refresh is programmed, the chip set will not send out CPU HOLD signal to hold the CPU. Instead, it will grant refresh cycle to refresh logic and refresh logic will start refresh cycle if DRAM and AT state machine is not busy.

High Speed Local Bus Support

The chip set supports VESA Local Bus devices. It will monitor pin 8 (NPRDYLC#) at the end of T2 to see if it is a local device cycle. if a local device cycle is detected, the chip set will not do anything, so the local device can fully control the local bus.

In order to support DMA access local device memory cycle, the chip set will generate an ADS#, driving M/IO#, W/R# after detecting a DMA memory cycle. For MASTER access local bus memory and IO devices, The chip set will perform the same action: driving ADS#, M/IO#, and W/R#.

Data Bus Conversion

The chip set performs data bus conversion for the following cycles:

1. CPU accesses 8 or 16 bit devices through 32/16 bit instructions.

2. DMA/Master cycles between local DRAM, Cache memory, on-board I/O devices and devices reside on AT Bus.

During the process, the chip set provides all the necessary control signals to the external bi-directional data buffers.

Parity Generation and Checking Logic

For local DRAM write cycle from both CPU and DMA/Master devices, the chip set generates byte-wise memory parity bits (MP[3:0]). These parity bits are stored into local DRAM along with the write data.

During the local DRAM read cycle, the data and parity bits are read from DRAM into the chip set. Parity checking logic would compare those parity bits with the parity generated from the read data. if a mismatch happens, and both system memory parity check and NMI are enabled, a NMI will be asserted by the chip set.

1-4 System Power Saving Mode

The CG486VL power saving mode reduces the electric power used by the system when it is not in use for a preset period of time. This is accomplished by the CG486VL automatically switching off the display, reducing the CPU clock speed, and reducing power used by the IDE hard drive.

The Green PC mode can be enabled or disabled in the BIOS setup. Also, the time delay before entering the power saving mode can be selected.

When there is no activity on the keyboard for the time period selected in the setup, the system will enter the power saving mode and "go to sleep". The CPU will continue to operate but at a much slower speed. When a key is typed on the keyboard, the system will "wake up".

Green PC HOT KEYS

There are three hot key sequences defined for power saving mode. These hot keys are active if the Green PC function is enabled in the BIOS setup.

<CTRL> <ALT> <\>
puts the system into immediate power saving mode.

<CTRL> <ALT> <[>
disables the Green PC power saving mode temporarily.

<CTRL> <ALT> <]>
enables the Green PC power saving mode.

Chapter 2

Installation

2-1 High Performance *CG486VL* System Components

The equipment listed in this section is required to build a high performance system based on the ***CG486VL Green Motherboard.*** In order to create the standard configuration, add the equipment listed as standard configuration below to the equipment listed as minimum system configuration. Similarly, for the full enhanced configuration, add the enhanced system configuration equipment listed below to the equipment itemized in the previous two lists.

Minimum System Configuration

- 200 W (minimum) power supply
- Chassis (Baby-AT, AT, portable/lunch box, or tower) with a speaker connected to a 4-pin connector, a push button switch with 2-pin connector for the reset function, and a keylock connected to a 5-pin connector (a 2-pin push button for hardware turbo switch is optional)
- CG486VL system board with four SIMM modules providing a total of 1 MB of memory (minimum)
- Floppy disk drive (1.2 MB, 360 KB, 1.44 MB, or 720 KB)
- Floppy/hard disk drive controller card with a FDD cable
- AT-compatible keyboard (84 or 101 style keyboard)

- Video card (Monochrome, CGA, EGA, VGA, or SuperVGA)
- Video display monitor

Standard System Configuration

- I/O card (serial port for mouse, parallel port for printer)
- Serial or bus mouse
- Parallel printer
- Additional floppy disk drive to allow system to accept both 5.25" and 3.5" diskettes
- Hard disk(s) with a set of hard disk flat cables

Enhanced System Configuration

- Tape drive (for backups)
- Modem/FAX card
- CD-ROM drive
- Digitizer/tablet
- Added system memory (on-board up to 128MB)
- SCSI, ESDI, RLL, or IDE controller and drives
- Standard VESA VL VGA Card or IDE Card

2-2 Static Sensitive Devices

Static-Sensitive electricity discharge can damage electronic components. To prevent damage to your system board, it is important to handle it very carefully. The following measures are generally sufficient to protect your equipment from static discharge:

Precautions

1. Use a grounded wrist strap designed for static discharge.
2. Touch a grounded metal object before you remove the board from the anti-static bag.
3. Handle the board by its edges only; do not touch its components, peripheral chips, memory modules, or gold fingers.
4. When handling chips or modules, avoid touching their pins.
5. Put the system board and peripherals back into their anti-static bags when not in use.
6. Be sure your computer system's chassis allows excellent conductive contacts between its power supply, case, mounting fasteners, and the system board for grounding purposes.

Unpacking

The system board is shipped in anti-static packaging to avoid static damage. When unpacking the board, be sure the person handling the board is static-protected.

2-3 Configuring the System Board Jumpers

Use the following settings to configure your system board. Refer to Figure 1-1 for an illustration of the jumpers.

Manufacturing Settings

The AMI BIOS can automatically sense the monitor card type you are using (mono, color, EGA or VGA). This frees up jumper JP4, so it can be used for password security. Three functions, Enable Password, Change Password, and Disable Password are

provided, when the password/security feature is enabled. (For the AMI BIOS, the default password is AMI.)

Jumper: **JP4** (for monitor selection)
Closed: Color, CGA
Open: Mono

Jumper: **JP4** (for security/password feature)
Security Enable: Closed
Security Disable: Open

Changing the CPU Type

The CG486VL Motherboard supports the Intel 486DX, 486DX2, 486SX, 487SX or OverDrive CPUs. To change the CPU type, you must also change JP8 JP9, JP10 as shown in the following table.

	486DX/DX2	486SX	487SX	P24T
JP8	1-2, 3-4	2-3	1-2, 3-4	1-2, 3-4
JP9	2-3	Open	Open	1-2
JP10	Open	Open	Open	Short

Table 2-1A. CPU Type Jumpers JP8-JP10

Changing the CPU Speed

The CG486VL Motherboard supports 486DX-50, 40, 33, and 25, 486DX2-66, 50, 486SX/487SX-25 and OverDrive-50, 40, 33. To change the CPU frequency see Table 2-1B.

	50MHz	40MHz	33MHz	25MHz
JP13	Open	Open	Open	Short
JP14	1-2, 3-4, 5-6	1-2, 3-4	1-2, 5-6	1-2
JP27	1-2	1-2	2-4	2-4
JP28	1-2	1-2	2-3	2-3

Table 2-1B. CPU Frequency

Hardware Turbo Switch

JP19: Connect to hardware switch button at computer case.

Jumper Settings

JP1:	*	1-2	=	Connect Battery to 206 (Default)
		2-3	=	Discharge 206
JP2:		For external Battery		
JP3:		Connect to Green PC Power Supply		
JP4:		IN	=	COLOR
	*	OUT	=	MONO (Default)
JP5: (Default)	*	1-2	=	+5V VPP to normal EPROM
		2-3	=	+12V VPP to flash EPROM
JP15:	*	1-2	=	Intel CPU (Default)
		2-3	=	Cyrix CPU
JP16:		Keylock Connector		
JP17:		Speaker Connector		
JP18:		Green PC LED		
JP19:		Turbo Switch		
JP20:		Hardware switch button for Green PC Mode		
JP21:		Turbo LED		
JP22:	IDE3:	IN	>	33 MHz
	*	OUT	=<	33 MHz (Default)
JP23:	IDE2:	IN	=	1 WAIT WRITE

* OUT = 0 WAIT WRITE (Default)

JP26: Connect to RESET Button

On Board Memory

There are no jumpers to configure for on-board memory (Bank 0 and Bank 1). One bank of memory is required, with an 1 MB minimum. This single bank of memory is contained in **four** pieces of SIMM modules. Please refer to Table 1.1 for DRAM speeds.

Cache Size Selection

The CG486VL system board supports 256 KB (with 32 K x 8 of static RAM), 512 KB (with 128 K x 8 static RAM) or 1MB (with 128 K x 8 static RAM) of cache memory. For each cache size, two jumpers are set accordingly:

JP18: Connect to Green PC LED at computer case.

JP20: Connect to hardware switch button at computer case for Green PC Mode.

	JP11	JP12	
256K	1-2	1-2	9 pieces of 32 K x 8 (U9-U12, U20-U24)
512K	2-3	2-3	4 pieces of 128 K x 8 (U9-U12), and 1 piece of 32 K x 8 (U24)
1MB	2-4	2-3	9 pieces of 128 K x 8 (U9-U12,U20-U24)

Table 2-2. Cache Size Jumpers JP11, JP12

2-4 Installing Cache Memory

As mentioned previously, the CG486VL system board's Write-back cache supports 256 KB, 512 KB or 1 MB cache memory. Two banks containing a total of nine SRAM pieces are required. For the 256 KB Cache, nine 32 K x 8 static RAM (SRAM) are required. For the 512 KB Cache, four 128 K x 8 and one 32 K x 8 SRAM are required. For the 1 MB Cache, nine 128 K x 8 SRAM are required. In any case, the SRAM chips are located in system board positions: U9-U12, U20-U23 and U24. See the "Configuring Jumpers" section of this chapter for appropriate jumper settings.

2-5 Connecting Cables

After you have securely mounted the system board to the chassis, you are ready to connect the cables.

Power Supply

Attach power supply cables to their matching connector J1 respectively. Do not force the cables, but make sure they are fully seated. The two black wires on each power cable sit next to each other when correctly installed. See Table 2-3 for pin definitions.

Connector Number	Pin Number	Function
J1	1	Power Good (Power on reset, TTL signal)
	2	+5 V DC
	3	+12 V DC
	4	-12 V DC
	5	Ground (Black wire to be connected)
	6	Ground (Black wire to be connected)
	7	Ground (Black wire to be connected)
	8	Ground (Black wire to be connected)
	9	-5 V DC
	10	+5 V DC
	11	+5 V DC
	12	+5 V DC

Table 2-3. Power Supply Pin Definitions

Reset Cable

The reset cable is a 2-pin cable with no polarity (S1).

Keylock/Power LED Cable

The keylock/power LED cable has five (5) pins. See Table 2-4 for pin definitions (JP16).

Pin Number	Function	Definition
1	+	Red wire, LED power
2	Key	No connection
3	GND	Black wire
4		Keyboard inhibit
5	GND	Black wire

Table 2-4. Keylock/Power LED Pin Definitions

Speaker Cable

The speaker cable has four (4) pins. See Table 2-5 for pin definitions (JP17).

Pin Number	Function	Definition
1	+	Red wire, speaker data
2	Key	No connection
3	GND	Black wire
4	Vcc	+5 V

Table 2-5. Speaker Cable Pin Definitions

Keyboard Connection Cable

The keyboard connection cable J2 has five (5) pins. See Table 2-6 for pin definitions.

Pin Number	Function
1	Keyboard Clock
2	Keyboard Data
3	Spare
4	Ground
5	+5 V

Table 2-6. Keyboard Connection Pin Definitions

Hardware Turbo Switch Connector

The JP19 hardware turbo switch connector has two pins. The connector attaches to the computer case for the hardware turbo switch button.

Turbo LED Connector

The (JP21) Turbo LED connector has two (2) pins. This connector attaches a Turbo LED cable to the front panel of the system chassis. When the system is in Turbo Mode, the LED is on.

2-6 Installing/Removing the SIMM Modules

The CG486VL system board can accommodate a maximum of 128 MB (two banks) of on-board memory, using standard 30-pin SIMM memory modules. You can use any 80 ns or 100 ns and 256 KB x 9, 1 MB x 9, 4 MB x 9, or 16 MB x 9 Fast Page Mode SIMM modules. The board supports any mixture of banks of the three types of SIMMs, as long as all four pieces of SIMM modules within each bank are of the same type. Please refer to Table 1.1 for DRAM speeds and Wait State.

To optimize memory SIMMs, the board has built-in support for Page and Page-Interleave Mode. If Banks 0 and 1 are SIMMs of the same type, they can operate in 2-way Page-Interleave Mode. In all other cases, each bank operates in Page Mode only. The BIOS automatically configures memory size.

Table 2-7 shows the recommended memory configurations available. Refer to Figure 2-1 and the instructions below for installing or removing SIMM modules.

CAUTION

Exercise extreme care when installing or removing the SIMM modules to prevent any possible damages.

SIMM Module Installation

1. Insert SIMM modules SIMM5, SIMM6, SIMM7, SIMM8 first. Follow with SIMM modules SIMM1, SIMM2, SIMM3, and SIMM4.
2. Insert each SIMM module into its socket at an angle away from the AT Slot. The component side of the SIMM modules must face the AT Slots.
3. Gently press the SIMM module in the direction of the CPU or Cache Memory until it snaps into place in the socket.

Removing SIMM Modules

1. Remove SIMM modules in correct descending order: from SIMM1 through SIMM4, and from SIMM5 to SIMM8.

2. Gently push the edge of the sockets to release the module. Remove one side of the SIMM module first, and then the other side, to prevent breaking the socket.

	Bank 0	Bank 1	Total Size	Interleave
	SIMM 5-8	SIMM 1-4		
1.	1M	None	1MB	None
2.	1M	1M	2MB	Yes
3.	4M	None	4MB	None
4.	4M	4M	8MB	Yes
5.	4M	16M	20MB	None
6.	16M	None	16MB	None
7.	16M	16M	32MB	Yes
8.	64M	None	64MB	None
9.	64M	64M	128MB	Yes

Table 2.8. CG486VL Memory Configurations

2-7 Mounting the System Board in the Chassis

The system board has ten standard mounting holes to fit all different types of chassis. Chassis may come with a variety of mounting fasteners, made of metal or plastic. Although a chassis may have both metal and plastic fasteners, metal fasteners are the most highly recommended because they ground the system board to the chassis. Therefore, use as many metal fasteners as possible for better grounding.

2-8 Connecting Floppy and Hard Disk Drives

Use the following information to connect the floppy and hard disk drive cables.

- The floppy disk drive cable has seven twisted wires. The hard disk drive cable has five wires.
- A red mark on a wire typically designates the location of pin 1.
- A single floppy disk drive cable has two connectors to provide for two floppy disk drives. The connector with twisted wires always connects to Drive A:, and the connector that does not have twisted wires always connects to drive B:.
- A single hard disk drive cable has 34 wires and two connectors to provide for two drives. The connector with twisted wires normally connects to Drive C:, and the connector that does not have twisted wires typically connects to drive D: (such as the Seagate ST251-1 disk drive).
- Each hard disk drive requires a data cable with 20 wires.
- Some manufacturers ship hard disk drives already set up to be drive C:, even though these drives have connectors without twisted wires, e.g., Toshiba MK134FA-1. To set the hard disk drive to be drive D: you must change DS1 and DS2 by moving the jumper in position 7 to position 8. The jumpers are located near the 34-pin edge connector at the rear of the drive's top circuit board.
- To select a disk drive as C:, you would normally set the drive select jumper on the drive to DS1, and to select a disk drive as D:, you would normally set the drive select jumper on the drive to DS2. Consult the documentation that came with your disk drive for details on actual jumper locations and settings.
- Some drives require a special controller card. Read your disk drive manual for details.

Chapter 3

AMI BIOS

NOTE

Due to AMI BIOS revisions and customization by resellers, some of the options described in this chapter may not be available on your system. Also, your system may have some options that are not described here. California Graphics and Peripherals, Inc. will make a great effort to supply addendum documentation whenever possible. Should you have any questions or problems, however, please contact your dealer or our Technical Support Department.

3-1 Getting Started

Conventions:

References to specific keys on the keyboard are enclosed by the symbols < >, e.g.,

< ESC > for the Escape key or
< F1 > for the Function 1 key.

What is AMI BIOS?

ROM BIOS (Read Only Memory Basic Input/Output System) controls all of the functions of the various hardware and software components of your system. In most cases, the AMI ROM BIOS will already be installed in your computer system. The main component of your system is known as the system board, or mother board, which contains the CPU (Central Processing Unit), the expansion BUS, and various other microchips. The ROM BIOS chips are also installed on the mother board.

Running AMI BIOS

When the system is powered on, the BIOS will enter the Power-On Self Test (POST) routines. These routines are divided into two phases:

System Test and Initialization (test and initialize system boards for normal operations) and

System Configuration Verification (compare defined configuration with hardware actually installed).

The AMI BIOS performs the various diagnostic checks at the time the system is powered up; if an error is encountered, the error will be reported in one of two different ways. If the error occurs before the display device is initialized, a series of beeps will be transmitted. Beep codes are found in Appendix C.

If the error occurs after the display device is initialized, the screen will display the error message. BIOS error messages are found In Appendix E. In the case of a non-fatal error, a prompt to press the < FI > key may also appear on the screen.

Normally, the only routine visible on the screen will be the memory test, Figure 3.1 displays the screen which appears when

the system is power on.

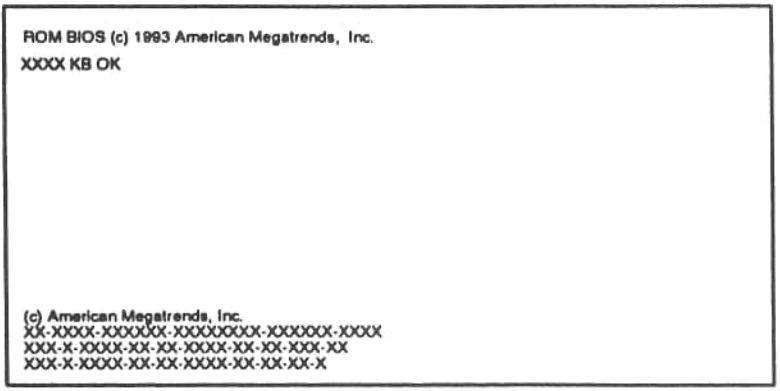


Fig. 3-1 - Power On Screen

At the left bottom corner of the screen, below the copyright message, a three (3) line reference string appears. This screen is used to determine the options installed in the AMI BIOS.

If a problem occurs with the system, copy these reference numbers down before consulting your system manufacturer.

To "freeze" the screen, power on the system and hold a key down on the keyboard. This will cause a "keyboard Error" message to appear on the screen and the system will wait for the <F1> key to be pressed. At this point, you may copy the three lines down and then press <F1> to continue the boot procedure.

NOTE

If the "Wait for <F1> If any Error option in the Advanced CMOS Setup Program of the BIOS SETUP program is set to "Disabled," it should be set to enabled prior to using this method to freeze the screen.

After the POST routines are completed, the following message appears:

"Hit <ESC> if you want to run SETUP"

To access the AMI BIOS SETUP program, press the <ESC> key.

A record of the computer's system parameter (such as amount of memory, disk drives, video displays, and numeric coprocessors) is stored in the CMOS (Complementary Metal Oxide Semiconductor) memory. When the computer is turned off, a back-up battery retains the system parameters in the CMOS memory.

Each time the system is powered-on it is configured with these values, unless the CMOS has been corrupted or is faulty. AMI's SETUP program is resident in the ROM BIOS (Read Only Memory Basic Input/Output System) so that it is available each time the computer is turned on.

If, for some reason, the CMOS becomes corrupted, the system is configured with the default values stored in this ROM file. There are two (2) sets of BIOS values stored in the ROM file: the BIOS Setup default values and the Power-On default values.

The BIOS Setup default values are those which should provide optimum performance for the system. They are the best case default values.

The Power-on defaults, which are the worst cased defaults, are the stable values for the system. They are to be used if the system is performing erratically because of hardware problems.

Listed below is an explanation of the keys displayed at the bottom of the screens accessed through the BIOS SETUP program:

ESC: Exit to previous screen.

ARROW KEYS: Use arrow keys to move cursor to desired selection.

PAGEUP / PAGEDOWN / CTRL-PAGEUP / CTRL-PAGEDOWN: Modify the default value of the options for the highlighted feature. If there are less than 10 available options, the Ctrl PageUp and Page Down keys function the same as the PageUp and PageDown keys.

F1: Displays help screen for selected feature.

F2/F3: Changes background and foreground colors.

F5: Retrieves the values which were resident when current setup session was started. These values will be CMOS values if the CMOS was uncorrupted at the start of the session, or they will be the BIOS Setup with the BIOS Setup default values.

F6: Loads all features in the Advanced CMOS Setup/Advanced Chip Set Setup with the Setup defaults.

F7: Loads all features in the Advanced CMOS Setup/Advanced Chip set Setup with the power-on defaults.

F10: Saves all changes made to Setup and exits program.

NOTE

The default value for the prompts which occur when the < F5 >, < F6 >, and < F7 > keys are pressed is always < N > (No). Actually executing these options requires changing the < N > to < Y > (Yes) and pressing < ENTER >.

The generic menu options of the BIOS SETUP Program are shown in Figure 3.2.

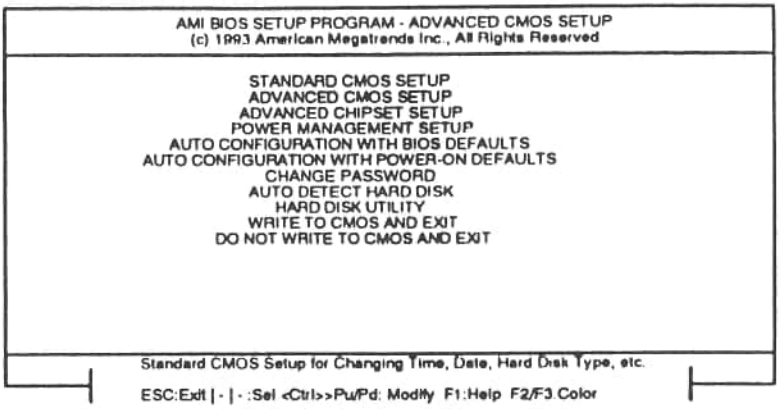


Fig. 3.2
BIOS Setup Screen

A warning message, shown in Figure 3.3, is displayed each time one of the first three options (Standard CMOS Setup, Advanced CMOS Setup, and Advanced Chip Set Setup) is selected before any changes are allowed to any of the setup parameters.

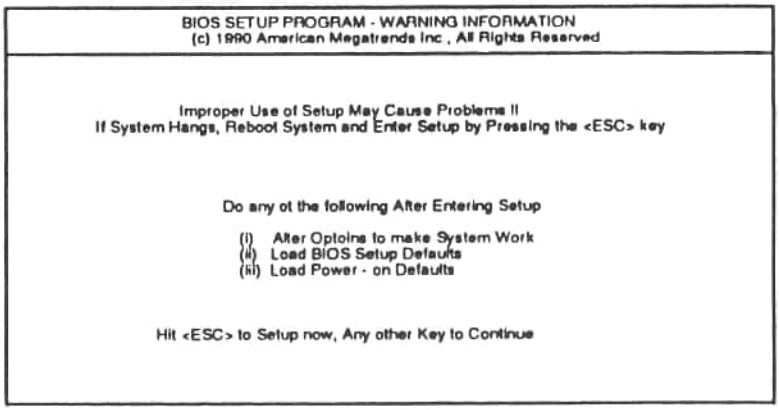


Fig. 3.3
Warning Screen

AUTO CONFIGURATION WITH BIOS DEFAULTS

The Auto Configuration With BIOS feature uses the default system values before the user has changed any CMOS values. If the CMOS is corrupted, the BIOS defaults will automatically be loaded.

If you wish to use the BIOS defaults, change the prompt to < Y > and press < ENTER >. The following message will appear on the screen:

"Default values loaded. Press any key to continue."

AUTO CONFIGURATION WITH POWER-ON DEFAULTS

This feature uses the default Power-On values. You may wish to use this option as a diagnostic aid if your system is behaving erratically.

If you wish to use the Power-On defaults, change the prompt to < Y > and press < ENTER >. The following message will appear on the screen:

"Default values loaded. Press any key to continue."

WRITE TO CMOS AND EXIT

The features selected and configured in the Standard Setup, Advanced CMOS Setup, Advanced Chip Set Setup, and the New Password Setup will be stored in the CMOS when this option is taken. The CMOS checksum is calculated and written to the CMOS. Control is then passed back to BIOS.

Pressing < N > (No) and < ENTER > will return the user to the Main Menu.

Pressing < Y > (Yes) and < ENTER > will save the system parameters and continue with the booting process.

DO NOT WRITE TO CMOS AND EXIT

This option passes control back to BIOS without writing any changes to the CMOS.

Pressing < N > (No) and < ENTER > will return the user to the Main Menu.

Pressing < Y > (Yes) and < ENTER > will continue with the booting process without saving any system parameters.

3-2 Standard CMOS Setup

Standard CMOS Setup is the first option on the main setup menu. Press < ENTER > at the highlighted selection to access this option. The screen in Figure 3.8 will appear.

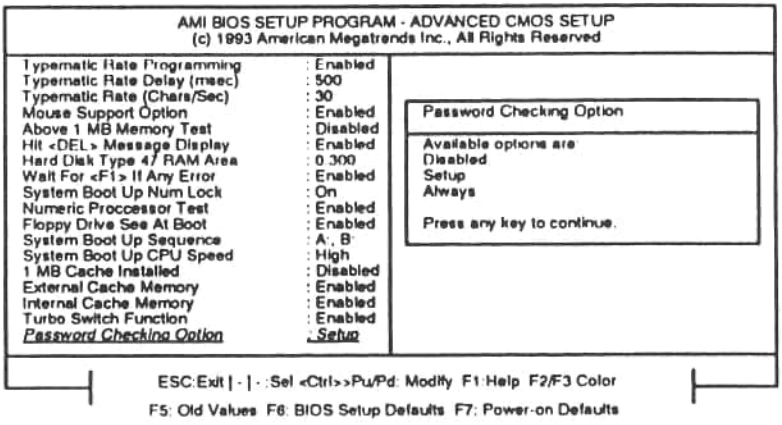


Fig. 3.8
Standard CMOS Setup

The Standard CMOS Setup utility is used to configure the following features:

Date: Month, Date, and Year. Ranges for each value are listed below in prompt box in the left corner of the CMOS Setup screen (Figure 3.8)

Time: Hour, Minute, and Second. Use 24-hour clock format, i.e., for PM numbers, add 12 to the hour. You would enter 4:30 P. M. as 16:30:00.

Daylight Savings: Disabled or Enabled.

Hard Disk C and Hard Disk D: Hard disk types from 1 to 46 are standard ones, type 47 is user-definable. The user must enter the hard disk parameters for each drive.

NOTE

The USER definition entry allows you to perform a test on a disk drive not defined in ROM. The USER definition entry is valid only during the period that the test is performed.

The drive types are identified by the following characteristics:

Type	This is the number designation for a drive with certain identification parameter.
Cyl.	This is the number of cylinders found in the specified drive type.
Heads	This is the number of heads found in the specified drive type.

Wpcom	WPcom is the read delay circuitry which takes into account the timing differences between the inner and outer edges of the surface of the disk platter. The number designates the starting cylinder of the signal.
L-zone	L-zone is the landing zone of the heads. This number determines the cylinder location where the heads will normally park when the system is shut down.
Capacity	This is the formatted capacity of the drive based on the following formula: (# of heads) X (# of cylinder) X (17 sec./Cyl.) X (512 bytes/sec.)

Listed below are the attributes for disk types 1 through 46.

Type	Cyln	Head	WPcom	LZone	Sect	Size
1	306	4	128	305	17	10 MB
2	615	4	300	615	17	20 MB
3	615	6	300	615	17	31 MB
4	940	8	512	940	17	62 MB
5	940	6	512	940	17	47 MB
6	615	4	65535	615	17	20 MB
7	462	8	256	511	17	31 MB
8	733	5	65535	733	17	30 MB
9	900	15	65535	981	17	112 MB
10	820	3	65535	828	17	20 MB
11	855	5	65535	855	17	35 MB
12	855	7	65535	855	17	50 MB
13	306	8	128	319	17	28 MB
14	733	7	65535	733	17	43 MB
16	612	4	0	663	17	20 MB
17	977	5	300	977	17	41 MB
18	977	7	65535	977	17	57 MB
19	1024	7	512	1024	17	60 MB

Type	Cyln	Head	WPcom	LZone	Sect	Size
20	733	5	300	732	17	30 MB
21	733	7	300	732	17	43 MB
22	733	5	300	733	17	30 MB
23	306	4	0	336	17	10 MB
24	925	7	0	925	17	54 MB
25	925	9	65535	925	17	69 MB
32	1024	15	65535	1024	17	128 MB
33	1024	5	1024	1024	17	43 MB
34	612	2	128	612	17	10 MB
35	1024	9	65535	1024	17	77 MB
36	1024	8	512	1024	17	68 MB
37	615	8	128	615	17	41 MB
38	987	3	987	987	17	25 MB
39	987	7	987	987	17	57 MB
40	820	6	820	820	17	41 MB
41	977	5	977	977	17	41 MB
42	981	5	981	981	17	41 MB
43	830	7	512	830	17	48 MB
44	830	10	65535	830	17	69 MB
45	917	15	65535	918	17	114 MB
46	1224	15	65535	1223	17	152 MB

- "Not Installed" is available for Use as an Option. This option could be Used for diskless workstations and SCSI hard disks. Type 47 may be used for both hard disks C: and D:.

- The parameters for type 47 under Hard Disk C: and Hard Disk D: may be different, which effectively allows 2 different user-definable hard disk types.

- Floppy Drive A and Floppy Drive B: The Options are 360 KB 5 1/4", 1.2 MB 5 1/4", 720 KB 3 1/2", 1.44 MB 3 1/2", and not Installed. Not Installed could be used as an option for diskless workstations.

- Primary Display: Options are Monochrome, Color 40 x 25, VGA/PGA/EGA, Color 80 x 25, and Not Installed. The "Not Installed" option could be used for network files servers.

- Keyboard: Options are Installed or Not Installed.

3-3 Advanced CMOS Setup

The Advanced CMOS Setup program is equipped with a series of help screens, accessed by the <FI > key, which will display the options available for a particular configuration feature and special help for some of the options.

The options for the following features of the Advanced CMOS setup are either "Disabled" or "Enabled:"

Typematic Rate Programming
Extended Memory Test
Memory Test Tick Sound
Memory Parity Error Check
Hit < ESC > Message Display

Wait for < FI > If Any Error

Internal/External Cache Memory
(486) or Cache Memory (386)
*Fast Gate A20 Option

*Video or Adapter ROM Shadow
*GA20 Line After System Boot

The options for the following features of the Advanced CMOS setup are either "Present" or "Absent:"

Numeric Processor
Weitek Processor

The options for Power-On Up Num Lock are "On" or "Off."

The options for System Boot Up Speed are "High" or "Low."

NOTE

Depending on the particular hardware and chip set combination of each individual system, the options in Figure 3.9 may or may not appear on the Setup Screen or they may not appear in the same order. There may also be more options for your system than those shown on the Setup screen.

See Figure 3.9 for generic screen sample.

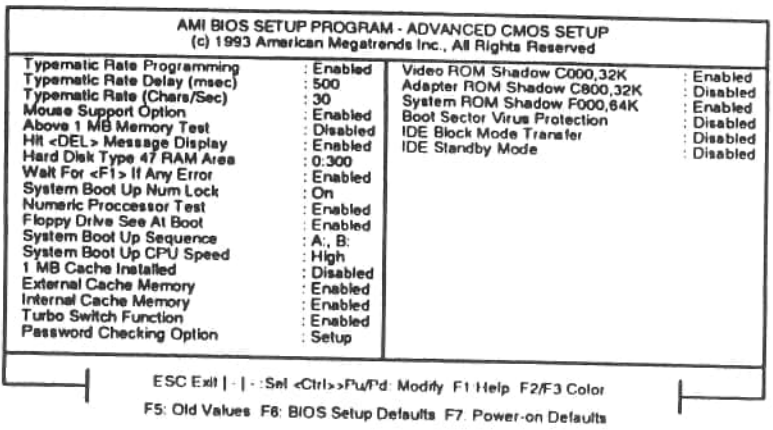


Fig. 3.9
Advanced CMOS Setup Screen

A short description follows for each of the options on the Advanced CMOS Setup Screen.

Typematic Rate Programming: By enabling this option, the user can adjust the rate at which a keystroke is repeated. The options "Typematic Rate Delay" and "Typematic Rate" affect this rate. When a key is pressed and held down, the character appears on the screen and after a delay set by the Typematic Rate Delay, it keeps on repeating at a rate set by the Typematic Rate value. When two or more keys are pressed and held down simultaneously, only the last key pressed will be repeated at the typematic rate. This stops when the last key pressed is released, even if other keys are depressed.

See figure 3. 1 0 and 3.1 1 for the values for these rates.

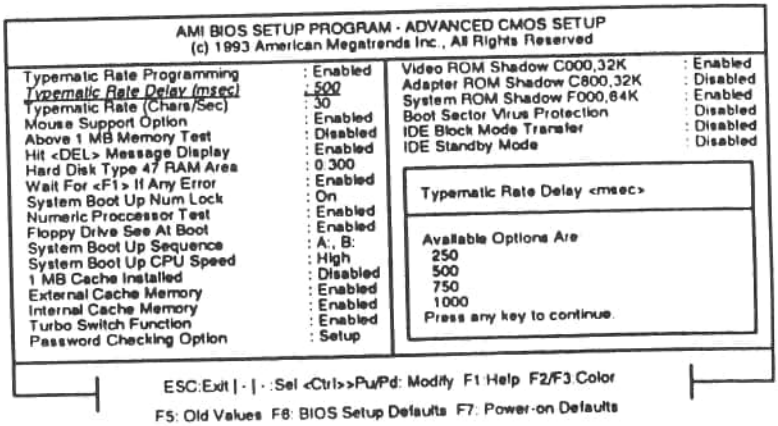


Fig. 3.10
Typematic Rate Delay Help Screen

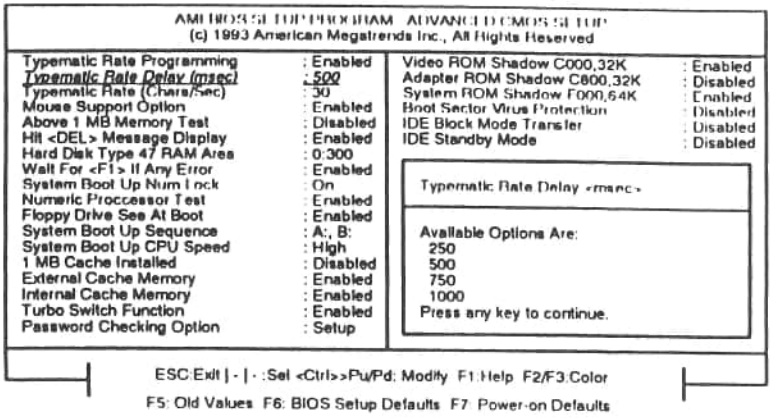


Fig. 3.11
Typematic Rate Help Screen

Extended Memory Test: This feature, when enabled, will invoke the POST memory routines on the RAM above 1 MB (if present on the system). If disabled, the BIOS will only check the first 1 MB of RAM.

Memory Test Tick Sound: This option will enable (turn on) or disable (turn off) the "ticking" sound during the memory test.

Memory Parity Error Check: If the system board does not have parity RAM, the user may disable the memory parity error checking routines in the BIOS. The user should check with the manufacturer regarding the proper setting of this option.

Hit < ESC > Message Display: Disabling this option, will prevent the message:

```
"Hit < ESC > if you want to run SETUP"
```

from appearing on the screen when the system boots-up.

Hard Disk Type 47 Data Area: The AMI BIOS SETUP features two user-definable hard disk types. Normally, the data

for these disk types are stored at 0:300 in lower system RAM. If a problem occurs with other software, this data can be located at the upper limit of the DOS shell (640 KB). If the option is set to "DOS 1 KB," the DOS Shell is shortened to 639 KB, and the top KB is used for the hard disk data storage. Please refer to Figure 3.12 for this option.

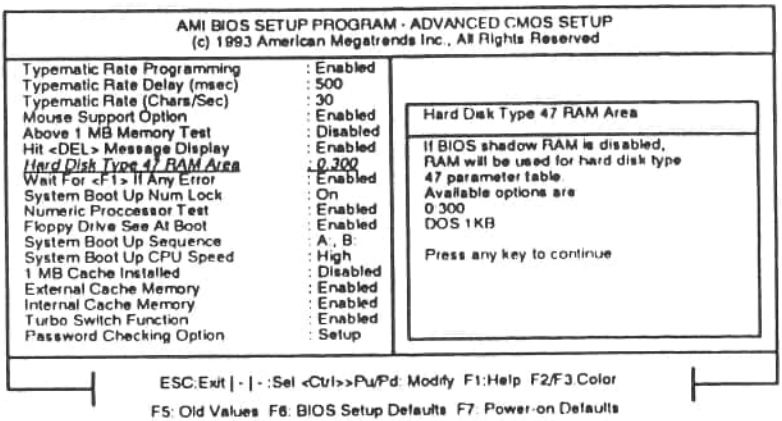


Figure 3.12
Hard Disk Type 47 Data Area Help Screen

Wait for F1 If Any Error: Before the system boots-up, the BIOS will execute the POST routines, a series of system diagnostic routines. If any of these tests fail, but a non-fatal error has occurred and the system can still function, the BIOS will respond with an appropriate error message followed by the following statement:

"Press < F1 > to continue."

If this option is disabled, any non-fatal error which occurs will not generate the above statement, but the BIOS will still display the appropriate error message. This will eliminate the need for any user response to a non-fatal error condition message. A list of error messages and their corresponding explanations appears in Appendix E.

System Boot Up Num. Lock: The user may turn off the "num. lock" option on his Enhanced Keyboard when the system is powered on. This will allow him to use the arrow keys on the numeric keypad instead of using the other set of arrow keys on the Enhanced Keyboard. The BIOS will default to turning the "num lock" on.

Numeric/Weitek Processor(s): These options allow the user to mark the numeric processor (INTEL 80X87 or compatible) or the Weitek numeric processor (WTL3167 or 4167) as present or absent.

Floppy Drive Seek At Boot: The default for this option is "Disabled" to allow a fast boot and to decrease the possibility of damage to the heads.

System Boot Up Sequence: The AMI BIOS will normally attempt to boot from floppy drive A: (if present), and if unsuccessful, it will attempt to boot from hard disk C: This sequence can be switched using this option. If the option is set to "C:, A:," the system will attempt to boot from the hard drive C:, and then A:. If the option is set to "A:, C:," the sequence is reversed. Please refer to Figure 3.13 for this option.

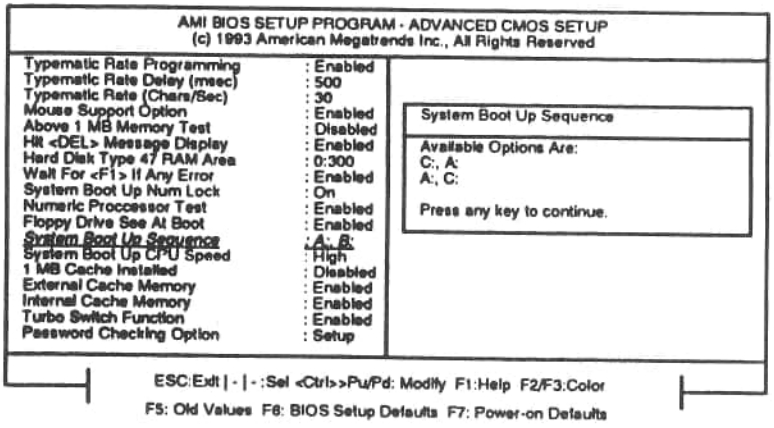


Fig. 3.13 - System Boot Up Sequence Help Screen

System Boot UP CPU Speed: The speed at which the system will boot up is determined with this option. Choices for this option are "high" or "low." The default speed is "low."

Password Check Option: Controlled by the system manufacturer's preferences, the password feature can be used to prevent unauthorized system boot-up or unauthorized use of BIOS SETUP. The option in the BIOS SETUP only allows the user to enable the password check option every time the system boots or upon entering SETUP only. A third option is to disable the password option entirely. See Figure 3.14.

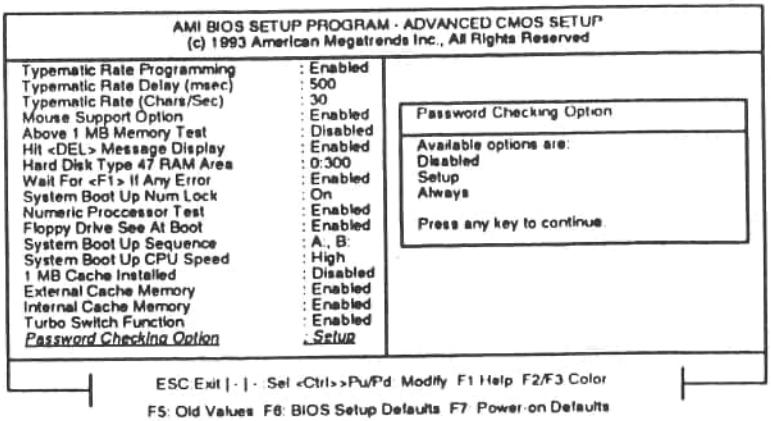


Fig. 3.14
Password Checking Option Screen

The default option is "Disabled." The prompt for the password will not appear when the system is re-booted.

If the "Always" option is chosen at Setup, each time the system is turned on, i.e. "booted," the prompt for user password will appear.

If the "Setup" option is chosen at Setup, the password prompt will not appear when the system is turned on, but will appear if the user attempts to enter the Setup program.

The program allows three attempts to key in the correct password. After each incorrect attempt, the prompt to enter the current password will appear, followed by an "X." After the third incorrect attempt, the system will lock and it will be necessary to reboot. The screen will not display the characters entered.

See Section 3-5 for instructions on changing the user password.

NOTE

Your system hardware may not be equipped with some or all of the following options and, therefore, may or may not appear on the BIOS SETUP Program screen. Refer to Appendix C for more detailed information on your particular system and/or chip set.

The Internal Cache Memory and External Cache Memory options should appear on 486TM systems. On 386TM systems, the option appearing on the screen will be Cache Memory Controller.

Internal Cache Memory: This option will appear only on 486TM systems which use CPU's (Central Processing Units) with an internal cache structure. With this option, the user may enable or disable the internal cache of the system's CPU.

External Cache Controller: This option appears only on 486TM systems which can have a caching scheme external to the CPU. With this option, the user may specify whether the external cache is present or absent.

Fast Gate A20: This option uses the fast gate A20 line supported In some chip sets, to access any memory above 1 MB. Normally, all RAM access above 1 MB is handled through the keyboard controller chip. Using this option will make the access faster than the normal method. This option is very useful in networking operating systems.

Video or Adapter ROM Shadow: ROM shadow Is a procedure in which BIOS code is copied from slower ROM to faster RAM. The BIOS is then executed from the RAM. These options are chip set specific and are dependent on the system hardware. They may or may not appear on the BIOS screen. Each option, when it does appear, allows for a segment of 16 KB to be shadowed from ROM to RAM. If one of these options Is enabled, and there is BIOS present in that particular 16 KB segment, the BIOS will be shadowed.

System ROM Shadow: The same concept applies here as above, except that in this case, the system BIOS (64 KB In length) is shadowed.

GA20 LIne After System Boot: This option will enable or disable the use of Gate A20 after the system has booted. Gate A20 is an alternate method for accessing system RAM above 1 MB.

3-4 Advanced Chip Set Setup

This portion of the BIOS Setup is entirely chip set specific and requires detailed knowledge about the PC system. This option is used to change the register values for the chip set Registers. These registers control most of the system options in the computer.

CAUTION

Before changing any screen parameters, be sure you fully understand what you are doing; otherwise, the system may become unstable or the system speed may be degraded. If this happens, reset your system, enter the CMOS setup main screen again, and select the AUTO CONFIGURATION.

The BIOS setup screen (Figure 3.14A) will give you a basic idea of how to operate the BIOS Advanced Chip Setup program included with this system board.

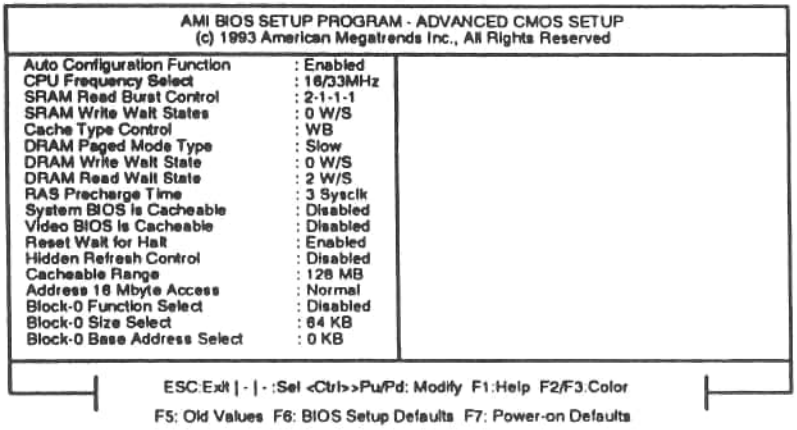


Fig. 3.14A
Advanced Chip Setup

The default AT Bus Clock is depending on the "CPU Frequency Select." For a 50 MHz System using a 50 MHz OSC, the default AT Bus Speed is 50/6=8.33 MHz when the "CPU" Frequency Select" is selected to 50 MHz. You can change the "CPU" Frequency by pushing the Page-up or Page-Down key to change the "CPU" Frequency Select". For example, if you like to change AT Bus Clock to 12.5 MHz, you can select the "CPU Frequency Select" to 33 MHz and it will be default to 50/4=12.5 MHz. For a 33 MHz system using a 33 MHz OSC System, the default AT Bus Speed is equal to 33/4=8.24 MHz if you select the CPU Frequency Select" to 16/33 MHz. The change AT Bus Speed to 5.5 MHz, you can push the Page-up or Page-down key and select the CPU Frequency Select" to 50 MHz (i.e. the default value is 33/6=5.5 MHz.)

The default value of divided by 2, 2.5,3,4, or 6 is controlled by the selection of "CPU Frequency Select" and is summarized as follow:

CPU Frequency Select	**Default "Divided Value"**
50 MHz	6
16/33 MHz	2 for 16 MHz OSC, 4 for 33 MHz OSC
25 MHz	3
20 MHz	2.5

3-5 Change Password

This BIOS SETUP program has a new optional password feature. The system may be configured so that the user is required to enter a password every time the system boots, or whenever an attempt is made to enter the SETUP programs. The password function may also be disabled, which means that the prompt will not appear under any circumstances.

This section of the manual deals with changing the user password. The password check function is enabled or disabled in Advanced CMOS Setup (refer to Section 3-3 for a more detailed view), The password check function is enabled by choosing either "Always" or "Setup."

The password, which will be stored in the CMOS, cannot exceed 6 characters in length. A default password, to be used if the CMOS is corrupted, is stored in the ROM. The default password is <AMI>. Check your system documentation in the event the default password has been changed by your system dealer.

To change the user password, select the Change Password option from the main Setup screen, by using the arrow keys to move the cursor to this selection and pressing < ENTER >
The screen in Figure 3.15 will appear.

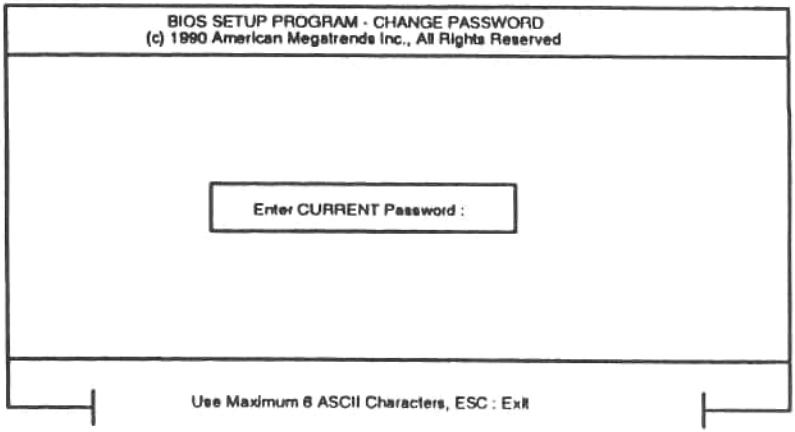


Fig. 3.15
Password Opening Screen

The first time you select this option, enter the default password < AMI >, or the default password specified in your system documentation, then press < ENTER > to complete your selection.

The screen will not display the characters entered. After the current password has been correctly entered, the screen in Figure 3.16 will appear, prompting you for the new password.

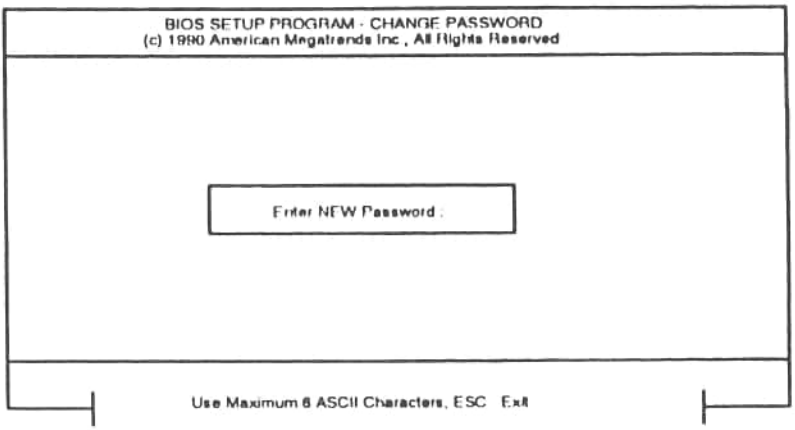


Figure 3.16
New Password Screen

After the new password Is entered, the prompt in Figure 3.17 will appear. Re-enter the new password and press < ENTER >.

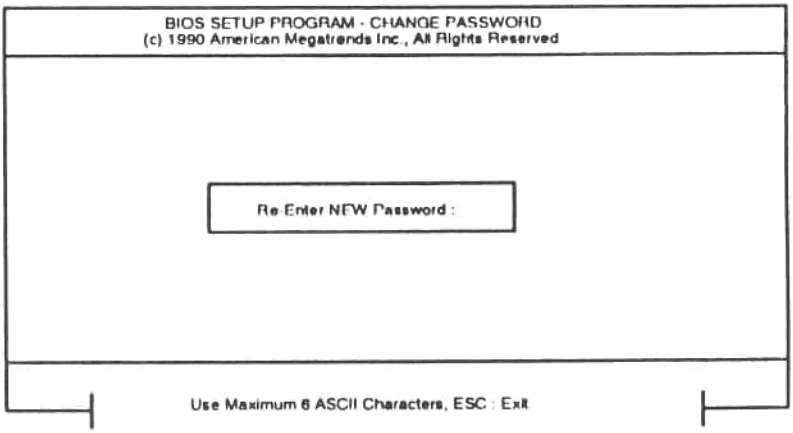


Figure 3.17
Password Confirmation Screen

If the password confirmation is erratic (miskeyed), the error

screen in Figure 3.18 will appear. If the new password confirmation is entered without error, the screen in Figure 3.19 will appear. Press <ESC> to return to the Main Setup menu.

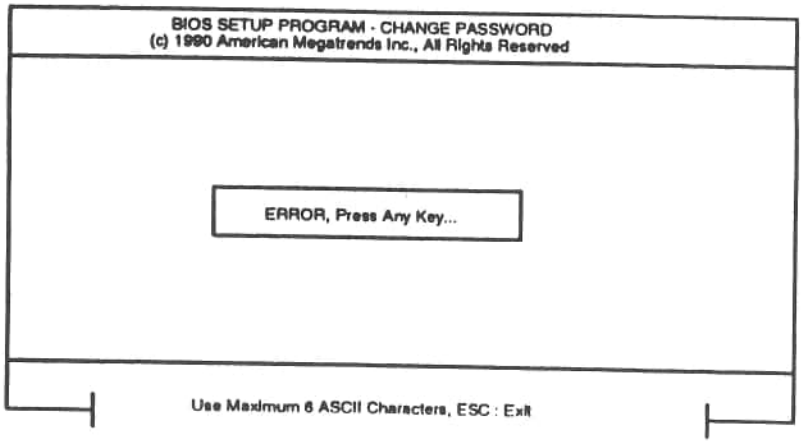


Figure 3.18
Password Error Screen

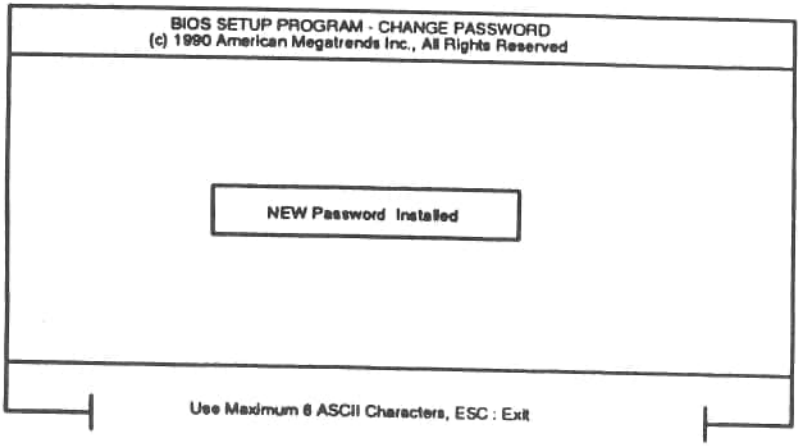


Figure 3.19
Password Installation Confirmation Screen

Once Setup is completed and the changed values have been stored in the CMOS, when the system next boots the user will be prompted for the password if the password function is present and has been enabled.

When and if the prompt appears is dependent upon the options chosen in Advanced CMOS Setup:

If the "Always" option was chosen in Advanced CMOS Setup, the prompt will appear each time the system is powered on.

If the "Setup" option was chosen in Advanced CMOS Setup, the prompt will not appear when the system is powered on, but will appear each time an attempt is made to enter the Setup program.

If the "Disabled" option was chosen in Advanced CMOS Setup, the password prompt will never appear.

When the password prompt appears, the new password, which is now stored in the CMOS, should be entered and the < Enter > key pressed. If the CMOS is corrupted, e.g., the batteries fall out or are loosened, the default ROM password mentioned above should be used instead.

NOTE

When the password is changed, however, it is important that a record of the change be kept in a safe place. In the event the password check has been enabled in Setup and the user forgets or loses the new password, the default password stored in the ROM cannot be used unless the CMOS is disabled. A relatively safe way to do this would be to disconnect the CMOS batteries.

3-6 Hard Disk Utility

CAUTION

Performing the Hard Disk Format, Auto Interleave, and/or Media Analysis will destroy any data on the hard disk registered. Back up the hard disk(s) before actually performing any of these routines.

Notice that these routines are not valid for a SCSI Disk Drive.

The Hard Disk Format option performs a 'low level' format of the hard drive(s). The user should check with the system or hard drive manufacturer to determine If this option should be taken.

The **Auto Interleave** option determines the optimum interleave factor prior to the format of the hard drive(s).

The **Media Analysis** option performs an analysis of each track of the hard drive to determine whether it is usable. If it is not usable, the track is marked as "bad" so that data cannot be stored there in the future.

A more detailed explanation of the above options is found in the individual sections on the options. See Appendix F for a list of error messages which may occur during these procedures.

If you are installing a **new, unused hard disk (drive)**, the manufacturer of the hard drive usually provides a list of "bad tracks" with the hard drive. Your system documentation might also include the optimum interleave factor.

In this case, assuming that you have a list of bad tracks and know the interleave factor, it will not be necessary to take the auto interleave and media analysis options. Simply follow the instructions in the **Hard Disk Format** section below. If you have a bad track list but have not been provided with the optimum interleave factor, follow the instructions in the **Auto Interleave** section.

If you are installing a used hard disk or reformatting an existing hard disk, perform the Media Analysis and then follow the instructions in the Auto Interleave section.

Once the Hard Disk Diagnostics option is taken by pressing < ENTER > at the Main Setup Menu, the screen in Figure 3.20 will appear.

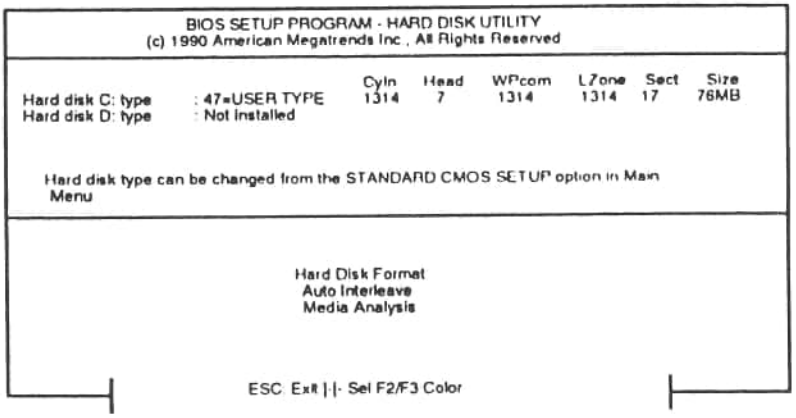


Figure 3.20
Hard Disk Utility Setup Screen

Use the Arrow Keys to select one of the three options and press < ENTER >.

Hard Disk Format Utility

WARNING !!

Performing the Hard Disk Format, Auto Interleave, and/or Media Analysis will destroy any data on the hard disk being tested. Back up the hard disk(s) before actually performing any of these routines.

NOTE: This routine is not valid for a SCSI Disk Drive.

Use the Hard Disk Format option to integrate a new hard disk to the system, or to reformat a used hard disk which has developed some bad patches as a result of aging or poor handling. To find these bad patches on a used drive, you may select the Media Analysis option.

When you press < ENTER > at the Hard Disk Format option, the Screen in Figure 3.21 appears.

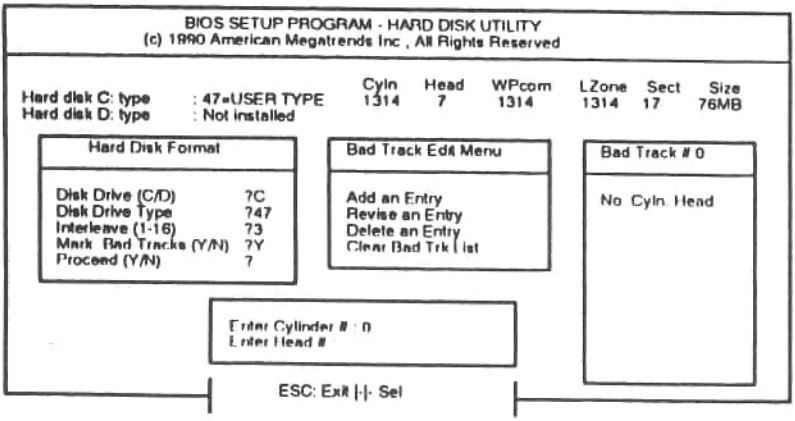


Figure 3.21
Hard Disk Format Screen

The box on the left of the screen contains a series of questions (prompts) which must be answered before performing the Hard Disk Format. The first two questions may already have been answered for you if the value was previously entered for one disk only at the Standard CMOS Setup screen.

The value for Disk Drive is C for a C: Drive or D for a D:Drive. If two disk drives have been previously entered at the Standard CMOS Setup Screen, then the ID (C/ D) will appear to the right of the question mark following the Disk Drive field. Choose which drive you wish to format by selecting the appropriate letter and pressing < ENTER >. If only one drive was selected at the Standard CMOS Setup screen, the cursor will automatically be placed at the interleave prompt.

The Disk Drive Type is read from the CMOS. The interleave factor can be selected manually, or can be determined with the Auto Interleave feature of the SETUP program.

The manufacturer of the hard drive usually provides a list of "bad tracks" with the hard drive. These tracks should be entered with this option, and they will then be marked as "bad" in order to prevent data from being stored there in the future.

The screen in Figure 3.22 is displayed when the prompt to Mark Bad Tracks is changed to < Y > and the < ENTER > key is pressed and an option to add, delete, revise, or clear is selected from the Bad Track Edit Menu.

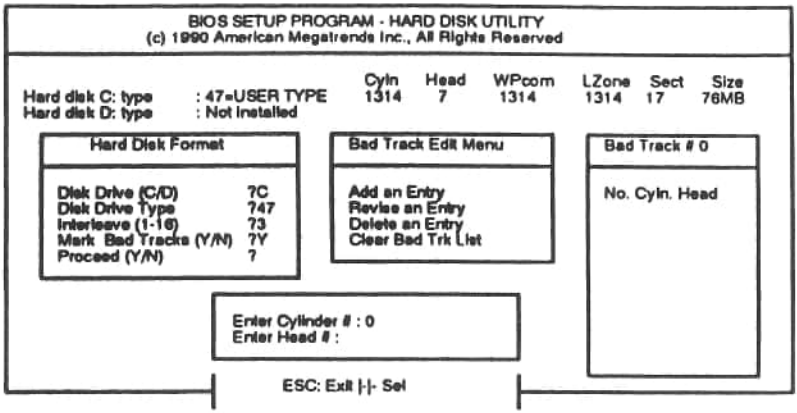


Figure 3.22 - Hard Disk Utility Options

When the Proceed prompt is changed to < Y > and the < ENTER > key pressed, the warning screen in Figure 3.23 will be displayed. The default for the Continue prompt is < N > to prevent accidental formatting of the hard drive and subsequent loss of data.

Once this prompt is changed to < Y > and the < ENTER > key pressed, any data residing on the hard drive will be irrevocably lost.

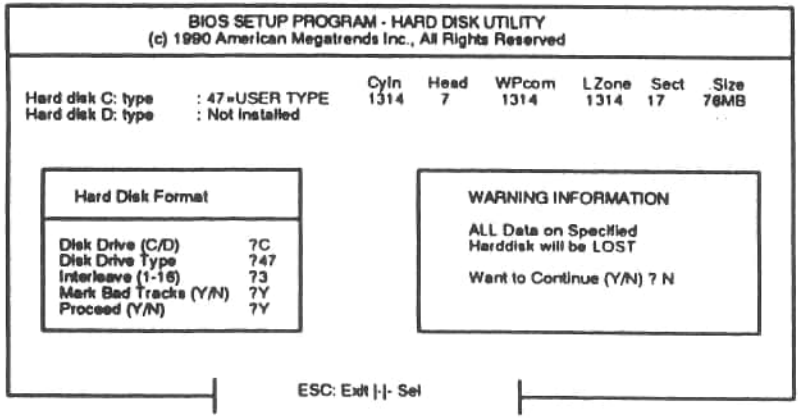


Figure 3.23 - Hard Disk Format Warning Screen

Media Analysis Utility

WARNING!!
Performing the Hard Disk Format, Auto Interleave, and/or Media Analysis will destroy any data on the hard disk being tested. Back up the hard disk(s) before actually performing any for these routines.

NOTE: These routines are not valid for a SCSI Disk Drive.

The Media Analysis utility performs a series of tests to locate bad or damaged patches on the hard disk as a result of aging or poor handling. This utility locates all bad tracks on the hard disk and lists them in the Bad Track List Box. Since this test writes to all cylinders and heads on the hard disk to verify any bad tracks, the test may require several minutes to complete. For best results, run this test in its entirety.

To run the Media Analysis utility, use your arrow keys to select the option from the main Hard Disk Utility Menu and press < ENTER >. The screen shown in Figure 3.24 will appear.

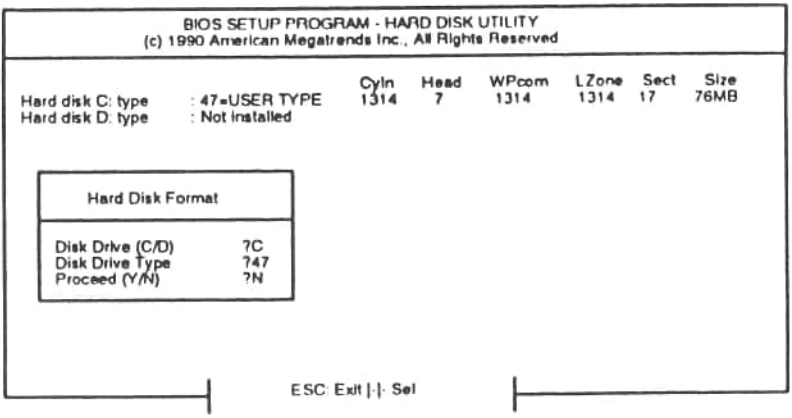


Figure 3.24
Media Analysis Screen

The cursor will appear at the Proceed prompt. When you press < ENTER >, the warning screen in (Figure 3.25) will appear.

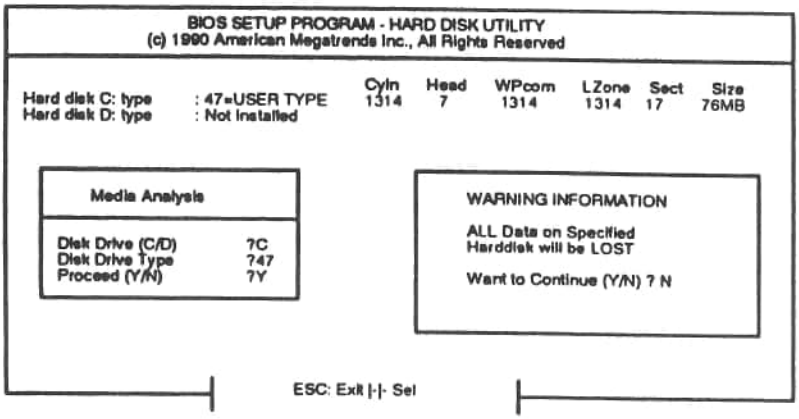


Figure 3.25
Media Analysis Warning Screen

If you do not wish to proceed at this point, press the < Enter > key and you will be returned to the main Hard Disk Utility screen. If you wish to proceed with the analysis, change the prompt to < Y > and press < Enter >.

Auto Interleave Utility

!!WARNING!!
Performing the Hard Disk Format, Auto Interleave, and/or Media Analysis will destroy any data on the hard disk being tested. Back up the hard disk(s) before actually performing any of these routines.

NOTE: These routines are not valid for a SCSI Disk Drive.

The Auto Interleave utility calculates the optimum interleave value through trial and error by measuring the transfer rate for four different interleave values. To determine the best interleave factor, the system will format a portion of the hard disk for each transfer rate calculated. The cylinders, heads and sectors formatted for each value will be displayed in the activity box on the screen.

To begin the Auto Interleave process, use your arrow keys to select this function on the main Hard Disk Utility Screen (Figure 3.20). Press < ENTER > to select this option. The screen in Figure 3.26 will appear.

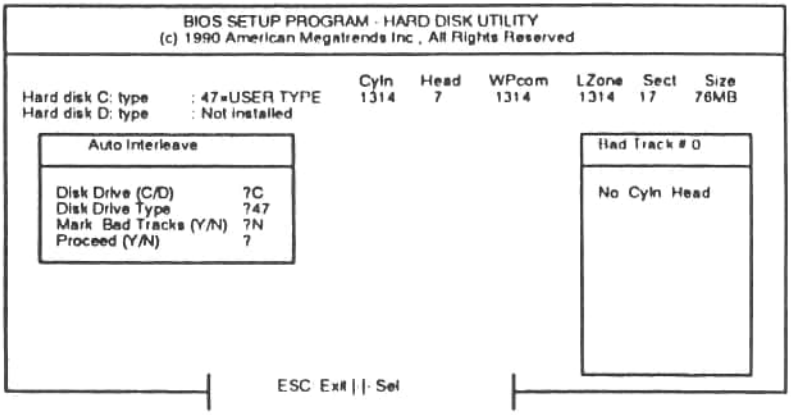


Figure 3.26
Interleave Utility Options

The cursor will be placed at the Mark Bad Tracks prompt. The default for this prompt is < N >. To mark additional bad tracks, change the prompt to < Y > and press < ENTER >.

Power Management Setup

- Green-PC Time Delay is programmable by the user. The manufacture default is set as "Disabled." The user needs to use the "UP/PD" key to change the default setting and to define the desired "delay" time.

- Monitor-Off Time Delay is also user-definable. The default setting is "disabled." Please use the "UP/PD" key to enter the new desired "Monitor-Off Time" default setting.

Auto Detect Hard Disk

The parameter setting of the IDE hard drive can be programmed automatically or manually. To set the parameter setting manually, select the Standard CMOS Setup.

Chapter 4

Troubleshooting

4-1 Troubleshooting Procedures

If you should encounter problems, use the following procedures to troubleshoot your system.

No Video

Use the following steps for troubleshooting your system configuration.

1. Check all cable connections..
2. Check for missing jumpers or improper installation of the ROM BIOS.
3. Make sure the video card and its jumper setting (as appropriate) match the monitor type.
4. Ensure that all peripheral cards are properly installed in their slots.

6. Ensure that the I/O Bus speed is running in the standard 8 MHz range.

7. Use the speaker to determine if any beep codes exist. Refer to Appendix C for details about beep codes.

NOTE

If you are a system integrator, VAR, or OEM, a POST diagnostics card is recommended for Port 80h codes. (Refer to Appendix D.)

Memory Error/Parity Error

If you encounter memory or parity errors, follow the procedures below.

1. Check to determine if SIMM modules are improperly installed.

2. Make sure that different types of SIMM's have not been installed in the same bank, (e.g., a mixture of 265 KB x 9 and 1 MB x 9).

3. Determine if different speeds of SIMM'S have been installed in the same or different banks and the BIOS setup is configured for the fastest speed of RAM used. It is recommended to use the same RAM speed for SIMM'S in different banks.

4. Check for bad SIMM modules or chips.

5. Ensure that cache memory jumpers are correctly set to enable the cache memory.

Losing the System's Setup Configuration

1. Ensure that you are using a high quality power supply. A poor quality power supply may cause the system to lose CMOS setup. Refer to Chapter 1 of this manual for details.
2. Determine if the rechargeable battery is bad. If it is bad, connect four AA-type batteries to JP2.
3. If the above steps do not fix the Setup Configuration problem, contact your vendor for repair.

Appendix A

Technical Specifications

A-1 System Specifications

CPU:

Intel 80486DX, 80486DX2, 80486SX, 80487SX or Over-Drive, including Intel P23T and P24T CPUs

Coprocessor:

- On-chip floating point Math coprocessor (for 80486DX, 80486DX2 or 80487SX)

Cache:

- 8 K-byte on-chip 4-way set associative cache
- 256 KB/512 KB/1 MB burst mode Write-back secondary cache on-board to support 0-wait state CPU speed
- Four blocks of non-cacheable memory area

Memory:

- 128 MB SIMM socket on-board
- Supports 16 MB x 9, 4 MB x 9, 1 MB x 9 and 256 KB x 9 SIMM modules (mixed banks)
- Supports page mode and 2 way page interleave mode

Turbo:

- Hardware turbo switch available

- Turbo Light

BIOS:

- Supports AMI BIOS
- Built-in setup functions
- Supports shadow RAM and 256 KB of memory remapping
- Software programmable DRAM wait states
- Fast Reset and gate A20 to optimize OS/2

Software Compatibility:

- 100% IBM PC/AT compatible
- DOS, UNIX, XENIX, Windows 3.0, Novell, and OS/2

Battery:

On-board rechargeable battery for real time clock and CMOS setup

Speed and Ratings:

Designed to work at 66, 50, 40, 33 and 25 MHz in a 486DX/ DX2/SX- or 487SX-based system

	CG486VL 486DX 50	CG486VL 486DX2-66	CG486VL 486DX/SX 33	CG486VL 486SX 25
CPU Clock Speed	50 MHz	33 MHz	33 MHz	25 MHz
CPU	486DX 50	486DX2-66	486DX/SX 33	486SX 25
I/O Bus Speed	8.33 MHz	8.33 MHz	8.33 MHz	8.33 MHz
Performance Rating				
Landmark V1.14	200+	200+	152	114.1
Norton SI V4.5	83.1	110.6	57.7	39
Power Meter (V1.7)	22.3	27.3	14.76	11.1

Table A-1. System Board Speeds and Ratings

A-2 Memory Address Map

Address (Hex)	Size	Function
0000000 - 009FFFF	640 KB	System board memory
00A0000 - 00BFFFF	128 KB	Video RAM display buffer
00C0000 - 00DFFFF	128 KB	Reserved for add-on cards ROM BIOS, i.e., V/EGA
00E0000 - 00EFFFF	64 KB	System ROM BIOS expansion
00F0000 - 00FFFFF	64 KB	System ROM BIOS
0100000 - 0FDFFFF	32 KB	Extended memory
0FE0000 - 0FEFFFF	64 KB	Duplicates of System ROM BIOS expansion at 0E0000 - 0EFFFF
0FF0000 - 0FFFFFF	64 KB	Duplicates of System ROM BIOS at 0F0000 - 0FFFFFF
1000000 - 7FFFFFF	112 MB	Extended memory
0000000 - 7FFFFFF	**128 MB**	**Total memory space addressable by *CG486VL* System Board**

Table A-2. Memory Address Map

A-3 I/O Address Map

The I/O Address Map for the System board is locations 00-FFh,and for I/O it is 100h - 3ffh, as follows:

Address	Function
000 - 01F	DMA controller 1, 8237A-5
020 - 021	Interrupt controller 1, 8259A, Master
022 - 023	Chipset Address
040 - 04F	Timer 1, 8254
050 - 05F	Timer 2, 8254
060 - 06F	8042 keyboard/controller
070 - 07F	Real Time Clock (RTC), Non-Maskable Interrupt (NMI) mask
080 - 09F	DMA page registers
0A0 - 0BF	Interrupt controller 2, 8259A
0C0 - 0DF	DMA controller 2, 8237A - 5
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
1F8 - 0FF	Math Coprocessor
1F0 - 1F8	Fixed Disk
200 - 207	Game Ports
278 - 27F	Parallel printer port 2 (PIO-2)
2F8 - 2FF	Serial Port 2 (SIO-2)
300 - 31F	Prototype Card/Streaming Tape Adapter
360 - 363	PC Network, Low Address
368 - 36B	PC Network, High Address
378 - 37F	Parallel Printer Port 1 (PIO-1)
380 - 38F	SDLC, Bisynchronous 2
3A0 - 3AF	Bisynchronous 1
3B0 - 3BF	Monochrome Display and Printer Adapter
3C0 - 3CF	EGA Adapter
3D0 - 3DF	Color/Graphics Monitor Adapter
3F0 - 3F7	Diskette Controller
3F8 - 3FF	Serial Port 1 (SIO-1)

Table A-3. I/O Address Map

A-4 I/O Expansion Slots

Input/output direction is determined from the system board's viewpoint. "I" is input from the I/O bus to the system board. "O" is output from the system board to the I/O bus.

Ground	GND	B1	A1	-I/O CHCK	I
O	RESET DRV	B2	A2	SD7	I/O
Power	+5 Vdc	B3	A3	SD6	I/O
I	IRQ 9	B4	A4	SD5	I/O
Power	-5 Vdc	B5	A5	SD4	I/O
I	DRQ2	B6	A6	SD3	I/O
Power	-12 Vdc	B7	A7	SD2	I/O
I	0WS	B8	A8	SD1	I/O
Power	+12 Vdc	B9	A9	SD0	I/O
Ground	GND	B10	A10	-I/O CHRDY	I
O	-SMEMW	B11	A11	AEN	O
O	-SMEMR	B12	A12	SA19	I/O
I/O	-IOW	B13	A13	SA18	I/O
I/O	-IOR	B14	A14	SA17	I/O
O	-DACK3	B15	A15	SA16	I/O
I	DRQ3	B16	A16	SA15	I/O
O	-DACK1	B17	A17	SA14	I/O
I	DRQ1	B18	A18	SA13	I/O
I/O	-REFRESH	B19	A19	SA12	I/O
O	CLK	B20	A20	SA11	I/O
I	IRQ7	B21	A21	SA10	I/O
I	IRQ6	B22	A22	SA9	I/O
I	IRQ5	B23	A23	SA8	I/O
I	IRQ4	B24	A24	SA7	I/O
I	IRQ3	B25	A25	SA6	I/O
O	-DACK2	B26	A26	SA5	I/O
O	T/C	B27	A27	SA4	I/O
O	BALE	B28	A28	SA3	I/O
Power	+5 Vdc	B29	A29	SA2	I/O
O	OSC	B30	A30	SA1	I/O
Ground	GND	B31	A31	SA0	I/O
I	-MEMCS16	D1	C1	-BHE	I/O
I	-I/OCS16	D2	C2	LA23	I/O

Continued on next page...

I	IRQ10	D3	C3	LA22	I/O
I	IRQ11	D4	C4	LA21	I/O
I	IRQ12	D5	C5	LA20	I/O
I	IRQ15	D6	C6	LA19	I/O
I	IRQ14	D7	C7	LA18	I/O
O	-DACK0	D8	C8	LA17	I/O
I	DRQ0	D9	C9	-MEMR	I/O
O	-DACK5	D10	C10	-MEMW	I/O
I	DRQ5	D11	C11	SD08	I/O
O	-DACK6	D12	C12	SD09	I/O
I	DRQ6	D13	C13	SD10	I/O
O	-DACK7	D14	C14	SD11	I/O
I	DRQ7	D15	C15	SD12	I/O
Power	+5 Vdc	D16	C16	SD13	I/O
I	-MASTER	D17	C17	SD14	I/O
Ground	GND	D18	C18	SD15	I/O

A-5 82C206 Integrated Peripheral Controller (IPC)

Details for the Integrated Peripheral Controller (IPC) chip Direct Memory Address (DMA) channels, controller registers, page register addresses, interrupts and timer/counter are given below.

DMA Channels

Channel	Function
0	Spare (8-bit, 64 KB block transfer)
1	SDLC (8-bit, 64 KB block transfer)
2	Floppy Disk (8-bit, 64 KB block transfer)
3	Spare (8-bit, 64 KB block transfer)
4	Cascade for DMA controller 1
5	Spare (16-bit, 128 KB block transfer)
6	Spare (16-bit, 128 KB block transfer)
7	Spare (16-bit, 128 KB block transfer)

DMA Controller Registers

Address (Hex)	Command Code
C0	CH0 base and current address
C2	CH0 base and current word count
C4	CH1 base and current address
C6	CH1 base and current word count
C8	CH2 base and current address
CA	CH2 base and current word count
CC	CH3 base and current address
CE	CH3 base and current word count
D0	Read Status Register/Write Command Register
D2	Write Request Register
D4	Write Single Mask Register Bit
D6	Write Mode Register
D8	Clear Byte Pointer Flip-Flop
DA	Read Temporary Register/Write Master Clear
DC	Clear Master Register
DE	Write All Mask Register Bits

Page Register Addresses

Page Register	I/O Address (Hex)
DMA Channel 0	87
DMA Channel 1	83
DMA Channel 2	81
DMA Channel 3	82
DMA Channel 5	8B
DMA Channel 6	89
DMA Channel 7	8A
Refresh	8F

Interrupt Controller

Level	Function
NMI	System memory parity error or I/O channel check
0	System timer 0 output
1	Keyboard Output buffer full
2	Interrupt from controller 2 (levels 8-15)
8	Real-time clock
9	Software re-direct to INT 0AH from hardware IRQ2
10	Reserved
11	Reserved
12	Reserved
13	Coprocessor interrupt
14	Hard disk controller
15	Reserved
3	Serial port 2
4	Serial port 1
5	Parallel port 2
6	Floppy disk controller
7	Parallel port 1

Timers/Counters

Channel	Function	
0	System Timer	
	Gate 0:	Always Enabled
	Clock In 0:	1.19 MHz clock
	Clock Out 0:	IRQ 0

Timers / Counters (cont.)

Channel	Function
1	Memory Refresh Request/Generator Gate 1: Always Enabled Clock In 1: 1.19 MHz clock Clock Out 1: Refresh request cycle
2	Speaker Tone Generator Gate 2: Bit 0 of I/O port 61H Clock In 2: 1.19 MHz Clock Out 2: Audio frequency to speaker

CMOS RAM Address Map

Address (Hex)	Description
00 - 0D*	Real-time clock

Hex	Decimal	Function
0	0	Seconds
1	1	Second alarm
2	2	Minutes
3	3	Minute alarm
4	4	Hours
5	5	Hour alarm
6	6	Day of week
7	7	Date of month
8	8	Month
9	9	Year
A	10	Status Register A
B	11	Status Register B

Hex	Decimal	Function
C	12	Status Register C
D	13	Status Register D

Address (Hex)	Description
0E*	Diagnostic status byte
0F*	Shutdown status byte
10	Floppy Disk Drive type byte
11	Reserved
12	Fixed disk type byte, for drives C: and D:, type 1-14
13	Reserved
14	Equipment byte
15	Base memory, low byte
16	Base memory, high byte
17	Expansion memory, low byte
18	Expansion memory, high byte
19	Fixed disk C: extended byte, for type 15-47
1A	Fixed disk D: extended byte, for type 15-47
1B - 2D	Reserved
2E - 2F	CMOS RAM checksum, 2 bytes
30*	Expansion memory, low byte
31*	Expansion memory, high byte
32*	Date century byte
33*	Information flag byte set during powerup
34 - 3F	Reserved

* This byte is not included in the checksum calculation and is not part of the configuration record.

A-6 Keyboard Controller

The 8042 keyboard controller is a single chip microcomputer that interfaces between the system board and keyboard. It performs the following functions:

- o Interacts with the system powerup initialization.
- o Receives data from the keyboard, translates it into system scan codes, puts the scan codes in a data buffer, and then interrupts the system to receive the data, or waits until the system polls the status register.
- o Transmits system commands to the keyboard, and reports the keyboard response to the system.
- o Directs its I/O ports to perform control functions for the system.

Status Register

The status register is an 8-bit Read-Only register, located at 64h.

Bit	Function	Status
7	Parity Error	
	0:	Odd parity
	1:	Even parity
6	Receive Time-Out	
	0:	No timeout
	1:	Timeout
5	Transmit Time-Out	
	0:	No timeout
	1:	Timeout

Status Register (cont.)

Bit	Function	Status
4	Inhibit Switch	
	0:	Keyboard is inhibited
	1:	Data is placed in the keyboard controller's output buffer
3	Command/Data	
	0:	If data port 60h is written
	1:	If command port 64h is written
2	System Flag	
	0:	Controller will set to 0 at power on test
	1:	Controller will set to 1 after self test
1	Input Buffer Full	
	0:	Input buffer empty
	1:	Input buffer full, will become 0 after read
0	Output Buffer Full	
	0:	Output buffer empty
	1:	Output buffer full, will become 0 after read

Input Buffer:

I/O port 60h, Read-Only, 8-bit

Output Buffer:

I/O port 60h or 64h, Write-Only, 8-bit

Write 60h: Data Write
Write 64h: Command Write

Keyboard I/O Ports

The keyboard controller has two I/O ports, one for input, and the other for output. The bit definitions follow.

Bit	Function	Status
7	Keyboard Inhibit Switch	
	0:	Keyboard inhibited
	1:	Keyboard not inhibited
6	Display type	
	0:	Color adapter
	1:	Monochrome adapter
5	Reserved	
4	RAM on system board	
	0:	Disable second 256 KB system RAM
	1:	Enable second 256 KB system RAM
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	
7	Keyboard data output	
6	Keyboard clock output	
5	Input buffer empty indicator	
	0:	Input buffer not empty
	1:	Input buffer empty
4	Output buffer full	
	0:	Output buffer not full
	1:	Output buffer full
3	Reserved	
2	Reserved	
1	Gate A20	
	0:	Gate A20 inhibited
	1:	Gate A20 not inhibited
0	System Reset	
	0:	System reset
	1:	System not reset

Appendix B

BIOS Hard Disk Drive Types

AMI BIOS Hard Disk Drive Types

Type	Cyl	Heads	Write Precomp	Land Zone	Capacity
Not Installed					
1	306	4	128	305	10 MB
2	615	4	300	615	20 MB
3	615	6	300	615	31 MB
4	940	8	512	940	64 MB
5	940	6	512	940	48 MB
6	615	4	None	615	21 MB
7	462	8	256	511	31 MB
8	733	5	None	733	31 MB
9	900	15	None	901	115 MB
10	820	3	None	820	21 MB
11	855	5	None	855	36 MB
12	855	7	None	855	51 MB
13	306	8	128	319	21 MB
14	733	7	None	733	44 MB
15	000	0	000	000	00 MB
16	612	4	0	663	21 MB
17	977	5	300	977	42MB
18	977	7	None	977	58 MB
19	1024	7	512	1023	61 MB
20	733	5	300	732	31 MB

AMI BIOS Hard Disk Drive Types (continued)

Type	Cyl	Heads	Write Precomp	Land Zone	Capacity
21	733	7	300	732	42 MB
22	733	5	300	733	31 MB
23	306	4	0	336	10 MB
24	925	7	0	925	56 MB
25	925	9	None	925	72 MB
26	754	7	754	754	46 MB
27	754	11	None	754	72 MB
28	699	7	256	699	42 MB
29	823	10	None	823	71 MB
30	918	7	918	918	55 MB
31	1024	11	None	1024	98 MB
32	1024	15	None	1024	133 MB
33	1024	5	1024	1024	44 MB
34	612	2	128	612	10 MB
35	1024	9	None	1024	80 MB
37	615	8	128	615	42 MB
38	987	3	987	987	21 MB
39	987	7	987	987	60 MB
40	820	6	820	820	42 MB
41	977	5	977	977	42 MB
42	981	5	981	981	42 MB
43	830	7	512	830	50 MB
44	830	10	None	830	72 MB
45	917	15	None	918	117 MB
46	User-Defined Type				
47	User-Defined Type				

Appendix C:

BIOS Error Beep Codes

During the POST (Power On Self Test) routines, which are performed each time the system is powered on, errors may occur.

Non-fatal errors are those which, in most cases, allow the system to continue the boot up process. The error messages normally appear on the screen. See Appendix E for BIOS Error Messages.

Fatal Errors are those which will not allow the system to continue the boot up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list below correspond to the number of beeps for the corresponding error. All errors listed, with the exception of #8, are fatal errors.

No. of Beeps	Error Message
1	Refresh Failure - The memory refresh circuitry of the mother board is faulty.
2	Parity Error - A parity error was detected in the base memory (the first block of 64KB) of the system.

No. of Beeps	Error Message
3	**Base 64 KB Memory Failure** - A memory failure occurred within the first 64 KB of memory.
4	**Timer Not Operational** - Timer #1 on the system board has failed to function properly.
5	**Processor Error** - The CPU (Central Processing Unit) on the system board has generated an error.
6	**8042 - Gate A20 Failure** - The keyboard controller (8042) contains the Gate A20 switch which allows the CPU to operate in virtual mode. This error message means that the BIOS is not able to switch the CPU into protected mode.
7	**Processor Exception Interrupt Error** - The CPU on the mother board has generated an exception interrupt.
8	**Display Memory Read/Write Error** - The system video adapter is either missing or its memory is faulty. ***Please Note:** This is not a fatal error.

No. of Beeps	Error Message
9	**ROM Checksum Error** - ROM checksum value does not match the value encoded in the BIOS.
10	**CMOS Shutdown Register Read/Write Error** - The shutdown register for the CMOS memory has failed.

Appendix D

AMI BIOS POST Diagnostic Error Messages

This section describes the power-on self-tests (POST) port 80 codes for the AMI BIOS.

CHECK-POINT	DESCRIPTION OF CHECK-POINT
01	Processor register test about to start, and NMI to be disabled.
02	NMI is Disabled. Power on delay starting.
03	Power on delay completed. Any initialization before keyboard BAT is in progress.
04	Any initialization before keyboard BAT is competed. Reading keyboard SYS bit, to check soft reset/power-on.
05	Soft reset/power-on determined. Going to enable ROM, i.e., disable shadow RAM/Cache if any.

CHECK-POINT	DESCRIPTION OF CHECK-POINT
06	ROM is enabled. Calculating ROM BIOS checksum, and waiting for KB controller input buffer to be free.
07	ROM BIOS checksum passed, KB controller I/B free. Going to issue the BAT command to keyboard controller.
08	BAT command keyboard controller is issued. Going to verify the BAT command.
09	Keyboard controller BAT result verified. Keyboard command byte to be written next.
0A	Keyboard command byte code is issued. Going to write command byte data.
0B	Keyboard controller command byte is written. Going to issue Pin-23, 24 blocking/unblocking command.
0C	Pin 23, 24 of keyboard controller is blocked/unblocked. NOP command of keyboard controller to be issued next.
0D	NOP command processing is done. CMOS shutdown register test to be done next.
0E	CMOS shutdown register R/W test passed. Going to calculate CMOS checksum, and update DIAG byte.
0F	CMOS checksum calculation is done, DIAG byte written. CMOS initialize. to begin (If "INIT CMOS IN EVERY BOOT IS SET").

CHECK-POINT	DESCRIPTION OF CHECK-POINT
10	CMOS initialization done (if any). CMOS status register about to initialize for Date and Time.
11	CMOS Status register initialized. Going to disable DMA and Interrupt controllers.
12	DMA controller #1, #2 interrupt controller #1, #2 disabled. About to disable Video display and initialize port-B.
13	Video display is disabled and port-B is initialized. Chipset initialize/ auto memory detection about to begin.
14	Chipset initialization/ auto memory detection over. 8254 timer test about to start.
15	CH-2 timer test halfway. 8254 CH-2 timer test to be completed.
16	Ch-2 timer test over. 8254 CH-1 timer test to be completed.
17	CH-1 timer test over. 8254 CH-1 timer test to be completed.
18	CH-0 timer test over. About to start memory refresh.
19	Memory refresh started. Memory Refresh test to be done next.
1A	Memory Refresh line is toggling. Going to check 15 micro second ON/OFF time.

CHECK-POINT	DESCRIPTION OF CHECK-POINT
1B	Memory Refresh period 30 micro-second test competed. Base 64 KB memory test about to start.
20	Base 64 KB memory test started. Address line test to be done next.
21	Address line test passed. Going to do toggle parity.
22	Toggle parity over. Going for sequential data R/W test.
23	Base 64 KB sequential data R/W test passed. Any setup before Interrupt vector initialize about to start.
24	Setup required before vector initialization completed. Interrupt vector initialization about to begin.
25	Interrupt vector initialization done. Going to read I/O port of 8042 for turbo switch (if any).
26	I/O port of 8042 is read. Going to initialize global data for turbo switch.
27	Global data initialization is over. Any initialization after interrupt vector to be done next.
28	Initialization after interrupt vector is completed. Going for monochrome mode setting.
29	Monochrome mode setting is done. Going for Color mode setting.

2A	Color mode setting is done. About to go for toggle parity before optional ROM test.
2B	Toggle parity over. About to give control for any setup required before optional video ROM check.
2C	Processing before video ROM control is done. About to look for optional video ROM and give control.
2D	Optional video ROM control is done. About to give control to do any processing after video ROM returns control.
2E	Return from processing after the video ROM control. If EGA/VGA not found, then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. About to do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. About to look for the alternate display retrace checking.
33	Video display checking over. Verification of display type with switch setting and actual card to begin.
34	Verification of display adapter done. Display mode to be set next.

CHECK-POINT	DESCRIPTION OF CHECK-POINT
35	Display mode set completed. BIOS ROM data area about to be checked.
36	BIOS ROM data area check over. Going to set cursor for power on message.
37	Cursor setting for power on message ID complete. Going to display the power on message.
38	Power on message display complete. Going to read new cursor position.
39	New cursor position read and saved. Going to display the reference string.
3A	Reference string display is over. Going to display the Hit <ESC> message.
3B	Hit <ESC> message is displayed. Virtual mode memory test about to start.
40	Preparation for virtual mode test started. Going to verify from video memory.
41	Returned after verifying from display memory. Going to prepare the descriptor tables.
42	Descriptor tables prepared. Going to enter in virtual mode for memory test.
43	Entered in the virtual mode. Going to enable interrupts for diagnostics mode.

CHECK-POINT	DESCRIPTION OF CHECK-POINT
44	Interrupts enabled (if diagnostics switch is on). Going to initialize data to check memory remap at 0:0.
45	Data initialized. Going to check for memory remap at 0:0 and finding the total system memory size.
46	Memory remap test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640 KB memory.
48	Patterns written in base memory. Going to find out amount of memory below 1 MB memory.
49	Amount of memory below 1 MB found and verified. Going to find out amount of memory above 1 MB memory.
4A	Amount of memory above 1 MB found and verified. Going for BIOS ROM data area check.
4B	BIOS ROM data area check over. Going to check <ESC> and to clear memory below 1 MB for soft reset.
4C	Memory below 1 MB cleared. (SOFT RESET.) Going to clear memory above it.
4D	Memory above 1 MB cleared. (SOFT RESET.) Going to save the memory size.

CHECK-POINT	DESCRIPTION OF CHECK-POINT
4E	Memory test started. (NO SOFT RESET.) About to display the first 64 KB memory test.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory test below 1 MB completed. Going to adjust memory size for relocation/ shadow.
51	Memory size adjusted due to resolution/ shadow. Memory test above . 1 MB to follow.
52	Memory test above 1 MB completed. Going to prepare to go back to real mode.
53	CPU registers are saved including memory size. Going to enter into real mode.
54	Shutdown successful, CPU in real mode. Going to restore registers saved during preparation for shutdown.
55	Registers restored. Going to disable gate A20 address line.
56	A20 address line disable successful. BIOS ROM data area about to be checked.
57	BIOS ROM data area check halfway. BIOS ROM data area check to be completed.
58	BIOS ROM data area check over. Going to clear Hit <ESC> message.

CHECK-POINT	DESCRIPTION OF CHECK-POINT
59	Hit <ESC> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. About to verify from display memory.
61	Display memory verification over. About to go for DAM #1 base register test.
62	DMA #1 base register test passed. About to go for DMA #2 base register test.
63	DMA #2 base register test passed. About to go for BIOS ROM data area check.
64	BIOS ROM data area check halfway. BIOS ROM data area check to be completed.
65	BIOS ROM data area check over. About to program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. About to initialize 8259 interrupt controller.
67	8259 initialization over. About to start keyboard test.
80	Keyboard test started. Clearing out buffer, checking for stuck key. About to issue keyboard reset command.
81	Keyboard reset error/stuck key found. About to issue keyboard controller interface test command.

CHECK-POINT	DESCRIPTION OF CHECK-POINT
82	Keyboard controller interface test over. About to write command byte and initialize circular buffer.
83	Command byte written. Global data initialize done. About to check for lock-key.
84	Lock-key checking over. About to check for memory size mismatch with CMOS.
85	Memory size check done. About to display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup completed. Going to CMOS setup program.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup completed. Going to display power on screen message.
8A	First screen message displayed. About to display <WAIT...> message. Mouse check and initialization to be done next.
8B	<WAIT...> message displayed. Mouse check and initialize done. About to do Main and Video BIOS shadow.

CHECK-POINT	DESCRIPTION OF CHECK-POINT
8C	Main and Video BIOS shadow successful. Setup options programming after CMOS setup about to start.
8D	Setup options are programmed. Going for hard disk, floppy reset.
8E	Hard disk, floppy reset applied. About to go for floppy check.
8F	Floppy check returns that floppy is to be initialized. Floppy setup to follow.
90	Floppy setup is over. Test for hard disk presence to be done.
91	Hard disk presence test over. Hard disk setup to follow.
92	Hard disk setup complete. About to go for BIOS ROM data area check.
93	BIOS ROM data area check halfway. BIOS ROM data area check to be completed.
94	BIOS ROM data area check over. Going to set base and extended memory size.
95	Memory size adjusted due to mouse support, hdisk type-47. Going to verify from display memory.
96	Returned after verifying from display memory. Going to do any init before C800 optional ROM control.

CHECK-POINT	DESCRIPTION OF CHECK-POINT
97	Any initialize before C800 optional control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control.
99	Any initialization required after optional ROM test over. Going to set up timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before co-processor test.
9C	Required initialization before co-processor test is over. Going to initialize the coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after coprocessor test.
9E	Initialization after coprocessor test is completed. Going to check extd keyboard, keyboard ID and num-lock.
9F	Extd keyboard check is done, ID flag set, num-lock on/off. Keyboard ID command to be issued.
A0	Keyboard ID command is issued. Keyboard ID flag to be reset.

CHECK-POINT	DESCRIPTION OF CHECK-POINT
A1	Keyboard ID flag reset. Cache memory test to follow.
A2	Cache memory test over. Going to display any soft errors.
A3	Soft error display complete. Going to set the keyboard typematic rate.
A4	Keyboard typematic rate set. Going to program memory wait states.
A5	Memory wait states programming over. Screen to be cleared next.
A6	Screen cleared. Going to enable parity and NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
00	System configuration is displayed. Going to give control to INT 19h boot loader.

Appendix E:

BIOS Non-Fatal Error Messages

If a non-fatal error occurs during the POST routines performed each time the system is powered on, the error message will appear on the screen in the following format:

ERROR Message Line 1
ERROR Message Line 2
Press <F1> to RESUME

Note the error message and press the <F1> key to continue with the boot up sequence.

NOTE
If the "Wait for <F1> If Any Error" option in the Advanced CMOS Setup portion of the BIOS SETUP PROGRAM has been set to "disabled," the <F1> prompt will not appear on the third line.

For most of the error messages, there is no ERROR Message Line 2. Generally, for those messages containing a line 2 ERROR Message the text will be "RUN SETUP UTILITY." Pressing the <F1> key will invoke the BIOS SETUP PROGRAM.

A description of the error messages appears below.

1. CH-2 Timer Error - Most AT™ standard system boards include two timers. An error with timer #1 is a fatal error, explained in Appendix C. If an error occurs with timer #2, this error message appears.

2. INTR #1 Error - The interrupt channel #1 has failed the POST routine.

3. INTR #2 Error - The interrupt channel #2 has failed the POST routine.

4. CMOS Battery State Low - There is a battery in your system which is used for storing the CMOS values. This battery appears to be low in power and needs to be replaced.

5. CMOS Checksum Failure - After the CMOS values are saved, a checksum value is generated to provide for error checking. If the previous value is different from the value currently read, this error message appears. To correct this error, you should run BIOS SETUP Program.

6. CMOS System Options Not Set - The values stored in the CMOS are either corrupt or nonexistent. Run the BIOS SETUP Program to correct this error.

7. CMOS Display Type Mismatch - The type of video stored in CMOS does not match the type detected by the BIOS. Run the BIOS SETUP Program to correct this error.

8. Display Switch Not Proper - Some systems require that a video switch on the mother board be set to either color or monochrome, depending upon the type of video you are using. To correct this situation, set the switch properly. (Remember to shut down the system first.)

9. Keyboard Is Locked...Unlocked It - The keyboard lock on the system is engaged. The system must be unlocked to continue the boot up procedure.

10. **Keyboard Error** - The BIOS has encountered a timing problem with the keyboard. Make sure you have an AMI Keyboard BIOS installed in your system. You may also set the "Keyboard" option in the BIOS SETUP Program Standard CMOS Setup to "Not Installed", which will cause the BIOS to skip the keyboard POST routines.
11 **KB/Interface Error** - The BIOS has found an error with the keyboard connector on the system board.

12. **CMOS Memory Size Mismatch** - If the BIOS finds the amount of memory on your system board to be different from the amount stored in CMOS, this error message is generated. Run the BIOS SETUP Program to correct this error.

13. **FDD Controller Failure** - The BIOS is not able to communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered off.

14. **HDD Controller Failure** - The BIOS is not able to communicate with the hard disk drive controller. Check all appropriate connections after the system is powered down.

15. **C: Drive Error** - The BIOS is not receiving any response from hard disk drive C:. It may be necessary to run the Hard Disk Utility to correct this problem. Also, check the type of hard disk selected in the Standard CMOS Setup of the BIOS SETUP Program to see if the correct hard disk drive has been selected.

16. **D: Drive Error** - The same error has occurred with hard drive D:. Follow the procedures in Error #15 to correct the situation.

17. **C: Drive Failure** - The BIOS cannot get any response from the hard disk drive C:. It may be necessary to replace the hard disk.

18. **D: Drive Failure** - The same error as #17 has occurred with hard drive D:.

19. **CMOS Time & Date Not Set** - Run the Standard CMOS Setup of the BIOS SETUP Program to set the date and time of the CMOS.

20. **Cache Memory Bad, Do Not Enable Cache!** - The BIOS has found the cache memory of the mother board to be defective. Consult your system manufacturer to repair this program.

21. **8042 Gate-A20 Error** - The Gate-A20 portion of the keyboard controller (8042) has failed to operate correctly. The 8042 chip should be replaced.

22. **Address Line Short!** - An error has occurred in the address decoding circuitry of the mother board.

23. **DMA #2 Error** - An error has occurred with the second DMA channel on the mother board.

24. **DMA #1 Error** - An error has occurred with the first DMA channel on the mother board.

25. **DMA Error** - An error has occurred with the DMA controller on the mother board.

26. **No ROM BASIC** - This error occurred when a proper bootable sector cannot be found on either the floppy diskette drive A: or the hard disk drive C:. The BIOS will try at this point to run ROM Basic, and the error message will be generated when the BIOS does not find it.

27. **Diskette Boot Failure** - The diskette used to boot-up in floppy drive A: is corrupt, which means you cannot use it to boot-up the system. Use another boot diskette and follow the instructions on the screen.

28. **Invalid Boot Diskette** - The BIOS can read the diskette in floppy drive A:, but it cannot boot-up the system with it. Use

another boot diskette and follow the instructions on the screen.

29. **On Board Parity Error*** - The BIOS has encountered a parity error with some memory installed on the system board. The message will appear as follows:

ON BOARD PARITY ERROR
ADDR (HEX) = (XXXX)

Where XXXX is the address (in hexadecimal) at which the error has occurred. "On Board" means that it is part of the memory attached directly to the system board, as opposed to memory installed via an expansion card in an I/O (BUS) slot.

30. **Off Board Parity Error*** - The BIOS has encountered a parity error with some memory installed in an I/O (BUS) slot. The message will appear as follows:

OFF BOARD PARITY ERROR
ADDR (HEX) = (XXXX)

Where XXXX is the address (in hexadecimal) at which the error has occurred. "Off Board" means that it is part of the memory installed via an expansion card in an I/O (Bus) slot, as opposed to memory attached directly to the system board.

31. **Parity Error ????*** - The BIOS has encountered a parity error with some memory in the system, but it is not able to determine the address of the error.

* Memory diagnostic software, such as AMIDIAG, can be used to find and correct memory problems.

Appendix F

Hard Disk Utility Error Messages

The following messages may appear during execution of the Hard Disk Utility section of the AMI BIOS SETUP Program.

The first group of errors listed below may appear during the initialization process, before anything else happens.

1. **No Hard Disk Installed** - The program could not find a hard disk drive installed on the system. This message appears if there is no hard disk on the system and you have chosen to run the Hard Disk Utility.

2. **FATAL ERROR Bad Hard Disk** - The program is not getting a response from the hard disk, or the hard disk is not repairable. Check all cable and power connections to the hard disk.

3. **Hard Disk Controller Failure** - The program is getting an error response from the reset command sent to the hard disk controller. Check to see that the controller is seated properly in the BUS slot.

4. **C: (D:) Hard Disk Failure** - The hard disk drive (C: or D:) is not responding to commands sent to it by the program. Check power and cable connections to the hard disk.

The errors listed below may appear during operation:

5. **Undefined Error- Command Aborted** - An error condition has occurred which the program cannot identify.

6. **Address Mark Not Found** - The address mark (initial address) on the hard disk could not be found.

7. **Requested Sector Not Found** - The sector currently requested on the hard disk could not be found.

8. **Reset Failed** - The program issued a reset command to the hard disk, but this command did not properly reset the hard disk.

9. **Drive Parameter Activity Failed** - The program has sent a reset command to the controller, followed by the drive parameters. Using the parameters sent to it, the controller is not getting a response from the hard disk drive. Check to see if the drive type selected in the Standard CMOS Setup is correct for the disk drive being used.

10. **Bad Sector Flag Detected** - The program has tried to perform an operation on a sector which has been flagged, i.e., marked as "bad."

11. **Bad ECC on Disk Read** - When the program attempts to write to the disk, it also calculates an ECC (Error Correction Code) value for the data being written. This ECC value is written to the drive and then read back. If the value read back is different from the one calculated, then, this error will occur.

12. **ECC Corrected Data Error** - The ECC value (explained above) read from the disk is not the same value which was written to the disk; therefore, the program assumes that the data is not correct. It, then, attempts to correct the data, but the ECC value is not corrected. In this situation, this message appears.

13. **Controller Has Failed** - The program has issued a diagnostic command to the controller, which has failed; therefore, the controller has failed as well.

14. **Seek Operation Failed** - The program has issued a seek command to the drive and this operation has failed. A seek operation is the act of finding a particular sector on the hard disk.

15. **Attachment Failed to Respond** - No response has been received from the hard disk drive. This message appears if an operation has already begun and the hard disk does not respond, when it has responded earlier.

16. **Drive Not Ready** - The program is trying to perform an operation on the hard disk drive, and it has waited beyond a preset specified time limit. This situation is know as "timeout."

17. **Write Fault on Selected Drive** - A "Write Fault" has occurred during the write operation on the hard disk.