

BISON II

The material in this manual is for information only and is subject to change without notice.

REVISION: 1.0

IBM, IBM PC/XT/AT, PC-DOS, MS-DOS, OS/2, INTEL, AMI, Pentium ARE THE TRADEMARKS OR REGISTERED TRADEMARKS OF THEIR RESPECTIVE OWNERS.

RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- * Reorient the receiving antenna.
- * Relocate the computer away from the receiver.
- * Move the computer away from the receiver.
- * Plug the computer into a different outlet so that computer and receiver are on different branch circuits.
- * Ensure that card slot covers are in place when no card is installed.
- * Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.
- * If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

Note

1. Electronic components are sensitive to dust and dirt. Do inspect and clean the computer system regularly.
2. Turn off the power whenever you install or remove any connector, memory module and add-on card. Before turning on the power, make sure that all the connectors, memory modules and add-on cards are secured.
3. After power is on, wait for a minute. The system BIOS are going through a self-test during this period and nothing is shown on the screen. After the self-test, the system BIOS will initialize the display adaptor and show messages.
4. The SIMM sockets are fragile device. Do not force the SIMM modules into the sockets. It may break the locking latches.

Table of Content

Chapter 1 **INTRODUCTION** 1-1

Chapter 2 **GENERAL FEATURES**

Specifications	2-1
The Central Processing Unit	2-3
Cache Subsystem	2-4
DRAM Subsystem	2-4
DRAM Configuration	2-6

Chapter 3 **CONFIGURING THE SYSTEM**

Installing the Processor	3-1
Installing RAM Modules	3-2
Configuring the Cache Memory	3-3
Control of System Speed	3-4
Reset CMOS Setup Information	3-4
System Board Jumper and Connector	3-6
Summary	
System Board Jumper Setting	3-7
System Board Connectors	3-8

Chapter 4 **TECHNICAL INFORMATION**

Memory Mapping	4-1
I/O Address Map	4-2
System Timers	4-4
System Interrupts	4-6
Direct Memory Access (DMA)	4-7
Real Time Clock and CMOS RAM	4-8
CMOS RAM Address Map	4-9
Real Time Clock Information	4-10
System Expansion Bus	4-11

Appendix A **OPERATION AND MAINTENANCE**

Static Electricity	A-1
Keeping The System Cool	A-1
Cleaning The "Golden Finger"	A-2
Cleaning The Motherboard	A-2

Appendix B **TROUBLESHOOTING**

Main Memory Error	B-1
-------------------	-----

Chapter 1

Introduction

OCTEK BISON II is a workstation class platform that can meet the demand of most time critical applications nowadays. With the Pentium processor and 64 bit interleaved memory system, it delivers the highest performance among the PC/AT class machines that ever been.

ISA bus and VESA bus are incorporated to adapt the most popular add-on card standard.

Next-generation design remains 100% binary and PC/AT compatible that boosts up the existing applications without modification.

THIS PAGE IS INTENTIONALLY LEFT BLANK

Chapter 2

General Features

Specifications:

Processor:

Pentium 60MHz or 66MHz CPU

Speed:

Turbo/normal speed

I/O Slot:

Six 16 bit ISA slots

One 8 bit ISA slot

Two VESA VL-bus slots (supporting one VL master)

Cache:

Internal cache inside Pentium:

8K instruction cache

8K data cache

External cache:

64K external cache expandable to 512K

Both caches can be programmed as write back or write through mode.

DRAM:

Supports 4 banks of 32 bit wide SIMM modules with 1MB, 4MB or 16MB page-mode DRAMs.

Supports DRAM configurations from 2MB to 64MB.

Two non-cacheable regions for VL/ISA bus masters.

DRAM post write buffer.

Supports pipeline DRAM burst cycles.

Others:

Fast GateA20 and reset emulations.

The Central Processing Unit

The Pentium processor is the next-generation member of 80486 family of microprocessors. It contains all of the features of the 80486 and provides significant enhancements and additions. It is 100% binary compatible with the X86 CPU.

The superscalar architecture of the Pentium processor contains two instruction pipelines and floating-point unit on the Pentium processor are capable of independent operation. Each pipeline issues hit instructions in a single clock. The dual pipes can issue two integer instructions in one clock, or one floating-point instruction in one clock.

The branch prediction unit includes two prefetch buffers, one to prefetch code in a linear fashion, and one to prefetch code according to the Branch Target Buffer so that the needed code is almost always prefetched before it is needed for execution.

The floating point unit is redesigned and runs at least three times faster than 80486.

The Pentium processor includes separate 8K code cache and 8K write-back data cache. Each cache is 32 byte line size and is 2-way set associative. The data cache is configurable to be write-back or write-through on a line-by-line basis and follows the MESI protocol. The code cache is a write-protected cache.

The Pentium processor has widened the data bus to 64 bits to improve the data transfer rate. Burst read and burst writeback cycles are supported by the Pentium processor.

In summary, the Pentium processor provides an ultimate performance levels and retains compatibility with the existing applications.

Cache Subsystem

The external cache of BISON II is write-back, direct-mapped with sizes of 64K, 128K, 256K or 512K. It is organized by single or dual bank. Dual bank is accessed in interleaved manner and it can support 3-2-2-2 burst read cycle.

DRAM Subsystem

The memory controller is 64 bit wide and has the following features:

- Hidden refresh is used to increase the CPU bandwidth. The DRAM can be refreshed in the background while the CPU is accessing the internal cache.
 - Page Mode is used for faster data access from the DRAMs.
 - Posted-Write to the DRAM improves the write-cycle timing. One quad-word deep data buffer is used to hold the data from the CPU without waiting for the external DRAM cycle.
-

Shadow RAM is available as an option. System BIOS and video BIOS residing in slow EPROM can be copied to local DRAM to speed up accesses to BIOS code. Shadow RAM addresses range from C0000h to FFFFFh. 16K granularity is provided for address range C0000h to EFFFFh, while the area F0000h - FFFFFh can only be shadowed as a whole. Video BIOS at C0000h - C7FFFh can be cached in the external cache after shadowing.

Two DRAM control regions can be selected to adapt the bus mastering add-on cards. For the memory region that bus master would write to, set it to non-cacheable or write-through would improve bus bandwidth owing to the elimination of the time-consuming cache invalidation cycle. For the card with its own memory mapping overlaid to the system memory, holes can be enabled to allow accessing to the memory on the ISA or VESA bus.

DRAM CONFIGURATION

Bank 0 + Bank 1 (bits)	Bank 2 + Bank 3 (bits)	Total (bytes)
256K x 64	---	2M
256K x 64	256K x 64	4M
256K x 64	1M x 64	10M
256K x 64	4M x 64	34M
1M x 64	---	8M
1M x 64	1M x 64	16M
1M x 64	4M x 64	40M
4M x 64	---	32M
4M x 64	4M x 64	64M

70ns 32-bit wide SIMM modules can be used.

Chapter 3

Configuring The System

Important Note: Turn off the power before installing or replacing any component.

Installing the processor

Pentium is a 273 pin PGA device. Make sure the pin 1 of Pentium (with a notch at the corner) is line up with the pin 1 of the socket.

Before installing the processor, make sure that all the pins are straight. The pins are very fragile. Once these pins are bent, the processor may be damaged.

Installing RAM modules

BISON II has four banks on board for SIMM modules. Bank 0 and bank 1 must be installed first. Make sure pin 1 of the SIMM module inserted near the power connector. Lock it firmly with the latches on the socket.

Extra SIMM module should be inserted at bank 2 and bank 3.

Configuring the cache memory

Note: If you have any question about the configuration of the cache memory, consult your local dealer. Improper configuration will cause the system malfunction.

The external cache is organized by single bank or dual banks with sizes of 64KB to 512KB. Follow the tables below to configure the system.

Cache size	JP6	JP23	JP22	JP21	JP20	JP19
64K	2-1	2-1	2-1	OPEN	OPEN	OPEN
128K	2-3	2-3	2-3	OPEN	OPEN	CLOSE
256K	2-1	2-1	2-1	OPEN	CLOSE	CLOSE
512K	2-3	2-3	2-3	CLOSE	CLOSE	CLOSE

Cache size	U30	U31	BANK 0	BANK 1
64K	OPEN	8K x 8	8K x 8	OPEN
128K	OPEN	8K x 8	8K x 8	8K x 8
256K	OPEN	8K x 8	32K x 8	OPEN
512K	8K x 8	8K x 8	32K x 8	32K x 8

CONTROL OF SYSTEM SPEED

System speed can be controlled by keyboard and turbo switch. To change the speed by keyboard, use '-' and '+' of the numeric keypad. Press **Ctrl** **Alt** and '-' for slow speed and press **Ctrl** **Alt** and '+' for fast speed.

RESET CMOS SETUP INFORMATION

Sometimes, the improper setting of system setup may make the system malfunction. In this case, turn off the power and set JP1 to 1-2 for a while. The internal CMOS status register is reset. Then set the jumper to 2-3 of JP1 and turn on the power. The BIOS finds the CMOS status register is reset and regards the setup information is invalid. So it will prompt you to correct the information.

**SYSTEM BOARD JUMPER AND CONNECTOR
SUMMARY**

	Description
J1	Keyboard Connector
JP1	Reset CMOS
J10,J11	Power Supply Connector
J9	External Battery Connector
JP2	Display Selection
JP6	Cache Size Selection
JP19-JP23	Cache Size Selection
JP20	Power LED 6 Ext-Lock Connector
JP18	Speaker Connector
JP24	Power-Good Selection
JP27	Cooling Fan Power Selection
JP26	Cooling Fan Connector
JP25	Hardware Reset Connector

SYSTEM BOARD JUMPER SETTING

There are several options which allows user to select by hardware switches.

JP2 - Display Selection

JP2	
CLOSE	CGA, EGA, VGA (default)
OPEN	Monochrome display

JP24 - Power-good Selection

PIN	
1-2	Power-good signal from power supply (default)
2-3	On board power-good signal

JP27 - Cooling Fan Power Selection

PIN	
1-2	12Vdc (default)
2-3	15Vdc

SYSTEM BOARD CONNECTORS

Under typical conditions, these connectors should be connected to the indicators and switches of the system unit. The functions and the pin assignment of the connectors on the motherboard are listed below.

JP18 - Speaker Connector

Pin	Assignment
1	Data out
2	+5 Vdc
3	Ground
4	+5 Vdc

JP25 - Hardware Reset Connector

Pin	Assignment
1	Selection Pin
2	Ground

J20 - Power LED & Ext-Lock Connector

Pin	Assignment
1	+5 Vdc
2	Key
3	Ground
4	Keyboard inhibit
5	Ground

J10,J11 - Power Supply Connector

Pin	Assignment
1	POWERGOOD
2	+5 Vdc
3	+12 Vdc
4	-12 Vdc
5	Ground
6	Ground

Pin	Assignment
1	Ground
2	Ground
3	-5 Vdc
4	+5 Vdc
5	+5 Vdc

CONFIGURING THE SYSTEM

6	+5 Vdc
---	--------

J9 - External Battery Connector

Pin	Assignment
1	+ Vdc
2	not used
3	Ground
4	Ground

JP26 - Cooling Fan Connector

Pin	Assignment
1	+ 5Vdc
2	Ground

J1 - Keyboard Connector

Pin	Assignment
1	Keyboard clock
2	Keyboard data
3	Spare
4	Ground
5	+5 Vdc

THIS PAGE IS INTENTIONALLY LEFT BLANK

Chapter 4

Technical Information

This section provides technical information about BISON II and is intended for advanced users interested in the basic design and operation of BISON II.

MEMORY MAPPING

Address	Range	Function
000000-7FFFFFFF	000K-512K	System Board Memory (512K)
080000-09FFFF	512K-640K	System Board Memory (128K)
0A0000-0BFFFF	640K-768K	Display Buffer (128K)
0C0000-0DFFFF	768K-896K	Adaptor ROM / Shadow RAM (128K)
0E0000-0EFFFF	896K-960K	System ROM / Shadow RAM (64K)
0F0000-0FFFFFFF	960K-1024K	System BIOS ROM / Shadow RAM (64K)
100000-7FFFFFFF	1024K-8192K	System Memory
800000-FFFFFFF	8192K-16318K	System Memory

I/O ADDRESS MAP

I/O Address Map on System Board

I/O address hex 000 to 0FF are reserved for the system board I/O.

ADDRESS (HEX)	DEVICE
000-01F	DMA Controller 1, 8237
020-03F	Interrupt Controller 1, 8259, Master
040-05F	Timer, 8254
060-06F	Keyboard Controller
070-07F	Real Time Clock, NMI (non-maskable interrupt) mask
080-09F	DMA Page Register, 74LS612
0A0-0BF	Interrupt Controller 2, 8259
0C0-0DF	DMA Controller 2, 8237
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor Port

I/O address hex 100 to 3FF are available on the I/O channel.

ADDRESS (HEX)	DEVICE
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

SYSTEM TIMERS

BISON II has three programmable timer/counters controlled by Headland chipset and they are defined as channels 0 through 2:

Channel 0	System Timer
Gate 0	Tied on
Clk in 0	1.190 Mhz OSC
Clk out 0	8259 IRQ 0

Channel 1	Refresh Request Generator
Gate 1	Tied on
Clk in 1	1.190 Mhz OSC
Clk out 1	Request Refresh Cycle

Channel 2	Tone Generation of Speaker
Gate 2	Controlled by bit 0 of port hex 61 PPI bit
Clk in 2	1.190 Mhz OSC
Clk out 2	Used to drive the speaker

Note : Channel 1 is programmed to generate a 15-micro-second period signal.

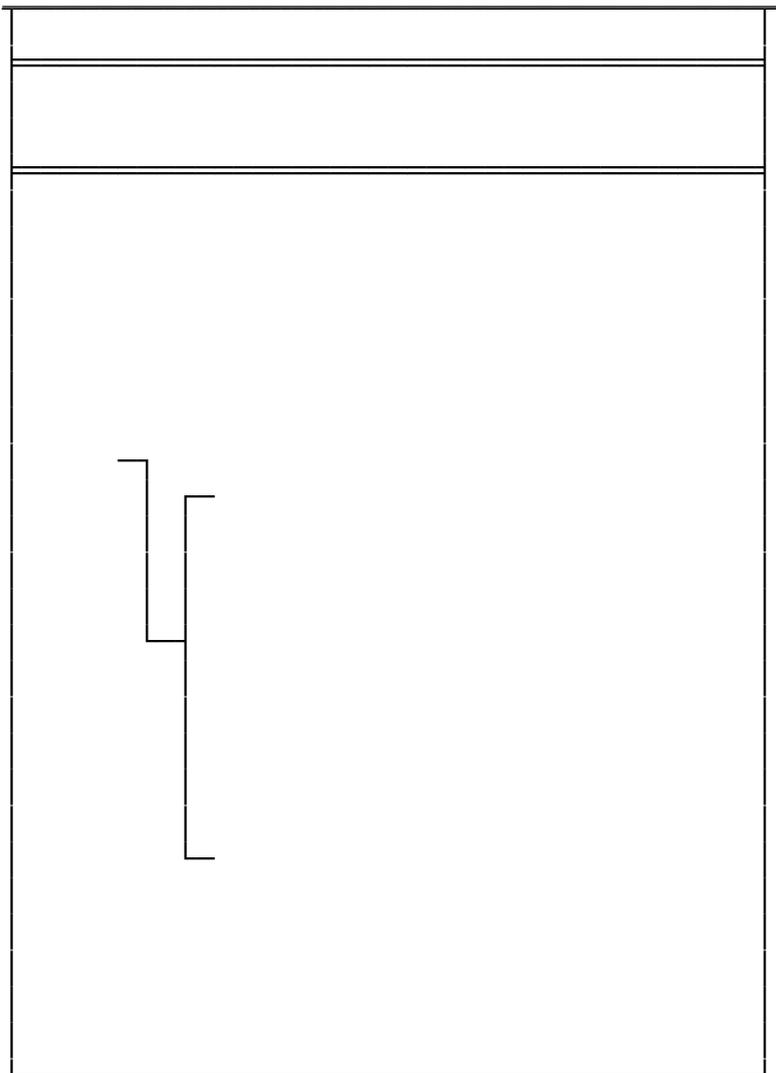
The 8254 Timer/Counters are treated by system programs as an arrangement of four programmable external I/O ports. Three are treated as counters and the fourth is a control register for mode programming.

SYSTEM INTERRUPTS

Sixteen levels of system interrupts are provided on BISON II. The following shows the interrupt-level assignments in decreasing priority.

Level	Function
Microprocessor NMI	Parity or I/O Channel Check
Interrupt Controllers	
CTLR 1 CTLR 2	
IRQ0	Timer Output 0
IRQ1	Keyboard (Output Buffer Full)
IRQ2	Interrupt from CTLR 2
	IRQ8 Real-time Clock Interrupt
	IRQ9 Software Redirected to INT 0AH (IRQ2)
	IRQ10 Reserved
	IRQ11 Reserved
	IRQ12 Reserved
	IRQ13 Coprocessor
	IRQ14 Fixed Disk Controller
	IRQ15 Reserved
IRQ3	Serial Port 2
IRQ4	Serial Port 1
IRQ5	Parallel Port 2
IRQ6	Diskette Controller
IRQ7	Parallel Port 1





DIRECT MEMORY ACCESS (DMA)

BISON II supports seven DMA channels.

Channel	Function
0	Spare (8 bit transfer)
1	SDLC (8 bit transfer)
2	Floppy Disk (8 bit transfer)
3	Spare (8 bit transfer)
4	Cascade for DMA Controller 1
5	Spare (16 bit transfer)
6	Spare (16 bit transfer)
7	Spare (16 bit transfer)

The following shows the addresses for the page register.

Page Register	I/O Address (HEX)
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082
DMA Channel 5	008B
DMA Channel 6	0089
DMA Channel 7	008A
Refresh	008F

REAL TIME CLOCK AND CMOS RAM

Real time clock and CMOS RAM are contained on board. Real time clock provides the system date and time. CMOS RAM stores system information. Both are backed up by battery and will not lose information after power off. The following page shows the CMOS RAM Address Map.

CMOS RAM ADDRESS MAP

Addresses	Description
00-0D	* Real-time clock information
0E	* Diagnostic status byte
0F	* Shutdown status byte
10	Diskette drive type byte - drives A and B
11	Reserved
12	Fixed disk type byte - drives C and D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	* Low expansion memory byte
31	* High expansion memory byte
32	* Date century byte
33	* Information flags (set during power on)
34-3F	Reserved

REAL TIME CLOCK INFORMATION

The following table describes real-time clock bytes and specifies their addresses.

Byte	Function	Address
0	Seconds	00
1	Second alarm	01
2	Minutes	02
3	Minute alarm	03
4	Hours	04
5	Hour alarm	05
6	Day of week	06
7	Date of month	07
8	Month	08
9	Year	09
10	Status Register A	0A
11	Status Register B	0B
12	Status Register C	0C
13	Status Register D	0D

SYSTEM EXPANSION BUS

BISON II provides six 16-bit slots and two VL-bus slots.

The I/O channel supports:

- * I/O address space from hex 100 to hex 3FF*
 - * Selection of data access (either 8 or 16 bit)*
 - * 24 bit memory addresses (16MB)*
 - * Interrupts*
 - * DMA channels*
 - * Memory refresh signal*
-

The following figure shows the pin numbering for I/O channel connectors (A-side and B-side).

The following figure shows the pin numbering for I/O channel connectors (C-side and D-side).

The following tables summarize pin assignments for the I/O channel connectors.

I/O Channel (A-Side)

I/O Pin	Signal Name	I/O
A1	-I/O CH CK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	-I/O CH RDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O

TECHNICAL INFORMATION

A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

I/O Channel (B-Side)

I/O Pin	Signal Name	I/O
B1	GND	Ground
B2	RESET DRV	I
B3	+5 Vdc	Power
B4	IRQ9	I
B5	-5 Vdc	Power
B6	DRQ2	I
B7	-12 Vdc	Power
B8	OWS	I
B9	+12 Vdc	Power
B10	GND	Ground
B11	-SMEMW	O
B12	-SMEMR	O
B13	-IOW	I/O
B14	-IOR	I/O
B15	-DACK3	I
B16	DRQ3	O
B17	-DACK1	I
B18	DRQ1	O
B19	-Refresh	I/O
B20	CLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	-DACK2	O
B27	T/C	O
B28	BALE	O

TECHNICAL INFORMATION

B29	+5 Vdc	Power
B30	OSC	O
B31	GND	Ground

I/O Channel (C-Side)

I/O Pin	Signal Name	I/O
C1	SBHE	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	-MEMR	I/O
C10	-MEMW	I/O
C11	SD8	I/O
C12	SD9	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

I/O Channel (D-Side)

I/O Pin	Signal Name	I/O
D1	-MEM CS16	I
D2	-I/O CS16	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	-DACK0	O
D9	DRQ0	I
D10	-DACK5	O
D11	DRQ5	I
D12	-DACK6	O
D13	DRQ6	I
D14	-DACK7	O
D15	DRQ7	I
D16	+5 Vdc	Power
D17	-MASTER	I
D18	GND	Ground

The following table summary pin assignments for VESA VL-bus connector.

VL-bus (side A)

I/O Pin	Signal Name
A1	CD1
A2	CD3
A3	GROUND
A4	CD5
A5	CD7
A6	CD9
A7	CD11
A8	CD13
A9	CD15
A10	GROUND
A11	CD17
A12	POWER
A13	CD19
A14	CD21
A15	CD23
A16	CD25
A17	GROUND
A18	CD27
A19	CD29
A20	CD31
A21	CA30
A22	CA28
A23	CD26
A24	GROUND

TECHNICAL INFORMATION

A25	CA24
A26	CA22
A27	POWER
A28	CA20

VL-bus (side A)

I/O Pin	Signal Name
A29	CA18
A30	CA16
A31	CA14
A32	CA12
A33	CA10
A34	CA8
A35	GROUND
A36	CA6
A37	CA4
A38	WBACK-
A39	BEO-
A40	POWER
A41	BE1-
A42	BE2-
A43	GROUND
A44	BE3-
A45	ADS-
A46	LRDY-
A47	LDEV-
A48	LREQ-
A49	GROUND
A50	LGNT-
A51	POWER
A52	ID2
A53	ID3
A54	ID4
A55	LKEN-
A56	LEADS-

VL-bus (side B)

I/O Pin	Signal Name
B1	CD0
B2	CD2
B3	CD4
B4	CD6
B5	CD8
B6	GROUND
B7	CD10
B8	CD12
B9	POWER
B10	CD14
B11	CD16
B12	CD18
B13	CD20
B14	GROUND
B15	CD22
B16	CD24
B17	CD26
B18	CD28
B19	CD30
B20	POWER
B21	CA31
B22	GROUND
B23	CA29
B24	CA27
B25	CA25
B26	CA23
B27	CA21
B28	CA19

VL-bus (side B)

I/O Pin	Signal Name
B29	GROUND
B30	CA17
B31	CA15
B32	POWER
B33	CA13
B34	CA11
B35	CA9
B36	CA7
B37	CA5
B38	GROUND
B39	CA3
B40	CA2
B41	n/c
B42	RESET-
B43	D/C-
B44	M/IO-
B45	W/R-
B46	RDY-
B47	GROUND
B48	IRQ9
B49	BRDY-
B50	BLAST-
B51	ID0
B52	ID1
B53	GROUND
B54	VLCLK
B55	POWER
B56	LBS16-

THIS PAGE IS INTENTIONALLY LEFT BLANK

Appendix A

Operation and Maintenance

STATIC ELECTRICITY

When installing or removing any add-on card, DRAM module or processor, you should discharge the static electricity on your body. Static electricity is dangerous to electronic device and can build-up on your body. When you touch the add-on card or motherboard, it is likely to damage the device. To discharge the static electricity, touch the metal of your computer. When handling the add-on card, don't contact the components on the cards or their "golden finger". Hold the cards by their edges.

KEEPING THE SYSTEM COOL

The motherboard contains many high-speed components and they will generate heat during operation. Other add-on cards and hard disk drive can also produce a lot of heat. The temperature inside the computer system may be very high. In order to keep the system running stably, the temperature must be kept at a low level. A easy way to do this is to keep the cool air circulating inside the case. The power supply contains a fan to blow air out of the case. If you find that the temperature is still very high, it would be better to

install another fan inside the case. Using a larger case is recommended if there are a number of add-on cards and disk drives in the system.

CLEANING THE "GOLDEN FINGER"

Whenever inserting an add-on card to the motherboard, make sure that there is no dirt on the "golden finger" of the add-on card. If not, the contact between the "golden finger" and the slot may be poor and thus the add-on card may not work properly. Use a pencil eraser to clean the "golden finger" if dirt is found.

CLEANING THE MOTHERBOARD

The computer system should be kept clean. Dust and dirt is harmful to electronic devices. To prevent dust from accumulating on the motherboard, installing all mounting plates on the rear of the case. Regularly examine your system, and if necessary, vacuum the interior of the system with a miniature vacuum.

Appendix B

Troubleshooting

MAIN MEMORY ERROR

After power up, the monitor remains blank, and there are beep sounds indicating a main memory failure. In this case, turn off the power and remove all SIMM modules. Carefully place the modules back to the sockets and make sure that all the modules are locked by the locking latches firmly.

In some other cases, the total memory found by the BIOS is different from the actual amount of memory on board. (Note that 128K bytes memory is reserved for the shadow RAM function and will not be counted by the BIOS). It is also a memory failure and you can follow the instruction above.

THIS PAGE IS INTENTIONALLY LEFT BLANK
