BABY 286MB

MINI AT-SYSTEM BOARD

REFERENCE MANUAL

(VERSION 1.20)

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PART I

Introduction To BABY 286MB Mini AT-System Board

PART I

Introduction to BABY 286MB Mini AT-System Board

The **BABY 286MB** system board is based on the Intel 80286 microprocessor. Particular attentions have been paid to ensure the **BABY 286MB** is fully compatible with the IBM PC/AT **without** sacrificing the overall system performance.

All PC/AT programs can run on the **BABY 286MB** transparently. The only difference you may find is the speed since the **BABY 286MB** operates much faster than a standard PC/AT.

The **BABY 286MB** allows upto **8** expansion slots. The arrangements are 6 AT compatible (**16 bits**) slots and 2 PC/XT compatible (**8 bits**) slots. Memory on board can be 256K Bytes, 512K Bytes, 640K Bytes or 1024K Bytes. 1 MB memory on board can be split into 640KB base memory and 384KB extended memory.

BABY 286MB can be put into PC/XT, baby AT and also the standard size AT housing.

The **BABY 286MB** supports MS-DOS 2.0 or above, and XENIX 2.0 or later. Users can run applications designed for the PC/AT on the **BABY 286MB** *without any modification.*

1.1 CENTRAL PROCESSOR

The **BABY 286MB Mini AT-System Board** is based on the Intel 80286 CPU which incorporates a **16-bit** external data path and provides a **24-bit** (16 Megabytes) addressing space. The 80286 microprocessor gives two operating modes: The 8088, 8086 object code compatible with real address mode and the protected virtual address mode.

1.2 BABY 286MB BUS

BABY 286MB BUS is an innovative design. The objective of this design is to allow users to use some low speed I/O card and memory card. Instead of lowering down the CPU clock, which sacrifices the overall system performance, you can simply select an appropriate operational mode. Appropriate wait states will then be added automatically to the I/O and memory to fit for high speed processing.

Please refer to Part 2.4 for selection of BABY 286MB BUS.

1.3 OPERATING SPEED

BABY 286MB has two crystal oscillators installed. Only one crystal oscillator can be activated at any time. When 40MHz crystal oscillator is selected, the system runs at 10MHz or 6MHz. While the 48MHz crystal is selected, the system is operated at 12MHz or 8MHz. Crystal oscillator is selected by Jumper **(J5)**. Users can select between the high speed (10MHz/12MHz) or low speed (6MHz/8MHz) through hardware jumper **(J1)** or by keyboard selection. (Refer to 2.3 Operating Speed Selection)

If Award Bios 2.07 or above is used, the following table shows how the speed can be selected by keyboard.

Crystal Oscillators	KEY-IN SEQUENCE	SPEED OBTAINED	RESPONSE
40 MHz	CTRL_ALT_2 or CTRL_ALT_+	10 MHz	Turbo LED is on Beep twice
	CTRL_ALT_1 or CTRL_ALT_-	6 MHz	Turbo LED is off Beep once
48 MHz	CTRL_ALT_2 or CTRL_ALT_+	12 MHz	Turbo LED is on Beep twice
	CTRL_ALT_1 or CTRL_ALT_-	8 MHz	Turbo LED is off Beep once

1.4 VIRTUAL-ADDRESS MODE

The mode uses **32-bit** pointers, that consist of a 16-bit selector and offset components to provide a **1-gigabyte** virtual address space mapped onto a **16-megabyte** physical address space. The use of a virtual address that does not map to a physical memory location will cause a restartable interrupt. The selector specifies an index into a memory resident table and the 24-bit base address of the desired segment is obtained from the memory table. Then, the physical address is formed by adding the 16-bit offset to the segment base address.

The **80286** automatically references the tables whenever segment register is loaded with a selector. No additional program support is needed for instructions that load a segment register which will refer to the memory based-tables. The memory-based tables contain 8-byte values called *descriptors*.

1.5 REAL-ADDRESS MODE

In this mode, physical memory is a continuous array of upto 1 megabyte. The selector portion of the pointer is interpreted as the upper 16-bits of a 20-bit address, while the remaining 4 bits are set to zero. *This mode of operation is object code compatible with the 8088 and 8086.*

Segments in this mode are **64 KB** in size and may be read, written, or executed. In this mode the information contained in the segment does not use the full 64KB and the unused end of the segment may be overlapped by another segment to reduce physical memory requirements.

1.6 SYSTEM TIMERS/COUNTERS

The **Timer/Counter Chip 8254** controls these programmable timer/counters on the system via **Channels 0 through 2.**

Channel 0	System Timer
GATE 0	Tied on
CLK IN 0	1.190 MHz OSC
CLK OUT 0	8259A IRQ 0
Channel 1	Refresh Request Generator (*programmed to generate a 15 microsecond period signal)
GATE 1	Tied on
CLK IN 1	1.190 MHz OSC
CLK OUT 1	Request Refresh Cycle
Channel 2	Tone Generation for Speaker
GATE 2	Controlled by bit 0 of port hex 61 PP1 bit
CLK IN 2	1.190 MHz OSC
CLK OUT 2	Used to drive the speaker

The **8254-2 Timer/Counter** is treated as four programmable external I/O ports by the BIOS (system programs). The first three arrangements are timer/counters, the fourth one is a control register for mode programming.

1.7 ROM (READ ONLY MEMORY) SUB-SYSTEM

The **ROM Sub-system** consists of two 32K by 8-bit ROM/EPROM socket and housed by two 16K by 8 bit ROM/EPROM modules organized as a 16K by 16-bit arrangement which contains the BIOS. *Parity-checking is not done on ROM.* {The top of the first megabyte and the bottom of the last megabyte address space is assigned to ROM (hex 0F0000 and hex FF0000).} The odd and even address codes are resident in separate modules.

BABY 286MB has implemented a special design for ROM sub-system which allows users using 150 ns ROM for both 10 MHz and 12 MHz.

1.8 RAM SUB-SYSTEM

The **16M** addressing space of the RAM Sub-system starts at address hex 00000. BABY 286MB consists of either 256KByte, 512KByte, 640KByte or 1MByte (maximum) on board memory. **Memory cycle time** is 200 nanoseconds (minimum) and the **access time** is 100 nanoseconds. Memory-refresh forces one memory cycle every 15 microseconds via channel 1 of the timer/counter.

The following functions are performed by the RAM initialization program:

i) Memory write operation to any memory location

ii) Initializes channel 1 of the timer/counter to the rate generation mode (15 microseconds)

NOTE: The memory can be used only after being accessed or refreshed eight times.

1.9 SYSTEM INTERRUPTS

The **80286 NMI** and two **8259A Interrupt Controller Chips** provide **16** levels of system interrupts. The interrupt-level priority assignments are as follow:

Level		Function
MicroProcessor NMI		Parity or I/O Channel Check
Interrupt Controllers		
CTRL 1	CTLR 2	
IRQ0		Timer Output 0
IRQ1		Keyboard (Output Buffer Full)
IRQ2		Interrupt from CTLR 2
	IRQ8	Realtime Clock Interrupt
	IRQ9	Software Redirected to INT ϕAH (IRQ2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	Reserved
	IRQ13	Coprocessor
	IRQ14	Fixed Disk Controller
	IRQ15	Reserved
IRQ3		Serial Port 2
IRQ4		Serial Port 1
IRQ5		Parallel Port 2
IRQ6		Diskette Controller
IRQ7		Parallel Port 1

1.10 DMA (DIRECT MEMORY ACCESS)

The **BABY 286MB Mini AT-System Board** supports **7 DMA** channels by using two 8237A-5 DMA controller chips (each with 4 channels). Controller 1 is cascaded to the channel 4 of controller 2.

The DMA channels assignments are as follow:

CTLR 1	CTLR 2
Ch 0-Spare	Ch 4-Cascade for CTLR 1
Ch 1-SDLC	Ch 5-Spare
Ch 2-Diskette	Ch 6-Spare
Ch 3-Spare	Ch 7-Spare

Channels 0 through 3 are contained in DMA contrbller 1, **8-bit** data transfers between 8-bit I/O adapters and 8-bit or 16-bit system memory, are supported by these channels.

Each of these channels will transfer data, in **64KB** blocks, throughout the 16-megabyte system-address space.

Channels 4 through 7 are contained in DMA controller 2. *To cascade channels 0 through 3 to the microprocessor, channel 4 is used.* 16-bit data transfers between 16-bit I/O adapters and 16-bit system memory are supported by channels 5, 6 and 7. DMA channels 5 through 7 will transfer data, in **128KB** blocks, throughout the 16-megabyte system-address space. These channels will not transfer data on odd byte boundaries.

The address for the page register are as follows :

Page Register	I/O Hex Address
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082
DMA Channel 5	008B
DMA Channel 6	0089
DMA Channel 7	008A
Refresh	008F

Page Register Address

Address generation for the DMA channels are as follows :

Source	DMA Page Registers	8237A-5
Address	A23 < ------ > 16	A15 < ----- >A0

Address Generation for DMA Channels 3 through 0

NOTE : To generate the addressing signal 'byte high enable' (BHE), invert address line A0.

Source	DMA Page Registers	8237A-5
Address	A23 < ------- > A17	A16 < ----- > A1

Address Generation for DMA Channels 7 through 5

NOTE: The 'BHE' and 'A0' addressing signals, are forced to a logic 0.

DMA channel addresses do not increase or decrease through page boundaries (64KByte for channels 0 through 3 and 128KByte for channels 5 through 7).

1.11 I/O CHANNEL

The I/O channel supports:

1) Refresh of system memory

2) Selection of data access (either 8 or 16 bit)

3) Interrupts

4) 24-bit memory address (16MB)

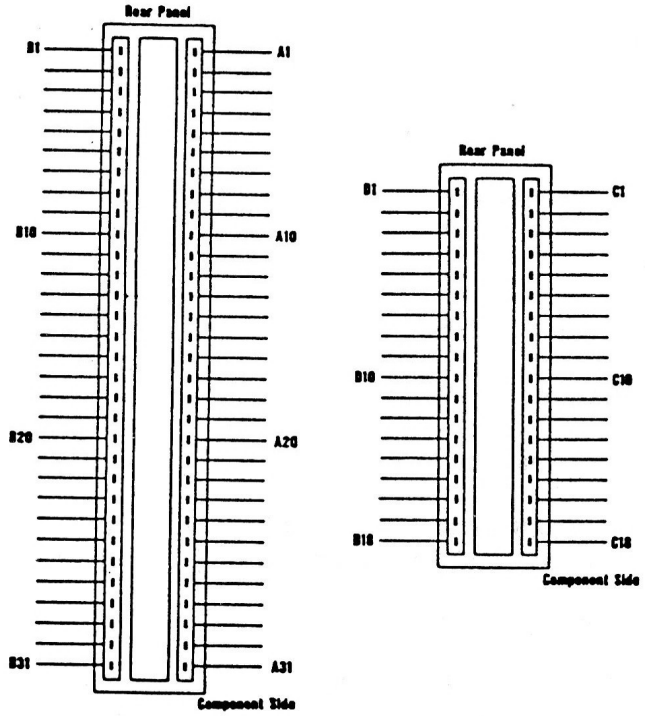
5) I/O wait-state generation

6) I/O address space hex 100 to hex 3FF

7) Open-bus structure (allowing multiple microprocessors to share the system's resources, including memory)

8) DMA channels

The numbering of the I/O slots are as follows:



NOTE: This board consists 8 I/O slots (6 with a 36 and a 62 pin card-edge socket, and 2 with only the 62 pin card-edge socket).

I/O Pin	Signal Name	I/O
A1	-I/O CH CK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	-I/O CH RDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

I/O Channel (A-Side, J1 through J8)

I/O Pin	Signal Name	I/O
B1	GND	Ground
B2	RESET DRV	O
B3	+5 Vdc	Power
B4	IRQ9	I
B5	-5VDc	Power
B6	DRQ2	I
B7	-12Vdc	Power
B8	OWS	I
B9	+12Vdc	Power
B10	GND	Ground
B11	-SEMEMW	O
B12	-SEMEMR	O
B13	-IOW	I/O
B14	-IOR	I/O
B15	-DACK3	O
B16	DRQ3	I
B17	-DACK1	O
B18	DRQ1	I
B19	-Refresh	I/O
B20	CLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	-DACK2	O
B27	T/C	O
B28	BALE	O
B29	+5Vdc	Power
B30	OSC	O
B31	GND	Ground

I/O Channel (B-Side J1, through J8)

I/O Pin	Signal Name	I/O
C1	SBHE	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	-MEMR	I/O
C10	-MEMW	I/O
C11	SD08	I/O
C12	SD09	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

I/O Channel (C-Side J10 through J14 and J16)

I/O Pin	Signal Name	I/O
D1	-MEM C516	I
D2	-I/O CS16	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	-DACK0	O
D9	DRQ0	I
D10	-DACK5	O
D11	DRQ5	I
D12	-DACK6	O
D13	DRQ6	I
D14	-DACK7	O
D15	DRQ7	I
D16	+5Vdc	Power
D17	-MASTER	I
D18	GND	Ground

I/O Channel (D-Side, J10 through J14 and J16)

1.12 COPROCESSOR CONTROL

The mathematics Coprocessor, **80287** is treated as an I/O device through I/O port address hex 0F8, 0FA and 0FC. The microprocessor sends OP codes and operands through these I/O ports. The microprocessor also receives and stores results through the same I/O ports. The **"BUSY"** signal generated by the coprocessor signifies to the microprocessor to wait until the coprocessor has finished executing.

The following describe the mathematics coprocessor control ports:

0F0 *The latched Mathematics Coprocessor busy signal can be cleared with an 8-bit, Out command, to port F0. The coprocessor will latch "BUSY", if it asserts its error signal. Data output should be zero.*

0F1 *The Mathematics Coprocessor will reset to real address mode which is 8087 compatible if an 8-bit Out command is sent to port F1. Again, the data output should be zero.*

PART II

Jumper Setting

PART II

Jumper Setting

2.1 RAM JUMPER SETTING AND RAM CHIPS INSTALLATION (SW1-3 & SW1-4)

The system board has dual dip switches identified as **SW1-3** and **SW1-4**, which determines the RAM size on the system board. User can configure either **640KB** or **1MB** memory by these dip switches.

The on board memory can be configurated by selecting the switch 3, 4 of dip switch SW1.

MEMORY SIZE		SWITCH SETTING		RAM LOCATION	
BASE	EXTENDED	SW1-3	SW1-4	U14 - U31	U32 - U49
256K	0	ON	ON	4164	4164
512K	0	OFF	ON	41256	NONE
640K	0	ON	OFF	41256	4164
640K	384K	OFF	OFF	41256	41256

NOTES: For 1024KB memory, configuraton is set with **Base Memory** of 640KB and **Extended memory** of 384KB.

2.2 SYSTEM CLOCK AND MEMORY WAIT STATE SELECTION

BABY 286MB can be operated at 10 MHz zero wait state, 10 MHz one wait state, 12 MHz one wait state and 12 MHz zero wait state. Jumper should be set according to the following tables:

10 MHz Zero Wait State

J5	1-2
J11	1-2
J2	CLOSE
J8	CLOSE

10 MHz One Wait State

J5	1-2
J11	1-2
J2	OPEN
J8	OPEN

12 MHz One Wait State

J5	2-3
J11	2-3
J2	OPEN
J8	OPEN

12 MHz Zero Wait State

J5	2 - 3
J11	2 - 3
J2	CLOSE
J8	CLOSE

2.3 OPERATING SPEED (J1 & J5)

The operating speed of the system can be changed by the system clock speed selection jumper (**J1**) and master crystal selector **(J5)**. Also software selection via keyboard is allowed if appropriate BIOS is used.

SYSTEM CLOCK SELECTION	J5		J1
Hardware Select Mode	1-2	2-3	
	6 MHz	8 M	1-2
	10 MHz	12 M	OPEN
Software Select Mode			2-3

REMARKS: Software selection of operating speed - refer to Chapter 1.3 Operating Speed on P.4 of this manual.

2.4 SELECTION FOR BABY 286MB BUS

There are many add-on cards in the market. Most of them are designed for 6 MHz or 8 MHz clock rate. Some new design add-on cards have the capability to run on 10 MHz zero wait state and 12 MHz.

To allow both high speed and low speed add-on cards working on 10 MHz at zero wait state and 12 MHz, **BABY 286MB Bus** will optionally insert wait state for different card requirement. By selecting appropriate mode through dip switches **SW1-2** and **SW1-1**, wait states are then added. Mode 0 is designed for high speed add-on cards. If problem is found when running on mode 0, users can try on mode 1, 2 and 3.

SW1-1	SW1-2	MODE	8 bit mem/IO	16 bit mem	16 bit IO
ON	ON	0	0 (6)	0 (3)	0 (3)
ON	OFF	1	0 (6)	1 (4)	0 (3)
OFF	ON	2	1 (7)	1 (4)	1 (4)
OFF	OFF	3	2 (8)	2 (5)	1 (4)

X (Y) : X # of added wait state.
Y # of total cycles.

Remarks: SW1-5 has no pre-set function, it can be set either ON or OFF.

2.5 ROM JUMPER SETTING AND ROM CHIPS INSTALLATION (J15)

The system board has jumper (**J15**) which determines the ROM size and type of ROM being used in this system board.

JUMPER SETTING	ROM CHIP INSTALLATION		TOTAL ROM SIZE & TYPE
J15	U60	U61	
1-2	27256	27256	64K EPROM
2-3	27128	27128	32K EPROM

2.6 DISPLAY ADAPTER SELECTION (SW1-6)

A dip switch named SW1-6 is used to tell the system which display adapter is activated.

SW1-6	ADAPTER TYPE
ON	Color Graphics ADAPTER OR Enhanced Graphics Adapter
OFF	Monochrome ADAPTER

2.7 80287 CO-PROCESSOR CLOCK RATE SELECTION (J6 & J7)

The co-processor clock rate depends on the co-processor clock speed and also the CPU clock speed. Users need to select the appropriate jumper according to their co-processor part number.

COPROCESSOR PART NO.	CPU CLOCK RATE		J7	J6	ACTUAL COPROCESSOR CLOCK RATE	
	HIGH	LOW			HIGH	LOW
80287-12	12	8	OPEN	1-2	12	8
	10	6	OPEN	1-2	10	6.7
80287-10	12	8	CLOSE	2-3	8	5.3
	10	6	OPEN	1-2	10	6.7
80287-8	12	8	CLOSE	2-3	8	5.3
	10	6	CLOSE	2-3	6	4.4
80287-6	12	8	CLOSE	1-2	4	2.6
	10	6	CLOSE	2-3	6	4.4

2.8 BATTERY SELECTOR (J12 & J13)

J12 & J13 are used to determine what kind of battery will be used for this system board. Either off-board battery pack or on-board lithium battery can be selected.

JUMPER SETTING		BATTERY TYPE
J12	J13	
1-2	CLOSE	ON BOARD DOUBLE LITHIUM BATTERY COINS (3V EACH)
OPEN	CLOSE	OFF BOARD LITHIUM BATTERY PACK (6V)
OPEN	OPEN	OFF BOARD ALKALI BATTERY PACK (6V)

CAUTION: Never connect off board battery pack with on board battery option selected.

2.9 POWER GOOD SELECTOR

J14 is used to select Power Good reset source from either power supply or on board circuitry. The on-board power good generator is used for XT upgrade, using XT power supply without Power Good signal or signal not complied with the required specification.

J14	POWER GOOD RESET SOURCE
2-3	POWER SUPPLY
1-2	ON-BOARD POWER GOOD GENERATOR

PART III

Connectors Pin Assignment

PART III

Connectors Pin Assignment

3.1 SPEAKER CONNECTOR (P1)

PIN NUMBER	FUNCTION
1	SPEAKER +
2	KEY
3	GND
4	SPEAKER -

3.2 KEY LOCK & POWER LED CONNECTOR (P4)

PIN NUMBER	FUNCTION
1	+5
2	POLARIZATION PIN
3	GND
4	KBD INH
5	GND

3.3 RESET CONNECTOR (P3)

3.4 EXTERNAL BATTERY CONNECTOR (P8)

PIN NUMBER	FUNCTION
1	+6V
2	KEY
3	SPARE
4	GND

3.5 KEYBOARD CONNECTOR (P7/P6)

PIN NUMBER	FUNCTION
1	CLOCK
2	DATA
3	SPARE
4	GND
5	+5V

3.6 TURBO LED CONNECTOR (P2)

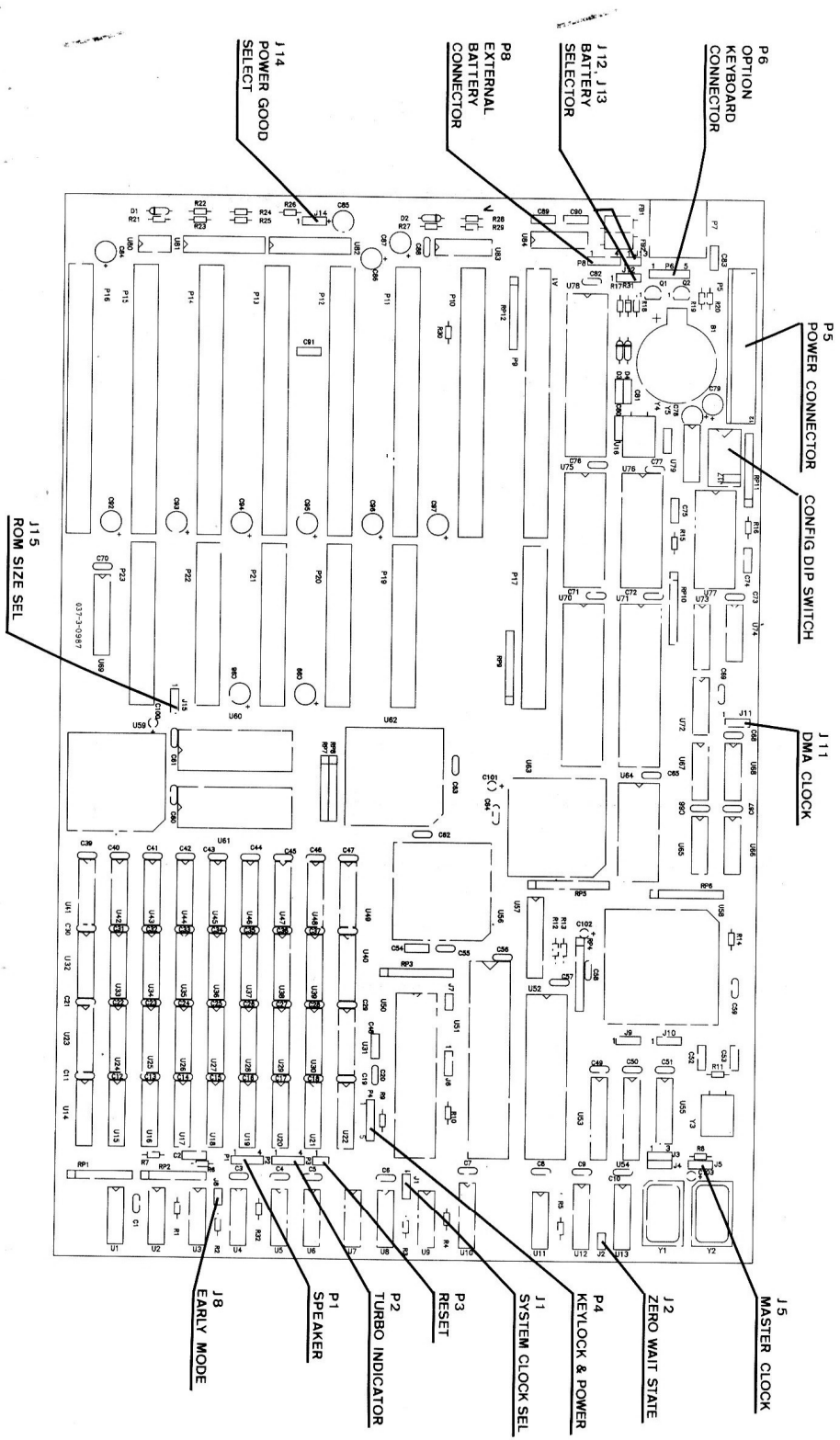
PIN NUMBER	FUNCTION
1	SPARE
2	SPARE
3	CATHODE
4	ANODE

3.7 POWER CONNECTOR (P5)

PIN NUMBER	FUNCTION
1	POWER GOOD
2	+5V
3	+12V
4	-12V
5	GND
6	GND
7	GND
8	GND
9	-5
10	+5
11	+5
12	+5

PART IV

Layout Of BABY 286MB
MINI AT-SYSTEM BOARD

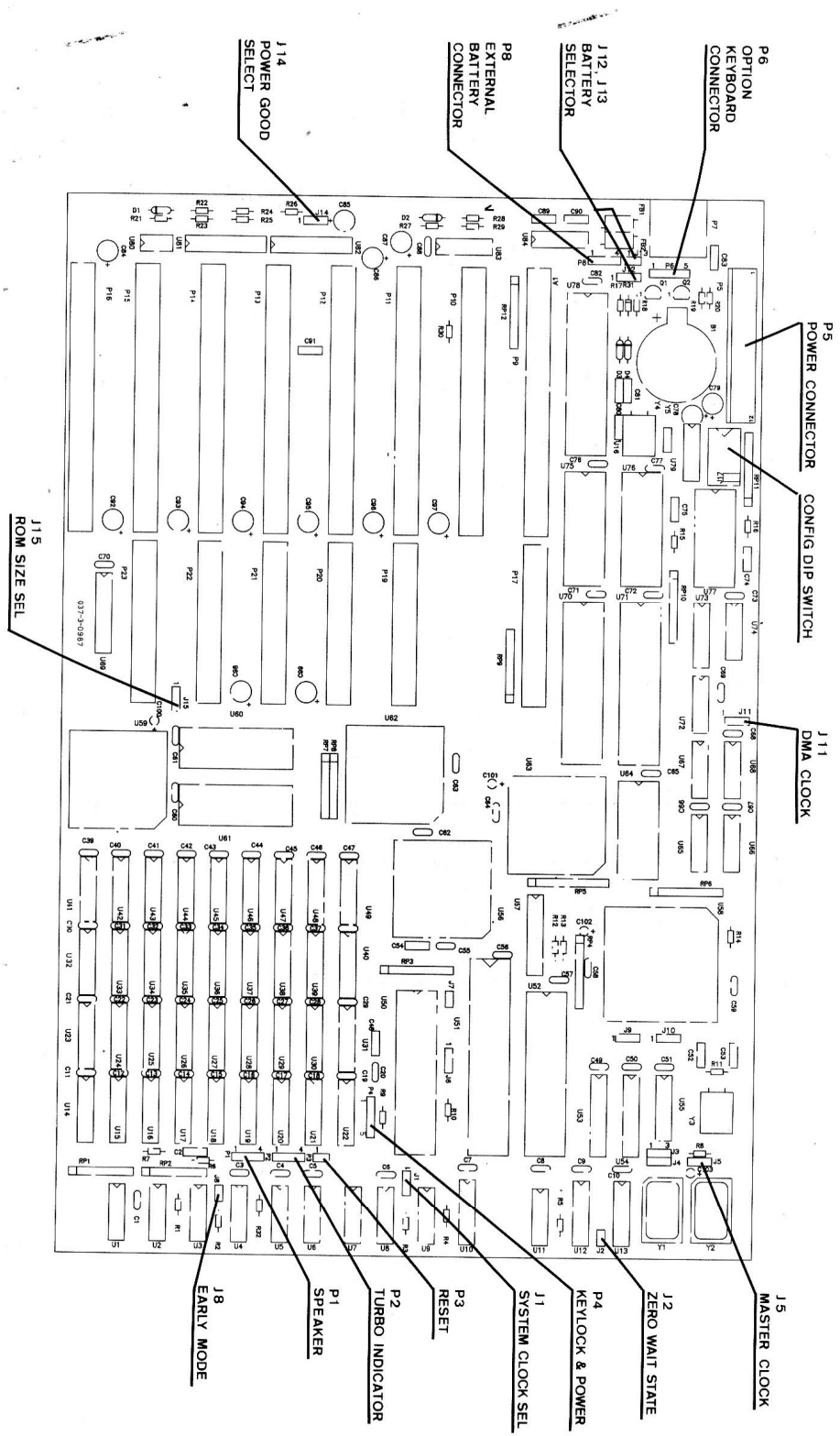


FACTORY SETTING

Thank you for the purchase of our product.

This mother board has jumpers and dip switch for configuration setting. Please refer to the reference manual Part IV for the location of jumpers and dip switch. The following jumpers has pre-set in the factory. If your configuration is different, please change acccording the Part II of the manual.

SETTING		CONFIGURATION
SW1-1 SW1-2	ON ON	MODE 0
SW1-3 SW1-4	OFF OFF	1 MB
SW1-6	ON	CGA/EGA
J1	2 - 3	SOFTWARE SELECT MODE
J6 J7	2 - 3 CLOSE	80287-8
J5 J11 J2 J8	1 - 2 1 - 2 CLOSE CLOSE	10 MHz ZERO WAIT STATE
J12 J13	OPEN OPEN	OFF BOARD BATTERY
J14	2 - 3	POWER SUPPLY POWER GOOD
J15	2 - 3	32K EPROM (27128)



NOTE TO USER

1. Introduction

BABY286MB Plus is an upgrade to BABY286MB. This mother board is using 12 MHz CPU, 12MHz Chip Set and has factory pre-set to be operated at 12MHz zero wait state. A 48 MHz crystal oscillator is installed on the mother board which allows users to operate at 12MHz and 8 MHz.

2. Amendment to BABY286MB MINI AT-SYSTEM BOARD REFERENCE MANUAL (VERSION 1.10):

I) 2.2 SYSTEM CLOCK AND MEMORY WAIT STATE SELECTION (P.19-21)

12MHz One Wait State

J2 Open
J8 Open

12MHz Zero Wait State

J2 Close
J8 Close

II) 2.3 OPERATING SPEED (J1 & J5) (P.22)

Hardware Select Mode		J1
	8 M	1_2
	12 M	OPEN
Software Select Mode		2_3

III) 2.7 80287 CO-PROCESSOR CLOCK RATE SELECTION (J6 & J7) (P.26)

COPROCESSOR PART NO.	CPU CLOCK RATE		J7	J6	ACTUAL COPROCESSOR CLOCK RATE	
	HIGH	LOW			HIGH	LOW
80287-12	12	8	OPEN	1_2	12	8
80287-10	12	8	CLOSE	2_3	8	5.3
80287-8	12	8	CLOSE	2_3	8	5.3
80287-6	12	8	CLOSE	1_2	4	2.6