

# **APEX II**

**Single Board Computer  
(SBC)**



**BLUE CHIP TECHNOLOGY**

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**User Manual**

# **APEX II**

## **User Manual**

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## Amendment History

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3.0	07/06/96	EGW	Revised for PCB Issue 3.x. 386 option removed. 3v3 option added. Clock synth options added. -5 & -12 V connectios added. Contents re-instated. Bus Connector table errors corrected. List of supported CPUs updated. Ext battery voltage was 3.6 V.
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## **Company Profile**

Blue Chip Technology is the leading specialist PC product manufacturer in UK/Europe.

Blue Chip Technology provides innovation with quality design and manufacturing from a single source.

Based in the North West, our purpose built complex contains one of the most advanced research and development facility, engineering workshop and production lines.

Specialising in the provision of industrial computing and electronic solutions for a wide range of UK and European organisations, Blue Chip Technology has one of the UK's largest portfolios of industrial PCs, peripherals and data acquisition cards. This extensive range of products, coupled with our experience and expertise, enables Blue Chip Technology to offer an industrial processing solution for any application. APEX II is the latest addition to our portfolio, providing a cost effective product development and volume production tool for OEMs.

A unique customisation and specialised system integration service is also available, delivering innovative solutions to customers problems. The company's success and reputation in this area has led to a number of large design and manufacturing projects for companies such as BNFL, Aston Martin, Jaguar Sport and British Gas.

British Standards Institute approval (BS EN ISO 9001) means that all of Blue Chip Technology's design and manufacturing procedures are strictly controlled, ensuring the highest levels of quality, reliability and performance.

Blue Chip Technology also continue to invest in the latest technology and skills to provide high performance computer and electronic solutions for a worldwide customer base.

Blue Chip Technology would like to thank you for purchasing this product and we hope the APEX II enables you to prosper in the future.



## **Preface**

### **The PC as an Embedded Control Solution**

As today's OEMs battle to develop leading edge products as fast as possible and with minimal cost, the APEX II SBC provides an innovative solution. Designed to provide a high performance, compact hardware solution, with maximum configuration, compatibility and flexibility, APEX II is a complete PC on a single card. This allows OEMs to incorporate PC microprocessor control into a wide range of products with ease.

Traditional methods of embedding computer control into products are being challenged by the latest developments in embedded PC technology. This has resulted in a dramatic increase in the number of applications which are using the PC as an embedded control solution.

Until recently, the only options were expensive and bulky bus board products such as VME or STE or the resource hungry solution of designing a micro controller from scratch. By using the APEX II processor as a "drop-in" alternative, OEMs can gain clear cut advantages in design, production and product enhancement.

The following examples show why :

- The PC is the best understood hardware interface in the world
- The APEX II is a complete sub-system, so design is minimised
- Resource can be focused on the application specific features of the target product
- Development resource is reduced, saving time and money
- PC application software enhances product functionality
- User familiarity with DOS and Windows interfaces enhances product attractiveness
- Low cost and well understood development tools reduce personnel learning curves
- An off-the-shelf solution reduces material needs and costs
- Reduced time to market maximises sales and optimises profit

The PC has become the control solution for many current applications, some of these include :

- Food and Drink Processing
- Water/Gas/Oil and Electricity control
- Retailing (EPOS etc.)
- Marine
- Medical Equipment
- Security Systems
- Mobile Data Terminals
- Banking and Insurance services

The list is almost endless and demonstrates the true versatility of the PC platform.

## **1. INTRODUCTION**

### **1.1 Manual Objectives**

This manual describes in detail the Blue Chip Technology APEX II Single Board processor card.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of APEX II.

The manual is sectioned into logical parts and includes a User Guide which will help the non technical get the unit up and running. A Troubleshooting Guide is also included to help when things go wrong.

We strongly recommend that you study this manual carefully before attempting to interface with APEX II or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen move J9 to "clear" position for 5 minutes.

For further detailed information on this problem please see the section under AMI BIOS Set-up in the Software Technical section.

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Support department with the relevant details.

## 1.2 Limitations of Liability

In no event shall Blue Chip Technology be held liable for any loss, expenses or damages of any kind whatsoever, whether direct, indirect, incidental or consequential, arising from the design or use of this product or the support materials supplied with this product. If this product proves to be defective, Blue Chip Technology is only obliged to replace or refund the purchase price at Blue Chip Technology's discretion according to their Terms and Conditions of Sale.

## 1.3 CMOS Static Discharges

### WARNING

The devices on this card can be fatally damaged by static electricity. Ensure that you take necessary static precautions, ideally wear an approved wrist strap or touch a suitable ground to discharge any static build up. This should be repeated if the handling is for any length of time.

When carrying the board around, please place it into the non-conductive bag in which it came. This will prevent any static electricity build up.

## 1.4 On-Board Battery

This board is fitted with a Lithium battery. Great care should be taken with this type of battery. Under NO circumstances should :

- \* the outputs be shorted
- \* be exposed to temperatures in excess of 100°C
- \* be burnt
- \* be immersed in water
- \* be unsoldered
- \* be recharged
- \* be disassembled

If the battery is mistreated in any way there is a possibility of fire, explosion, and harm.

## 1.5 Related Publications

The following publications will provide useful information related to the Standard Personal Computer and can be used in conjunction with this manual.

- IBM Personal Computer AT Technical Reference, 1502494, IBM, 1984.
- IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference, 15F0306, IBM, 1987.
- The Programmers PC Sourcebook, Microsoft
- The Winn L. Rosch Hardware Bible, Brady
- PC104 Consortium Technical Specification

For more information on the major integrated circuits used in APEX II please refer to the following technical manuals :

- UMC UM8498 and UM8496 Applications Data Book
- Cirrus Logic CL-GD62XX Application Book Rev 5.0
- SMC 37C663 Applications Data Book
- Megakey 8742 Technical Reference

## 1.6 Trademarks

IBM, PC, AT and PS/2 are trademarks of International Business Machines Corporation (IBM).

AMI WinBIOS BIOS is a trademark of American Megatrends Inc.

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All 80x86 processors are registered trademarks of Intel Corporation.

MSDOS and WINDOWS are registered trademarks of the Microsoft Corporation.

SimulSCAN is a registered trade mark of Cirrus Logic Inc.

PC/104 is a registered trademark of the PC/104 Consortium.



## 2. THE APEX II PRODUCT RANGE

### 2.1 General Overview

Where space and complexity rule out a passive backplane or card cage, the APEX II SBC comes into its own. All of the normal PC functions are provided on a single card. If your space requirements are too small for APEX II, please ask for information on our APEX 104 range of PC/104 compatible stacking modules.

All the normal PC functions are present on APEX II. It can be used as a standalone development tool simply by adding a keyboard, monitor and disk drives (IDE or floppy).

APEX II can also be plugged into a custom electronics assembly (via its PC/104 optional stack through connectors), allowing you to add microprocessor control to any application specific electronic design. Or alternatively, further functionality can be designed in by adding one or more of our PC/104 compatible Support Modules.

For extra flexibility we have also included one standard 16 bit ISA slot so that any PC XT/AT card can simply be plugged in and used. This can be useful if you have a custom AT card, or if the I/O functionality you require is not available via the PC/104 range.

By using a small ISA riser card, PC/AT cards can be made to mount on top of the APEX II board thus making a compact PC solution. Please call our Sales department for further assistance.

## 2.2 APEX II Specification

- Choice of microprocessor 486SX25 to 486DX4 and Pentium P24T in PGA format.
- Up to 16 MBytes of DRAM memory using two 72 pin SIMM sockets. Supports 256K x 36, 1M x 36 and 4M x 36 bit SIMM modules.
- Up to 512KBytes SRAM in one 32 pin DIL socket.
- 1MB of on-board Flash as standard (Expandable up to 3MBytes by one 32 pin DIL socket).
- VIDEO drive for both LCD and CRT displays (640x480 and 1024x768 respectively).
- 512KBytes of Video Memory.
- AMI BIOS with built in set-up program.
- Megakey BIOS.
- Hardware EMS support (LIM 3.2 and 4.0 compatible).
- PC/104 Compatible interface (FULL PC/AT pin out specification).
- One 16-bit ISA slot.
- Selectable Shadow RAM for system and video BIOS.
- Selectable Bus speed.
- Automatic or Manual Peripheral Configuration.
- Two Asynchronous serial ports (16C550 compatible) with LC filters - Both software selectable as either RS232 or RS485.
- Channel programmable Digital I/O (8255 compatible).
- Bi-Directional parallel port.
- IDE interface for AT hard drives (2 drives supported). LBA modes supported.
- Floppy Disk controller (UPD72065B compatible).
- AT and PS/2 compatible keyboard port.
- PS/2 Mouse port.
- Customer "sign-on" information held in E<sup>2</sup>PROM (64 Bytes available for user operation).
- Software selectable Watchdog timer.
- On-board speaker with external drive provided.
- On-board "Power Good" signal generation.
- On-board 3.6 Volt battery for SRAM and RTC.
- +5 Volt only operation. Additional cards connected directly to the APEX II may require  $\pm 12$  and/or -5 Volts for correct operation. These must be provided by the user.
- 0 °C to + 55 °C operating temperature.



- -25 °C to + 85 °C storage temperature.
- 0 to 95% non-condensing relative humidity.
- 8-Layer PCB using conventional and Surface Mount Technology.

### 2.3 Power Requirements

Due to the variable nature of this type of product, it is difficult to give definitive values. However, we offer the following list as a guide to typical current requirements:

Standard APEX II with a 486SX25 + 4MB DRAM = 2.10 Amps  
Standard APEX II with a 486SX25 + 8MB DRAM = 2.30 Amps  
Standard APEX II with a DX4/100 + 4MB DRAM = 2.50 Amps  
Standard APEX II with a DX4/100 + 8MB DRAM = 2.60 Amps

### 2.4 PC/104 Support Modules

A range of support modules have also been designed. Measuring 90mm by 96mm, they provide a wide range of I/O interfaces to the outside world. We list the items that we currently offer below.

<b>Planned Modules</b>	<b>Description</b>
APX-NET	Ethernet LAN controller card
APX-PCM	PCMCIA card controller
LCD-PSU	LCD BIAS display controller card
APX-SIO4	4 Channel serial card

## **2.5 Standard PC AT I/O cards**

As APEX II has a single ISA slot fitted as standard, it is possible to insert any of the currently available standard PC/AT cards. This enables your final design to incorporate functions not found on the standard range of PC/104 cards.

For more information on this see the Technical Hardware section later in this manual.

Blue Chip Technology is one of the UKs leading manufacturers of PC data acquisition and specialised I/O cards.

Our design and manufacturing capabilities enable us to provide a customised embedded processing solution, providing you with a range of cards tailor-made for your application needs.

If the module you require is not listed or you need a standard PC/AT card, please call our Sales Office for further information and pricing.

## 3. USER GUIDE

### 3.1 Introduction

This section of the manual describes how to connect the APEX II Single Board Computer to other PC hardware. It also describes how to add memory to the SBC.

**We strongly recommend** that you study this User Guide before attempting to interface to APEX II, as incorrect use of the I/O connections may result in permanent damage.

This section is intended to get the unit up and running as quickly as possible. For further technical information on APEX II please read the Hardware and Software Technical sections of this manual.

#### WARNING

The devices on this card can be fatally damaged by static electricity. Ensure that you take necessary static precautions, ideally wear an approved wrist strap or touch a suitable ground to discharge any static build up. This should be repeated if the handling is for any length of time.

#### 3.1.1 Initial Inspection

Before you begin to install or connect to your APEX II unit, please make sure that the following materials have been shipped :

- 1 x APEX II unit to your order specification (CPU/Memory where ordered).
- 1 x APEX II Software Utilities Disk (SUD).
- 2 x APEX II Screen Driver Disks.
- 1 x APEX II VGA cable.

If you should find any items missing or damaged, please contact Blue Chip Technology immediately.

We have carefully inspected the APEX II unit mechanically and electrically before despatch. It should be free from marks and scratches and in perfect working order upon receipt.

As you unpack the APEX II unit, check it for signs of shipping damage (damaged box, scratches, dents, etc.). If it is damaged or it fails to meet the specifications, notify our Customer Service department immediately. Also notify the carrier. Retain the shipping carton and packaging material for inspection by the carrier. After inspection we will make arrangements to replace or repair the unit.

If for any reason you need to contact us please read Appendix L at the rear of this manual.

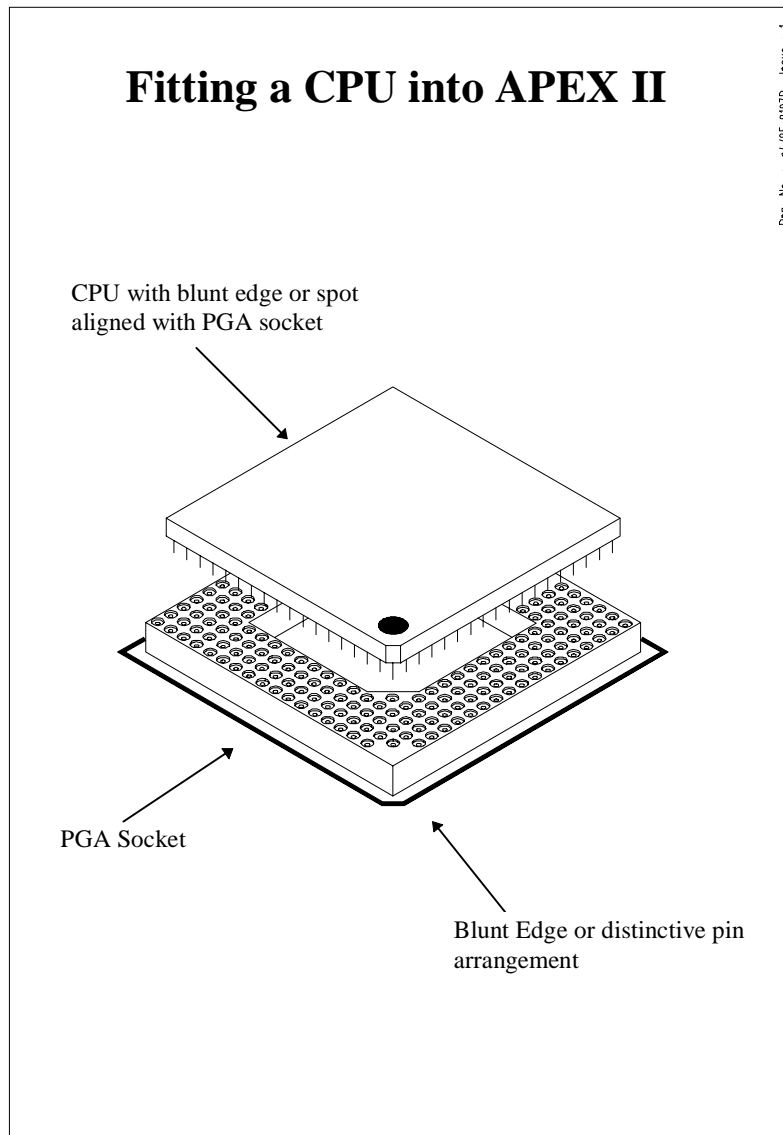
## 3.2 Getting Started

### Fitting a CPU?

If you have ordered your APEX II SBC without a factory fitted CPU please follow the following procedure:

- Ensure that all power is removed from the APEX II SBC and its peripherals.
- To prevent damage from static discharge to the CPU and APEX II, touch the metal chassis of the computer to ground yourself.
- Check that the CPU you intend to fit is supported by the APEX II hardware and BIOS. A list of supported CPUs is provided in Appendix P. Ensure that if the CPU you intend to fit is not a 5 Volt device, that you set the correct jumpers on header J13. Failure to do so could result in serious damage.
- APEX II is fitted with a 237 pin Low Insertion Socket (LIS) Pin Grid Array (PGA) CPU socket located near to the ISA expansion connector (see Appendix A). It has four rows of pins. The inner are used for DX/2 CPUs and above. The outer pins are used only by P24T devices.
- It is essential that the CPU is correctly orientated to the PGA socket for success. Failure to correctly align the CPU may result in damage to both the CPU and APEX II. Before inserting the CPU please refer to the accompanying figure which illustrates the correlation between the blunt edge or spot on one of the CPU corners and the distinctive pin arrangement on one corner of the socket plus the blunt edge on the silkscreen on the PCB..

- 
- Once the CPU is correctly orientated then firm and equal pressure is required to push home the CPU into the socket correctly.
  - Please check that the frequency selection links are correctly set for the selected CPU, see section 3.2.1 for further details.
  - Finally, once the SBC is powered on check the setup options in the BIOS to ensure that any frequency dependant parameters are set before attempting to boot an operating system.



If you have not ordered the APEX II with a complete set of cables or want to build your own, the following pages will show you how to connect to ALL of the output connectors found on the unit.

Appendix B at the rear of this manual shows an outline plot of APEX II.

Using this plot and the table shown in part 3.2.1 of this section, make sure that the configuration jumpers are set in the default positions.

#### Note

If you are not certain of the function of the pin outs of the connectors and want to check this information, the Hardware Technical section of this manual provides more in-depth information.

If you still are uncertain then either call your area sales engineer or the Customer Support department at Blue Chip Technology for assistance. Please consult the Documentation and Technical Support section before telephoning.

### 3.2.1 Start-up Configurations for Option Jumpers

The link settings shown below are the default settings and not the only ones possible. Please refer to Appendix C for the full list of options.

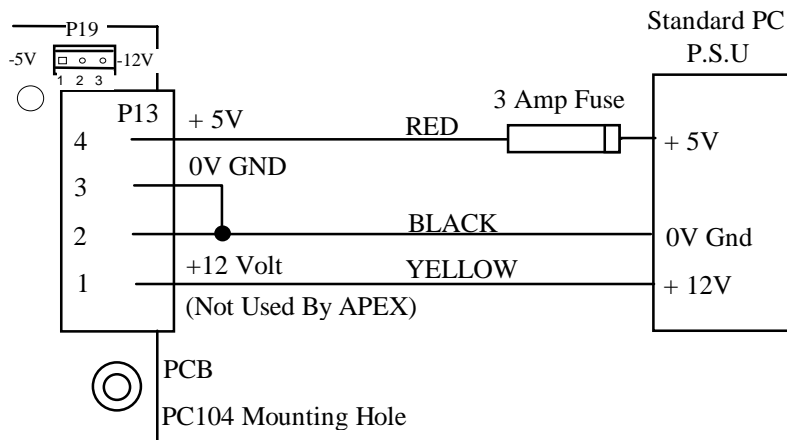
Jumper	Area of Influence	Default Link	Action
J1	Selects the frequency of the on board clock which drives the microprocessor. Four links are used numbered 1, 2, 3 and 4. A = Link Absent P = Link Present	<b>1 2 3 4</b> P A P A A A P A	<b>Processor Freqy.</b> 25 MHz 33 MHz The defaults are processor dependent. See Appendix C
J2	Selects 486 SX or DX operation Two links are fitted for DX option and one link for SX option	<b>1 2 3 4</b> 1-2 3-4 2 - 3	<b>Processor Dependent</b> 486 DX 486 SX
J3	Selects the LCD Display type to be interfaced. Three links are used for this numbered 1,2, and 3. Please see Appendix M for more information.	<b>1 2 3</b> A A P A P P P A P P P P	<b>Display Type Dependent</b> TFT Colour 9/12/18 bits Monochrome Dual Scan STN Colour Dual Scan STN Colour Single Scan
J4	On Board Video Control	2 - 3	On board video Enabled
J5	Power Save Switch	Open	Do not use
J6	IDE Ground Link	Link	P12 Pin 34 shorted to ground
J7	LPT Printer IRQ Selection	1 - 2	IRQ 7 Selected LPT 1
J8	Selects either Internal or External Battery supply	2 - 3	Selects Internal Battery
J9	CMOS Battery Clear Connects to power CMOS	1 - 2	Battery Connected
J10	Selects the control mode of serial port 1 P12 if used in RS485 mode	None	Full Duplex Selected
J11	Selects the control mode of serial port 2 P12 if used in RS485 mode	None	Full Duplex Selected
J12	Selects Processor Type 3 pins adjacent to J2 (Pin1 at top)	1 - 2 2 - 3	<b>Processor Dependent</b> 486 DX or SX P24T
J13	Selects Processor Voltage 4 pairs of pins adjacent to J2 (Pin 1 at top)	<b>1 2 3 4</b> A A A A P P P P	<b>Processor Dependent</b> 3V3 CPU 5V CPU



### 3.3 Connecting to the I/O headers

#### 3.3.1 Connecting the Power Lead

Locate the connector P13 (a 5¼" disk drive type connector) at one corner of the PCB. Either connect the cable labelled Power to this connector or wire the connector as shown below. The use of an in-line fuse is recommended.



#### WARNING

Please ensure that you follow the power wiring as shown above and not the numbers that might be shown on any connectors you are using.

The +12 Volt input (Yellow wire) at P13, and the -5 Volt and -12 Volt connections provided at P19 are not required for correct operation of the APEX II unit, but may be required by either PC/104 or ISA expansion cards. They are provided only for compatibility with existing expansion cards.

Connector	P13	P19		
	pin 1	+12 V	pin 1	-5 V
	pin 2	0 V	pin 2	0 V
	pin 3	0 V	pin 3	-12 V
	pin 4	+5 V		

**DO NOT SWITCH ON THE POWER SUPPLY YET.**

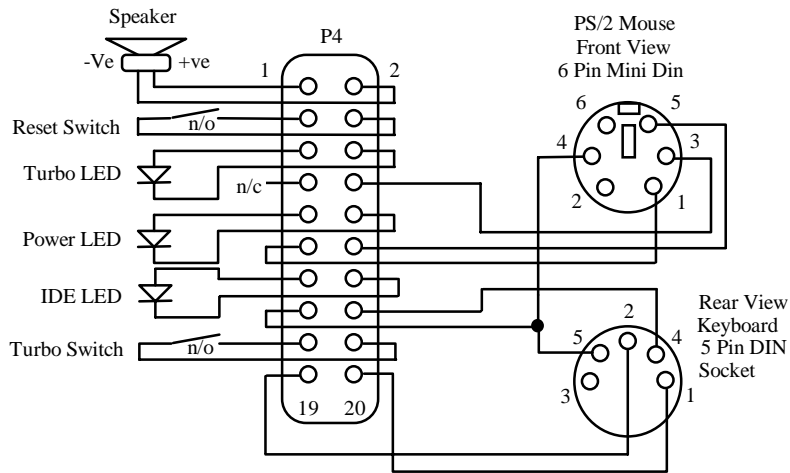
### 3.3.2 Connecting to the Peripherals / Utilities header

Locate connector P4 on the PCB.

This header provides connections to the following :

- Keyboard.
- PS/2 Mouse.
- Speaker Drive.
- Reset switch.
- Power LED.
- Turbo LED.
- IDE Status LED.
- Turbo Switch Input.

Either connect the optional cable labelled Perif to this connector or wire the connector as shown below:



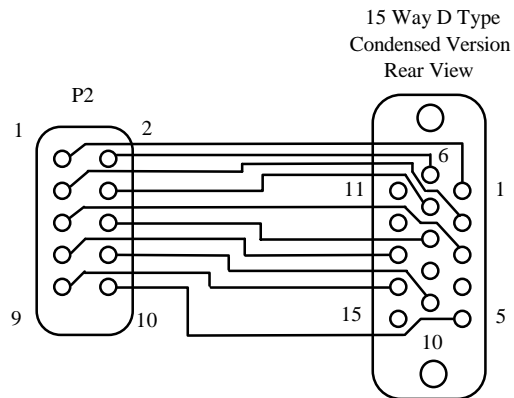
#### Note

All LED drive outputs have a 220 $\Omega$  serial resistor connected to the +5 Volt supply rail, and the +5 Volt supply to the keyboard is fused (by an SMD fuse) at 2 Amp.

### 3.3.3 Connecting to the CRT Display Header

The specifications of the types of CRT displays you can use via this connector are listed in the Technical Hardware section, but as a good starting point use either a standard VGA or SVGA PC compatible CRT screen.

Locate connector P2 on the PCB and either connect the optional cable labelled CRT to this connector or wire the connector as per the details below :



Note

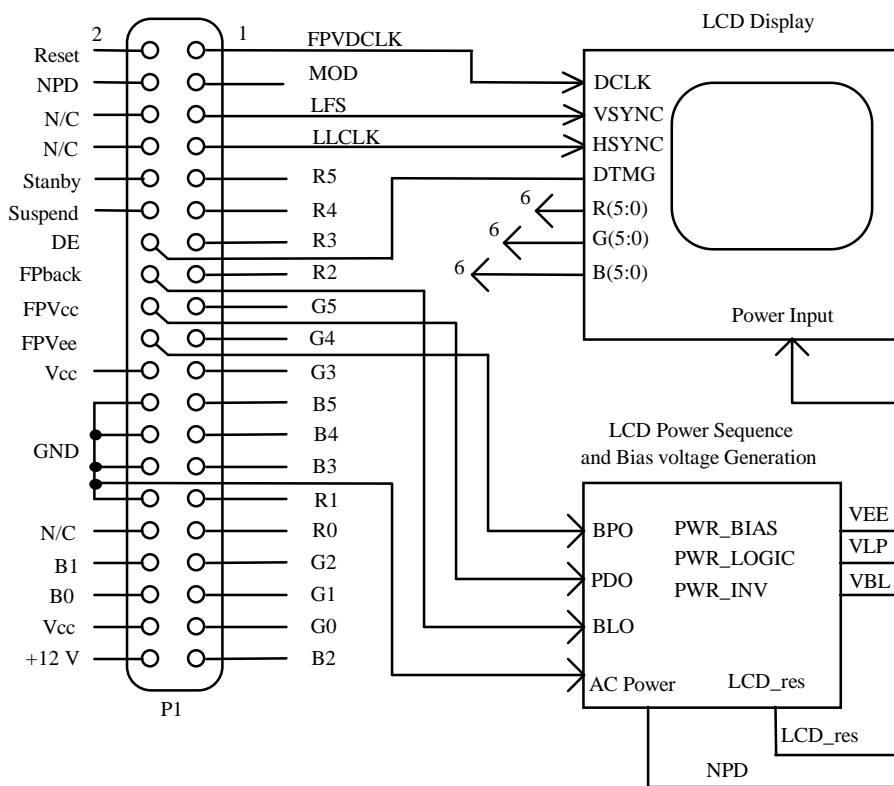
The pinout of P2 does not directly match the normal condensed 15 way D type connector pinout used to drive CRT displays.

Please insure that you follow the above wiring diagram carefully.

We would also recommend the use of crimp style subminiature D connectors for the CRT end of the cable.

### 3.3.4 Connecting to the LCD Display Header

The specifications of the types of LCD displays you can use via this connector are listed in the Technical Hardware section and Appendix M gives detailed information on Flat Panel Interface Connection details. However, the basic wiring concepts are shown below for guidance.



#### Note

A cable is not supplied for this connector due to the wide variety of displays available.

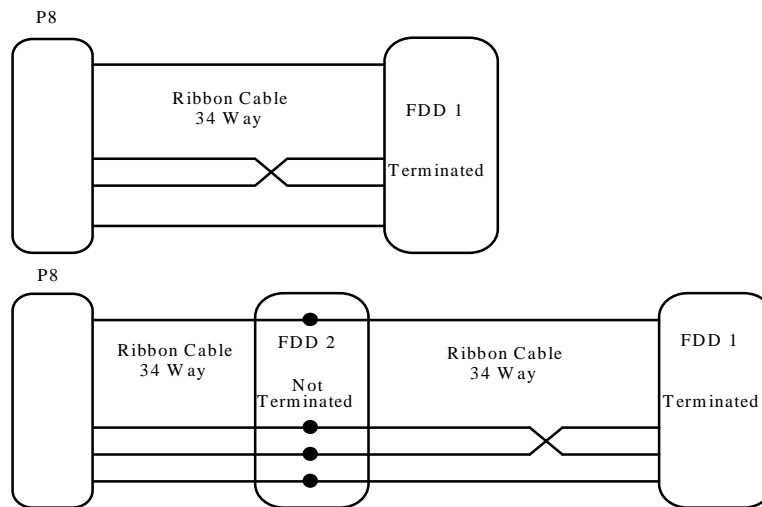
### 3.3.5 Connecting to the Floppy Disk Drive Header

The specifications of the floppy disk drives that can be attached are listed in the Technical Hardware section. A 1.44 MByte 3½" disk drive is the default.

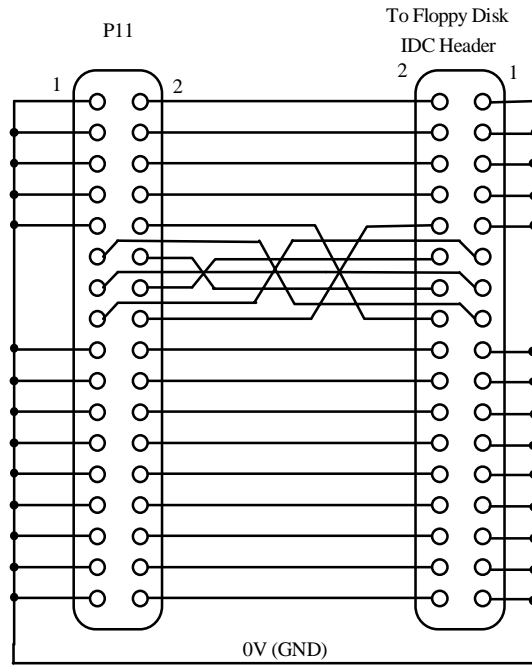
Locate the connector P8 on the PCB and connect the optional cable labelled FDD to this connector and the other end to the floppy disk drive. Then add a power cable to the disk drive, which is part of the Development kit power supply. Alternatively, wire the disk drive as per the details in section 3.3.5.1.

You can attach 1 or 2 disk drives to the APEX II.

The jumpers on the disk drives should be set to drive 1 not drive 0. To connect only 1 drive, use a cable with a twist in it (between pins 10 and 16) at the disk drive end. For 2 drives use a daisy chain cable with the twist in the second section leading to drive 1.



If you want to make up your own single drive cable then wire the connectors as follows :



Note

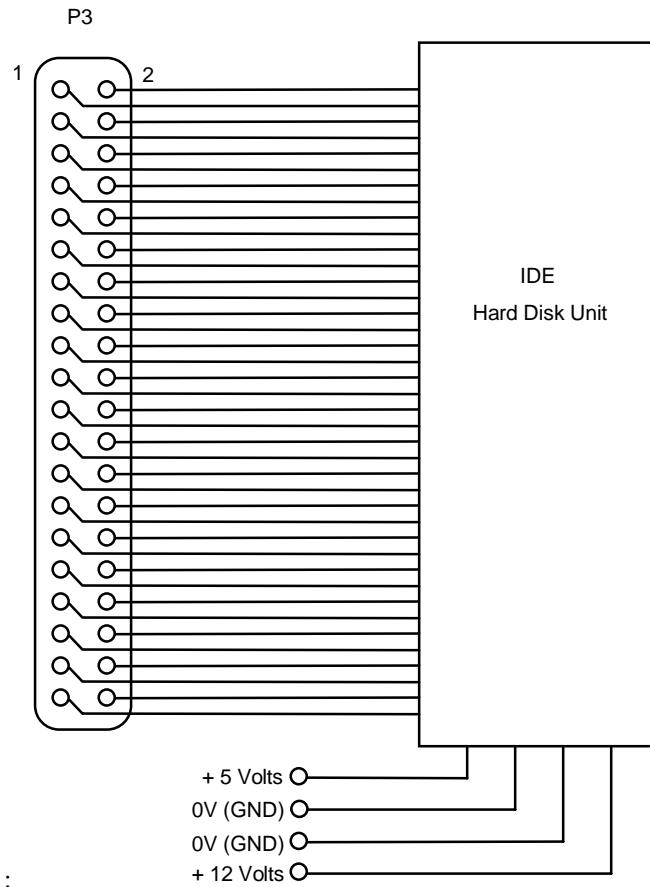
The above wiring is for a single disk drive which is terminated and set to drive 1, not drive 0.

Also note that the cable is just a point to point IDC ribbon cable with a twist, starting at wire 10 and going to 16.

### 3.3.6 Connecting to the IDE Disk Drive Header

The specifications of the hard disk drives you can use via this connector are listed in the Technical Hardware section, but as a good starting point use a modern PC 3½" IDE drive.

Locate connector P3 on the PCB and connect the optional cable labelled IDE HDD to this connector and connect the other end to the hard disk. Then add a power cable to the disk drive, which is part of the power supply. Alternatively, wire the disk drive as per the details below:

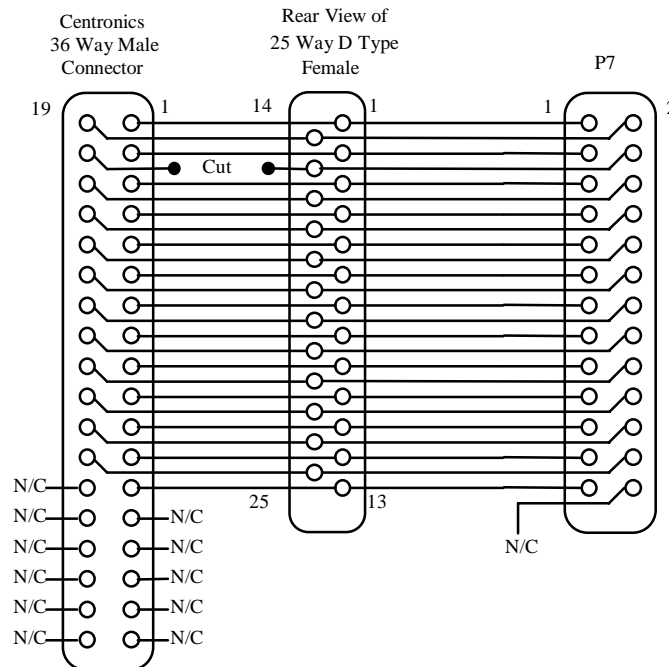


### 3.3.7 Connecting to the Parallel Port

Locate connector P7 on the PCB and connect the optional cable labelled PAR to this connector. Alternatively, wire the cable as per the details below:

#### Note

The direct pin out of P7 is **different** from that on a standard 25 way 'D' type. This is shown below.



#### Note

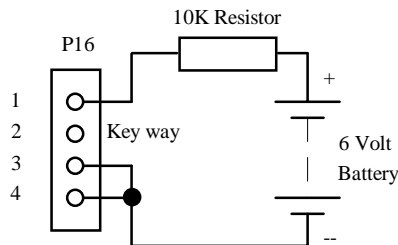
The Centronics connector shown is a IDC ribbon type and when assembled, wire 4 (pin 15 of 25 way D) **MUST BE CUT** for correct operation



### 3.3.8 Connecting an External Battery

As the APEX II unit comes complete with its own on-board battery you should not need to worry about this section. However, if your application needs an external battery, then please follow the procedures as detailed below:

Locate connector P16 on the PCB (near the PC/104 connectors) and wire an external battery to the diagram below:



The battery should have an output of 6 Volts, a capacity of 1.8AH and be fitted with a 10K series resistor for safety.

#### WARNING

Great care should be taken with Lithium batteries. Under NO circumstances should :

- \* the outputs be shorted
- \* it be exposed to temperatures in excess of 100°C
- \* it be burned
- \* it be immersed in water
- \* it be unsoldered
- \* it be recharged
- \* it be disassembled

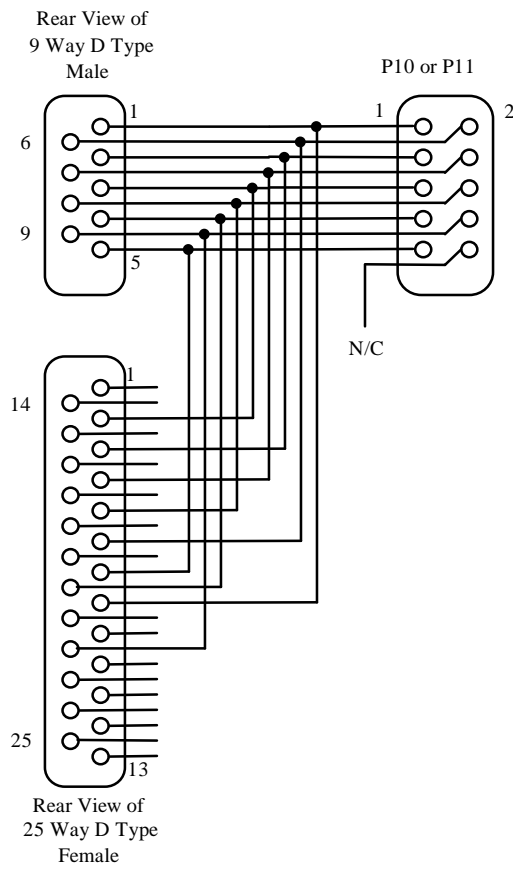
If the battery is mistreated in any way there is a possibility of fire, explosion and harm.

Re-fit jumper J8 to short between positions 1 and 2 to select EXT battery.

### 3.3.9 Connecting to the Serial Headers

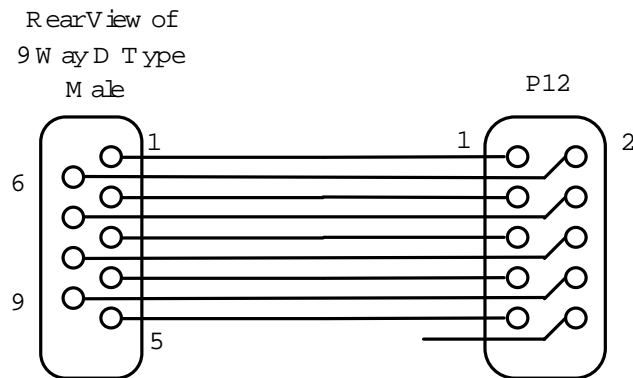
#### Wiring 9 or 25 way 'D' types as RS232

Locate connectors P10 and P11 on the PCB and connect the cables labelled Serial 1 and Serial 2 to these connectors. Alternatively, wire the connectors as per the details below:



### 3.3.10 Wiring 9 way 'D' types as RS485

Locate connector P12 on the PCB and connect the cable labelled RS485 to this connector. Alternatively, wire the connectors as per the details below:

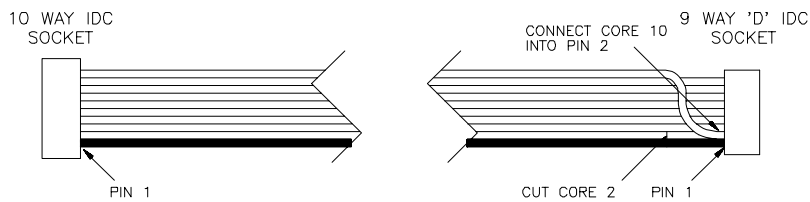


Note

Unlike the RS232 standard there is no recognised standard for wiring RS485 connectors. The above diagram shows how our RS485 cable is wired and how the wiring would look using standard IDC type connectors.

#### RS485 Port Configuration

To retain continuity, and for ease of support, APEX II units supplied with the 485 port option, should have the ribbon cable connecting the 10-way IDC Header to the 9-way D-Type Female connector configured as :



This would give the following signals on the 9-way D-Type :

<u>RS-485 Port 1</u>		<u>RS-485 Port 2</u>	
<u>Pin</u>	<u>Function</u>	<u>Pin</u>	<u>Function</u>
1	Tx +	7	Tx +
2	Tx -	8	Tx -
3	Rx +	9	Rx +
4	Rx -	6	Rx -

Pin 5 is GND

A 9-way Loop-Back Connector for testing purposes should be wired as follows:

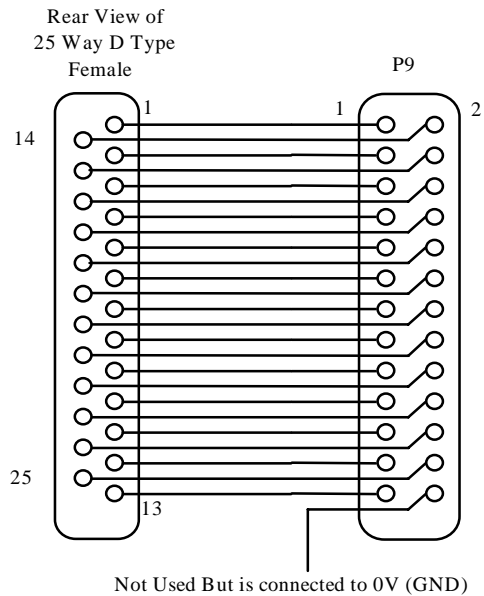
Pin 1 ----- Pin 3  
 Pin 2 ----- Pin 4  
 Pin 7 ----- Pin 9  
 Pin 8 ----- Pin 6

### 3.3.11 Connecting to the Digital I/O Header

Locate the connector P9 on the PCB and connect the optional cable labelled PIO to this connector. Alternatively, wire a cable as per the details below:

#### Note

The Digital I/O port has many applications and as such it is impossible to provide a definitive wiring diagram. However, the details below show the basic wiring to a 25 way 'D' type. Appendix H at the rear of this manual gives a complete insight into the workings of the 70155 PI/O and how to terminate the outputs. All outputs can be pulled up to the Vcc rail or down to GND via the optional on-board 10K SIL resistor packs.

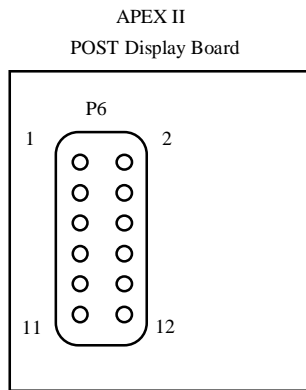


### 3.3.12 Connecting to the APEX II POST Display Header

If you have the APEX II POST Deader Display unit. Locate connector P6 on the PCB and connect the POST Display unit to it. When fitted the display will show the progress of the single board PC through the Power On Self Test which is executed on start-up. This can assist debugging when conflicts exist.

If you do not have the APEX POST Display unit then you will either need to purchase one, or build you own if you want to make use of the POST Header information.

The APEX POST Display is a self contained unit and is designed to be used as part of a fault finding/diagnostic development kit.



If you require to add this function to your application as a permanent feature, please contact Blue Chip Technology for further details on how to build your own POST board.

### 3.3.13 Connecting a PC/104 Module

The APEX II unit allows you to connect via the standard PC/104 stack through PC/104 connectors, up to a maximum of three PC/104 Support Modules.

As the APEX II unit has both the XT and AT (16 bit) connectors, any of the currently available PC/104 units will work with this unit.

#### **WARNING**

Before connecting any external devices or cards to the APEX II unit make sure that the power is disconnected.

Locate the connectors P15 and P17 on the PCB (connectors at the edge opposite the SIMM sockets). Connector P17 is the equivalent of the AT connector and P15 is the equivalent of the XT connector.

Locate the four PC/104 mounting holes and insert 4, 16mm PCB stand-off spacers.

To ensure that the APEX II board will operate correctly with the module, please consult the manual that came with the unit.

Push the PC/104 card's bus pins into the APEX's PC/104 sockets until the stand-offs touch the underside of the module. Reconnect the power to the unit and configure the system to work with your newly installed PC/104 board.

#### Note

For more information on the subject of driving PC/104 cards, please see the Passive Backplane Driving section in the Hardware Technical section later in this manual.

### 3.3.14 Connecting a Standard PC ISA Card

APEX II allows you to connect via the standard ISA slot (AT 16 bit), 1 or more PC XT/AT expansion cards.

#### **WARNING**

Before connecting any external devices or cards to the APEX unit make sure that the power is disconnected.

Locate the connectors P5 and P14 on the PCB (large ISA slot down one edge of board). Connector P5 is the AT connector and P14 is the XT connector. Note, however, that this pair of connectors is normally referred to as one ISA AT 16 bit connector.

To ensure that the APEX II board will operate correctly with add-on PC card, please consult the manual that came with the PC card.

Push the PC card into the APEX's ISA sockets until the board is firmly seated.

Reconnect the power to the unit and configure the system to work with your newly installed PC I/O card.

#### Note

For more information on the subject of driving PC ISA cards, please see the Hardware Technical section later in this manual.



## 3.4 Adding Memory

### 3.4.1 Adding DRAM SIMM Modules

The APEX II unit can accommodate up to two 72 pin SIMM modules using its two SIMM sockets: SIMM1 and SIMM2.

These sockets are located on the edge of the PCB near the microprocessor. If you have ordered the APEX II with DRAM memory then one or both of the sockets will be occupied.

#### WARNING

Great care should be taken when handling memory devices as a build up of static electricity can destroy them. Ensure that you touch a suitable ground to discharge any static build up before touching the card or any new memory units. This should be repeated if the handling is for any length of time. Always ensure that the power is turned off before attempting to add or change memory modules.

#### DRAM Memory Options

Option	SIMM1	SIMM2	Total DRAM
1	1MB	-	1 MByte
2	1MB	1MB	2 MBytes
3	4MB	-	4 MBytes
4	4MB	1MB	5 MBytes
5	4MB	4MB	8 MBytes
6	16MB	-	16 MBytes
7	-	16MB	16 MBytes

#### Notes

- SIMM units should be a 72 pin by 36 (32 without parity) bit wide type i.e. 256K x 4 Bytes = 1MByte.
- You can use 72 pin by 32 bits wide type i.e. 4 Bytes with no parity but you will need to change the Set-up BIOS to action this.
- ALL SIMMs must have an access time of 70ns or faster (e.g. 60ns)
- It is possible to mix SIMM sizes. See memory options above.

### 3.4.2 Adding Flash

The APEX II unit can accommodate up to 1 additional 32 pin DIL integrated circuit (IC) via its on-board DIL socket (IC32).

This socket is located next to the EPROM IC near the battery. If you have ordered this unit with extra Flash (The standard build is 1MByte on-board via a surface mount device) then this socket will be in use.

#### **WARNING**

Great care should be taken when handling memory devices as a build up of static electricity can destroy them. Ensure that you touch a suitable ground to discharge any static build up before touching the card or any new memory units. This should be repeated if the handling is for any length of time. Also make sure that the power is turned off before attempting to add or change memory modules.

Flash memory can be added in one of 3 ways :

### 3.4.3 Standard 32 Pin Flash DIL IC's

Conventional 32 pin DIL Flash IC's from Intel or other such manufacturers can be used. The following memory sizes were available at time of publishing :

128KBytes	(P28F010A-200 or 150)
256KBytes	(P28F020A-150)
512KBytes	(P28F004A-150)

### 3.4.4 Custom 32 Pin Flash Memory Modules

By the use of Blue Chip Technology's custom made Flash Memory Modules. These units are DIL devices and are similar to standard DIL IC's but are made using a small PCBs with either one or two, 1MByte TSOP devices mounted on the PCB. They are available in the following sizes :

1 MByte	(971-183)
2 MBytes	(971-184)

### 3.4.5 Standard 32 Pin Flash Cards (Not PCMCIA)

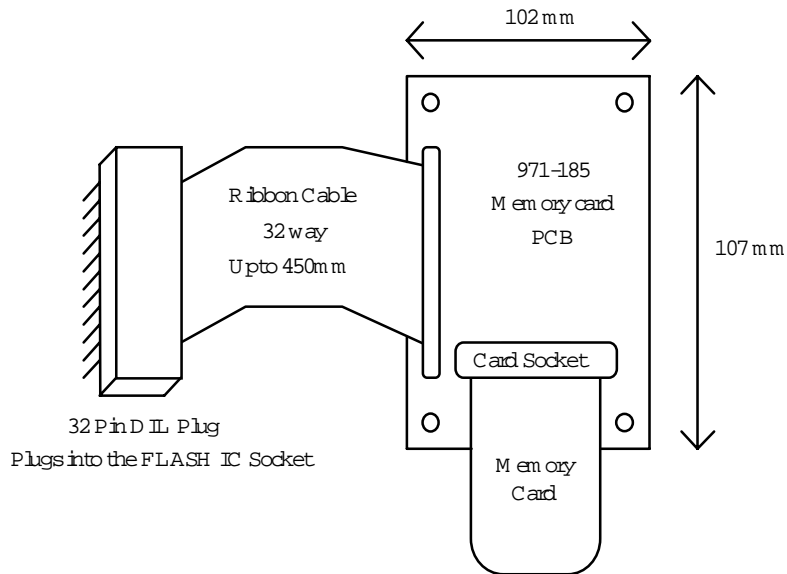
A number of third party manufacturers offer credit card sized memory cards. These cards are similar to PCMCIA cards but have a different pinout and interface.

Blue Chip Technology has designed a remote card socket PCB which will allow up to 1 card to be accessed by the standard on-board 32 pin Flash DIL socket. The standard card size is 1MByte.

The part number for the Memory Card Socket is 971-185.

The drawing that follows shows its basic principle.

#### Memory Card Diagram



The PCB has 2 sets of mounting holes. One set fits the standard 3½" floppy disk drive mounting holes and the other the standard PC/104 mounting holes. This allows the PCB to be used in many various ways.

Please call Blue Chip Technology for more detailed information and pricing.

### 3.4.6 Adding SRAM

The APEX II unit can accommodate up to one 32 pin DIL integrated circuit (IC) using its on-board SRAM DIL socket (IC34).

This socket is located near to the EPROM IC and the battery. If you have ordered this unit with SRAM memory then this socket will be in use.

#### WARNING

Great care should be taken when handling memory devices as a build up of static electricity can destroy them. Ensure that you touch a suitable ground to discharge any static build up before touching the card or any new memory units. This should be repeated if the handling is for any length of time. Also make sure that the power is turned off before attempting to add or change memory modules.

SRAM memory can be added using a conventional 32 pin DIL SRAM IC. The following memory sizes were available at the time of publishing:

128 KByte	HM628128
512 KByte	HM628512

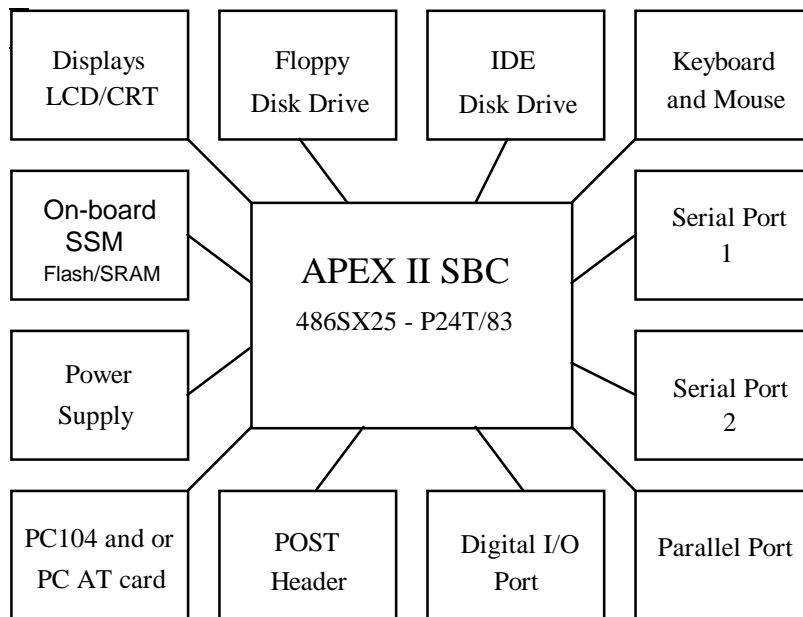
These may be up to 150 nS access time, but must be low power parts.

Note: Large SRAM Modules will require an external battery to preserve the contents. If the on-board battery remains connected (Jumper J8) it will be discharged at a greater rate.

### 3.5 Final wiring checks

#### The completed APEX II assembly

The block diagram below shows functionally a completely assembled unit. It would be advantageous at this point to re-check any of the connections you have made to the unit whilst using the User Guide.



#### Note

The diagram is intended to show the total flexibility of the APEX II unit NOT the actual connector positions. Please see Appendix B for a PCB plot which will indicate the actual positions.

### **3.6 Connecting the power and switching on**

Before you finally switch the unit on **please ensure that the unit IS NOT on a conductive surface.**

You must also make sure that you have some form of Operating System (e.g. MS DOS) loaded onto one of the connected disk drives, or that you are using the remote disk drive function to access the floppy disk drive of another PC. Please consult your chosen operating systems manual for set-up procedures.

You can now switch the unit on and if all is well, the unit should power up like a normal desk top PC.

#### **IMPORTANT NOTES**

Due to the way the BIOS is stored in the EPROM (it is a compressed file and has to uncompress first), the APEX unit will take about 10 seconds to display anything onto a connected screen. This action is correct and not a fault of the unit.

If you are running DOS then after the AMI BIOS has checked the system, the unit will load and run DOS or any other application you have instructed the AUTOEXEC.BAT file to run (e.g. Windows).

If for any reason this does not happen please refer to the Trouble Shooting section which follows.

## 4. TROUBLESHOOTING GUIDE

### 4.1 Introduction

In the Troubleshooting Guide we have tried to list some of the most common problems we have encountered or can imagine. This main section is sub-divided into 13 sub-sections which should enable you to solve the particular problem you have.

It must be noted at this point that we have assumed that you have read and carefully followed the connection details as described in the USER GUIDE section of this manual and that the jumper links are as detailed in part 3.2.1 of that section.

If this is the case please move onto section 4.1.1.

However, if the above is not the case and you have altered any of the jumper links or have altered the AMI BIOS start-up settings, then please follow the steps detailed below before moving onto section 4.1.1.

#### 4.1.1 Resetting the APEX II Unit to a Known State

Firstly, make sure that ALL of the jumper links are as detailed in section 3.2.1.

Then reset the CMOS RAM that defines the configuration of the APEX II by using jumper J9. Change the link to position 2-3.

Leave this connected for 5 minutes and then return J9 back to its original position (across pins 1 and 2).

This action will cause the CMOS RAM to clear and any altered BIOS setting will be lost. The BIOS will now load its default settings when you reconnect the power.

### 4.2 Power Supply Problems

Always check the power supplied to APEX II before exploring other potential problems.

Is there +5 Volts actually getting to the +5 Volt pin on the APEX power connector when referenced to the GND input pin, and is the APEX II power connector the right way round ?

Is the power supply capable of supplying the current required to operate not only the APEX II unit but any other connected items ?

Are all of the power connections of the other items connected to the APEX II unit wired correctly ?

Is the voltage supplied between 4.9 Volts and 5.1 Volts ?

If the answers to the above questions are YES, then it is unlikely that there is a power supply problem.

### **4.3 BIOS Start up Problems**

The BIOS is fundamental to the correct operation of the unit and as such you should read the Software Technical section now if the unit is not getting past the basic BIOS start up routines.

If after reading the Software Technical section you still can not get the unit to start up correctly, please read Appendix L at the rear of this manual on contacting the Technical Support department.

#### **4.3.1 BIOS is losing configuration set-up**

Most of the changes you make to the BIOS set-ups are held in battery backed CMOS RAM by the on-board battery with some being held in the E<sup>2</sup>PROM device. If after altering the BIOS settings you get the old/default BIOS values back at the next power on of the unit, then the CMOS RAM is losing its power supply.

Check to see if link J8 is set incorrectly to external battery supply, or that link J9 is not set to clear the CMOS RAM.

If both of these links are set correctly for your mode of operation then the only item left is the battery itself.



If you check to see what voltage level is across the on-board battery, please do so with the main power input disconnected.

The reading should be about 3.6 Volts. If it is below 3.0 Volts then the battery will need replacing. Please read the battery section of the Technical Hardware section before attempting to tamper with the battery.

#### **4.3.2 APEX II Unit Beeps at you at power on**

If the APEX II unit beeps at you when you are in a power on reset state, then consult the BIOS Beep codes Appendix G section 13.1 to determine the possible cause.

### **4.4 CRT Screen Problems**

Display problems are normally quite straightforward to correct.

Are ALL of the wires from the APEX CRT display connector connected to the correct pins of the 15 way condensed 'D' type and are they all electrically sound ?

Is the Video enabled on the APEX unit ? Check J4 is set correctly i.e. across pins 2 and 3.

Is the display a standard VGA or SVGA PC screen ?

Has the screen previously worked on a PC before being connected to the APEX II unit ?

If the display shows no information at all, check that the CPU links J1 are fitted correctly for the CPU fitted.

If the display shows the correct information but the colours are wrong and you have checked the wiring of the display cable it indicates that one or more of the outputs from the display driver is not working. If there is still no display, please call Blue Chip Technology for assistance.

## 4.5 Flat Panel Display Problems

Due to the nature of these types of displays it is very difficult to give a good level of troubleshooting answers. However, as a basic guide the most common problems are power supply and display data pin configuration. If you are happy that you have wired the display to the LCD connector output P1 correctly and that the power to the display is correct, please call our Technical Support department for assistance.

Please note that in most cases the display information will be feed via a power sequencing board which provides power sequencing and control of the contrast and brightness. If you are using this type of board, make sure that power is applied to the separate power input connectors and that the output form this card is good.

## 4.6 Keyboard and Mouse Problems

As the APEX II unit does not employ the standard mini DIN sockets, possible wiring problems can occur when connecting the keyboard and mouse to the Utilities connector.

Please make sure that the wiring is correct and that there is +5 Volts getting to both units. If the +5 Volt line which feeds the keyboard and mouse is not present when the main power is connected, then it is likely that the on-board 1 Amp fuse has blown.

This fuse is a Surface Mount Device and is located next to the Utilities connector below a mounting hole. Please call Blue Chip Technology for assistance if you need this fuse changing.

## 4.7 Memory Problems

The APEX II unit can employ three types of memory fitted by the user. These are DRAM, FLASH and SRAM. Each type of memory has its own set of potential problems which are now dealt with below.

### **4.7.1 DRAM Memory Problems**

The APEX II unit uses up to two 72 pin DRAM SIMM modules and can accommodate up to 32MBytes in these sockets. The DRAM memory must have an access time of 70nS or better (e.g. 60nS) but can be either with, or without, PARITY. If the DRAM modules you are using are of a non-parity type, please make sure that the BIOS is configured for this.

The SIMM sockets we have chosen are of a good mechanical design and should cope with most industrial applications. Always ensure that the DRAM memory you install is firmly seated into the sockets and that they are the correct way round.

### **4.7.2 Flash Memory Problems**

Flash on the APEX II unit is supported in two ways: an on-board 1MByte TSOP device and a 32 pin DIL socket. When using the 32 pin DIL socket please make sure that the device is inserted the correct way round. If you are having problems reading or writing to this form of memory please consult both the Software Technical and the Flash Programming Appendix I for more in-depth information.

### **4.7.3 SRAM Memory Problems**

SRAM on the APEX II unit is supported by a 32 pin DIL socket. When using the 32 pin DIL socket please make sure that the device is inserted the correct way round. If you are having problems reading or writing to this form of memory please consult both the Software Technical section and the Memory Map Appendix N for more in-depth information.

## **4.8 Floppy Disk Drive Problems**

The most common floppy disk problems are that of connections to the host PC's connectors and their settings. Please make sure that the cable used to provide data is connected to both the APEX II unit and the floppy disk unit the correct way round and that the disk drive is set to the correct drive setting (1 or 0) for the cable you are using. Please refer to the User Guide for more information.

If the floppy disk still fails to operate after checking the above, please try the disk unit on another PC to ascertain if the disk is at fault or whether the APEX II controller device may have a problem.

Please call our Technical Support department for assistance if the latter proves to be the problem.

## **4.9 IDE Hard Disk Problems**

Most IDE hard disk drives give little trouble if configured correctly (see the Software Technical section about Auto Select Hard Disk Drives. The pointers listed in section 4.8 above will be true for IDE drives with the exception of the drive selection values 1 and 0.

If the hard drive still fails to operate even after checking the above, please try the hard disk unit on another PC to make sure if the disk is at fault or whether the APEX II controller device may have a problem.

Please call our Technical Support department for assistance if the latter proves to be the problem.

### **4.9.1 Auto-detect IDE Hard Disks**

When in the BIOS SETUP mode and trying to auto-detect hard disk drives connected to the APEX IDE port, the BIOS will not see the disk drive on the very first attempt if the CMOS RAM has been cleared.

You must save any other changes you have made and then re-enter the BIOS SETUP and auto-detect the IDE disk drives again.

You will find that on the second attempt the disk(s) will be located correctly. This is a BIOS error and not a hardware fault and we are currently awaiting a fix from AMI.

## **4.10 Serial Problems**

The serial ports on the APEX II unit can be set for either RS232 or RS485. Please make sure that the BIOS settings are correct for your application needs.

Part of the set of cables provided with either the Development kit or the APEX II test wiring kit is a serial loop back tester. Connect this cable between the two serial ports and run the Serial Test Program (Serial\_T.exe) on the APEX II Software Utilities Disk.

#### **4.10.1 RS485 Serial Problems**

When using the serial ports in RS485 mode, check that you have the full/half duplex jumper links set correctly. Please refer to section 4.0 of the Hardware Technical section for more information.

### **4.11 Parallel Problems**

The parallel port of the APEX II unit can be set to either uni or bi-directional mode. Please check the BIOS setting for correct operation. Check jumper link J7 to insure correct IRQ settings. Check the cable wiring (see User Guide).

### **4.12 Digital I/O Problems**

Ensure that the BIOS is set correctly for your applications needs. Using a parallel loop back test cable run a simple loopback test program. If you require help with this ask for a copy of APEX II test program DIGIO\_T.EXE.

Please refer to Appendix H for an in-depth look at the operation of the digital I/O port.

### **4.13 PC/104 and PC XT/AT Card Problems**

Almost all of the problems encountered when trying to access another card connected either via the PC/104 bus or the ISA slot are related to configuration of the host system, in this case the APEX II unit or the setup of the card being attached.

The card(s) that are to be added will be supplied with a set-up manual which explains how to configure the host PC. Please read this information carefully and alter the BIOS settings accordingly.

If you are using more than one ISA card (normally in a PC riser card), make sure that the connections are sound and that the bus termination, if used is

correct. Please refer to the Hardware Technical section for a more in-depth look at using these connectors.

#### **4.14 Using the APEX II unit with a Host PC**

The APEX II unit can be operated in conjunction with a host PC. Please refer to Appendix I section 15.2 for a more in-depth information.

## **5. HARDWARE TECHNICAL SECTION**

### **5.1 Introduction**

This section of the manual cover all aspects of the APEX II hardware specifications and should be read fully before attempting to alter or interface with any of the on-board electronics.

### **5.2 APEX II ISA and PC/104 Bus Signal Descriptions**

The following sections describe the functions of all of the standard ISA and PC/104 bus signals. All signal lines are TTL compatible.

#### **5.2.1 AEN (O)**

'Address Enable' is used to negate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus Read command lines (memory and I/O), and the Write command lines (memory and I/O).

#### **5.2.2 BALE (O) (Buffered)**

'Address latch enable' is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is available to the I/O channel as an indicator of a valid microprocessor or DMA address (when used with 'AEN'). Microprocessor addresses SA0 through SA19 are latched with the falling edge of 'BALE. 'BALE' is forced high during DMA cycles.

#### **5.2.3 CLK (O)**

This is the system clock. The clock has a 50% duty cycle. This signal should only be used for synchronisation. It is not intended for uses requiring a fixed frequency.

#### **5.2.4 -DACK0 to -DACK3 and -DACK5 to -DACK7 (O)**

-DMA Acknowledge 0 to 3 and 5 to 7 inclusive are used to acknowledge DMA requests (DRQ0 to DRQ7). They are active low.



### **5.2.5 DRQ0 to DRQ3 and DRQ5 to DRQ7 (I)**

DMA Requests 0 to 3 and 5 to 7 inclusive are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). They are prioritised, with DRQ0 having the highest priority and DRQ7 having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding 'DMA Request Acknowledge' (DACK) line goes active. DRQ0 to DRQ3 will perform 8-bit DMA transfers; 'DRQ5' to DRQ7 will perform 16-bit transfers.

### **5.2.6 -I/O CHCK (I)**

'-I/O channel check' provides the system board with parity (error) information about memory or devices on the I/O channel. When this signal is active, it indicates an in-correctable system error.

### **5.2.7 I/O CHRDY (I)**

'I/O channel ready' is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles. This signal should be held low for no more than 2.5 microseconds.

### **5.2.8 -I/O CS16 (I)**

'-I/O 16-bit Chip Select' signals the system board that the present data transfer is a 16-bit, 1-wait-state, I/O cycle. It is derived from an address decode. '-I/O CS 16' is active low and should be driven with an open collector or tri-state driver capable of sinking 20mA.

### **5.2.9 -IOR (I/O)**

'-I/O Read' instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

### **5.2.10 -LOW (I/O)**

'I/O Write' instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is active low.

### **5.2.11 IRQ3 to IRQ7, IRQ9 to IRQ12 and IRQ14 to 15 (I)**

Interrupt Requests 3 through 7, 9 through 12, and 14 through 15 are used to signal the microprocessor that an I/O device needs attention. The interrupt requests are prioritised, with IRQ9 through IRQ12 and IRQ14 through IRQ15 having the highest priority (IRQ9 is the highest) and IRQ3 through IRQ7 having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine).

### **5.2.12 LA17 to LA23 (I/O)**

These signals (unlatched) are used to address memory and I/O devices within the system. They give the system up to 16MB of address capability. These signals are valid when 'BALE' is high. LA17 through LA23 are not latched during microprocessor cycles and therefore do not stay valid for the whole cycle. Their purpose is to generate memory decodes for 1 wait-state memory cycles. These decodes should be latched by I/O adapters on the falling edge of 'BALE.' These signals also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

### **5.2.13 Master (I)**

This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a '- DACK'. Upon receiving the '- DACK', an I/O microprocessor may pull '- Master' low, which will allow it to control the system address, data, and control lines (a condition known as tri-state). After '- Master' is low, the I/O microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15 microseconds, system memory may be lost because of a lack of refresh.

#### **5.2.14 -MEMCS16 (I)**

'-MEM 16 Chip Select' signals the system board if the present data transfer is a 1 wait-state, 16 bit, memory cycle. It must be derived from the decode of LA17 through LA23. '-MEM CS 16' should be driven with an open collector or tri-state driver capable of sinking 20mA.

#### **5.2.15 OSC (O)**

'Oscillator' (OSC) is a high speed clock with a 70 nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

#### **5.2.16 -OWS (I)**

The 'Zero Wait State' (OWS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16 bit device without wait cycles, 'OWS' is derived from an address decode gated with a Read or Write command.

In order to run a memory cycle to an 8 bit device with a minimum of two wait states, 'OWS' should be driven active on system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to a 8 bit device are active on the falling edge of the system clock. 'OWS' is active low and should be driven with an open collector or tri-state driver capable of sinking 20mA.

#### **5.2.17 -Refresh (I/O)**

This signal is used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel.

#### **5.2.18 Reset Drive (O)**

'Reset drive' is used to reset or initialise system logic at power up time or when the power supply drops below its minimum level. This signal is active high.

### 5.2.19 SA0 to SAI9 (I/O)

Address bits 0 through 19 are used to address memory and I/O devices within the system. These twenty address lines, in addition to LA17 through LA23, allow access of up to 16MB of memory. SA0 through SAI9 are gated on the system bus when 'BALE' is high and are latched on the falling edge of 'BALE.' These signals are generated by the microprocessor or DMA Controller. They also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

### 5.2.20 -SBHE (I/O)

'Bus High Enable' (system) indicates a transfer of data on the upper byte of the data bus, SD8 through SD15. 16 bit devices use 'SBHE' to condition data bus buffers tied to SD8 through SD15.

### 5.2.21 SD0 to SD15 (I/O)

These signals provide data bus bits 0 through 15 for the microprocessor, memory, and I/O devices. D0 is the least significant bit and D15 is the most significant bit. All 8 bit devices on the I/O channel should use D0 through D7 for communications to the microprocessor. The 16 bit devices will use D0 through D15. To support 8 bit devices, the data on D8 through D15 will be gated to D0 through D7 during 8 bit transfers to these devices. 16 bit microprocessor transfers to 8 bit devices will be converted to two 8 bit transfers.

### 5.2.22 -SMEMR (O), -MEMR (I/O)

These signals instruct the memory devices to drive data onto the data bus. '-SMEMR' is active only when the memory decode is within the low 1MB of memory space. '-MEMR' is active on all memory read cycles. '-MEMR' may be driven by any microprocessor or DMA controller in the system. '-SMEMR' is derived from 'MEMR' and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive '-MEMR', it must have the address lines valid on the bus for one system clock period before driving '-MEMR' active. Both signals are active low.

### 5.2.23 T/C (O)

'Terminal Count' provides a pulse when the terminal count (end of) for any DMA channel is reached.

### 5.2.24 -SMEMW (O), -MEMW (I/O)

These signals instruct the memory devices to store the data present on the data bus. '- SMEMW' is active only when the memory decode is within the low 1 MB of the memory space. '- MEMW' is active on all memory write cycles. '- MEMW' may be driven by any microprocessor or DMA controller in the system. '- SMEMW' is derived from '- MEMW' and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive '- MEMW', it must have the address lines valid on the bus for one system clock period before driving '- MEMW' active. Both signals are active low.

## 5.3 IEEE P996 Specification Information

This concludes the control bus signal description part of the Hardware Technical Section. If you require a more in depth look at how the standard PC bus signals are used and defined please read the IEEE P996 specification.

## 5.4 Video Outputs

The APEX II unit offers dual output video drive capability. By using the CIRRUS LOGIC CL-GD6235 video controller the APEX II unit is capable of driving both CRT and LCD displays in various modes. Connected to the video controller is 512KBytes of video memory in the form of a single 256K x 16 bit memory IC, (IC8). These devices offer the user a wide range of display types giving excellent display features.

A full specification of the CIRRUS LOGIC CL-GD6235 IC is obtainable from Blue Chip Technology Ltd. However, we have listed in the following sections some of the more important features which we think will be of use and interest in helping you get the most from this unit.

### 5.4.1 CRT Display Mode

The CRT output P2 is capable of driving VGA displays with resolutions of up to 1024 x 768 pixels with 16 colours and 800 x 600 with 256 colours.

The 16 bit local bus interface is used to connect to the 486 microprocessor.

Using the SimulSCAN™ feature (a technique introduced by Cirrus Logic for achieving simultaneous CRT and LCD output) you have the ability to develop your application on a desktop PC screen and then to move over to an LCD display with the smallest of effort. In fact you can run both displays together to test out your display options even more quickly.

### 5.4.2 CRT Display Types

The Cirrus Logic 6235 display driver will drive most of the CRT display configurations available today. If the CRT display you wish to use does not perform in the way you think it should, please call our Technical Support department for further information, or call your nearest Cirrus Logic dealer for the full Data Applications Handbook. The two display driver diskettes supplied with the unit contain the most popular display drivers for both CRT and LCD screens. More information can be found in Appendix J.

### 5.4.3 Flat Panel Display Modes

The flat panel output P1 is capable of driving the following display types :

- Dual-Scan Monochrome LCD
- Dual-Data Monochrome LCD
- Passive-matrix Monochrome LCD
- Colour TFT LCD (9-bit panels) \*
- Colour STN LCD
- Dual Scan STN LCD
- Monochrome EL Panels (With custom Blue Chip Video BIOS)

\* (An optional custom Blue Chip Video BIOS is available for 18-bit panels)

Greyscale mapping is provided by AutoMap™ which maps 256 colours into a monochrome image; the colours then appear either in 16 shades of grey with greyscale enhancement, or 64 shades of grey in 256-colour mode. There are also four greyscale mapping options available through register control:

- NTSC weighted
- DAC Look-up table "green" output
- 4 or 6 bit video data direct
- Attribute Controller 64-shade colour data

When driving a colour STN panel it can drive 8 or 16 bit interfaces, and give 256 simultaneous colours from a palette of 256K.

When driving a colour TFT display it will support 9, 12, 15 and 18 bit panels and give 256 simultaneous colours from a palette of 256K.

The CL-GD6235 offers true packed-pixel addressing, colour expansion for 8 bit-per-pixel graphics, and a hardware cursor, thus improving Windows performance.

#### **5.4.4 Power Management Information**

The 6235 also offers standby and suspend power-management modes which reduce the power consumption when the system is not in active use. The internal standby counter initiates standby mode without software intervention.

During this reduced power mode, the LCD panel is turned off while the video memory can still be accessed and modified.

The CL-GD6235 provides efficient power management of the display system by turning off, or shutting down the LCD flat panel and CRT when not being used. The device offers both hardware methods (using device pins) and software methods (using programmable timers and on chip registers) to control the LCD panel and or CRT display.

In Normal Mode the LCD is being used, and the following occur :

- Display is active and receives power
- Full screen refresh occurs
- CPU and access :
  - Video memory
  - RAMDAC
  - I/O registers
- Refresh is provided to the video memory

In Standby Mode the controller stops power to the LCD panel. As a result the following occurs :

- LCD panel power down sequence occurs automatically when this mode is entered
- VCLK oscillator is stopped
- MCLK is divided by 6
- No clock is provided to the CRT controller
- Video DAC is in lower power mode
- Video display memory refresh is maintained
- CPU can access and modify the video memory
- When standby mode is terminated the previous state is restored

More information on power management and power sequencing is given later in this section.

Please call our Technical Support department for further information.



### 5.4.5 Flat Panel Connector Pin out Details

The following table shows the pinout for the Flat Panel connector together with a description for each pin. Note the connector is a female type and the table shows looking down on top of the connector from the main component side of the PCB.

Pin N°	Description	Pin N°	Description
2	LCDRST	1	FPVDCLK
4	NPD	3	MOD
6	FVSYNC	5	LFS
8	FHSNYC	7	LLCLK
10	STANBY	9	R5
12	SUSPEND	11	R4
14	DE	13	R3 / SUD7
16	FPBACK	15	R2 / SUD6
18	FPVCC	17	G5 / SUD5
20	FPVEE	19	G4 / SUD4
22	VCC (APEX)	21	G3 / SUD3
24	GND (APEX)	23	B5 / SUD2
26	GND (APEX)	25	B4 / SUD1
28	GND (APEX)	27	B3 / SUD0
30	GND (APEX)	29	R1 / SLD7 / UD3
32	N/C	31	R0 / SLD6 / UD2
34	B1 / SLD1 / LD1	33	G2 / SLD5 / UD1
36	B0 / SLD0 / LD0	35	G1 / SLD4 / UD0
38	VCC (APEX)	37	G0 / SLD3 / LD3
40	+ 12 Volt	39	B2 / SLD2 / LD2

#### Note

The labels given for the pinouts on connector P1 are biased towards LCD drive. If you need to control an EL panel then the pins to use are not obvious. Please consult the Panel Interface Connection Appendix M at the rear of this manual.

### LCD Signal Descriptions

#### 5.4.6 B[5:0]

BLUE BITS [5:0]. These bits contain the BLUE colour data for TFT colour flat panel displays.

#### **5.4.7 DE**

DISPLAY ENABLE. For those flat panels that require an external display enable, this pin is used to provide a data enable. For the CL-GD6235 it is the second Shift Clock output for STN single-scan dual-clock colour panels.

#### **5.4.8 FPDCLK**

FLAT PANEL VIDEO CLOCK. This signal is used to drive the flat panel shift clock which is designated as CP0 by some panel manufactures.

#### **5.4.9 G[5:0]**

GREEN BITS [5:0]. These bits contain the Green colour data for TFT colour flat panel displays.

#### **5.4.10 LD[3:0]**

LOWER DATA [3:0]. The lower Data bits [3:0] are typically used with monochrome dual-scan flat panels to provide 4 bit parallel data for the lower portion of the panel.

#### **5.4.11 LFS**

LCD FRAME START. This output provides a pulse to start a new frame on flat panels.

#### **5.4.12 LLCLK**

LCD LINE CLOCK. This output is used to drive the LCD panel line clock. This signal is also designated as LP or CP by some panel manufacturers.

#### **5.4.13 MOD**

MODULATION. This output provides AC inversion. It should be connected to the MOD, FR or DF inputs of the panel, and is appropriate. Some panel manufacturers provide this function in the panel circuitry.

**5.4.14 R[5:0]**

RED BITS [5:0]. These bits contain the Red colour data for TFT colour flat panel displays.

**5.4.15 SLD[7:0]**

STN LOWER DATA [7:0]. The lower data bits [7:0] are for use with colour STN LCD panels.

**5.4.16 SUD[7:0]**

STN UPPER DATA [7:0]. The upper data bits [7:0] are for use with colour STN LCD panels.

**5.4.17 UD[3:0]**

UPPER DATA. The Upper Data bits [3:0] are typically used with monochrome dual-scan flat panels to provide 4-bit parallel data for the upper portion of the panel.

**5.4.18 LCDRST**

LCD Reset. This active low signal is an optional LCD display reset input. Any logic high to low transition on this input will clear both the LCD and CRT enable bits in the power management register (CR20[6:5]). This will initiate the LCD-panel power down sequence, and will stop video memory refresh.

The logic high to low transition on this pin does not restore the CRT or LCD enable bits. These bits must be restored by writing to the appropriate registers.

This pin has an internal pull-up resistor. Avoid connecting to the pin if the function is not used.

**5.4.19 STANDBY (Input or Output function pin)**

When the panel is on and this input is driven high, the power down sequence will start to put the system into Standby Mode. Standby Mode terminates when this pin goes low, as long as CR20[4] = '0' and the standby timer has been reset.

Please ask for more detailed information if your application needs to make use of this function.

#### **5.4.20 SUSPEND**

This input pin can be used in one of two ways :

1. To initiate the Hardware Suspend mode. If the Suspend pin is used to control Suspend Mode, CPU access will not be allowed.
2. To turn off the LCD display for a 'closed cover' type condition. In a closed cover type condition, CPU access is allowed, and the CRT outputs remain active.

Please ask for more detailed information if your application needs to make use of this function.

#### **5.4.21 FPBACK (Output pin)**

Flat Panel Backlight. This output pin is part of the panel power sequencing, and it should be used to drive a suitable power controller switch (e.g. Mosfet transistor) which in turn will be connected to the panels backlight power input pin. If you are using the LCD-PSU controller boards the power sequencing function of this output is taken care of. Please see Appendix M for more details.

#### **5.4.22 FPVCC (Output pin)**

Flat Panel VCC. This output pin is part of the panel power sequencing, and it should be used to drive a suitable power controller switch (e.g. Mosfet transistor) which in turn will be connected to the panels VCC power input pin. If you are using the LCD-PSU controller boards the power sequencing function of this output is taken care of. Please see Appendix M for more details.

#### **5.4.23 FPVEE (Output pin)**

Flat Panel VEE. This output pin is part of the panel power sequencing, and it should be used to drive a suitable power controller switch (e.g. Mosfet transistor) which in turn will be connected to the panels VEE power input pin. If you are using the LCD-PSU controller boards the power sequencing function of this output is taken care of. Please see Appendix M for more details.

#### **5.4.24 NPD (Input pin)**

NO POWER-DOWN. This pin, when 'high', stops the power down counters from decrementing. This pin is used to inhibit automatic power down when, for example, the system is supplied from an AC power source.

#### **5.4.25 FVSYNC**

VERTICAL SYNC. This is a copy of the vertical sync line as output on the CRT display connector and would not be used in normal LCD flat panel operation.

#### **5.4.26 FHSYNC**

HORIZONTAL SYNC. This is a copy of the horizontal sync line as output on the CRT display connector and would not be used in normal LCD flat panel operation.

#### **5.4.27 LCD Power Sequencing**

The internal logic of the 6235 controls the sequencing of the LCD contrast voltage, logic power, data input and control pins. To minimise the possibility of damage to the LCD display, the 6235 provides the recommended power up/down sequences shown below. These sequences meet most LCD panel manufacturer's specifications.

It should be noted, however, that most LCD display panels do not provide direct input channels for power sequencing control. Please ask your panel supplier for this information. If the panel you intend to use does not support power sequencing directly, then a power sequencing circuit will be needed to carry out these functions.

Blue Chip Technology can supply suitable boards, at extra cost, to provide all power sequencing and bias voltage generation.

LCD-PSU is a small daughter board providing simple positive and negative LCD bias voltage generation and all power sequencing.

Appendix M gives more detailed information on the use of the bias board. Please ask our Sales department for further information.

#### **5.4.28 LCD Panel Power-Down Sequence**

- 1) Shut off FPVEE and FPBACK
- 2) Wait 96 - 128 ms
- 3) Force all 6235 panel control signals low
- 4) Wait 32 ms
- 5) Shut off FPVCC
- 6) Shut off internal VCLK

#### **5.4.29 LCD Panel Power-Up Sequence**

- 1) Turn on VCLK increase MCLK frequency
- 2) Wait 32 ms
- 3) Enable FPVCC
- 4) Wait 32 ms
- 5) Enable 6235 panel control signals
- 6) Enable FPVEE and FPBACK

The above information was taken from the Cirrus Logic Flat Panel CL-GD6235 Applications Book. Please contact us if the specific information you require is not listed or contact your local Cirrus Logic Dealer to obtain a copy of the Applications Book.

### **5.5 Serial Ports RS232 and RS485**

Two asynchronous 16C550 compatible interfaces are provided by APEX II and are part of the 37C663 Peripheral Controller IC18. This IC also handles the parallel port, and both disk drive outputs.

Both serial ports can operate in either RS232 or RS485 modes.

The outputs for RS232 operation is generated by two LT1133 ICs (RS232 line drivers), which have LC networks fitted as standard to their outputs.

The RS485 signals are provided by 75176 line driver IC's, two for each interface channel.

When in RS485 mode either half (2 wire) or full (4 wire) duplex operation can be selected via software selection (see configuration table for further details). DTR is used for direction control and is selected by the correct use of jumper links J10 (output 1) and J11 (output 2).

As the APEX II unit generates its own RS232 levels on-board, this allows for a convenient +5 Volt only operation.

The AMI BIOS provides built-in configuration of I/O addresses and interrupt usage. Please refer to the BIOS Peripheral Support section in the Software Technical section of this manual for further details.

Care should be taken when connecting to these outputs as damage to the control ICs outputs will mean a surface mount device change which is not always possible in the field.

#### Note

If the APEX II unit's serial ports are enabled as COM1, and COM2 then any additional serial ports added to the unit will become COM3 and COM4.

## **5.6 Parallel Port (Printer Port)**

One IBM PC/XT/AT Bi-directional parallel printer interface is provided on the APEX II unit and offers 24mA output drivers, ensuring reliable operation even in the harshest of environments.

This output is part of the 37C663 peripheral controller IC and our connector connects directly to the output pins of the controller.

Via jumper link J7 the IRQ for this output may be selected as either IRQ5 (LPT1) or IRQ7 (LPT2).

Care should be taken when connecting to these outputs as damage to the control IC's outputs will mean a surface mount device change, which is not always possible in the field.

The interface can operate in either uni or bi-directional modes and is configured by the AMI BIOS.

Please refer to the BIOS Peripheral Support section in the Software Technical section of this manual for further details.

## 5.7 24 Channel Digital Programmable I/O

The APEX II unit has an on-board NEC 71055 (8255) programmable I/O device, allowing up to 24 digital (TTL) input/outputs.

Connector P9 is a 26 way header providing interfacing for three 8 bit I/O ports with two digital grounds (0 Volts).

Care should be taken when connecting to these outputs as damage to the control IC's outputs will mean a surface mount device change.

For full details on programming and using this device see Appendix H at the rear of the manual.

## 5.8 Disk Drives

### 5.8.1 Floppy Disk Drives

The APEX II unit has built in support for two floppy disk drives. These drives can be any permutation of the following :

Capacity	Drive Size
360KB	5¼"
720KB	3½"
1.2MB	5¼"
1.44MB	3½"
2.88MB	3½"

The BIOS Set-up allows you to configure the drives for your installation and application.

A standard PC 34 way ribbon cable with twisted lines can be connected to two drives both set as drive 1 (as opposed to 0). This is possible because the IBM



convention twists the drive select and motor control lines between the two drive connections.

Connection to the floppy disk is made at connector P8.

Remember that only one drive in the chain should be terminated, and that it should be the drive furthest from the APEX II unit. Without correct termination drive operation can be unreliable.

In high noise environments it may be necessary to use shielded ribbon cable with the shield connected to GND.

Please do not extend the cable length beyond 1 metre (for both drives) as unreliable operation may result.

Care should be taken when connecting to these outputs as damage to the control IC's outputs will mean a surface mount device change, which is not possible in the field.

### **5.8.2 IDE Hard Disk Drives**

The on-board IDE interface allows for the connection of up to two hard disk drives.

These connect to the APEX II unit via P3 which is a 40 way IDC header.

The maximum length of ribbon cable to be used for reliable operation is 450mm.

Each drive can be set to one of the standard drive types as listed in the AMI BIOS or alternatively a custom type 47.

Please note that if you have two disks connected, they can both be set to have different custom type 47 specifications.

## Hard Disk Drive Identification

Hard disk drive types are identified by the following parameters:

Parameter	Description
Type	A designation for a hard disk drive with redefined parameters
Cylinders	The number of cylinders in the disk drive.
Heads	The number of heads.
Write Pre-compensation	The size of a sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write pre compensation circuitry difference in sector size by boosting the write current for sectors on inner tracks. This parameter is the track number where write pre compensation begins.
Landing Zone	The number is the cylinder location where the heads normally park when the system is shut down.
Sectors	The number of sectors per track. Hard drives that use MFM have 17 sectors per track. RLL drives have 26 sectors per track. ARLL and ESDI drives have 34 sectors per track. SCSI and IDE drives may have even more sectors per track.
Capacity	The formatted capacity of the drive based on the following formula: $(\text{Number of heads}) * (\text{Number of cylinders}) * (\text{Number of sectors per cylinder}) * (512 \text{ bytes per sector})$

### 5.8.3 Custom Type 47 Disk Drive Selection

Using the AUTO HARD DISK SELECTION part of the BIOS, any modern IDE hard disk connected to the APEX II unit will be automatically detected and its form loaded into the BIOS.

This can be invaluable in providing an efficient way of establishing the type of drive connected without the need to refer to the drive manuals.

Care should be taken when connecting to these outputs as damage to the control IC's outputs will mean a surface mount device change.

## 5.9 Battery (Internal and External)

The APEX unit comes complete with its own on board 3.6 Volt LCT Lithium battery. However, if your application needs to have an external battery supply then this on-board battery can be switched out of circuit using jumper J8 and an external battery fitted to connector P16.

The external battery should have an output of 6 Volts, capacity of 1.8AH and be fitted with a 10K series resistor for safety.

Please note that the APEX II unit has two series protection diodes fitted to the external battery positive input pin.

The battery will provide power for the Real Time Clock (RTC) and CMOS RAM when there is no power applied to the main board (as is the operation of the on-board battery if selected). Under normal conditions the on-board battery should last for several years. The on-board battery is insufficient to maintain additional SRAM: an external battery must be added.

Great care should be taken with this type of battery. Under NO circumstances should :

- \* the outputs be shorted
- \* it be exposed to temperatures in excess of 100°C
- \* it be burned
- \* it be immersed in water
- \* it be unsoldered
- \* it be recharged
- \* it be disassembled

If the battery is mistreated in any way there will be a possibility of fire, explosion, and harm.

## 5.10 Power Supply Inputs

The standard build of the APEX II unit requires only a +5 Volt supply to function correctly. It utilises a standard 5¼" disk drive type connector (P13) to provide the power supply connection.

Although only a +5 Volt supply is required to function correctly, the disk drive type of connectors allows for, and in fact provides +12 Volts (if taken from a normal PC PSU) to the board. There also exists a connector (P19) adjacent to P13 which permits the connection of -5 Volts and -12 Volts to the board if required. These supplies are routed to the appropriate expansion connectors.

They are provided solely to allow the addition of PC/104 modules or ISA expansion cards requiring these voltages on the PC104 and ISA connectors.

Please note that there is no on-board in-line fuse connected to the +5 Volt rail. Therefore it is your responsibility to incorporate an in-line fuse to protect the unit.

If you have any concerns about the powering of the APEX II unit please call Blue Chip Technology's Technical Support department.

## **5.11 Peripheral (Utilities) Connector Items**

The peripherals header P4 allows you to connect to all of the normal PC type LEDs and switches including the keyboard and mouse, by just using one IDC connector.

In the User Guide section of this manual we have shown you how to connect to all of the I/O pins found on this header.

The following list gives a more detailed description of each of the pin's functions.

### **5.11.1 Speaker Drive Pins 1 and 2**

This pair of pins are used to drive an external speaker having the following specification :

8 $\Omega$  coil with a 200mW maximum power rating.

Pin 1 is connected via a 20R resistor to Vcc and pin 2 is driven by a 7407 gate, which in turn, is connected to the collector of a BCX19 transistor. The transistor's base is driven by the microprocessor.

### 5.11.2 Reset Switch Pins 3 and 4

These pins are used to read the state of a normally open non latching switch, which when pressed will cause a complete system RESET. Pin 3 goes directly to an input pin on the microprocessor whilst pin 4 is connected to GND.

### 5.11.3 Keyboard Pins 15, 16, 19, 20 and 7

The keyboard input to the APEX II unit will accept all standard IBM XT/AT and PS/2 type data and the diagram in the Users Guide shows how to wire them to a standard 5 pin DIN type socket.

**Pin 15** is the +5 Volt supply to the keyboard and mouse and is fused on-board by a 2 Amp fuse. Note that this pin should NOT be used to connect to or supply any other electronic circuits as noise on this line can cause reliability problems when reading in keyboard/mouse data.

**Pin 16** is the 0 Volt GND supply for the keyboard. Note that this pin should NOT be used to connect to or supply any other electronic circuits as noise on this line can cause reliability problems when reading in keyboard/mouse data.

**Pin 19** is the Keyboard data pin and should be connected to the output data pin of a suitable keyboard controller circuit.

**Pin 20** is the Keyboard clock pin and should be connected to the output clock pin of a suitable keyboard controller circuit.

**Pin 7** is used to reset the keyboard as requested by the system. However, this pin is now seldom used and would not normally be connected.

### 5.11.5 Mouse Pins 11, 12, 15 and 16

The Mouse input pins on the APEX unit will accept data from a standard PS/2 TTL serial type mouse.

These pins have the same functions as detailed for the Keyboard pins except that they are connected to the Mouse port.

#### **5.11.4 Power LED Pins 9 and 10**

These pins are used to simply drive an LED to indicate that the main +5 Volt supply to the APEX unit is on. Pin 9 is connected via a 220R resistor to Vcc. Pin 10 is GND.

#### **5.11.5 IDE LED drive Pins 13 and 14**

These pins are used to drive the IDE access LED. Pin 13 is connected via a 220R resistor to Vcc. Pin 14 is GND.

### **5.12 POST (Power On Self Test) Information**

The APEX II unit via the AMI BIOS provides POST information as the unit carries out the various power on tests. This information is presented in two ways: by sending a code to I/O address 80H which can be read by the use of the POST display board via P6 or by sending Audible POST information to the speaker.

#### **5.12.1 POST Connector**

The POST connector P6 provides the output signals required to drive a simple circuit which will display the status of the POST code as it progresses through the AMI BIOS tests.

The POST display board can be ordered as a separate item part.

A full list of POST codes can be found in Appendix G at the rear of this manual.

#### **5.12.2 POST Audible Beep Codes**

If the BIOS cannot configure the display controller, it will communicate the identification of fatal errors (except error code 8) via a series of beeps by using the speaker drive circuit.

These errors will only occur during power-on tests. The beep codes are included in Appendix G at the rear of this manual.

## 5.13 Passive Backplane Driving

APEX II combines the traditional IBM/AT PC via its on-board ISA slot and the convenience of the compact physical arrangement of the PC/104 specification connectors. The pin outs for both of these output connectors are detailed in depth in the Connector section.

### 5.13.1 PC/104 Specification Information

It should be noted that although the PC/104 specification allows a relaxed bus drive of 6mA, the APEX II unit will supply 16mA drive of the standard ISA bus.

The PC/104 specification calls for the unique self stacking bus type connectors which allow the user to add PC/104 add on boards to both the top and bottom planes of the main CPU board. APEX II still uses this type of connector to allow you to add PC/104 board to the top side of the unit, but to reduce the overall height of the unit, the PC/104 connectors DO NOT protrude through the APEX II board, so it is not possible with the standard build to add PC/104 boards to the bottom of the APEX II unit. However, it is possible to add this option (at a small cost) as an Order Time Option if your required application quantities require this functionality. Please ask our Sales department for details.

### Using the PC104 Connectors

The PC/104 interface, as provided by APEX II, allows for cards to be stacked on top of the main unit.

Alternatively, APEX II can be inserted onto an application specific PCB thereby minimising size and cost.

### 5.13.2 Using the on-board standard 16 bit ISA slot

This configuration is particularly valuable when in the early stages of a development allowing the APEX II processor to directly control current PC XT/AT cards or prototype cards.

A single card can be mounted directly into this slot. Or, if more than one card is to be connected, you can attach a riser module.

### **5.13.3 Simple riser cards**

Using this option a 2 or 3 slot ISA riser card can be inserted into the on board slot enabling you to fit upto 3 PC XT/AT cards for your development period or even the final production unit (with suitable supporting hardware). Please ask the Blue Chip sales desk for further information on riser cards and mounting hardware.

## **5.14 Watchdog and Reset Control**

The APEX II unit is fitted with an on-board microprocessor monitor chip MAX1232CPA

### **5.14.1 Power Rail Reset**

In this standard non-configurable mode, the chip acts as the main reset control device and if the Vcc rail of the APEX II unit falls below the chips internal reference voltage of :

Vcc trip point 5% - 4.50 (min) 4.74V (max)

a reset signal is sent to the microprocessor and AT bus.

The reset pulse is always greater than 250ms on power up/down and brown-out conditions.

### **5.14.2 External Reset Input**

The external reset switch input found on the peripheral header is fed directly into pin 1 of this chip and is referenced to ground. This input pin has a debounce circuit to ensure bounce free operation and when shorted to ground the chip produces a full reset pulse.

### **5.14.3 Watchdog Control Mode**

In this mode the chip is used to monitor the APEX II for a software or hardware processor failure and it can be enabled or disabled via the BIOS software. This allows the user to decide whether their application requires protection against such a potential processor failure.



Two functions are available to control the watchdog. These are :

- Enable/Disable Watchdog
- Reset Watchdog

Please see the Software Technical section for programming information.

## 5.15 E<sup>2</sup>PROM Access and Control

The E<sup>2</sup>PROM on the APEX II unit is a 9348 serially programmed device which is accessed through a single register at port 100 Hex.

Unlike the Flash device, E<sup>2</sup>PROM does not require to be completely erased before a single location is written to. It is therefore much more useful for the storage of configuration information.

There are 64, 16 bit words of E<sup>2</sup>PROM - the lower 32 are reserved for use by Blue Chip Technology for configuration information.

The top 32, 16 bit words are available for user information.

The E<sup>2</sup>PROM's individual control lines are arranged as follows at port 100 Hex :

7	6	5	4	3	2 Data In	1 Clock for serial data	0 Chip Select / Data Out
---	---	---	---	---	-----------------	-------------------------------------	--------------------------------------

### 5.15.1 E<sup>2</sup>PROM Control

The APEX II BIOS extension provides two functions to allow access to the E<sup>2</sup>PROM. These are :

- Write to a single E<sup>2</sup>PROM Memory location
- Read from a single E<sup>2</sup>PROM Memory location

Please see the Software Technical section for programming information.

## **5.16 Memory Maps**

Please see Appendix N at the rear of this manual for this information.

## **5.17 I/O Address Map**

Please see Appendix F at the rear of this manual for this information.

## **5.18 DMA Channels**

Please see Appendix E at the rear of this manual for this information.

## **5.19 Interrupts**

Please see Appendix D at the rear of this manual for this information.

## **5.20 Physical and Environmental Considerations**

The APEX II unit has been designed with the greatest of care and can be used in many environments. More detailed information follows overleaf.

### **5.20.1 PCB Information**

The PCB is an 8 layer board made to BS4584, Part 12.

The dimensions are :   Length   204mm  
                                  Width    147mm

The height will be dependant upon the items fitted.

The minimum height including DRAM SIMM modules is 33mm. If one PC/104 module is added then the height is 38mm (Including Connectors). For each additional PC/104 module add 20mm to the height.

### **5.20.2 Operating Temperatures**

The APEX II unit will work in ambient temperatures from 0°C to +55°C. For lower ambient operating temperatures you will need to ensure that the unit is heated. This can be either via other heat generating components in the application's enclosure or by means of a heated enclosure for the APEX II unit.

Please note that the surface temperature of the components should not exceed +70°C anywhere on the board during operation. Operating the unit in temperatures in excess of this may result in permanent damage.

We recommend that for 486SX33 CPU's and above a CPU heatsink is fitted to prevent the processor from overheating.

### **5.20.3 Storage Temperatures**

The APEX II unit can be stored from -20°C to + 100°C. Please note that the unit would need to reach the operating temperatures before being switched on.

### **5.20.4 Relative Humidity**

This should be in the range of 0 to 95% non-condensing.

## **5.21 Unit Reliability**

Blue Chip Technology has designed the APEX II unit to give a long and trouble free life. We have carefully selected the components that will provide the best all round performance and product reliability. However, as many users now ask for some form of reliability figure we have tried to give the most meaningful figure possible.

Based upon the information supplied to us by the relevant semiconductor manufactures and using past product return data, Blue Chip Technology has calculated the M.T.B.F figure as 65,000 Hours.

## 5.22 Adding Memory

### WARNING

Great care should be taken when handling memory devices as a build up of static electricity can destroy them.

Ensure that you touch a suitable ground to discharge any static build up before touching the card or any new memory units. This should be repeated if the handling is for any length of time. Also make sure that the power is turned off before attempting to add or change memory modules.

### 5.22.1 Adding DRAM SIMM Modules

The APEX II unit can accommodate up to two 72 pin SIMM modules in the two SIMM sockets (SIMM1 and SIMM2).

These sockets are located on the edge of the PCB near the microprocessor. If you have ordered this unit with DRAM memory then one or both of the sockets will be in use.

Memory can be added to either socket and the unit will auto-configure the DRAM mapping to suit the memory.

### DRAM Memory Options

Option	SIMM1	SIMM2	Total DRAM
1	1MB	-	1 MByte
2	1MB	1MB	2 MBytes
3	4MB	-	4 MBytes
4	4MB	1MB	5 MBytes
5	4MB	4MB	8 MBytes
6	16MB	-	16 MBytes
7	-	16MB	16 MBytes

### Notes

- SIMM units should be a 72 pin by 36 (32 without parity) bit wide type i.e. 256K x 4 Bytes = 1MByte.
- This should be taken into account when ordering.
- You can use 72 pin by 32 bits wide type i.e. 4 Bytes with no parity but you will need to change the Set-up BIOS to action this

- ALL SIMMs must have an access time of 70ns or faster (e.g. 60ns)
- It is possible to mix SIMM sizes.
- Auto configuration of memory allows either SIMM socket to be used

### 5.22.2 Adding Flash

The APEX II unit can accommodate one 32-pin DIL integrated circuit (IC) via its on board DIL socket IC32.

This socket is located next to the EPROM IC, near the battery. If you have ordered this unit with extra Flash (The standard build is 1MByte on-board) then this socket will be in use.

Flash memory can be added in one of 3 ways:

### 5.22.3 Standard 32 Pin Flash DIL ICs

The use of conventional 32 pin DIL Flash ICs from Intel or other such manufacturers. The following memory sizes were available at time of publishing:

128 KBytes (P28F010A-200 or 150)  
256 KBytes (P28F020A-150)  
512 KBytes (MXIC4000)

Once you have added extra Flash memory to the unit, please see the SSD section of the Software Technical section to configure the APEX unit to access it.

### 5.22.4 Custom 32 Pin Flash Memory Modules

By the use of Blue Chip Technology's custom made Flash Memory Modules. These units are DIL devices and are similar to standard DIL ICs but are made using a small PCBs with either 1 or 2, 1MByte TSOP devices mounted onto the PCB. They are available in the following sizes :

1 MByte (981-183)  
2 MBytes (981-184)

Once you have added extra Flash memory to the unit, please see the SSD section of the Software Technical Section to configure the APEX unit to access it.

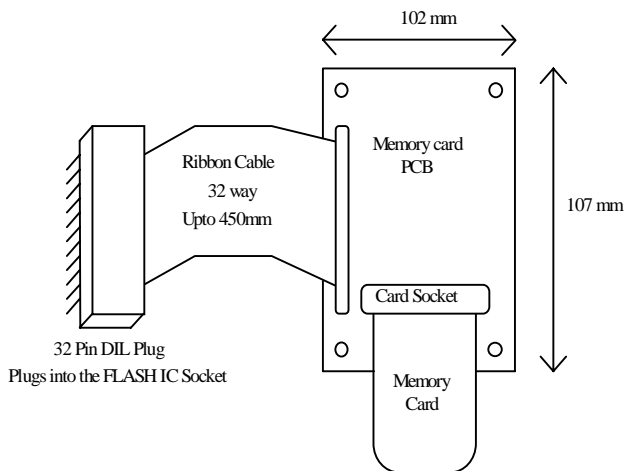
### 5.22.5 Standard 32 Pin Flash Cards (Not PCMCIA)

A number of third party manufacturers are making credit card sized memory cards using the TSOP type devices. Blue Chip Technology has designed a card socket PCB which will allow one card to be accessed by the on-board 32 pin Flash DIL socket.

The standard card size is 1 MByte. The part number for the Memory Card Socket is 971-185.

Once you have added extra Flash memory to the unit, please see the SSD section of the Software Technical section to configure the APEX unit to access it. The drawing that follows shows the basic principle:

#### Memory Card Diagram



The PCB has two sets of mounting holes. One set fits the standard 3 1/2" floppy disk drive mounting holes and the other the standard PC104 mounting holes. This allows the PCB to be used in many various ways. Please call Blue Chip Technology for more information and pricing.

### 5.22.6 Adding SRAM

The APEX II unit can accommodate one 32 pin DIL integrated circuit (IC) via its on-board SRAM DIL socket IC34.

This socket is located near to the EPROM IC, near the battery. If you have ordered this unit with SRAM memory then this socket will be in use.

SRAM memory can be added as follows :

### 5.22.7 Standard 32 Pin SRAM DIL IC's

The use of conventional 32 pin DIL SRAM ICs. The following memory sizes were available at the time of publishing:

128KByte  
512KByte

Once you have added extra SRAM memory to the unit, please see the Software Technical section to configure the APEX II unit to access it.

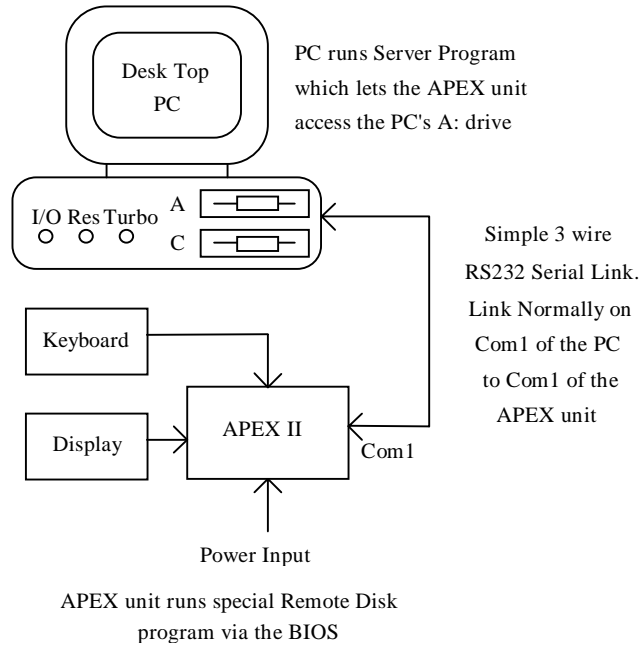
## 5.23 Using APEX II with a Host PC

Your desktop PC can be used as a programming tool or emulator to write application specific programmes, debug them, and then transfer them to the APEX II unit via a simple serial link.

This will allow you to develop your software in a known environment and take advantage of existing PC software. Then with little effort you can program the APEX II unit and see your application work.

For more detailed information on this topic please see the Flash programming, Appendix I at the rear of this manual.

A basic block diagram is shown below indicating the various links to the APEX II unit:





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## **6. SOFTWARE TECHNICAL SECTION**

### **6.1 Introduction**

This section covers all aspects of the APEX II's software systems and should be read fully before attempting to alter any of the System BIOS used to control the workings of this unit. It is possible to alter the state of the System BIOS so that a start boot is not possible and although this is not a catastrophic problem it can be very frustrating and time consuming to remedy.

### **6.2 BIOS Overviews**

There are several types of Basic Input Output System (BIOS) in a PC system.

#### **System BIOS**

This controls the local electronics. It also provides the interface to the hardware for the operating system.

#### **Video BIOS**

This controls the interface between the video hardware and the computer.

#### **Keyboard BIOS**

This controls the keyboard matrix operation and communicates with the PC.

#### **Adapter BIOS**

Adapter ROM BIOS' that control specific hardware add ons.

Each BIOS plays an important part to the total correct working of the PC. Each one of the BIOS types will now be described in more detail.

#### **6.2.1 System BIOS**

The primary function of the System BIOS is to provide a series of software interrupts, functions and sub-functions that perform specific system tasks; such as writing or reading to and from disks and video screens.

The operating system uses the System BIOS as the route to communicate and control the microprocessor and its immediate peripherals. This exchange of data occurs via a strict protocol.

The secondary function of the System BIOS is the series of tests and initialisations that occur after power-on. The results of these operations are written to the POST display (not fitted as standard) as they are completed, thereby indicating its progress.

The System BIOS on the APEX is contained in a 128KB EPROM; of this space the System BIOS occupies 64KB. The EPROM is located at address F0000 Hex and continues to FFFFF Hex. The supplier of the BIOS is AMI, currently one of the leading suppliers of PC BIOS in the world. Blue Chip Technology have selected this supplier because of their experience, support and commitment to future developments in this critical area of a PC/AT design.

For more information about AMI and there BIOS support software please contact our Technical Support department who will be able to answer any questions you may have.

At Blue Chip Technology we can also offer a BIOS customisation service which will tailor the BIOS configuration to your applications needs.

This is normally free of charge with orders over 50 pieces. Please contact the Sales department for more information.

### **6.2.2 Video BIOS**

The Video BIOS acts as an interface between the System BIOS and the video hardware and sits at memory location C0000-C7FFFF. It is critical that this interface is compatible, fast and reliable. The Video BIOS provides a relatively high level of access to the hardware.

APEX II provides an on-board video interface and is based on the Cirrus Logic™ CL-GD6235 IC. This device offers proven VGA compatibility in a single device and is supported by 512KB of on board video memory (DRAM). The Video BIOS coexists in the System BIOS EPROM but locates in the address range C0000 to C7FFF hex. This BIOS is enabled and disabled with J4.

Due to the nature of some types of display (EL in particular), custom versions of this BIOS are needed to access these panels. Please contact Blue Chip

Technology Ltd or your supplier to ensure that your display is supported by the BIOS.

### 6.2.3 Keyboard and PS/2 Mouse BIOS

The keyboard and mouse BIOS is contained in the MegaKey 8742 keyboard controller. This device provides a parallel interface to the microprocessor bus allowing a bi-directional stream of data to be passed between the PC, keyboard and mouse. In addition to the keyboard and mouse the BIOS handles several of the switch and LED functions on the PC. As this BIOS is programmed into the 8742 it occupies none of the memory map. This new keyboard controller also provides several Green power saving features.

### 6.2.4 Expansion Bus ROMs

APEX II and conventional PC hardware allow add-on cards to be inserted on the AT expansion bus. If software is required to control the electronics on these cards the supplier may choose to provide this software in the form of an expansion ROM or adapter ROM. On power-up the PC, once initialised, checks for the presence of ROMs within the memory space of C8000 to DFFFF Hex. If present the code within the ROM is run and the specific hardware on the card controlled accordingly. In addition, this software can then be used as the interface to the electronics by the operating system; thereby acting as an extension to the System BIOS for the new electronics.

## 6.3 AMI WinBIOS System BIOS User Features

Features included are as follows :

- Keyboard Speed Switching
- Memory Detection
- Password Support
- Autodetection of IDE Hard Drive Parameters
- Autodetection of Processor Type and Speed
- Autodetection of Memory Size and Type
- Customisation of the System
- User definable Hard Disk Types
- PS/2 Mouse Support
- Boot Sector Virus Support
- Local Peripheral Support
- Shadow RAM Support
- Keyboard Typematic Rate and Delay
- Num Lock Power-on Status

- Fast Gate A20 Support

### 6.3.1 AMI WinBIOS Hot Key

The AMI WinBIOS provides a hot key to create a reset. These key operations are:

<Ctrl>,<Alt> and <DEL> Causes a Soft Reset

All keys should be pressed down together to operate the chosen function.

### 6.3.2 AMI BIOS Power-on Self Test (POST)

AMI WinBIOS provides all IBM standard POST routines as well as enhanced AMI BIOS routines. All POST checkpoint codes are written to the POST display at I/O location 80 Hex (not fitted as standard but available as an option fitted to connector P6).

Appendix G gives a complete list and a detailed description of all of the POST error codes. To view these error codes you will need the APEX II POST display adapter.

### 6.3.3 POST Error Messages and Beep Codes

If the BIOS cannot configure the video display controller it will communicate the identification of fatal errors (except error code 8) via a series of beeps. These errors will only occur during power-on tests. A full list of beep codes can be found in appendix G.

### 6.3.4 Accessing the AMI Set-up Screens

The AMI BIOS Set-up is accessed by pressing the 'DEL' key on the keyboard when the screen displays the message:

Hit <DEL> if you want to run Set-up

If you press the 'DEL' key too late, reset the unit and try again.

You can reset the unit by either switching the main input power off and on, or by using the HOT KEYS :-

<Ctrl>,<Alt> and <DEL> pressing them together.

### 6.3.5 Controlling the AMI Set-up Screens

This version of the AMI BIOS is designed to be controlled with a mouse installed onto the COM1 port (RS232). However, you can access all of the set-up routines without a mouse by using an attached keyboard and the following basic key inputs as detailed in section 3.6.

If your application does not have a locally attached keyboard or display, then you will need to run the APEX REMOTE ACCESS TERMINAL software. A BIOS setting allows the APEX II to send all VIDEO and KEYBOARD information via a serial link to a host PC also running suitable software. In this mode the APEX II unit can be completely configured remotely and thus removes the need to have access to the APEX II board at all. This will allow encapsulated or very remote applications to be configured with great ease.

Please contact Blue Chip Technology for further information.

### 6.3.6 AMI BIOS Keyboard Control Keys

The following keyboard keys can be used either with a mouse or instead of a mouse.

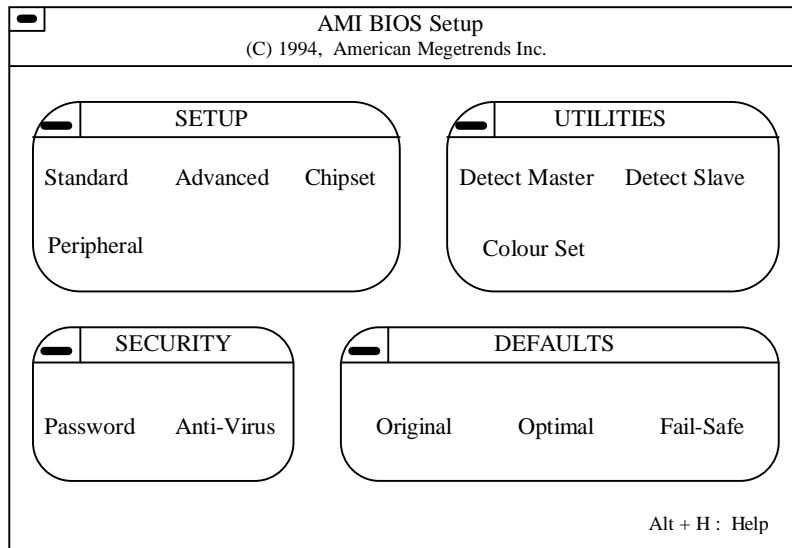
ESC	Escapes back one menu level and also to exit.
TAB and SHIFT TAB	Let you move around the various functions to be changed. Also used to jump from menu to menu.
ARROW keys	Lets you move up and down the menu lists under change.
ENTER key	Is used to enter your changes.
ALT + H	Provides HELP at any point
ALT + Space	Global Exit

## 6.4 AMI BIOS Main Set-up Screen

The AMI WinBIOS main set-up screen is divided into four parts:

SET-UP      sections 6.5 - 6.8  
UTILITIES    section 6.9  
SECURITY    section 6.10  
DEFAULTS    section 6.11

They are shown on the main screen as follows :



These four main sections are sub-divided into several smaller groups which are now dealt with in more detail in the following sections.



## 6.5 SET-UP Section

The SET-UP Screen allows the user to configure the standard PC system components like disk drives, time/date etc.

### 6.5.1 Standard (CMOS) Set-up

#### Date/Time

##### Date

This entry allows you to set the Day, Date, Month and Year.

##### Time

This entry allows you to set the Hours, Minutes and Seconds. The clock operates in 24 hour mode; that means for a p.m. time add 12 to the hour e.g. enter 6:35 PM as 18:35:00.

#### Floppy A and Floppy B Disk Configuration

The APEX II unit via the BIOS will support 2 floppy disk drives A: and B:. The configuration list is as follows :

Not Installed	
360KB	5¼"
720KB	5¼"
1.2MB	5¼"
1.44MB	3½"
2.88MB	3½"

Both disk drives can be selected and can have either the same or different configurations.

#### Master Disk and Slave Disk Configuration

Two hard disk drives are supported directly by the BIOS these being C: and D:.

Each drive can be selected as either drive types 1 to 46, custom 47, ESDI or SCSI. Custom type 47 (user) is user definable allowing all parameters for the drive to be customised. Both drives can be set to a different type 47 if required.

When custom 47 option is selected and auto detect is accessed (via the Utilities Set-up) the system will detect the hard disk parameters for hard disk drives connected with IDE interfaces.

It then displays the parameters that it detects and allows you to accept or reject the parameters. If accepted, these parameters are displayed for the hard disk drive.

Please note that when Auto Detect is run on a drive that is not present (drive D: in most systems), there will be a delay before the test is completed.

## **6.6 Advanced (CMOS) Set-up**

The Advanced set-up screen allows you to customise various primary parts of the BIOS. These are in order as follows :

### **6.6.1 Typematic Rate, Delay and Programming**

The control of Typematic rate Programming allows the auto repeat and delay before repeat to be selected. The defaults and options are as shown on the screen. The Typematic Rate Delay describes the delay before auto repeat starts. The Typematic Rate is the frequency of the key generation once in auto repeat.

### **6.6.2 System Keyboard**

The APEX II keyboard interface is AT and PS/2 compatible, and can be connected to either AT or PS/2 keyboards. The default setting is Enabled. If your system is to operate without a keyboard then select Disabled. Failure to do this will result in an error being generate during the power-on diagnostics check.

### **6.6.3 Primary Display**

This entry allows the user to select between one of the following :

MDA™, CGA™ or EGA/PGA/VGA display controllers.

If your system is to operate without a display then select Disabled. Failure to do this will result in an error being generated during the power-on diagnostics check.

#### **6.6.4 Mouse Support**

This enables or disables the mouse support option. The mouse control is effected by the 8742 keyboard controller on the APEX II unit and is PS/2 compatible.

#### **6.6.5 Above 1MB Memory Test**

By enabling this test any RAM above 1MB will be exercised by the POST diagnostics thereby taking longer to boot. If your unit is not fitted with more than 1MB of RAM or you wish to shorten the boot time, set this option to disabled. If you wish to ensure maximum DRAM integrity then set this option to Enabled.

#### **6.6.6 Memory Test Tick Sound**

This option selects whether an audible indication of the presence of memory during the POST is generated or not. Once either <ESC> or <DEL> is depressed the audio output is disabled.

#### **6.6.7 Parity Error Check**

This option selects whether the parity circuit is active on the system DRAM. We strongly recommend that this is set to enabled at all times thereby providing communication of any RAM corruption. If this option is not required select disabled.

#### **6.6.8 Hit "DEL" Message Display**

Disabling this option removes this message prompt from appearing during power-up. This may be required when you do not wish to draw attention to existence of the Set-up Menus within the BIOS. The default is enabled.

#### **6.6.9 Extended BIOS RAM Area**

The system BIOS holds data in a BIOS table in an area of RAM set by this function. The 2 settings are 0:300 or DOS 1K

The system default is 0:300.

### **6.6.10 Wait for "F1" If any Error**

If any of the tests run during the POST cause an error then this message will be displayed. If this message is enabled then after displaying it the DX1 will halt waiting for <F1> to be pressed. If you expect errors during the POST or do not wish the boot to be halted if any error occurs then disable this option.

### **6.6.11 System Boot Up Num Lock**

If you wish the numeric keypad to be active after a boot then select ON. If, however, you wish the ←,↑,↓ and → keys to be available after power-up then set this option to OFF.

### **6.6.12 Floppy Drive Seek At Boot**

If enabled, a seek is performed on floppy drive A: at system boot time. The options are Enabled or Disabled. By disabling this option the boot time can be reduced. If very old 360KB drives are used it may be necessary to enable this option to ensure that the heads are recalibrated before any data is accessed.

### **6.6.13 Floppy Disk Swapping**

This function allows the user to swap the floppy disk drives on his system. Two floppy disk units on the system say A: = 3½" and B: = 5¼" swapped would then be the A: = 5¼" and the B: = 3½"

The options for this BIOS function are :

Enabled or Disabled.

The system default is disabled.

### **6.6.14 System Boot Up Sequence**

The default boot sequence is drive A: and then C:. This would mean that if drive A: is not ready then the boot occurs from drive C:. The alternative is to boot from drive C: and if C: is not ready then drive A. Hence the settings are either: "A:, C:" or "C:, A:".

### **6.6.15 System Boot Up CPU Speed**

The function allows the selection of the CPU speed at boot time. The default is High speed. The alternative is Low.

### **6.6.16 Internal Cache**

This option enables the CPU internal cache memory. The settings are Enabled or Disabled. The BIOS Set-up default is Enabled.

### **6.6.17 Turbo Switch Function**

This option enables the externally mounted hardware Turbo switch. The settings are Enabled or Disabled.

The default is Disabled.

### **WARNING**

Do not set to “Enabled”. APEX II does not support a Turbo switch.

### **6.6.18 Password Checking**

This option enables a password check every time the systems boots or Set-up is executed. The settings are:

- |        |  |
|--------|--|
| Always | If Always is selected the user password prompt appears every time the system is turned on. |
| Set-up | If Set-up (the default) is chosen, the password prompt appears if Set-up is executed.      |

#### Note

If the BIOS does not have a valid password held in CMOS RAM then the above options will not apply and the system will not request a password at any point.

### 6.6.19 Video Shadow C000, 16K Video Shadow C400, 16K

These options specify if the contents of the ROM memory area from C0000 – C3FFFh and C4000 – C7FFFh are shadowed to RAM and if these contents can be stored in cache memory.

Setting	Description
Into-486	The contents of memory are shadowed from ROM to RAM and can be written to or read from the internal cache memory on the 486,
Cached	The contents of memory are shadowed from ROM to RAM and can be written to or read from cache memory.
Disabled	The contents of memory cannot be shadowed from ROM to RAM and cannot be written to or read from cache memory.
Enabled	The contents of memory are shadowed from ROM to RAM but cannot be written to or read from cache memory.

The BIOS Set-up and Power-On defaults are Disabled.

### 6.6.20 Shadow C800, 16K Shadow CC00, 16K Shadow D000, 16K Shadow D400, 16K Shadow D800, 16K Shadow DC00, 16K Shadow E000, 32K Shadow E800, 32K

This option specifies if the contents of the ROM memory area are shadowed to RAM and if these contents can be stored in cache memory.

Setting	Description
Into-486	The contents of memory are shadowed from ROM to RAM and can be written to or read from the internal cache memory on the 486,
Cached	The contents of memory are shadowed from ROM to RAM and can be written to or read from cache memory.
Disabled	The contents of memory cannot be shadowed from ROM to RAM and cannot be written to or read from cache memory.
Enabled	The contents of memory are shadowed from ROM to RAM but cannot be written to or read from cache memory.

The BIOS Set-up and Power-On defaults are :

C8000 - CBFFFh	Into-486
CC000 - CFFFFh	Disabled
D0000 - D3FFFh	Disabled
D4000 - D7FFFh	Disabled
D8000 - DBFFFh	Disabled
DC000 - DFFFFh	Disabled
E0000 - E3FFFh	Disabled
E8000 - E3FFFh	Disabled

#### **6.6.21 Main BIOS Cache F000, 64K**

The default is Disabled. We recommend that this setting is not changed.

#### **6.6.22 IDE Block Mode**

This BIOS function allows the system to pass information to and from the IDE hard disk in block mode. As not all IDE drives can make use of this higher speed transfer rate, the ability to Disable this mode is included. The functions can be set as follows:

Disabled or Enabled  
The system default is Disabled.

#### **6.6.23 Primary Master IDE LBA Mode**

This option turns on or off the hard disk drive's LBA mode support. Logical Block Addressing (LBA) is used to support drives with densities greater than 540MB.

The available options are:

Enabled LBA mode support on( for drives greater than 540MB)  
Disabled LBA mode support off

#### **6.6.24 Primary Slave IDE LBA Mode**

This option is as above but for the Primary Slave IDE drive.

### **6.6.25 Secondary IDE Drives present**

As standard the APEX II is fitted with a primary IDE controller. If an additional controller is added via the ISA slot or the PC/104 connector, this option should be set accordingly.

The available options are:

None	No Secondary drives fitted (default)
One	1 Secondary master drive fitted
Two	2 Secondary master/slave drives fitted.

### **6.6.26 Secondary Master IDE LBA Mode**

This option is as above but for the secondary Master IDE drive.

### **6.6.27 Secondary Slave IDE LBA Mode**

This option is as above but for the secondary Slave IDE drive.

### **6.6.28 Auto Keylock Timeout (Min)**

This function allows the user to set a time in minutes (0 - XX)

### **6.6.29 CPU Selection**

This BIOS function sets the CPU type and is normally set and left to AUTO. However, this function can be set as follows :

AMD, Cyrix, IBM Intel, SGS Thompson, TI, UMC  
Auto

The system default is Auto.



## 6.7 Advanced Chipset Set-up

The advanced Chipset Set-up screen allows you to set more in-depth chip-set functions and they are described in more detail as follows.

### 6.7.1 Auto Config Function

The settings are Enabled or Disabled. If this option is set to Enabled, the following ADVANCED CHIPSET SET-UP options are automatically configured to optimal settings by AMI BIOS based on the APEX II and CPU frequency:

- DRAM Wait State Select
- DRAM Page Mode
- Keyboard Clock Select
- AT Clock Select

The BIOS Set-up and Power-On defaults are Enabled.

### 6.7.2 DRAM Wait State Select

This option sets the number of wait states inserted before all DRAM system memory operations. The settings are 0 W.S., 1 W.S., or 2 W.S.

The BIOS Set-up and Power-On default is 2 W.S.

### 6.7.3 DRAM Page Mode

This option specifies the type of DRAM used for system memory.

### 6.7.4 Keyboard Clock Select

This option sets the source of the keyboard clock.

The settings are as follows :

- CPUCLK/6, CPUCLK/5, CPUCLK/4, CPUCLK/3, CPUCLK/2,  
9.5 MHz, or 7.2 MHz.

The BIOS Set-up default is CPUCLK/3

The Power-On default is 9.5MHz

### 6.7.5 AT Clock Select

This option sets the source of the AT Clock (ATCLK).

The settings are as follows :

CPUCLK/6, CPUCLK/5, CPUCLK/4, CPUCLK/3, CPUCLK/2,  
CPUCLK/8, or 7.2 MHz.

The BIOS Set-up default is PCLK/4.

The Power-On default is PCLK/6.

### 6.7.6 Local Bus Ready Delay

This option sets the delay for the LBRDY# signal from the VL-Bus (video controller) and should always be set to delay 1T.

The BIOS options are:

No Delay Delay  
Delay 1T (default)  
Delay 2T  
Delay 3T

### 6.7.7 LDEV# Sample Time

This option is used for VL-Bus devices operating above 33MHz. This option should always be set for T3

The BIOS options are:

in T2  
in T3 (default)  
in T4  
in T5

### 6.7.8 ISA Bus Refresh Disable Bit

This option allows the user to switch off the ISA bus refresh cycle resulting in faster refresh cycles. The fast option should only be used if there are no ISA Refresh dependent ISA cards in the system

The available options are:

SLOW	ISA Refresh Enabled (default)
FAST	ISA Refresh Disabled

### 6.7.9 DRAM Refresh Method

This option selects between CAS and RAS Refresh cycles or RAS only refresh cycles. This selection will depend on the SIMM memory modules used but most SIMMs will support either. RAS Only cycles will give a slight performance increase.

The settings are :

RAS Only (Default)
CAS/RAS

### 6.7.10 Divider for Refresh

The frequency of refresh cycles is nominally set to 15 microseconds ( $\mu\text{S}$ ) i.e. a DRAM refresh is performed every  $15\mu\text{S}$ . This option allows the user to reprogram this frequency such that the refresh cycle occurs less frequently in multiples of  $15\mu\text{S}$  e.g.  $30\mu\text{S}$ ,  $60\mu\text{S}$  etc.

Whilst this option can improve system performance, if not used correctly it can make the system unreliable.

Blue Chip Technology strongly advise that this option be left set to its default setting of 15 $\mu$ S (1/1). The settings are :

1/1	Refresh cycle performed every 15 $\mu$ S (Default)
1/2	Refresh cycle performed every 30 $\mu$ S
1/4	Refresh cycle performed every 60 $\mu$ S
1/8	Refresh cycle performed every 120 $\mu$ S
1/16	Refresh cycle performed every 240 $\mu$ S
1/32	Refresh cycle performed every 480 $\mu$ S
1/64	Refresh cycle performed every 960 $\mu$ S

#### **6.7.11 IO Recovery Time**

This specifies the I/O command recovery time (in multiples of AT bus clock cycles) between successive I/O cycles. This value may need to be set to a high value when slow older I/O cards are used.

The options are:

0 BLK	
1 BLK	
2 BLK	
3 BLK	
5 BLK	(Default)
7 BLK	
9 BLK	
12 BLK	

### **6.7.12 CPU Hold Time**

This option is used to delay the CPU Hold time.

The available settings are:

- Disabled (Default)
- 1/16
- 2/16
- 3/16
- 4/16
- 5/16
- 6/16
- 7/16

### **6.7.13 Internal Cache State**

The available options are:

- Enabled
- Disabled

## **6.8 Peripheral Set-up**

The Peripheral Set-up Menu allows control of the APEX II's on-board peripheral devices. These devices include the disk drive controllers, serial and parallel outputs, digital I/O and Solid State Memory.

All of the peripheral outputs are now discussed in more detail.

### **6.8.1 Programming Mode**

The options are Manual or Automatic. During the POST the BIOS identifies all peripherals in the system. If automatic mode is selected then the on-board peripheral functions are mapped around those found by the POST.

This mode will override the following settings:

- On-board FDC
- On-Board IDE
- Serial 1
- Serial 2
- Parallel 1

In manual mode you have control as to how the following functions are configured.

### **6.8.2 On-Board FDC (Floppy Disk Controller)**

This option enables the floppy controller on the APEX II unit. The setting can either be Enabled or Disabled. The default is Enabled.

### **6.8.3 On-Board IDE (Hard Disk Controller)**

This option enables the IDE controller on the APEX II unit. This setting can either be Enabled or Disabled. The default is Disabled.

### **6.8.4 Serial Port 1 (Address)**

This option allows the first serial port address on the APEX II unit to be configured as either 03F8h (COM1), 03E8h (COM3), or Disabled

The interrupt selection will be made automatically to IRQ4.

“Disabled” will remove the interrupt connection.

### **6.8.5 Serial Port 1 Mode (RS232/RS485)**

This function selects either RS232 or RS485 modes. The options are:

RS232	This option allows RS232 output communications using connector P10.
RS485(H)	This option allows Half Duplex (2 wire) RS485 communications using half of connector P12.

RS485(F) This option allows Full Duplex (4 wire) RS485 communications using half of connector P12

The default is RS232.

### 6.8.6 Serial Port 2 (Address)

This option allows the second serial port address on the APEX II unit to be configured as either 02F8h (Com2), 02E8h (Com4) or Disabled.

The interrupt selection will be made automatically to IRQ3.

“Disabled” will remove the interrupt connection.

### 6.8.7 Serial Port 2 Mode (RS232/RS485)

This function allows you to select between RS232 and RS485 modes.

The options are :

RS232 This option allows RS232 output communications using connector P11.

RS485(H) This option allows Half Duplex (2 wire) RS485 communications using half of connector P12.

RS485(F) This option allows Full Duplex (4 wire) RS485 communications using half of connector P12

The default is RS232.

### 6.8.8 Parallel Port Address

This option allows the parallel port address on the APEX II unit to be configured as 0378h (LPT1), 0278h (LPT2) or Disabled.

The interrupt selection is made via J7.

For LPT1 J7 should be set to 1 - 2 (IRQ7)

For LPT2 J7 should be set to 2 - 3 (IRQ5)

### **6.8.9 Parallel Port Mode (Normal/Extended)**

This option controls the mode of the APEX unit's parallel printer port. This option can be either Normal or Extended. Normal setting is for standard printer operation. Extended setting provides bi-directional operation. The default is Extended.

### **6.8.10 Digital I/O Port**

The APEX II unit employs a 70155 (8255) PIO which has 24 lines of digital I/O. Its base address can be set to one of the following :

200H, 300H, or Disabled

The default setting is Disabled.

### **6.8.11 IRQ Active**

This option allows the user to select between positive edge (high) and negative edge (low) triggered interrupts. The settings for APEXII should always be set to positive edge (high).

It can be set to one of the following:

HIGH	Positive edge triggered interrupts
LOW	Negative edge triggered interrupts



### 6.8.12 On-Board Flash Memory

The APEX II's on-board standard Flash memory consists of a 1MByte TSOP device (IC36). This device can be set to one of the following 6 settings:

- |          |   |
|----------|---|
| Disabled | The Flash Device can not be used or programmed if this is selected.   |
| MemMap   | Selected for programming the Flash.   |
| EnDriveA | Will look like a normal floppy drive set to A: and will boot from it if the Flash contains the correct information.   |
| EnDriveB | Will look like a normal floppy drive set to B: and will boot from it if the Flash contains the correct information.   |
| CTrick A | This will cause the Flash to act as a true Read/Write disk drive when the APEX II unit is running the correct software. If selected the Flash will boot like a drive A: |
| CTrick B | This will cause the Flash to act as a true Read/Write disk drive when the APEX II unit is running the correct software. If selected the Flash will boot like a drive B: |

Please read the Flash Programming Appendix I at the rear of this manual for a more in-depth look at SSD usage.

### 6.8.13 Flash Socket

APEX II has one 32-pin byte-wide DIL Flash socket (IC32) capable of holding up to 2MBytes of memory. This socket can be configured in exactly the same way as the on-board Flash memory above and can be set to one of the following:

Disabled, MemMap, EnDriveA, EnDriveB, CTrick A, or CTrick B

The Flash socket can be used in conjunction with the on-board Flash to give a maximum of 3MBytes of Flash memory.

Please read the Flash Programming Appendix I at the rear of this manual for a more in-depth look at SSD usage.

#### 6.8.14 SRAM Socket

APEX II has one 32 pin byte-wide DIL SRAM socket (IC34) capable of holding up to 512KBytes of memory. This socket can be configured in exactly the same way as the on-board Flash memory above. It can be set to one of the following:

- Disabled      The SRAM Device can not be used or programmed if this is selected.
- MemMap      Selected for programming the SRAM.
- EnDriveA    Enables the SRAM as Drive A:
- EnDriveB    Enables the SRAM as Drive B:

Please read the Flash Programming Appendix I at the rear of this manual for a more in-depth look at SSD usage.

#### 6.8.15 Remote Disk

The remote disk facility allows the APEX II unit to communicate with floppy disk drives through a serial communications link to a PC based host computer running DOS.

The BIOS can be set to one of the following settings:

- Disabled              If selected means this function can not be used
- Enabled on Com1    Communications via Com1 (RS232)
- Enabled on Com2    Communications via Com2 (RS232)

For more detailed information on using this link please read Appendix I at the rear of this manual.

## 6.9 Utilities Set-up Screen

This BIOS main Set-up screen allows the user to auto detect both the master and slave hard disk units and also to set the BIOS system colours shown on the screen.

### 6.9.1 Detect Master

This option detects the hard disk parameters for hard disk drives connected as the master drive (C: normally) with IDE interfaces. It displays the parameters that it detects and allow the you to accept or reject the parameters.

If accepted, these parameters are displayed for the hard disk drive in standard CMOS Set-up.

Please note that when an Auto Detect is run on a drive that is not present (drive D: in most systems) then there will be a delay before the test is completed.

### 6.9.2 Detect Slave

This option detects the hard disk parameters for hard disk drives connected as the slave drive (D: normally) with IDE interfaces. It displays the parameters that it detects and allows you to accept or reject the parameters.

If accepted, these parameters are displayed for the hard disk drive in standard CMOS Set-up.

#### Note

When an Auto Detect is run on a drive that is not present (drive D: in most systems) then there will be a delay before the test is completed.

### 6.9.3 Colour Set

The screen colours that are used when the AMI BIOS is running can be chosen from a short list of 4 variants:

LCD  
ARMY  
PASTEL  
SKY

The default is “SKY”.

## **6.10 Security Set-up Screen**

Under this section you can set a password that is used as detailed under the PASSWORD BIOS instruction found in the Advanced CMOS Set-up screen, and also set the anti-virus option.

### **6.10.1 Bypassing Password Support**

You can bypass the password support by pressing <Enter> when the password prompt appears.

### **6.10.2 Enabling Password Support**

The password check option is enabled in Advanced CMOS Set-up by choosing either Always or Set-up. The password, which can be up to 6 characters in length, is stored in CMOS RAM.

### **6.10.3 If a Password is in Already in Use**

You must correctly type in the current password when

'enter CURRENT Password'

appears on the screen.

After the current password has been correctly entered, the user is asked to enter the new password.

### **6.10.4 Setting a new password**

The user is asked to enter up to a 6 character password and then press the enter key to accept it.

If the password information is incorrect, an error message appears.

If the new password confirmation is entered without error, the end user presses <Esc> to return to the Main Set-up Menu.

### **6.10.5 Password Storage**

The password is stored in CMOS RAM after you have finished all BIOS alterations and exited Set-Up. The next time the systems boots, you must enter the password if the password function is present and has been enabled.

Whether the prompt appears depends on the options chosen in the Advanced CMOS Set-up. If Always was set, the prompt appears every time the system is powered on. If Set-Up was set, the prompt will not appear when the system is powered on, but is displayed when Set-up is run.

### **6.10.6 Using a Password**

You should keep a record of the new password when the password is changed. If you forget the password and password protection is enabled; the only way to boot the system will be to disable the CMOS RAM. This is achieved on the APEX II unit by setting J9 to position 2 - 3 for approximately 5 minutes.

Ensure that J9 is reset to position 1 - 2 before powering on the system.

#### Note

All CMOS RAM contents will be lost as a result of this action. It is important that you keep a record of any changes you make to any of the Set-up screens so that they will not be lost forever.

## **6.11 Default BIOS Set-up Screen**

This screen allows the user to configure the BIOS settings to one of the following 3 states:

### **6.11.1 Original BIOS Settings**

This function will set any changed BIOS values back to the states that were present when the user entered the BIOS Set-up screen.

To select this option select ORIGINAL and answer either Yes or No as prompted.

### **6.11.2 Optimal BIOS Settings**

This will automatically configure the BIOS for OPTIMAL BIOS settings and will be dependant upon the APEX II system components. To select this option select OPTIMAL and answer either Yes or No as prompted.

### **6.11.3 Fail-Safe BIOS Settings**

This will automatically configure the BIOS with a Fail-Safe set of BIOS settings and will be dependant upon the APEX II system components. This option will always ensure that the APEX II unit starts up. To select this option select FAIL-SAFE and answer either Yes or No as prompted.

## **6.12 Saving and Exiting the AMI BIOS**

When you have completed all of your BIOS configuration changes you will need to save these changes to the CMOS memory.

From the main Set-up screen either press the ESC key or ALT + Space to access the exit routines. Use the TAB key to select the option you require and press return to action your save and exit request.

If you are uncertain then pressing the ESC key again will take you back to the main Set-up screen.

## **6.13 APEX II BIOS Extensions**

### **6.13.1 General Overview**

The APEX II unit provides a BIOS extension at address C800:0000 which provides the user with access to the additional hardware found on the board. The BIOS extension hooks into software interrupt 50 Hex. The user loads a particular function code into the AH register followed by a specific set of parameters in the other registers before executing the interrupt.

Most high level languages allow access to software interrupts through a particular function call.

For example, in Quick Basic

```
' Read E2 Data via interrupt 50 call
$include: 'QB.BI'

DIM INARY%(7),OUTARY%(7)
CONST AX=0,BX=1,CX=2,DX=3,BP=4,SI=5,DI=6,FL=7

INARY%(AX) = &H0400      ' Read e2 data
INARY%(BX) = &H31        ' address &H31
CALL INT86OLD(&H50,INARY%(),OUTARY%())' Call the APEX
'                               service
PRINT "E2 ADDRESS &H31 CONTAINS: ";OUTARY%(DX)
```

and similarly in C :-

```
#include <stdio.h>
#include <dos.h>

#define APEX 0x50

void main(void)
{
    union REGS regs;
    regs.x.ax = 0x0400;    /* read e2 */
    regs.x.bx = 0x31;     /* address 0x31 */
    int86(APEX, &regs, &regs);
    printf("e2 Address 0x31 contains %x\n",regs.x.dx);
}
```

### 6.13.2 System Identification

In order to detect what BIOS software is running on an APEX II unit a function has been provided which returns a BIOS identification and revision number.

Calling Registers: AH = 08H

Return Registers: AX = Current version of BIOS  
 AH = Major revision  
 AL = Minor revision in BCD format  
 BX = BIOS Identification value 4981 Hex

The following C routine demonstrates the use of this function.

```

unsigned int System_ID(void)
{
    /* return system ID code */

    struct REGPACKregs;
    reg.r_ax = 0x0900 /* Function to return ID code */
    reg.r_dx = 0x0000 /* Clear DX */
    intr(0x50,&reg) /* ID returned in DX */
    return reg.r_dx /* APEX II returns 0x4981 */
                /* Other systems returns 0x0 */
}

```

### 6.13.3 Flash Memory Functions

The standard APEX II has on-board 1024KBytes of Flash memory. It also contains an SRAM DIL socket which can accommodate up to 512K of SRAM and a Flash DIL socket which can accommodate up to a further 2048KBytes.

The APEX BIOS Extension provides four functions which allow the programmer access to the Flash/SRAM memory. These are:

- Read one or more Flash Sectors into RAM
- Write one or more Flash Sectors
- Erase all Flash
- Size Flash/SRAM

### 6.13.4 Read a Flash Sector

Calling Registers: AH = 00  
 AL = Device number (00 for internal Flash)  
                       (01 for SRAM Socket)  
                       (02 for Flash Socket)  
 CX = Number of sectors to transfer  
 DX = Start Sector  
 DS:BX = Pointer to users buffer

Return Registers: Carry **Clear** if successful



Carry **Set** if unsuccessful with error code in AX

This function is provided to allow the transfer of data from the internal Flash EPROM. Each Flash sector is 512Bytes long.

### 6.13.5 Write to a Flash Sector

Calling Registers: AH = 01  
AL = Device number (00 for internal Flash)  
(01 for SRAM Socket)  
(02 for Flash Socket)  
CX = Number of sectors to transfer  
DX = Start Sector  
DS:BX=Pointer to users buffer

Return Registers: Carry **Clear** if successfully  
Carry **Set** if unsuccessful

This function is provided to allow the transfer of data from a user buffer to the internal Flash. Each flash sector is 512 Bytes long.

#### Note

Each Flash sector can only be programmed once - in order to re-write a sector the Flash Format function must be called first.

### 6.13.6 Flash Format

Calling Registers: AH = 02  
AL = Device number (00 for internal Flash)  
(01 for SRAM Socket)  
(02 for lash Socket)

Return Registers: Carry Clear if successful  
Carry Set if unsuccessful

This function erases the entire contents of the Flash.

DL is loaded with 1 and a changing character pattern is shown at the current cursor position.

#### Note

Depending on the age of the Flash this can take up to 10 seconds to complete.

### 6.13.7 SRAM Memory Functions

The APEX II has on-board SRAM memory options of 128KB, 256KB, and 512KB provided by a 32 pin DIL socket.

The SRAM memory socket is battery backed by either the on-board battery or, if selected, an external battery. SRAM is by far the best memory to hold critical data in and the APEX II board also allows the SRAM socket to hold a SRAM Memory Module (a chip with on-board battery). This allows the device to be removed from the board without any data being lost.

The SRAM memory is located at memory location E80000-EBFFF.

### 6.13.8 Watchdog Control Mode

In this mode the chip is used to monitor the APEX II unit for a software or hardware failure. The AMI BIOS Setup Menu does not give access to this function but instead two in-built BIOS control codes are available which allows the user to decide whether their application requires protection against such a potential processor failure.

When enabled, the watchdog will generate a hardware reset if a RESET WATCHDOG function call is not made at least once every 500 milliseconds.

The two functions available to control the watchdog are as follows:

### 6.13.9 Enable/Disable Watchdog

Execute following code:

```
mov dx, 101h
mov al, 1h    ;enable watchdog
out dx, al

mov dx, 101h
mov al, 0h    ;disable watchdog
out dx, al
```

### 6.13.10 Reset Watchdog

Execute following code:

```
mov dx, 101h
in al, dx ;reset watchdog
```

If the Watchdog is enabled and I/O location 0101 Hex is not **read** within 500 milliseconds the Watchdog will generate a **Reset** to both the APEX II microprocessor and the PC/104 and XT/AT slot.

The Watchdog is disabled following a power-up or reset condition. Thereafter it may be controlled by using the above code fragments.

I/O Hex	Access	Operator	Action
0101	Write Only	Bit 1	0 - Disable Watchdog operation 1 - Enable Watchdog operation
0101	Read Only	Byte	Read every 500mS to reset timer

### 6.13.11 E<sup>2</sup>PROM Access and Control

The E<sup>2</sup>PROM on the APEX II unit is a 9348 serially programmed device which is accessed through a single register at port 100 Hex.

Unlike the Flash device, E<sup>2</sup>PROM does not require to be completely erased before a single location is written to. It is therefore much more useful for the storage of configuration information.

There are 64, 16-bit words of E<sup>2</sup>PROM - the lower 32 are reserved for use by Blue Chip Technology for configuration information.

The top 32, 16-bit words are available for user information.

The E<sup>2</sup>PROM's individual control lines are arranged as follows at port 100 Hex :

7	6	5	4	3	2 Data In	1 Clock for serial data	0 Chip Select / Data Out
---	---	---	---	---	-----------------	-------------------------------------	--------------------------------------

## 6.14 E<sup>2</sup>PROM Control

The APEX II BIOS extension provides two functions to allow access to the E<sup>2</sup>PROM memory. These are :

### 6.14.1 Write to E<sup>2</sup>PROM (Single Location)

Calling Registers: AH = 03  
BL = Location to write to (0-63)  
DX = Data to Write (16 bit value)

Return Registers: Carry flag clear if successful.  
Carry flag Set if unsuccessful.

### 6.14.2 Read E<sup>2</sup>PROM (Single Location)

Calling Registers: AH = 04  
BL = Location to read (0-63)

Return Registers: DX = E<sup>2</sup>PROM Data

## 6.15 Memory Maps

Please see Appendix N at the rear of this manual for this information.

## 6.16 I/O Address Map

Please see Appendix F at the rear of this manual for this information.

## **6.17 DMA Channels**

Please see Appendix E at the rear of this manual for this information.

## **6.18 Interrupts Assignments**

Please see Appendix D at the rear of this manual for this information.

## **6.19 APEX II Software Utilities**

The APEX II unit is supplied with a Software Utilities disk which contains a number of test and application programs. This software is under copyright control and is not to be copied without the written permission of Blue Chip Technology.

Appendix J at the rear of this manual gives a complete insight into the contents and usage of the Utilities Disk.

If you have any problems in using the disk, please contact the Blue Chip Technology's Technical Support department with your query.

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## 7. APPENDIX A : CONNECTOR PINOUTS

### 7.1 P1: LCD Connector (40 way Female header )

Pin N°	Signal	Pin N°	Signal
2	LCDRST	1	FPVDCLK
4	NPD	3	MOD
6	FVSYNC	5	LFS
8	FHSNYC	7	LLCLK
10	STANBY	9	R5
12	SUSPEND	11	R4
14	DE	13	R3 / SUD7
16	FPBACK	15	R2 / SUD6
18	FPVCC	17	G5 / SUD5
20	FPVEE	19	G4 / SUD4
22	VCC (APEX)	21	G3 / SUD3
24	GND	23	B5 / SUD2
26	GND	25	B4 / SUD1
28	GND	27	B3 / SUD0
30	GND	29	R1 / SLD7 / UD3
32	N/C	31	R0 / SLD6 / UD2
34	B1 / SLD1 / LD1	33	G2 / SLD5 / UD1
36	B0 / SLD0 / LD0	35	G1 / SLD4 / UD0
38	VCC (APEX)	37	G0 / SLD3 / LD3
40	+12 V	39	B2 / SLD2 / LD2

**7.2 P2: CRT Video Connector (10 way header)**

Pin N°	Signal	Pin N°	Signal
1	Analogue RED	2	0 Volts (Ground)
3	Analogue GREEN	4	0 Volts (Ground)
5	Analogue BLUE	6	0 Volts (Ground)
7	Horizontal Sync	8	0 Volts (Ground)
9	Vertical Sync	10	0 Volts (Ground)

**7.3 P3: IDE/Hard Drive Connector (40 way header)**

Pin N°	Signal	Pin N°	Signal
1	-Reset	2	0 Volts DC (Ground)
3	Data bit 7 (HD)	4	Data bit 8 (HD)
5	Data bit 6 (HD)	6	Data bit 9 (HD)
7	Data bit 5 (HD)	8	Data bit 10 (HD)
9	Data bit 4 (HD)	10	Data bit 11 (HD)
11	Data bit 3 (HD)	12	Data bit 12 (HD)
13	Data bit 2 (HD)	14	Data bit 13 (HD)
15	Data bit 1 (HD)	16	Data bit 14 (HD)
17	Data bit 0 (HD)	18	Data bit 15 (HD)
19	0 Volts DC (Ground)	20	Not used
21	Not used	22	0 Volts DC (Ground)
23	-IO Write (HD)	24	0 Volts DC (Ground)
25	-IO Read (HD)	26	0 Volts DC (Ground)
27	Not used	28	ALE (HD)
29	Not used	30	0 Volts DC (Ground)
31	IRQ14	32	IOCS16
33	Address 1 (HD)	34	Ground/Float (via link)
35	Address 0 (HD)	36	Address 2 (HD)
37	-Chip Select 0 (HD)	38	-Chip Select 1 (HD)
39	IDE LED Drive	40	0 Volts DC (Ground)



**7.4 P4: Peripheral / Utilities (20 way header)**

Pin N°	Signal	Pin N°	Signal
1	Audio +ve	2	Audio -ve
3	Reset +ve	4	Reset -ve (Ground)
5	Not Used	6	Not Used
7	Keyboard inhibit	8	0 V (Ground)
9	Power LED +ve	10	Power LED -ve
11	Mouse Data	12	Mouse clock
13	IDE LED +ve	14	IDE LED -ve
15	+5V (fused)	16	0 Volts (Ground)
17	Not Used	18	Not Used
19	Keyboard Data	20	Keyboard Clock

**7.5 P5: ISA AT Bus Connector (36 way)**

Side C	Signal	Side D	Signal
1	-SBHE	1	-MEMCS16
2	LA23	2	-IOCS16
3	LA22	3	IRQ10
4	LA21	4	IRQ11
5	LA20	5	IRQ12
6	LA19	6	IRQ15
7	LA18	7	IRQ14
8	LA17	8	-DACK0
9	-MEMR	9	DREQ0
10	-MEMW	10	-DACK5
11	SD8	11	DREQ5
12	SD9	12	-DACK6
13	SD10	13	DREQ6
14	SD11	14	-DACK7
15	SD12	15	DREQ7
16	SD13	16	+5 Volts
17	SD14	17	-Master
18	SD15	18	0 Volts (Ground)

**7.6 P6: POST Connector (12 way header)**

Pin N°	Signal	Pin N°	Signal
1	SD8	2	SD1
3	SD2	4	SD3
5	SD4	6	SD5
7	SD8	8	SD7
9	POST	10	0 Volts (Ground)
11	Vcc	12	Not Connected

**7.7 P7: Parallel (26 way header)**

Pin N°	Signal	Pin N°	Signal
1	-Strobe	2	-Auto Feed XT
3	Data bit 0	4	-Error
5	Data bit 1	6	-Initialise
7	Data bit 2	8	-Select (input)
9	Data bit 3	10	0 Volts (Ground)
11	Data bit 4	12	0 Volts (Ground)
13	Data bit 5	14	0 Volts (Ground)
15	Data bit 6	16	0 Volts (Ground)
17	Data bit 7	18	0 Volts (Ground)
19	-Acknowledge	20	0 Volts (Ground)
21	Busy	22	0 Volts (Ground)
23	Paper Empty	24	0 Volts (Ground)
25	Select (Output)	26	Not Used

**7.8 P8: Floppy Disk Drive Connector (34 way header)**

Pin N°	Signal	Pin N°	Signal
1	0 Volts (Ground)	2	+RPM/Low Current
3	0 Volts (Ground)	4	Not used
5	0 Volts (Ground)	6	Not used
7	0 Volts (Ground)	8	-Index
9	0 Volts (Ground)	10	-Motor 0
11	0 Volts (Ground)	12	-Drive select 1
13	0 Volts (Ground)	14	-Drive select 0
15	0 Volts (Ground)	16	-Motor 1
17	0 Volts (Ground)	18	+Direction
19	0 Volts (Ground)	20	-Step
21	0 Volts (Ground)	22	-Write Data
23	0 Volts (Ground)	24	-Write Gate
25	0 Volts (Ground)	26	-Track 0
27	0 Volts (Ground)	28	-Write Protect
29	0 Volts (Ground)	30	-Read Data
31	0 Volts (Ground)	32	+Head Select
33	0 Volts (Ground)	34	+Disk Change

**7.9 P9: Digital I/O Port Connector (26 way header)**

Pin N°	Signal	Pin N°	Signal
1	PA0	2	PB0
3	PA1	4	PB1
5	PA2	6	PB2
7	PA3	8	PB3
9	PA4	10	PB4
11	PA5	12	PB5
13	PA6	14	PB6
15	PA7	16	PB7
17	PC0	18	PC4
19	PC1	20	PC5
21	PC2	22	PC6
23	PC3	24	PC7
25	0 Volts (Ground)	26	0 Volts (Ground)

**7.10 P10: Serial 1 RS232 (10 way header)**

Pin N°	Signal	Pin N°	Signal
1	-Data Carrier Detect	2	-Data Set Ready
3	Receive Data	4	-Ready To Send
5	Transmit Data	6	-Clear To Send
7	-Data Term Ready	8	-Ringing Indicator
9	0 Volts (Ground)	10	Not used

**7.11 P11: Serial 2 RS232 (10 way header)**

Pin N°	Signal	Pin N°	Signal
1	-Data Carrier Detect	2	-Data Set Ready
3	Receive Data	4	-Ready To Send
5	Transmit Data	6	-Clear To Send
7	-Data Term Ready	8	-Ringing Indicator
9	0 Volts (Ground)	10	Not used

**7.12 P12: Serial ports 1 and 2 RS485 (10 way header)**

Pin N°	Signal	Pin N°	Signal
1	+ve Receive Data 1	2	10K $\Omega$ pull up (+5V)
3	-ve Receive Data 1	4	+ve Receive Data 2
5	+ve Transmit Data 1	6	-ve Receive Data 2
7	-ve Transmit Data 1	8	+ve Transmit Data 2
9	10K $\Omega$ pull down (0V)	10	-ve Transmit Data 2

**7.13 P13: Main Power Input (4 way header)****5¼" Disk Drive Connector**

Pin N°	Signal
See User Guide	+5 Volts DC (Pin next to C17 )
See User Guide	0 Volts (Ground)
See User Guide	0 Volts (Ground)
See User Guide	+12 Volts DC (Not required for APEX II operation. Only required for PC/104 or ISA cards that need +12V).

**7.14 P14: ISA PC/XT Bus Connector (62 way)**

Side A	Signal	Side B	Signal
1	-IOCHCK	1	0 Volts (Ground)
2	SD7	2	Resetdrv
3	SD6	3	+5 Volts
4	SD5	4	IRQ9
5	SD4	5	-5 Volts
6	SD3	6	DREQ2
7	SD2	7	-12 Volts
8	SD1	8	-0WS
9	SD0	9	+12 Volts
10	IOCHRDY	10	0 Volts (Ground)
11	AEN	11	-SMEMW
12	SA19	12	-SMEMR
13	SA18	13	-IOW
14	SA17	14	-IOR
15	SA16	15	-DACK3
16	SA15	16	DREQ3
17	SA14	17	-DACK1
18	SA13	18	DREQ1
19	SA12	19	-REF
20	SA11	20	CLK
21	SA10	21	IRQ7
22	SA9	22	IRQ6
23	SA8	23	IRQ5
24	SA7	24	IRQ4
25	SA6	25	IRQ3
26	SA5	26	-DACK2
27	SA4	27	T/C
28	SA3	28	BALE
29	SA2	29	+5 Volts
30	SA1	30	OSC
31	SA0	31	0 Volts (Ground)

**7.15 P15: PC104 PC/XT Bus Connector (64 way)**

Side A	Signal	Side B	Signal
1	-IOCHCK	1	0 Volts (Ground)
2	SD7	2	Resetdrv
3	SD6	3	+5 Volts
4	SD5	4	IRQ9
5	SD4	5	-5 Volts
6	SD3	6	DREQ2
7	SD2	7	-12 Volts
8	SD1	8	-0WS
9	SD0	9	+12 Volts
10	IOCHRDY	10	0 Volts (Ground)
11	AEN	11	-SMEMW
12	SA19	12	-SMEMR
13	SA18	13	-IOW
14	SA17	14	-IOR
15	SA16	15	-DACK3
16	SA15	16	DREQ3
17	SA14	17	-DACK1
18	SA13	18	DREQ1
19	SA12	19	-REF
20	SA11	20	CLK
21	SA10	21	IRQ7
22	SA9	22	IRQ6
23	SA8	23	IRQ5
24	SA7	24	IRQ4
25	SA6	25	IRQ3
26	SA5	26	-DACK2
27	SA4	27	T/C
28	SA3	28	BALE
29	SA2	29	+5 Volts
30	SA1	30	OSC
31	SA0	31	0 Volts (Ground)
32	0 Volts (Ground)	32	0 Volts (Ground)

**7.16 P16: Battery Connector (4 way header)**

Pin N°	Signal
1	+3.6 Volts DC
2	Not used (key)
3	0 Volts (Ground)
4	0 Volts (Ground)

**7.17 P17: PC104 AT Bus Connector (40 way)**

Side C	Signal	Side D	Signal
1	0 Volts (Ground)	1	0 Volts (Ground)
2	-SBHE	2	-MEMCS16
3	LA23	3	-IOCS16
4	LA22	4	IRQ10
5	LA21	5	IRQ11
6	LA20	6	IRQ12
7	LA19	7	IRQ15
8	LA18	8	IRQ14
9	LA17	9	-DACK0
10	-MEMR	10	DREQ0
11	-MEMW	11	-DACK5
12	SD8	12	DREQ5
13	SD9	13	-DACK6
14	SD10	14	DREQ6
15	SD11	15	-DACK7
16	SD12	16	DREQ7
17	SD13	17	+5 Volts
18	SD14	18	-Master
19	SD15	19	0 Volts (Ground)
20	No Connection	20	0 Volts (Ground)

**7.18 P18: Main Power Input Option 2 (4 way male header)****3½" Disk Drive Connector**

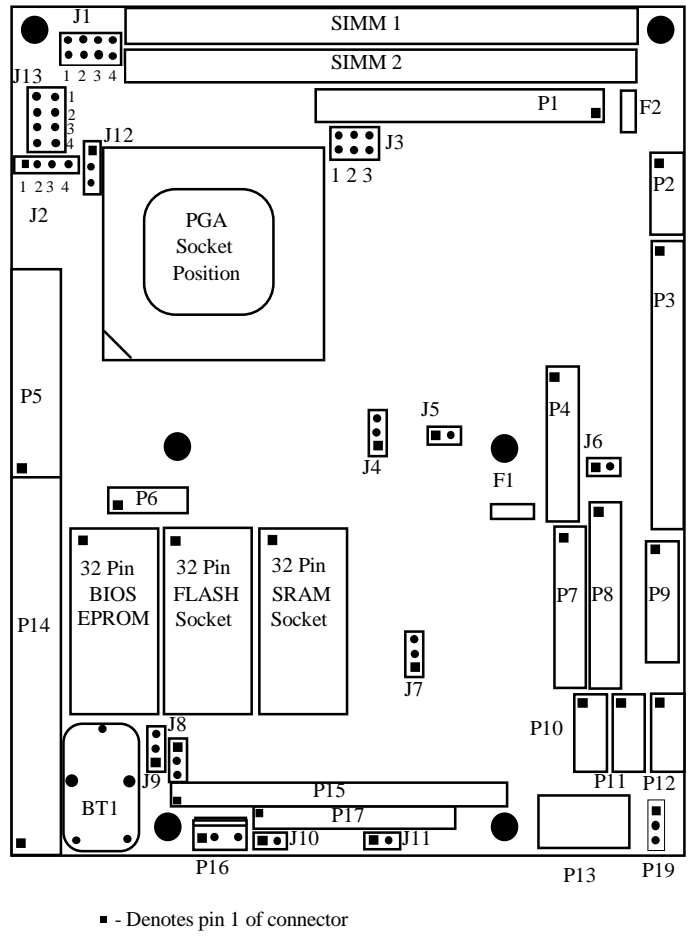
Note: This connector is not fitted as standard.

Pin. N°	Signal
See User Guide	+5 Volts DC (Near to C17 next to the edge of the PCB)
See User Guide	0 Volts (Ground)
See User Guide	0 Volts (Ground)
See User Guide	+12 Volts DC (Not used by APEX II) (Near PC104 mounting hole)

**7.19 P19: Auxiliary Power Connector**

Pin. N°	Signal
1	-5 Volts DC (Not used by APEX II)
2	0 Volts (Ground)
3	-12 Volts DC (Not used by APEX II)

### 8. APPENDIX B : PCB LAYOUT DIAGRAM



Note  
This drawing is not shown to scale.



## 9. APPENDIX C : CONFIGURATION JUMPERS

Jumper	Area of Influence	Link	Action
J1	Selects the frequency of the on board clock which drives the microprocessor. Four links are used numbered 1, 2, 3 and 4. The default state will depend upon the processor fitted. A = Link Absent P = Link Present	<b>1 2 3 4</b> P P P A P A P A A A P A P P A A A P A A P A A A	<b>Processor Freqy.</b> 16 MHz 25 MHz 33 MHz 40 MHz 50 MHz 66 MHz
J2	Selects 486 SX or DX operation Two links are fitted for DX option and one link for SX option	<b>1 2 3 4</b> 1-2 3-4 2 - 3	<b>Processor Type</b> 486 DX 486 SX
J3	Selects the LCD Display type to be interfaced. Three links are used for this numbered 1,2, and 3. Please see Appendix M for more information. A = Link Absent P = Link Present N/A = Not Allowed	<b>1 2 3</b> A A A A A P A P A A P P P A A P A P P P A P P P	<b>Display Type</b> N/A TFT Colour 9/12/18 bits N/A Monochrome Dual Scan N/A STN Colour Dual Scan N/A STN Colour Single Scan
J4	On Board Video Control Selection	1 - 2 2 - 3 None	On board video Disabled On board video Enabled Not Allowed
J5	Power Save Switch (Reserved for Future Use)	Open Link	Do not use Do not use
J6	IDE Ground Link Connects pin 34 of P12 to GND	Open Link	Pin 34 floating Pin 34 shorted to ground
J7	LPT Printer IRQ Selection Selects either LPT1 or LPT2	None 1 - 2 2 - 3	Not allowed IRQ 7 Selected LPT 1 IRQ 5 Selected LPT2
J8	Selects either Internal or External Battery supply	None 1 - 2 2 - 3	Not allowed if CMOS reqd. Selects External Battery Selects Internal Battery
J9	CMOS Battery Clear Either selects to power CMOS or clears the CMOS and SRAM	None 1 - 2 2 - 3	Not allowed Battery Connected Clear CMOS and SRAM
J10	Selects the control mode of serial port 1 P12 if used in RS485 mode	None Link	Full Duplex Selected DTR controls Half Duplex
J11	Selects the control mode of serial port 2 P12 if used in RS485 mode	None Link	Full Duplex Selected DTR controls Half Duplex
J12	Selects Processor Type 3 pins adjacent to J2 (Pin1 at top)	None 1 - 2 2 - 3	Not allowed 486 DX or SX P24T
J13	Selects Processor Voltage 4 pairs of pins adjacent to J2 (Pin 1 at top) A = Link Absent P = Link Present	<b>1 2 3 4</b> A A A A P P P P	<b>CPU Voltage</b> 3V3 5V

## 10. APPENDIX D : INTERRUPT ASSIGNMENTS

Interrupt	Device	APEX II (default)
NMI	Parity Check (generates IOCHCK on error)	Y
0	Timer	Y
1	Keyboard (Output Buffer Full)	Y
2	VGA Controller	Y
3	Serial Port 2 (also 4, 6 & 8 if sharing interrupts)	Y
4	Serial Port 1 (also 3, 5 & 7 if sharing interrupts)	Y
5	Parallel Port 2	N
6	Floppy Diskette Controller	Y
7	Parallel Port 1	Y
8	Real Time Clock	Y
9	Not Assignable	N
10	Unassigned	N
11	Unassigned	N
12	PS/2 Mouse	Y
13	Unassigned	N
14	Hard (Fixed) Disk Controller	Y
15	Unassigned	N

### Notes

Y denotes the Interrupt is used by APEX II

N denotes the Interrupt is free to be used.

## 11. APPENDIX E : DMA ASSIGNMENTS

DMA Channel	8/16 bit Peripherals	Device	APEX (default)
0	8 bit	Available	N
1	8 bit	Available	N
2	8 bit	Diskette Drive	Y
3	8 bit	Available	N
4	16 bit	Cascaded to 1st DMA controller	Y
5	16 bit	Available	N
6	16 bit	Available	N
7	16 bit	Available	N

### Notes

Y denotes the DMA line is used by the APEX II unit

N denotes the DMA line is available for use.

## 12. APPENDIX F : I/O ASSIGNMENTS

Hex Range	Device	Occupied by APEX II (default)
0000 - 001F	DMA Controller 1	Y
0020 - 003F	Interrupt Controller 1, Master	Y
0040 - 005F	Timer & Index registers for UMC491	Y
0060 - 006F	8042 (Keyboard & Mouse)	Y
0070 - 007F	Real Time Clock, NMI Mask	Y
0080 - 008F	POST & DMA Page Register	Y
00A0 - 00BF	Interrupt Controller 2, Slave	Y
00C0 - 00DF	DMA Controller 2	Y
00F0	Clear Maths Coprocessor Busy	Y
00F1	Reset Maths Coprocessor	Y
00F8 - 00FF	Maths Coprocessor	Y
0100 - 010F	Watchdog, E <sup>2</sup> PROM & Byte Wide Socket	Y
01F0 - 01F8	Hard (Fixed) Disk Controller	Y
0200 - 0207	Games port	N
0278 - 027F	Parallel Printer Port 2	N
0208 - 021A	EMS Page registers ( either 208 or 218, etc.)	Y
02E8 - 02EF	Serial Port 4	N
02F8 - 02FF	Serial Port 2	Y
0300 - 0303	PI/O	Y
0360 - 036F	Reserved	N
0378 - 037F	Parallel Printer Port 1	Y
0380 - 038F	SDLC, Bi-synchronous 2	N
03A0 - 03AF	Bi-synchronous 1	N
03B0 - 03DF	Video Adapter	Y
03E8 - 03EF	Serial Port 3	N
03F0 - 03F7	Floppy Diskette Controller	Y
03F8 - 03FF	Serial Port 1	Y

### Notes

Y denotes the I/O assignment is used by APEX II as standard.

N denotes the I/O assignment is free for use.

## 13. APPENDIX G : POWER ON SELF TEST

### 13.1 POST Error Beep Codes

The BIOS performs a **Power On Self Test (POST)** after a reset or reboot. During the POST the microprocessor indicates the status of the test by writing codes to the I/O port at address 80 Hex. If the BIOS cannot find and configure the display controller then the following beep codes will be produced via the speaker drive circuit.

Beeps	Error Messages	Description
1	Refresh Failure	Memory Refresh circuitry faulty.
2	Parity Error	Parity error in the first 64KB of memory.
3	Base 64KB Memory Failure.	Memory failure in the first 64KB.
4	Timer not Operational.	Timer 1 is not functioning. Alternatively, memory in the first 64KB faulty.
5	Processor error.	CPU error.
6	8042 - Gate A20 Failure.	BIOS cannot switch to protected mode.
7	Processor Exception Interrupt Error.	CPU generated an exception interrupt error.
8	Display Memory Read/Write Error.	Video adapter is not responding or its memory is faulty.
9	ROM Checksum Error.	ROM checksum embedded in the ROM does not match the calculated value.
10	CMOS Shutdown Register Read/Write Error.	The shutdown register in the CMOS RAM failed. Check access to CMOS.

#### What to do if the APEX II gives the following beep codes

If the system beeps.....	then.....
1,2 or 3 times	Reseat the SIMMs. If the APEX II still beeps, replace the SIMMs checking the access time.
6 times	Check the keyboard connections. If the beeps persist change the keyboard.
4,5,7,8,9,10 or 11	Contact Blue Chip Technology

## 13.2 POST Error Codes at the POST header

As the BIOS performs the **Power On Self Test (POST)** after a reset or reboot, the microprocessor indicates the status of the test by writing codes to the I/O port at address 80 Hex. The APEX II unit offers on-board decode of this information and can drive an optional POST display without modification. The following codes indicate the progress of the microprocessor during the test.

### Uncompressed INIT code checkpoints

Code (Hex)	Description
C2	NMI is Disabled. Power on delay starting
C5	Power on delay complete. Going to disable cache if any.
C6	Calculating ROM BIOS checksum
C7	ROM BIOS checksum passed. CMOS shutdown register to be tested
C8	CMOS shutdown register test done. CMOS checksum calculation next
CA	CMOS calculation done. CMOS Diagbyte written.
CB	CMOS status register init. done.
CD	BAT command to keyboard controller is to be issued
CE	Keyboard controller BAT result verified.
CF	Initialisation after KB controller BAT done.
D1	Keyboard controller command byte is written.
D2	Checking for pressing of <INS> key during power-on done.
D3	DMA controller #1, #2, interrupt controller #1, #2 disabled. Chipset init./ auto memory detection about to begin.
D4	Chipset init./ auto memory detection over. To uncompressed the RUNTIME code.
D5	RUNTIME code is uncompressed.
DD	Transfer control to uncompressed code in shadow RAM at F000:FFF0

These codes continue overleaf.

**Runtime code is uncompressed in F000 shadow RAM**

03	NMI is Disabled. To check soft reset/power on.
05	Soft reset/power-on determined. Going to disable Cache if any.
06	POST code to be uncompressed
07	POST code is uncompressed. CPU init. and CPU data init. to be done next.
08	CPU and CPU data area init. done. CMOS checksum calc to be done next.
09	CMOS checksum calc done. CMOS Diag byte written. CMOS init. to begin (If "Init. CMOS in every boot" is set)
0A	CMOS init. done (if any). CMOS status reg. about to init. for date/time.
0B	CMOS status register init. done. Any init. before keyboard BAT to be done next.
0C	KB controller I/B free. Going to issue the BAT command to keyboard controller.
0D	Bat command to keyboard controller is issued. Ging to verify the BAT command.
0E	Keyboard controller BAT result verified.
0F	Init. after KB controller BAT done. KB command byte to be written next.
10	KB controller command byte is written. Going to issue PIN-23,24 command.
11	Pin23,24 of keyboard controller is blocked/unblocked. Checking pressing of <INS> key during power-on.
12	Checking for pressing of <INS> key during power-on done. Going to disable DMA and Interrupt controllers
13	DMA controller #1, #2, interrupt controller #1, #2 disabled. Video display is disabled and port B is initialised. Chipset init. about to begin.
15	Chipset initialisation over. 8254 timer test about to start.
19	8254 timer test over. About to start memory refresh test.
1A	Memory refresh line is toggling. Going to check 15 micro second ON/OFF time.
20	Memory Refresh period 30 micro second test complete. Base 64K memory to be initialised.
23	Base 64K memory init. done. Going to set BIOS stack and to do any set-up before Interrupt vector init.
24	Set-up required before interrupt vector init. complete. Interrupt vector initialisation about to begin.
25	Interrupt vector initialisation done. Going to Input port 9042 for turbo switch (if any) and to clear password if post diag switch on.
26	Input port 8042 is read. Going to init. global data for turbo switch.
27	Global data init. for turbo switch is over. Any init. before setting video mode to be done.
28	Init. before setting video mode is complete. Going for monochrome mode and colour mode settings.
2A	Different BUSes init. (system, static, output devices) to start if present.
2B	About to give control for any set-up required before optional video ROM check.
2C	Processing before video ROM control is done. About to look for optional ROM and give control.
2D	Optional video control done. About to give control to do processing after video ROM returns control.

2E	Return from processing after video ROM control. If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. About to do alternate display memory R/W test.
32	Alternate display memory R/W test passed. About to look for the alternative display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power on message.
38	Different BUSES init. to start if present.
39	Display different BUSES init. error messages.
3A	New cursor position read and saved. Going to display the HIT DEL message.
3B	Hit DEL message displayed. Virtual mode memory test about to start.
40	Going to prepare the descriptor tables.
42	Descriptor tables prepared. Going to enter in virtual mode for memory test.
43	Entered in the virtual mode. Going to enable interrupts for dia mode.
44	Interrupts enabled. Going to init. data to check memory wrap around at 0:0
45	Data init. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base memory.
48	Patterns written in base memory. Going to find amount of memory above 1M memory.
49	Amount of memory below 1M memory found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found. Check for soft reset and going to clear memory below 1M for soft reset.
4C	Memory below 1M cleared. Going to clear memory above 1M.
4D	Memory above 1M cleared. Going to save the memory size.
4E	Memory test started. About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing and init. below 1M complete. Going to adjust displayed size for relocation/shadow.
51	Memory size display adjusted. Memory test above 1M to follow.
52	Memory test above 1M complete. Going to save memory size information/
53	Memory size info is saved. CPU registers saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI diable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT..> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.



62	DMA #1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialise 8259 interrupt controller.
67	8259 initialisation over.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started clearing output buffer, checking for struck key. About to issue keyboard reset command.
81	Keyboard reset error/struck key found. About to issue keyboard controller interface test command.
82	Keyboard controller interface test over. About to write command byte and init circular buffer.
83	Command byte written. Global data init done. About to check for lock-key.
84	Lock-key checking over. About to check for memory size mismatch with CMOS.
85	Memory size check done. About to display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. Going to uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8B	First screen message display. <WAIT...> message displayed. About to do Video BIOS shadow.
8C	Video BIOS shadow successful. Setup options programming after CMOS setup about to start.
8D	Setup options are programmed, mouse check and init to be done next.
8E	Mouse check and initialisation complete. Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
94	Hard disk setup complete. To set base and extended memory size.
95	Memory size adjusted due to mouse support. Init if different BUSES optional ROMs from C800 to start. (Please see Appendix-I for details of different BUSES).
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control.
99	Any initialisation required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialisation before coprocessor test.
9C	Required initialisation before coprocessor is over. Going to initialise the coprocessor next.
9D	Coprocessor initialised after coprocessor test.
9E	Initialisation after coprocessor test is complete. Going to check extd keyboard, keyboard ID and num-lock.

A0	Keyboard ID command issued, Keyboard ID flag to be reset.
A1	Keyboard ID flaf reset. Cache memory test to follow.
A2	Cache memory test over. Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Memory wait states programming over. Going to clear the screen and enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialisation required before giving control to optional ROM at E000.
A8	Initialisation before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialisation required after E000 optional ROM control.
AA	Initialisation after E000 optional ROM control is over. Going to display the system configuration.
B0	System configuration is displayed.
B1	Going to copu any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

If you have any difficulty in using this information please call Blue Chip Technology and ask for the Technical Support department.

## 14. APPENDIX H : USING THE DIGITAL PI/O

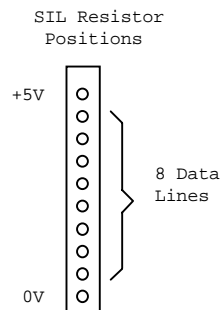
### 14.1 Introduction

This APEX II unit contains one  $\mu$ PD71055 (Intel i8255 look-alike) chip. The device has three, 8 bit ports which can be programmed as inputs or outputs by writing a control word to the control port. Ports A and B must be all input or all output, but Port C may be split into two 4 bit sections each of which may be either inputs or outputs.

### 14.2 Electrical Options

#### 14.2.1 Input/Output Conditioning

The  $\mu$ PD71055 has high impedance inputs. Provision has been made on the PCB to allow resistor SIL packs to terminate the 24 I/O lines. As standard the SIL packs will be fitted for PULL UP termination (+5V). If you need to terminate the I/O lines for PULL DOWN (to 0 Volts) then simply reverse the SIL packs. This is shown below.



For volume orders the SIL packs can be inserted to your specification.

Port A is terminated by SIL pack R2

Port B is terminated by SIL pack R1

Port C is terminated by SIL pack R3

### 14.2.2 Input/Output Connections

A 26 way insulation displacement connector (IDC) is provided (P9 on the APEX II board) for I/O channel signal connection. If access to individual channels is required, a 26 way IDC ribbon cable may be used to connect the I/O channels to screw terminal blocks or other similar output connectors.

### 14.3 Digital I/O Connector Pin Details (P9)

For a complete list of the output pins please refer to the Connectors Appendix A.

### 14.4 APEX II address Ports for the 71055 (8255)

#### 14.4.1 The 4 fixed port addresses

The device occupies 4 read/write addresses in the IBM-PC port map as can be seen below.

Address	Port
Base + 0	Port A
Base + 1	Port B
Base + 2	Port C
Base + 3	Command Port

The BASE Address of the port on the APEX II unit is fixed at 0300 Hex.

#### 14.4.2 Control Bit Operations

The control word controls the way the 71055 is used and programmed. The table below shows how each bit of the word is used.

BIT	FUNCTION	SETTING
Bit 0	Port C (Lower Nibble)	0 = Output 1 = Input
Bit 1	Port B	0 = Output 1 = Input
Bit 2	Mode Selection Ports B & C (Lower)	0 = Mode 0 1 = Mode 1
Bit 3	Port C (Upper Nibble)	0 = Output 1 = Input
Bit 4	Port A	0 = Output 1 = Input
Bit 5,6	Mode Selection Ports A & C (Upper)	00 = Mode 0 01 = Mode 1 1X = Mode 2
Bit 7	Mode Set Flag	0 = Inactive 1 = Active

#### 14.4.4 Commonly Used Control Words

The following table gives a summary of the most commonly used 'control words' which must be written to the control port to configure the 71055 before using this module.

Control Word (Hex)	Control Word Decimal	Sets All of Port A as	Sets All of Port B as	Sets High 4 Bits of Port C as	Sets Low 4 Bits of Port C as
80	128	Output	Output	Output	Output
81	129	Output	Output	Output	Input
82	130	Output	Input	Output	Output
83	131	Output	Input	Output	Input
88	136	Output	Output	Input	Output
89	137	Output	Output	Input	Input
8A	138	Output	Input	Input	Output
8B	139	Output	Input	Input	Input
90	144	Input	Output	Output	Output
91	145	Input	Output	Output	Input
92	146	Input	Input	Output	Output
93	147	Input	Input	Output	Input
98	152	Input	Output	Input	Output
99	153	Input	Output	Input	Input
9A	154	Input	Input	Input	Output
9B	155	Input	Input	Input	Input

### 14.4.5 The 71055's Three Operating Modes

The 71055 can operate in one of three modes (Mode 0-2).

By selecting the correct mode the function of the 70155 can be tailored to suit any application. A more in-depth look at these modes now follows:

#### 14.4.6 Mode 0 Operation

In the first mode (mode 0), the 71055 provides simple I/O for three 8-bit ports. Data is simply written to or read from a specified port (A, B or C) without the use of handshaking.

The Control Code Table in section 4.3 assumes mode 0 is required.

#### 14.4.7 Mode 1 Operation

Mode 1 enables the transfer of data to or from a specified 8-bit port (A or B) in conjunction with strobes or handshaking signals. The C port is used for handshaking and interrupt control signals.

#### 14.4.8 Mode 2 Operation

In mode 2, data is transferred via one bi-directional 8 bit port (A) with 5 lines of handshaking control (Port C).

## 14.5 Programming Guide

### 14.5.1 Reading the Input Lines

The state of the input lines may be determined by using either of the following methods :

(a) Microsoft BASIC A or GW BASIC

```
X = INP (P)
```

Returns the byte from port P and assigns this value to the variable, X.

**(b) 8088/8086 Assembly Language**

```
PORT EQU 0300H

GETDAT :

    MOV DX, PORT
    IN  AL, DX
    RET
```

**14.5.2 Writing to the Output Lines**

The state of the output lines may be modified by using either of the following methods:

**(a) Microsoft BASIC A or GW BASIC**

```
OUT P, D
```

Outputs the byte D to port P.

**(b) 8088/8086 Assembly Language**

```
PORT EQU 0300H

PITDAT :

    MOV DX, PORT
    MOV AX, DATA
    OUT DX, AL
    RET
```

**14.6 Example Program**

The following program written in Microsoft QBASIC will test the operation of the PIO if a loop back connector is fitted.

The loop back connector should loop all bits of port A to all bits of port B and the bottom four bits of port C to the top four bits of port C.

```
REM *** APEX PIO LOOP BACK TEST PROGRAM *****
REM Set base address of PIO
BASEADDR = &H300
REM Set PORT A to OUTPUT, PORT B to INPUT, Low 4 bits
REM of PORT C to OUTPUT, High 4 bits PORT C to INPUT
OUT BASEADDR + 3, &H83
errnum = 0
REM ** First check ports A and B **
outval = 0
errnum = 0
REM output to port A
DO
    OUT BASEADDR, outval
    REM Check the value on port B
    IF INP(BASEADDR + 1) <> outval THEN
        PRINT "PORT A-B Failed"
        outval = 256
        errnum = 1
    ELSE
        outval = outval + 1
    END IF
LOOP UNTIL outval = 256
IF errnum = 0 THEN PRINT "PORT A-B Passed"2

REM ** Now check port C **
outval = 0
errnum = 0
DO
    REM Output to port C
    OUT BASEADDR + 2, outval
    IF (INP(BASEADDR + 2) / 16) <> outval THEN
        PRINT "PORT C Failed"
        outval = 15
        errnum = 1
    ELSE
        outval = outval + 1
    END IF
LOOP UNTIL outval = 15
IF errnum = 0 THEN PRINT "PORT C Passed"
END
```



## 14.7 Application Notes for Interfacing to the 71055 I/O Port

The signals present at ports A, B and C on either the NMOS or CMOS 71055 are TTL (Transistor Transistors Logic) compatible, that is they will interface into standard 74LS logic.

However, TTL has limitations when interfacing to other circuitry.

The following should be considered when attempting to interface to the 71055 I/O Port.

1. The 71055 cannot drive high capacitances.
2. The 71055 cannot sink loads greater than 2.5mA and retain an output voltage that is TTL compatible.
3. The 71055 cannot source loads greater than - 200 $\mu$ A (1-400 $\mu$ A for CMOS version) and retain an output voltage that is TTL compatible.
4. The 71055 cannot interface to any voltage greater than VCC (VDD) + 0.5 Volts or lower than -0.5 Volts
5. The 71055 cannot drive long lengths of cable into other TTL compatible devices. TTL is a standard for on-board interfacing primarily and is too susceptible to interference and noise to be used with long cable runs.

### 14.7.1 General TTL Requirement

<b>LOW</b>	<b>HIGH</b>
Input 0.5 - 0.8V	2.0 - Vcc (VDD)
Output 0 - 0.45V	2.4 - Vcc (VDD)

Characteristics :

DC Parameter	Symbol	82C55/71055	
		MIN	MAX. LIMITS
Input Voltage High	VIH	2.2	VDD+0.3 V
Input Voltage Low	VIL	-0.5 V	0.8 V
Output Voltage High	VOH	3.5	IOH=400 $\mu$ A
Output Voltage Low	VOL	IOL=2.5 mA	0.4V
Input Leakage Current High	ILIH	VI=VDD	10 $\mu$ A
Input Leakage Current Low	ILIL	VI=0V	-10 $\mu$ A
Output Leakage Current High	IL0H	VO=VDD	10 $\mu$ A
Output Leakage Current Low	IL0L	VO = 0V	-10 $\mu$ A
Supply Current (Dynamic)	IDD1	15 mA	
Supply Current (Standby)	IDD2	15 mA	

#### 14.7.2 Glossary Of Terms used

- VIH High level input voltage - the minimum and maximum voltages that can be applied (reference to 0V) for a high to be recognised.
- VIL Low level input voltage - the minimum and maximum voltages that can be applied (reference to 0V) for a low to be recognised.
- VOH High level output voltage - the minimum voltage that will be presented at the output as a high at a given maximum current source current.
- VOL Low level output voltage - the maximum voltage that will be presented at the output as a low at a given maximum current load.

## **15. APPENDIX I : FLASH PROGRAMMING**

### **15.1 Introduction**

Programming the Flash memory on the APEX II CPU card depends on what external peripheral devices you have connected to the unit and the way you want to use the Flash memory. It can be used in its basic form as a form of EPROM in which you program it, and then set it to look like a Bootable Drive. In this mode it can be made to boot and run just like a Boot ROM.

Blue Chip Technology provides all of the necessary files free to enable this type of use and programming with the APEX II CPU board.

The Flash can also be used together with a Flash File System. (We currently use Cardtrick by Datalight which is a licensed software program purchased if required from Blue Chip Technology). This software makes the Flash act like a true disk drive allowing both read and write functions to be performed. As we are currently using CARDTRICK, all of the examples and step by step guides which follow are based around this software.

Please note that the Flash memory found on APEX II will work with other manufacturer's Flash File Software should you wish to use it.

#### **15.1.1 Flash Programming with the APEX II Development Kit.**

Using the APEX II Development Unit (APX-DEV) (which is a complete PC based around the APEX II CPU card) is the most convenient way to test the operation of the Flash device.

The development unit will operate in the same way as a normal desktop PC and comes complete with Disk drives, keyboard, display etc. and all required software. More information is given later in this section on programming with this kit.

### **15.1.2 Flash Programming for your production build.**

When you have proven your application software and want to embed the APEX II board in your production product, you may want to consider the methods of programming of the Flash.

#### **15.1.3 By using the Remote Serial link Option**

The Remote Serial Link has been designed to be as usable as possible and it is possible to configure the APEX II unit even without locally connected keyboard and displays. This will be of great use to those customers that need to re-program/re-configure the APEX II boards once installed into a piece of equipment. The link is made via the normal RS232 COM1 port and runs at 115K Baud. More in-depth programming information is given later in this section.

#### **15.1.4 Buying Pre-programmed APEX II units.**

At Blue Chip Technology we offer a programming service for the APEX II. This is the most cost effective way of programming the production units.

A small charge is made per unit to cover the programming and extra testing time. Please contact the Blue Chip Technology Sales Office if you want to make use of this service.

## **15.2 Remote Disk Connection and Operation**

The remote disk facility allows the APEX II unit to communicate with floppy disk drives through a serial communications link to a PC based host computer running DOS.

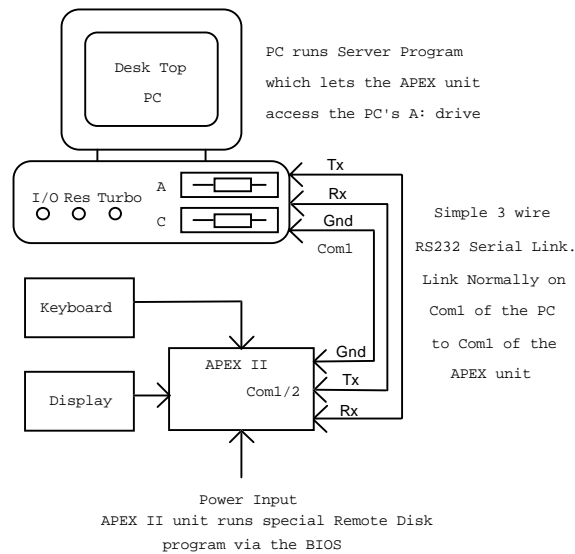
### **15.2.1 Making the Hardware Connection**

The remote disk requires only RX ,TX and ground lines from one of the serial ports to operate correctly.

Connect the RX line from the serial port on the host computer to the TX line on the serial port on the APEX II , and the RX line from the APEX II to the TX

line on the host. The GND line from each connector should also be connected. The following diagram shows this in more detail.

### 15.2.2 APEX II to HOST PC Connection Diagram



### 15.2.3 Making The Software Connection

In order for the host computer to operate as a server, two files are required from the APEX II UTILITIES disk. These are:

- REMSVR.SYS - A Device driver
- SERVER.EXE - A remote disk monitor program

Copy both of these files onto the host computers main disk drive (normally C:).>).

Then add the following entry to the CONFIG.SYS file

```
DEVICE = C:\Dirname\REMSVR.SYS /X
```

Where **X** is either:

- 1 for COM port 1 operation or
- 2 for COM port 2 operation

and "Dirname" is the directory where REMSVR.SYS is located.

Reboot the host computer and run SERVER.EXE - if the device driver is installed correctly, the remote disk status screen will be displayed, if not, check the entry in the CONFIG.SYS file.

#### **15.2.4 Using the Remote Disk**

Connect the APEX II to the host computer and reboot the APEX II unit with the host running the SERVER.EXE program. If all is well the APEX II unit should display:

```
REMOTE DISK INSTALLED
Remote Disk Connected OK
```

just prior to booting.

APEX II will then attempt to boot from the host's floppy disk drive. For the boot to be successful the floppy disk drive must contain a DOS bootable disk. Please note that the serial link operates at 115Kbaud - even so, the data transfer rate is typically only 2 or 3 Kbytes per second which is slow even compared to floppy disks, so please be patient!

#### **WARNING**

The remote disk will only operate correctly with operating systems which rely on the BIOS disk services for disk access - certain operating systems such as Windows which communicate directly with disk hardware will cause the remote disk to hang up. In extreme cases data on the disk can be corrupted.

Blue Chip Technology accept no responsibility for data corrupted in this way, we recommend that the remote disk is used initially to access floppy drives only, where potential damage is less serious. We would also suggest that you make copies of your application disks before attempting to program with this remote link.

The following sections now give detailed information on how to program the on-board Flash memory using the various programming options:

## 15.3 Development Kit Programming

An APEX II Development Kit is a complete standalone PC using an APEX II SBC as the main processing element. It would comprise the following peripheral hardware:

- The APEX II board
- One 3.5" 1.44Mbyte floppy disk drive.
- One IDE Hard disk minimum size 310MBytes.
- One 15 Pin 'D' Type VGA Display Connector
- One 9 Pin 'D' Type connectors for the Serial ports
- One 25 Pin 'D' Type Connector for the Parallel port
- One 25 Pin 'D' Type Connector for the Digital I/O
- One 5 Pin DIN Keyboard Socket
- One 5 Pin DIN Mouse Socket

This would be used with standard PC hardware i.e. VGA display, IBM Keyboard etc.

### Note

MS-DOS should be loaded on to the hard disk. Other software can be supplied on request at extra cost. Please contact the Sales Office for more information.

### 15.3.1 Blue Chip Technology Utilities Software

The APEX II unit comes with a 3½" floppy disk which contains the following Blue Chip Technology files. These programmes will be needed in various forms to enable the Flash to be programmed. For safety, please make a back-up of this disk before using it.

CLRFLASH.EXE	A Program to clear the Flash of all data and format.
PFREMOTE.EXE	This program is used to Program The Flash REMOTE. The APEX BIOS SETUP has this built in.
PROGFLAS.EXE	This program is used to Program the Flash when using an APEX II CPU directly connected to disk drives (e.g. the APEX II Development Kit)

SERVER.EXE	This program is run by a PC acting as a remote SERVER for the APEX unit and is used when programming via a remote serial link.
REMSVR.SYS	A Device driver used by a host PC when running the programme.
SERVER.EXE	The remote disk monitor program.

### 15.3.2 Creating a Read-Only Bootable Disk Drive

To use the Flash as a 1MByte 'EPROM' pseudo device you will need the following :

A 'BOOTAPPS' Disk - This disk is a Bootable DOS disk (see Creating a Bootable Floppy Disk for Flash section) and will contain your application programs.

#### Procedure

1. Reset the APEX II unit (Ctrl, Alt, Del / reset switch or power cycle) and at the prompt.

"Hit DEL to Enter the BIOS SETUP program"

press the 'DEL' Key.

If you miss the prompt reset and try again.

2. Enter the PERIPHERAL section of the Main SETUP Box  
Change / confirm the following :

Remote Disk Option : Disabled  
On-board Flash : Memory Mapped

Save and exit the BIOS Setup screen.

3. From the disk or directory that holds the program PROGFLAS, type:

PROGFLAS Drive: Device

and press Return.



Where "Drive:" is either "A:" or "B:", the drive containing the image for the flash; and "Device" is "0" for the on-board flash or "2" for the DIL flash socket.

This will execute PROGFLAS and set up the link to the Flash memory.

You will be asked to insert into the specified drive a 1.44 MByte floppy disk containing the image for the flash. Note that this must be a bootable floppy disk, and all the data for the flash must be stored on the first 1024 KBytes.

Insert the disk into the drive and press Return.

The PROGFLAS program will now read the disk sector by sector and load it into the FLASH device. This will take about 3 minutes for 1MByte of Flash memory.

Once this has finished the display should state that 2043 sectors have been copied. Note it will not show 2048 sectors copied.

4. Reset the APEX II and at the prompt:

"Hit DEL to Enter the BIOS SETUP program"

press the 'DEL' Key.

If you miss the prompt reset and try again.

5. Enter the PERIPHERAL section of the Main SETUP Box  
Change / confirm the following :-

Remote Disk Option : Disabled  
On-board Flash : Drive A

Save and exit the BIOS Setup screen.

6. If all is well, the APEX II unit inside the Development kit should now boot from the FLASH device and do what ever you have told it to do.

### Notes

At this point you will still be able to access the C: drive on the development equipment but the internal floppy disk drive will not be usable or respond to any commands.

To gain control of the internal floppy disk you will need to disable the on-board Flash.

This is carried out by repeating steps 4 and 5 above. In 5 set  
On-board Flash : Memory Mapped

Because of the way Cardtrick works, if you call up Drive B: then it will look like Drive A:. However, please only use Drive A: as trying to modify Drive B: may cause problems.

## **15.4 Read/Writeable Disk Drive**

To use the flash as a read / write disk drive you need to obtain the following Datalight files. These programs are issued on a 3½" diskette and are not issued as standard. Please contact the Sales Office for information.

CARDMAN.EXE - The program for formatting the flash device.

To set the APEX-II up to use the flash as a read / writeable disk use the following steps:

1. Reset the APEX-II unit and at the prompt:

“Hit DEL to Enter the BIOS SETUP program”

press the ‘DEL’ key.

If you miss the prompt, reset and try again.

2. Enter the PERIPHERAL section of the main SETUP box.  
Change / confirm the following options, dependant on whether you are using the onboard flash or the plug in DIL module:

On-board flash: Disabled, CTRICK A, CTRICK B.

Flash socket: Disabled, CTRICK A, CTRICK B.

The option A or B specifies which drive letter will be allocated for the flash disk.

3. From the disk or directory that holds the program CARDMAN.EXE run it as follows:

Type in CARDMAN and press return.

You will see a small 3 line menu :

F = Format the selected drive  
S = Select drive  
X = Exit

Press the F key and press return,

If you are using the on-board flash or the 1MByte DIL module then enter 1024. If you are using the 2MByte DIL module enter 2048.

Enter a Disk Label if required and press return,

At the prompt enter Y and press return.

After about 30 seconds the display should say:  
"Format Completed Successfully"

Enter X and press return to Exit.

4. If you require to make the flash disk a bootable disk then from the root drive of the PC type:

SYS <drive>

Where <drive> is A : or B: depending on your BIOS setup (see step 1).

5. The system will now allow files to be copied to the flash disk in the same way as to any other DOS drive. When the system is rebooted and if the drive is bootable then the system will boot from the flash drive.

NOTE: Any accesses made to the selected drive will go to the flash disk and not to the physical floppy drive.

6. Go into the application directory.

Using the `COPY *.* A:` command to copy all of the application files into the Flash drive A:

Once completed check that Drive A: contains all the correct information.

Restart the PC and if all is well the PC will boot from the Flash drive A: into your application (if you have set your `autoexec.bat` file to do this.)

Use the AMI BIOS set-up to remove disk drives C: and A: if required. This will speed up the boot up time.

## 15.5 Remote Serial Link Programming with Keyboard & Display

### With a display and keyboard connected to APEX II unit

The Remote Serial Link option is intended to be used when the APEX II SBC does not have any form of local disk drives connected directly to it.

A PC (this could be the APEX II SBC development unit or any standard PC) acts as a host/server to the APEX II thus providing the access to a remote floppy disk drive.

#### 15.5.1 Creating a Read-Only Bootable Disk Drive

Connect the APEX II CPU to the host PC.

This is carried out by using a simple 3 wire twisted link cable i.e. TX on host to RX on APEX II and RX on host to TX on APEX II and the GND pin of each computer linked.

The cable should connect to an RS232 Com port (normally COM1 of the APEX II board and normally to the COM1 port of the host). You can connect to COM2 of the host but make sure that this is reflected in the `CONFIG.SYS` file entry.

Note when using the remote server program "REMSVR.SYS" ensure that no other communication programs try to connect to the port.

In order for the Host PC to operate as a server, two files are required from the APEX II utilities diskette. These are:

- REMSVR.SYS - A Device driver
- SERVER.EXE - The remote disk monitor program

Copy both of these files into a directory of the host PC, and add the following line to the CONFIG.SYS file:

```
DEVICE = DRIVE:\DIRNAME\REMSVR.SYS /1
```

Note

The "/1" tells the PC to communicate via its COM1 port.

For COM2 operation use "/2" at the end.

### 15.5.2 Setup Disk

You now need a Set-up disk formatted and made up as follows:

This disk must be a system disk made by formatting the disk using the command `FORMAT A: /U /S`

Then add the following directories to the disk.

APPS - Holds application data

PROGINFO - Holding the following programming files:

- sys.com - the DOS System.com files
- clrflash.exe - a program to Clear the Flash
- progflas.exe - A flash programming file

When you are prompted to insert a disk please use this disk.

Restart the Host PC and run the SERVER program.

Insert the Set-up disk and press return.

Please note that once the host and APEX II board are communicating, the Server information screen does not have to be currently accessed for the link to carry on.

### 15.5.3 Making a BOOTAPPS Disk

1. Reset the APEX II unit and at the prompt:

"Hit DEL to Enter the BIOS SETUP program"

press the 'DEL' Key.

If you miss the prompt reset and try again.

2. Enter the BIOS setup and access the Peripheral set-up  
Change/confirm the following:

Remote Disk Option : Enabled on COM1

On-board Flash : Memory Mapped

Save and exit from the BIOS Set-up screen.

3. Restart the APEX II unit. As the system boots, look for the messages

Apex II Remote Disk v1.4 installed

Remote disk connected OK

If these appear the Remote Disk has connected correctly and the APEX II will boot from the Host PC's drive A:

If this does not work, please re-check the cable link between the host and APEX II and try again. If it still does not work edit your CONFIG.SYS file only to contain the DEVICE=C:\Dirname\REMSVR.SYS /X line (where X is either 1 or 2).

If you still experience problems please call the Technical Support department at Blue Chip Technology.

4. Once you have an A: prompt showing on the display connected to the APEX II unit, change directory to PROGINFO.

Run CLRFLASH.EXE. You will be told of a successful clearing.

Type PROGFLAS A: and press return to run the program Flash program.

You will be asked to insert into the PC's A: drive a 1.44 MByte floppy disk. Insert the disk into the drive and press return.

The program will now read the disk sector by sector and load it into the Flash device. This will take about 6-8 minutes.

Once this has finished the display should state that 2043 sectors have been copied.

Note

It will **not** show 2048 sectors copied.

5. Reset the APEX II unit and at the prompt:

"Hit DEL to Enter the BIOS SETUP program"

press the 'DEL' Key.

If you miss the prompt reset and try again.

6. Enter the BIOS setup and access the Peripheral set-up Change/confirm the following:

Remote Disk Option : Disabled  
On-board Flash : Enable As Drive A

Save and exit from the BIOS Setup screen.

7. If all is well the APEX II unit should now boot from the Flash device and perform any specified application.

#### **15.5.4 Read/writeable disk drive**

Connect the APEX II CPU to the host PC.

This is carried out by using a simple 3 wire twisted link cable i.e. TX on host to RX on APEX II and RX on host to TX on APEX II and the GND pin of each computer linked.

The cable should connect to an RS232 Com port (normally COM1 of the APEX II board and normally to the COM1 port of the host). You can connect to COM2 of the host but make sure that this is reflected in the CONFIG.SYS file entry.

Note when using the remote server program "REMSVR.SYS" ensure that no other communication programs try to connect to the port.

In order for the Host PC to operate as a server, two files are required from the APEX II utilities diskette. These are:

- REMSVR.SYS - A Device driver
- SERVER.EXE - The remote disk monitor program

Copy both of these files into a directory of the host PC, and add the following line to the CONFIG.SYS file:

```
DEVICE = DRIVE:\DIRNAME\REMSVR.SYS /1
```

#### Note

The "/1" tells the PC to communicate via its COM1 port.  
For COM2 operation use "/2" at the end.

### **15.5.5 Setup Disk for CardTrick Programming**

You now need a SETUP disk formatted and structured as follows:

This disk must be a system disk made by formatting the disk with the command  
FORMAT A:/U/S

Then add the following directories to the disk:

- APPS - To hold application data
- PROGINFO - Holding the following programs:
  - sys.com - the DOS "system.com" file
  - cardman.exe - the Cardtrick main formatting program

When you are prompted to insert a disk please use this disk.

Restart the host PC and run the SERVER program.



Insert the SETUP disk and press return.

Note

1. Once the host and APEX II board are communicating, the Server information screen does not have to be accessed for the link to continue.
2. The file CARDMAN.EXE is found on the CardTrick Utilities Disk, available from Blue Chip Technology. Please contact the Sales office for details.

You now need to make a BOOTAPPS disk as described previously.

1. Reset the APEX II unit and at the prompt:  
"Hit DEL to Enter the BIOS SET-UP program"  
press the 'DEL' Key.  
If you miss the prompt reset and try again.
2. Enter the BIOS setup and access the Peripheral Set-up  
Change/confirm the following:

Remote Disk Option : Enabled on COM1  
Onboard Flash : CTrick B

Save and exit from the BIOS Set-up Screen. This will make the flash device appear as drive B: whilst the remote floppy will appear as drive A:

3. Restart the APEX II unit and it should boot from the HOST PC's drive A:

If this does not work please re-check the cable link between the host and APEX and try again. If it still does not work edit your CONFIG.SYS file to only contain the line:

DEVICE=C:\Dirname\REMSVR.SYS/X  
(where X is either 1 or 2).

If you still experience problems please call the Technical Support department at Blue Chip Technology.

4. From the disk run CARDMAN.EXE as follows:

Type in CARDMAN and press return.



You will see a short 3 line menu:

F = Format the selected drive  
S = Select drive  
X = Exit

Press the F key and press return,

If you are using the on-board flash or the 1MByte DIL module then enter 1024. If you are using the 2MByte DIL module enter 2048.

Enter a Disk Label if required and press return

At the prompt enter Y and press return.

After about 30 seconds the display should say:  
"Format Completed Successfully"

Enter X and press return to Exit.

5. From the PROGINFO directory of the A drive type:

SYS B:        and press return.

This will make the new Flash disk a Bootable drive.

6. Then change the A: directory to APPS

Type in COPY \*.\* B:

This will copy all of your application programs into the Flash drive.

This will take a long time. Assume about 1 minute per 150 KBytes of data.

7. Reset the APEX II unit and at the prompt:

"Hit DEL to Enter the BIOS SETUP program"

press the 'DEL' Key.

If you miss the prompt reset and try again.

8. Enter the BIOS setup and access the Peripheral set-up

Change/confirm the following:

Remote Disk Option : Disabled  
Onboard Flash : CTrick A

Press F1 to save and exit.

Your application should now run from start-up in Flash.

## **15.6 Remote Serial Link Programming without Keyboard or Display**

### **Without a display or keyboard connected to the APEX II unit**

The Remote Terminal Serial Link (RTSL) option is intended to be used when the APEX II unit does not have any form of local disk drives, display or keyboard connected directly to it.

This can be very useful were the APEX II unit is embedded into an application where removal or access is not desirable or not possible.

A PC (this could be the APEX II Development Kit or any standard PC) acts as a host/server to the APEX II unit, thus enabling it to have access to a floppy disk drive remotely.

All display and keyboard information generated by the APEX II unit will be sent through one of its serial COMs links (RS232) and the host PC will run a special terminal program which allows the host PC's display and keyboard to be used as if they were connected to the APEX II unit directly.

As the APEX II unit will only be able to access the floppy disk drive of the host PC, all information that is to be sent to the APEX II board must be via this format.

If your application requires this type of control, please contact the Blue Chip Technical Support department for assistance.

## 15.7 Creating a Bootable Floppy Disk for Flash Programming.

This need only be carried out if you are to use the Flash as a ROM type device using the Blue Chip Technology software.

The program PROGFLAS copies the disk sector by sector from the start of the disk.

Due to the way DOS stores data to a floppy disk, if the disk is not formatted correctly then some of the data needed may reside outside the upper memory boundary of the Flash device. This would cause this data not to be copied to the Flash and so the application stored in the Flash would not be complete.

Therefore it is VERY IMPORTANT that you format the disk to hold the program data in the correct way.

### 15.7.1 Unformatted Disks

1. Format the 1.44 MByte disk on a PC running DOS 5.0 or higher by using the following command:

```
FORMAT A:/S
```

This will create a DOS system bootable disk .

2. Load all of the required information onto the disk via the PC.

#### Note

For a 1Mbyte Flash device you must only use 1MByte of the disk space. If this constraint is not observed then the Flash will not be programmed properly and the application software may not work correctly.

3. Once you have a disk that represents your application, place it into the A drive of your PC and reboot the PC. If all is well the PC will boot from your disk and run your application. If this does not happen then check that you have made the disk up correctly.

### **15.7.2 Previously Formatted Disks**

You MUST re-format the disk using the following command:

```
FORMAT A:/U /S
```

From here follow steps 2 and 3 under “Unformatted Disks” above.

If in doubt, format the disk as for unformatted disks.

## **16. APPENDIX J : SOFTWARE UTILITIES DISKS**

### **16.1 Introduction**

The Software Utilities Disks supplied with the APEX II unit contain all of the software needed to make use of all of the functions contained within the APEX II unit. You should have 3 disks labeled as follows:

Disk 1 - APEX II Software Utilities Disk (SUD)  
Version 1.x

Disk 2 - APEX II Display Drivers  
Disk 1 of 2  
Version 1.x

Disk 3 - APEX II Display Drivers  
Disk 2 of 2  
Version 1.x

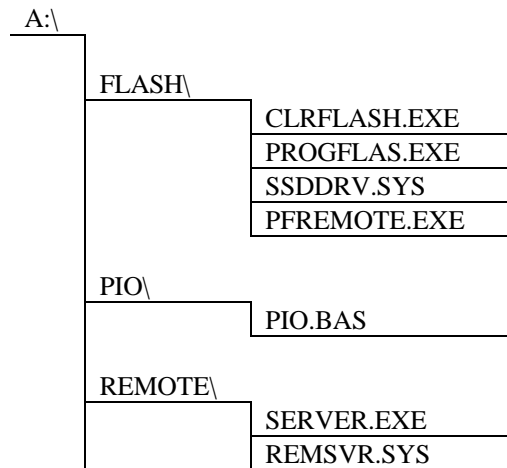
#### **IMPORTANT NOTE**

Please copy all disks NOW to ensure that if you corrupt them you have backups to work from.

In the unlikely event that the disks do become corrupted, please contact the Customer Support Department at Blue Chip Technology for assistance.

## 16.2 APEX II Software Utilities Disk

The APEX II software utilities disk contains the following files in the following directories :



## 16.3 APEX II Screen Drivers

These two disks contain software drivers for the Cirrus Logic 6235 video controller device found on the APEX II unit. The disks should be self-explaining but if you are not sure about any of the files please view the READ.ME file for further assistance. If you are still uncertain, please call the Customer Support department at Blue Chip Technology for assistance.



## **17. APPENDIX K : PERIPHERAL HARDWARE**

### **17.1 Introduction**

The following appendix lists suitable items of hardware that can be connected to the APEX II board. These include items such as connectors, screws and spacer types.

#### **17.1.1 Main I/O Connectors**

All of the main input and output connectors used on this board are of an IDC (Insulation Displacement Connector) type. However, both male and female types are used with some being open pin and some being box type. All of the connectors use the 0.1" pitch standard, so all types are readily available from most connector stockists or a complete overview of the function of the connectors please refer to Appendix A of this manual.

#### **17.1.2 Input Power Connectors**

The two power input connectors used are both based around the standard 3½" and 5¼" disk drive types found on all standard PC drives. Note that only one connector can be fitted at a time, with the 5¼" type being the standard build.

#### **17.1.3 External Battery Connector**

This connector P16 is a standard 0.1" pitch Amp locking type. You can now purchase batteries that are terminated with this type of connector.

#### **17.1.4 LCD Connection Cable and Connectors**

Due to the nature of the non-standard pinouts used by the various LCD manufacturers it is unlikely that you will be able to buy an off-the-shelf cable. Most flat panel displays are designed to use ribbon cable as the method of connection between the display and the controller board.

The connector used on APEX II is a 40 way Female IDC type. We chose a female type so as not to confuse this output with that of the IDE interface which is also a 40 way IDC type. You can purchase suitable IDC male plugs from the following suppliers:

Farnell Electronic Components, R.S Components and Electrospeed

For single shipments above 50 pieces Blue Chip Technology can supply custom made cables to suit the display you wish to use. Please call the Sales Office for more information.

### **17.1.5 Board Mounting Supports and Spacers**

There are six holes provided which can be used to secure the board, and all have a diameter of 3.2mm. However, four of these holes are designed to be used with an additional PC/104 board. If you intend to use extra PC/104 modules then the mounting supports required in these four holes will be different to that used for just the main board alone.

### **17.1.6 Main PCB Spacers/Stand offs**

The two most common type of support are:

Adhesive Backed Supports.  
Metal Screw Spacers.

Each type is available in various heights and can be purchased from most distributors dealing with this type of product. You can also obtain them from:

RS Components and Farnell Electronic Components

### **17.1.7 PC/104 Spacers**

The PC/104 specification calls for a minimum height between boards of 0.6" (15.24mm) and that the spacers used allow for extra PC/104 boards to be added if required. Therefore, we recommend that you use metal screw spacers with a minimum height of 16mm for the four PC/104 holes. These are available from distributors dealing with this type of product and the above listed Catalogue Distributors.

### **17.1.8 Replacement Lithium Battery**

The on-board battery is a PCB mounted Lithium LTC type, and the WARNINGS section of this manual **MUST** be read before attempting to change the battery.

For a replacement please contact our Technical Support department

### **17.1.9 Jumper links**

APEX II uses several jumper link blocks to adjust the operation of the board (see Jumper Appendix). We have included a small number of spares with each unit. If you need a replacement please contact our Technical Support department. They are normally sent free of charge.

### **17.1.10 Microprocessor Heatsink**

If you have purchased the APEX II unit without a microprocessor and intend to fit a 486 version, you must use a processor heatsink on all processors above a 486SX33. Normally the supplier of the microprocessor will be able to assist you in a suitable heatsink.

## **18. APPENDIX L : DOCUMENTATION AND TECHNICAL SUPPORT**

### **18.1 Technical Documentation**

Blue Chip Technology supplies only one copy of this manual to **OEM customers** with each delivery shipment. For non-OEM customers a copy per unit is supplied as standard.

#### **18.1.1 Obtaining further copies of this manual**

If you would like further copies of this manual you can follow one of the three steps listed below:

- a) Order them from Blue Chip Technology at a cost of £25.00 per copy, which includes postage and packing. The part number and revision number for this manual is shown on the inside front page.
- b) Obtain copyright permission from Blue Chip Technology to make extra copies for your customers. Permission is normally granted with a charge of £75.00, once you have asked in writing and we have sent back our acknowledgement.
- c) Obtain copyright permission from Blue Chip Technology to use the source files for this manual. The manuals are produced in Microsoft Word with illustrations using Microsoft Draw. The file is issued on a single 3½" Disk and comes as a zip file. Again permission is normally granted with a charge of £75.00.

### **18.2 Readers Comments**

As indicated in the front of this book, we welcome your comments or suggestions in ways to improve our documentation. Please contact our Technical Support department with any feedback.

## 18.3 Technical Support

Blue Chip Technology provides full technical support for all of its products with full time technical support engineers. Often your suggestions/problems lead to product enhancements as well as solutions for individual problems.

Before you telephone us to ask a question, report a problem or suggest an improvement, please make sure that the answer is not contained within this manual. We endeavour to provide the most accurate manual possible, possibly the answer you require will be contained within this manual.

However, if the answer is not in the manual (or you can't seem to find it) before you call, please make a note of the following items as it will greatly speed up the response process.

1. The product type e.g. APEX II.
2. The serial number and revision issue of the PCB.
3. The BIOS version number.
4. The version number of the title page of this manual.
5. The way the product is configured.
6. The way you are using it and, of course, the problem.

If the problem can be dealt with in writing, please send us a letter or fax, with the information listed above in as much detail as possible and we will contact you within 1 day of receiving your communication.

### 18.3.1 OEM Support for Your Customers

When *your* customer has a problem or technical question, we would prefer that they contact *you* in the first instance. You can then pass on the question to us and keep in touch with your customer's concerns.

It would be helpful if you can ask your customer the same questions as we ask of you so that the problem is dealt with as quickly as possible.

## **18.4 Copying Blue Chip Technology software**

Blue Chip Technology produces custom software, such as the Flash programming suite for use with its products. We only supply one copy of this software to OEM customers and it is free with the first order for that particular product.

If you would like to make copies of Blue Chip Technology software, you can obtain copyright permission from us by asking in writing. We will charge £35.00 for this and issue you with a certificate to state that you can copy the stated software.

## **18.5 Customer Service**

If you need information about deliveries, pricing, or want to change an order please contact our Sales department in the first instance. The Sales department is the centre point of all customer information and it is very important that the information flow is correct.

## **18.6 Faulty Products**

As stated already in this manual, all Blue Chip Technology products carry a 1 year warranty from the date of purchase, subject to Blue Chip Technology's Terms and Conditions.

This warranty applies to the ORIGINAL PURCHASER and not the end user (if supplied by an OEM).

We hope that all of our products, when used correctly, will give long and faithful service, but if you find that one of our products is unsatisfactory, or has been damaged, please let us know immediately.

## **18.7 Faulty Product Returns Procedure**

Please contact the CUSTOMER SUPPORT Department BEFORE sending anything back. They will issue you a Returns Number which must be stated when the product is returned.

When the product is returned please include a note listing the following :

1. The Returns Number
2. The serial number and description of the product.
3. The BIOS version number.
4. The circumstances in which the problem or fault was found including other hardware connected to the returned product and a description of any software being used at the time the problem or fault occurred.
5. The name of the person whom we can contact to clarify the fault.
6. Your company's name, address, phone and fax numbers.
7. The name and address of where the product was being used (optional).

### **18.7.1 Repair Under Warranty**

During the warranty period, all repairs required because of faulty components, workmanship etc. are free. If the product is beyond repair a new board will be issued and a new 1 year warranty will start from the date the new board is despatched.

### **18.7.2 Repairs outside Warranty**

For repairs of a Blue Chip Technology product outside the warranty period please contact the Customer Support department. They will follow the same procedure as detailed above.

We can offer free estimates for the cost of the repair, if required, and we will also indicate how long the repair is likely to take.

## **19. APPENDIX M : FLAT PANEL INTERFACE CONNECTION GUIDE**

### **19.1 Introduction**

The following pages detail the interface connection to a wide range of flat panel displays. The connections are made via the flat panel display header P1. The following information came from the Cirrus Logic CL-GD6235. Applications Book and concentrates on LCD panels of different types and manufactures. The display manufactures are listed in alphabetical order and are correct to the best of Blue Chip Technology's knowledge.

It should also be noted that the PLANAR range of EL panels has been tested and our Video BIOS modified to work correctly with the displays listed. The 6235 BIOS does not work correctly as standard with this type of display.

#### Note

A great number of LCD panels require their power inputs to be "Power Sequenced" to give correct operation of the display. Please read section 19.4 of this Appendix to find out more about the various boards Blue Chip Technology can offer to provide not only the power sequencing, but also the LCD BIAS voltage requirements. The tables make reference to displays that need a power sequence board and to the use of the power sequencing pins when used with the boards listed in section 19.4.



## 19.2 Panel Class Definitions

The connection tables have Panel Definition labels on the line below the panel part number. These definitions are as follows:

C256KSS-18 256K-Colour, Single Scan, 18 bit  
 C4096SS-12 4096-Colour, Single Scan, 12 bit  
 C512SS-9 512-Colour, Single Scan, 9 bit  
 C8DD-16 8-Colour, Dual Panel, Dual Scan, 16 bit  
 C8SSId-8 8-Colour, Single Panel, Single Scan, Interleaved, Dual Clock, 8 bit  
 C8SS-16 8-Colour, Single Panel, Single Scan, 16 bit  
 M2DD-8 Monochrome, 2 Shade, Dual Panel, Dual Scan, 8 bit  
 M2SS-4 Monochrome, 2 Shade, Dual Panel, Dual Scan, 4 bit

## 19.3 Panel Jumper Selection

The APEX II unit has a jumper selection block to select which type of display the APEX II is to control. The following table gives the full information needed.

Panel Class	Supported Panels	Display Type	J3 1	J3 2	J3 3	‡
0	C8SS-16	16-Bit STN	On	On	On	Y
1	M2DD-8	4/6.3 Mhz Monochrome	Off	On	On	Y
2	C8DD-16	Dual-Scan Colour	On	Off	On	Y
3	C256KSS-18 C4096SS-12 C512SS-9	18, 12, & 9 Bit Colour Active Matrix TFT	Off	Off	On	Y

‡ = SimulSCAN™. This lets both a CRT and LCD operate at the same time.

## **19.4 LCD Power Sequencing and BIAS generation.**

Blue Chip Technology has produced an LCD Bias controller board, LCD-PSU.

This board provides the basic Power Sequencing functions needed for all types of LCD display. It provides an LCD BIAS generation circuit producing up to  $\pm 50$  volt, and separate positive and negative contrast voltages. This board is designed to be as small as possible (77 x 64 mm) and would normally fit directly onto the APEX II unit.

A complete description of this board is given in the LCD-PSU manual supplied with the board.

## **19.5 Flat Panel Interface Tables**

The following pages show in more detail the connection to various types of LCD panels from many different suppliers. If the panel you require is not shown please contact Blue Chip Technology for advice.





























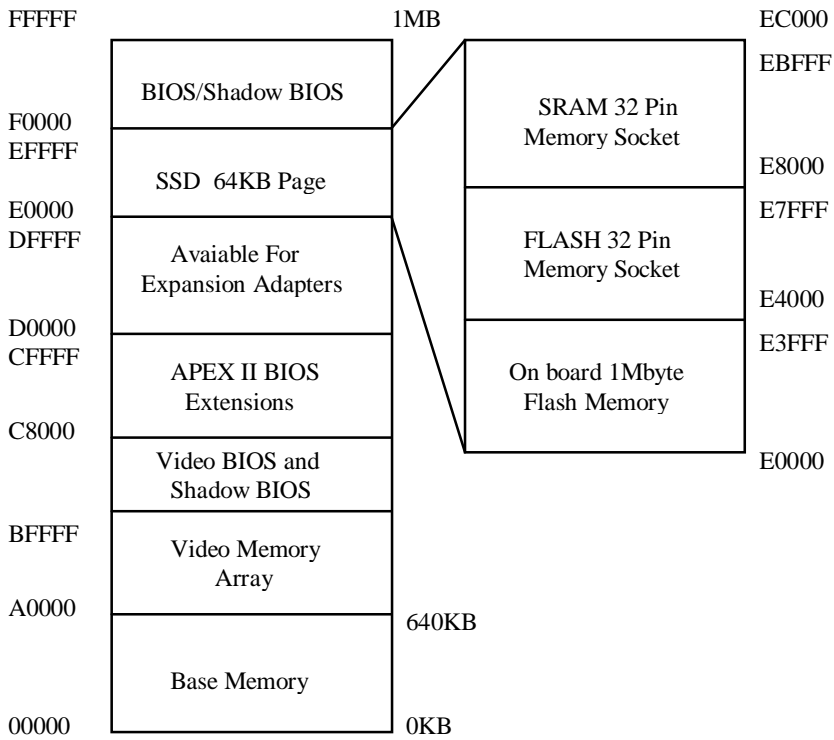






## 20. APPENDIX N : APEX II MEMORY MAP

Below is a typical memory map for an APEX II unit fitted with 1MByte of DRAM.



## 21. APPENDIX O : ELECTROMAGNETIC COMPATIBILITY

This product meets the requirements of the European EMC Directive (89/336/EEC) and is eligible to bear the CE mark.

It has been assessed in a Blue Chip Technology Axis chassis as a representative enclosure for an embedded industrial application. However, because the board is designed to be installed in a variety of enclosures, certain conditions have to be applied to ensure that the compatibility is maintained. It meets the requirements for an industrial environment (Class A product) subject to those conditions.

- The board must be installed in a conductive housing which provides screening suitable for the industrial environment. Avoid holes wherever possible, where they are essential keep them as small as possible. Many small holes are preferable to a few large ones. All covers should be earthed and should not create slots in the housing.
- The board must be securely screwed to the chassis to ensure good contact at the fixing holes. Cutting washers are essential.
- The power supply must be capable of filtering mains-borne transients, and must not create mains interference.
- Most EMC problems are caused by the external cabling to boards. Intermediate connectors at the chassis are recommended rather than connecting external cables direct to the board. This facilitates the screening of the external cables. Keep internal wiring as short and direct as possible. Where practicable run internal cables against the metal chassis.
- It is imperative that any external cabling to the board is totally screened, and that the screen of the cable connects to the metal chassis and hence to earth. This allows the interference to be shunted to earth rather than allowing it inside the chassis and hence onto the board.
- It is recommended that round screened cables with a braided wire screen are used in preference to those with a foil screen and drain wire. Use metal connector shells which connect around the full circumference of the screen; they are far superior to those which earth the screen by a simple "pig-tail".

- The display must be compatible with the EMC requirements.
- The keyboard, if fitted, will play an important part in the compatibility of the processor card since it is a port into the board. A fully compatible keyboard must be used otherwise the keyboard itself may radiate interference or behave as if keys are pressed when subject to external interference. Under these circumstances it may be beneficial to add a ferrite clamp on the keyboard lead as close as possible to the connector. A suitable type is the Chomerics type H8FE-1004-AS.
- Ensure that the screens of any external cables are bonded to a good RF earth at the remote end of the cable.

Failure to observe these recommendations may invalidate the EMC compliance.

**Warning**

This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

### EMC Specification

The card meets the following specification when installed in a suitable representative housing:

Emissions	EN 55022:1995	
	Radiated	Class A
	Conducted	Class A & B
Immunity	EN 50082-2:1995 incorporating:	
	Electrostatic Discharge	IEC 801-2:1991 Performance Criteria A
	Radio Frequency Susceptibility	ENV 50140:1993 Performance Criteria A
	Fast Burst Transients	IEC 801-4:1988 Performance Criteria A

## 22. APPENDIX P : APEX II SUPPORTED CPUS

APEX II currently supports the following CPUs:

AMD:	486DX2/66		
	486DX4/75	486DX4/100	
Intel:	486SX25	486SX33	486SX2/50
	486DX33	486DX2/66	
	P24T/63	P24T/83	
SGS Thompson:	486DX33	486DX2/66	

**NOTE:** APEX II can provide 3.3 or 5 volts to the CPU. If 5 volts is applied to a 3.3 volt CPU then the device, and possibly the APEX II board, could be destroyed. Always check that the jumpers are set correctly.