# APEX 104 CPU
**&**
# APEX 104 CI-2


**User Manual**

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# User Manual

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|---|---|
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| Ci | 07/03/95 | PD | Split and updated |
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# CONTENTS

## Introduction

This manual describes the Blue Chip Technology APEX processor card. There are several versions of the card; these will be identified separately where appropriate. We strongly recommend that you study this manual carefully before attempting to change the configuration. Whilst all necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier to effect any changes. Please be aware that it is possible to create configurations that make booting impossible. If this should happen disconnect the battery for approximately two hours, then reconnect the battery and on power-up the default values will be written into the CMOS. This product uses the Chips & Technologies 82C836 VLSI device, this provides a complete AT compatible environment. For further detailed information on this device please call your supplier.

### WARNING

The devices on this card can be fatally damaged by static electricity. Ensure that you touch a suitable **ground** to discharge any static build up before touching the card. This should be repeated if the handling is for any length of time.

If this product proves to be defective, Blue Chip Technology is only obliged to replace or refund the purchase price at Blue Chip Technology's discretion according to the accompanying terms and conditions of the registration card.

### Limitations of Liability

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# Company Profile

Blue Chip Technology is based in the North West, the purpose built 15,000 sq ft complex contains our research & development facility, engineering workshop, conventional & SMT production lines.

Specialising in the provision of industrial computing and electronic solutions for a wide range of UK and European organisations we have one of the UK's largest portfolios of industrial PC's, peripherals and data acquisition cards. This extensive range of products coupled with our experience and expertise enables Blue Chip Technology to offer an industrial processing solution for any application. APEX is the latest addition to our portfolio, providing a cost effective product development and volume production tool for OEMs.

A unique customisation and specialised system integration service is also available, delivering innovative solutions to customers problems. The company's success and reputation in this area has lead to a number of large design and manufacturing projects for companies such as BNFL, Aston Martin, Jaguar Sport and British Gas.

British Standards Institute approval (**BS5750 Part1, ISO 9001**) means that all of Blue Chip Technology's design and manufacturing procedures are strictly controlled, ensuring the highest levels of quality, reliability and performance.

Blue Chip Technology are committed to the single European market and continue to invest in the latest technology and skills to provide high performance computer and electronic solutions.

# Preface

## The PC as an Embedded Control Solution

As today's OEMs battle to develop leading edge products as fast as possible with minimal cost, the APEX embeded PC system provides a innovative solution. Designed to provide a high performance, compact hardware solution with maximum configuration compatibility and flexibility, APEX is essentially a range of modular building blocks wich allow OEMs to embedd microprocessor control into a wide range of products.

Traditional methods of embedding computer control into products are being challenged by the latest developments in embedded PC technology. This has resulted in a dramatic increase in the number of applications which are using PC as an embedded control solution.

Until recently, the only options were expensive and bulky bus board products such as VME or STE or the resource hungry solution of designing a microcontroller from scratch. By using the APEX processor as a "drop-in" alternative, OEMs can gain clear cut advantages in design, production and product enhancement.

- PC is the best understood hardware interface in the world
- Because the PC is a complete subsystem, design effort is minimised
- Resource can be focused on the application specific features of the target product
- Development resource is reduced, saving time and money
- Access to PC application software enhances product functionality
- A large pool of engineering and programming talent reduces development times
- User familiarity with DOS and Windows interfaces enhances product attractiveness
- Low cost and well understood development tools reduce personnel learning curves
- An off the shelf solution reduces material needs and costs
- Reduced time to market maximises sales and optimises profit window

## The APEX Product Range

The APEX range consists of a processor base and a series of Functional Support Modules which allow highly integrated control systems can be built. All of the products in the range can be plugged into an OEM circuit board, connected via the AT stackthrough bus or plugged into a standard passive backplane.

### Summary of Product Range

APX-3S/4SL Processor

### Functional Support Modules

APX-CI 2 General interface controller

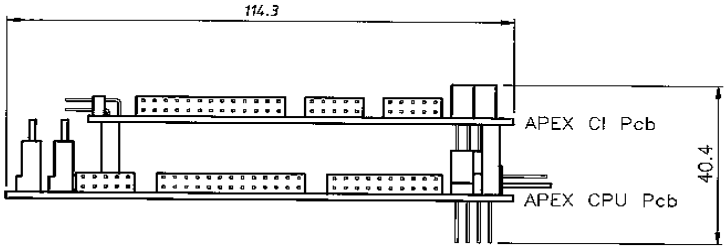
### Other Functional Support Modules

A range of functional support modules have also been designed. Measuring 90mm by 96mm, they provide a wide range of interfaces to the outside world.

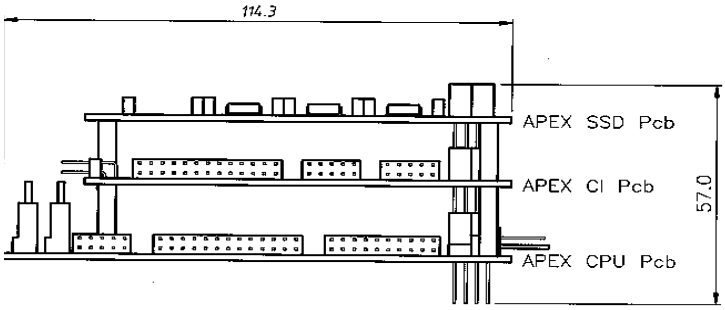
Blue Chip Technology are one of the UK's leading manufacturers of data acquisition and specialised I/O cards. Our unique design and manufacturing capabilities, enable us to provide a customised embedded processing solution, providing you with a range of FSM's tailor made for your needs.

# Typical Configurations of APEX Modules

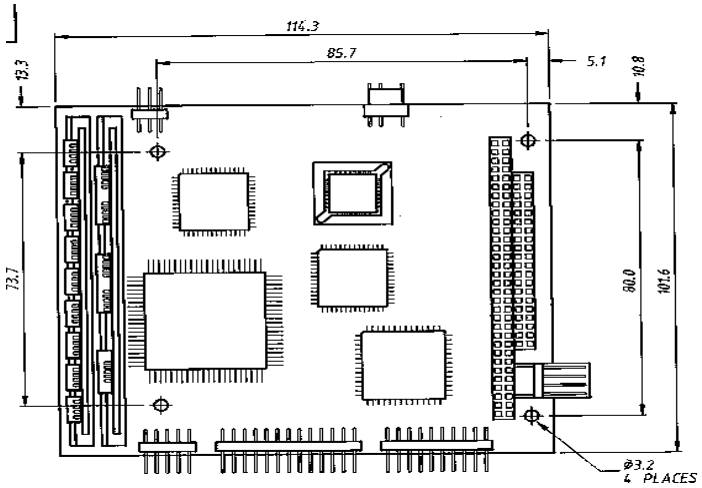
## APEX 104 CPU & CI-2 Stack




## APEX 104 CPU, CI-2 & SSD Stack



## APEX 104 CPU Outline



## Stacking and Embedding the APEX System

Where space and complexity rule out a passive backplane or card cage, APEX modules can be stacked on top of each other to form the complete subsystem. The example below shows how a unit can be configured to allow a fully functional PC with VGA, IDE, 24 channels of programmable I/O and solid state disk capability, to be achieved in a form factor of (100mm x 114mm x 48mm). This allows the APEX to be used as a standalone development tool. By adding a keyboard and monitor, you have a complete PC system which will function exactly the same as your desktop PC.

APEX can also be plugged into a custom built electronic assembly, allowing you to add microprocessor control to any application specific electronic design. Further functionality can be designed in by adding FSM's as required.

## Using the APEX with a Desktop PC

Your desktop PC can be used as a programming tool or emulator to write application specific programmes, debug them, then transfer them to APEX processor. An adapter card (APX-PC) allows all APEX products to be plugged into a standard passive backplane for this purpose. This allows you to develop your software in a known environment and take advantage of existing PC software.

# Specification

The Blue Chip Technology APEX embedded PC is an ultra compact high performance computer that provides 100% IBM PC/AT compatibility.

## On-board Features

- Choice of 25 MHz 80386SX 80486sSLC or 80486SLC2 50MHz microprocessor
- 80387SX coprocessor support (optional)
- Up to 8MB of DRAM memory, supports 256K x 9, 1MB x 9, and 4MB x 9 SIMM modules.
- High performance memory Page Interleave access
- Up to 1MB on board FLASH
- AMI BIOS with built in setup program
- Hardware EMS support (LIM 3.2 & 4.0 compatible)
- PC/104 Compatible
- Selectable Shadow RAM for system & video BIOS
- Selectable Bus speed
- Automatic or Manual Peripheral Configuration.
- 2 Asynchronous serial ports (16C450 compatible) with LC filters - 1 RS232 & 1 RS485
- Uni-directional parallel port
- AT compatible keyboard port
- PS/2 Mouse port
- Customer "sign-on" information held in EEPROM (64 bytes available for user operation)
- Software selectable Watchdog timer
- On-board "Power Good" generation
- Speaker drive circuitry
- 5 Volt only operation
- 6 layer PCB with Surface Mount Technology (SMT)

## Memory Options

| Option | SIMM1 | SIMM2 | Total DRAM |
|---|---|---|---|
| 1 | 256KB | 256KB | 512KB |
| 2 | 1MB | 1MB | 2MB |
| 3 | 4MB | 4MB | 8MB |

Note:

- Bank 0 is made up of two 30 pin standard SIMM carriers.
- All SIMMs must have an access time of 70ns or faster (e.g 60ns).
- Three chip SIMMs are prefered because of their lower power consumption.
- All SIMMs within a Bank **must** be the same, you **cannot** mix 256KB, 1MB and 4MB within the same Bank.
- JP4 selectes between option 1&2 or 3

## Power Requirement (typical)

| Configuration | Current @ 5V |
|---|---|
| APEX 386SX @ 25MHz with 8MBytes of DRAM | 1.2 Amperes |
| APEX 486SLC @ 25MHz with 8MBytes of DRAM | 1.3 Amperes |
| APEX 386SX @ 25MHz with 8MBytes of DRAM + CI | 1.6 Amperes |
| APEX 486SLC @ 25MHz with 8MBytes of DRAM + CI | 1.8 Amperes |
| APEX 486SLC2 @ 50mhz with 8mbytes of DRAM + CI | 2.0 Amperes |

## Environment

Operating Temperature 0°C to 60°C.
Storage Temperature -20°C to 70°C.
Relative Humidity 10-90% non-condensing.

# BIOS

## Introduction

There are several types of Basic Input Output Systems (BIOS) in a PC system.

### System BIOS
This controls the local electronics. It also provides the interface to the hardware for the operating system.

### Video BIOS
This controls the interface between the video hardware and the computer.

### Keyboard BIOS
This controls the keyboard matrix operation and communicates with the PC.

### Adapter
Adapter ROM BIOSes that control specific hardware add-ons.

Each of these BIOSes will now be described :

### System BIOS
The primary function of the System BIOS is to provide a series of software interrupts, functions and subfunctions that perform specific system tasks; such as writing or reading to and from disks and video screens.

The operating system uses the System BIOS as the route to communicate and control the microprocessor and its immediate peripherals. This exchange of data occurs via a strict protocol .

The secondary function of the System BIOS is the series of tests and initialisations that occur after power-on. The results of these operations are written to the POST display (not fitted) as they are completed, thereby indicating its progress.

The System BIOS on the APEX is contained in a 128KB EPROM; of this space the System BIOS occupies 64KB. The EPROM is located at address F0000 hex and continues to FFFFF hex. The supplier of the BIOS is AMI, currently the leading supplier of PC BIOSes in the world. BLUE CHIP TECHNOLOGY have selected this supplier because of their experience, support and committment to future developments in this critical area of a PC/AT design.

### Video BIOS

The Video BIOS acts as an interface between the System BIOS and the video hardware. It is critical that this interface is compatible, fast and reliable. The Video BIOS provides a relatively high level of access to the hardware. The companion APEX-CI 2 provides a video interface and is based on the Cirrus Logic 6235. This device offers proven VGA compatibility in a single device and is able to drive both CRT & LCD displays simultaneously. It is supported by a 512KB of video memory. The Video BIOS coexists in the System BIOS EPROM and locates in the address range C0000 to C7FFF hex. This BIOS is enabled and disabled with J2 on the APEX CPU board(fit to disable).

### Keyboard BIOS

The Keyboard BIOS is contained in the 8042 (or 8742) keyboard controller. This device provides a parallel interface to the microprocessor bus allowing a bi-directional streams of data to be passed between the PC and the keyboard. In addition the Keyboard BIOS handles several of the switch and LED functions on the PC. The BIOS is programmed into the 8042. It occupies none of the memory map.

### Expansion ROMs

APEX and conventional PC hardware allow add-on cards to be inserted on the expansion bus. If software is required to control the electronics on the card the supplier may choose to provide this software in the form of an expansion ROM or adapter ROM. On power-up the PC, once initialised, checks for the presence of ROMs within the memory space of C8000 to DFFFF hex. If present the code within the ROM is run and the specific hardware on the card controlled accordingly. In addition this software can then be used as the interface to the electronics by the operating system; therby acting as an extension to the System BIOS for the new electronics.

## AMI Hi-Flex System BIOS

### Features

- Keyboard Speed Switching
- Memory Detection
- Password Support
- Autodetection of IDE Hard Drive Parameters
- Autodetection of Processor Type and Speed
- Autodetection of Memory Size and Type
- Customisation of the System
- User definable Hard Disk Types
- PS/2 Mouse Support
- Boot Sector Virus Support
- Local Peripheral Support
- Shadow RAM Support
- Keyboard Typematic Rate and Delay
- Num Lock Power-on Status
- Fast Gate A20 Support

### Hot Keys

The Hi-Flex AMIBIOS provides hot keys to switch speed and cache operation. These key operations are:

| | |
|---|---|
| <Ctrl>,<Alt> and <+> | Selects High Speed |
| <Ctrl>,<Alt> and <-> | Selects Low Speed |
| <Ctrl>,<Alt>,<Shift> and <+> | Enables External Cache |
| <Ctrl>,<Alt>,<Shift> and <-> | Disables External Cache |
| <Ctrl>,<Alt> and <DEL> | Causes a Soft Reset |

All keys should be pressed down together.

## AMIBIOS Power-on Self Test

The Hi-Flex AMIBIOS provides all IBM standard POST routines as well as enhanced AMIBIOS routines. All POST checkpoint codes are written to the POST display at I/O location 80 hex (not fitted). See the POST error codes on page 58 for detailed checkpoint codes.

### POST Error Messages and Beep Codes

If the BIOS cannot configure the display controller it will communicate the identification of fatal errors (except error code 8) via a series of beeps. These errors will only occur during power-on tests. The beep codes are as follows:

| Beeps | Error Messages | Description |
|---|---|---|
| 1 | Refresh Failure | Memory Refresh circuitry faulty. |
| 2 | Parity Error | Parity error in the first 64KB of memory. |
| 3 | Base 64KB Memory Failure. | Memory failure in the first 64KB. |
| 4 | Timer not Operational. | Timer 1 is not functioning. Alternatively, memory in the first 64KB faulty. |
| 5 | Processor error. | CPU error. |
| 6 | 8042 - Gate A20 Failure. | BIOS cannot switch to protected mode. |
| 7 | Processor Exception Interrupt Error. | CPU generated an exception interrupt error. |
| 8 | Display Memory Read/Write Error. | Video adapter is not responding or its memory is faulty. |
| 9 | ROM Checksum Error. | ROM checksum embedded in the ROM does not match the calculated value. |
| 10 | CMOS Shutdown Register Read/Write Error. | The shutdown register in the CMOS RAM failed. Check access to CMOS. |

## AMIBIOS Setup

The Hi-Flex AMIBIOS Setup utility is divided into five parts:

## Standard CMOS Setup

The Hi-Flex AMIBIOS Standard CMOS Setup permits the user to configure and set system components such as floppy drives, hard disk drives, time and date, monitor type and keyboard. These options are discussed on page 20.

## Advanced CMOS Setup

The Advanced CMOS Setup allows the user to configure more advanced parts of memory operation and peripheral support. These options are discussed on page 22.

## Advanced Chipset Setup

The Advanced Chipset configures the C&T SCATSX specific features and is discussed further on page 26.

## Peripheral Setup

The Peripheral Setup configures the APEX-CI 2 companion card's floppy, IDE, serials and parallel devices. These are all controlled by the C&T 82C711 device. These options are discussed further on page 31.

## Utilities

The AMIBIOS provides support for Password security access. This will be discussed further on page 33.

## Running the AMIBIOS Setup

The system parameters (such as amount of memory,disk drives, video displays and numeric coprocessors) are stored in CMOS RAM. When the APEX is turned off, a back-up is provided by an external battery (3.7V Lithium) connected to P5.

Each time the APEX is powered-on, it is configured with these values, unless the CMOS RAM has been corrupted. The AMIBIOS Setup resides in the ROM BIOS and is available each time the APEX is switched on.

If, for some reason, the CMOS RAM becomes corrupted, the system is reconfigured with the default values stored in the System BIOS. There are two sets of BIOS values stored in the BIOS: the BIOS default values and the Power-On default values.

## Accessing Setup

Setup is accessed by pressing the 'DEL' key on the keyboard when the screen displays the message:

Hit <DEL> if you want to run Setup

If you press 'DEL' too late, reset the APEX and try again.

## Setup Key Use

| Keystroke | Action |
|---|---|
| Esc | Returns to the previous screen. |
| →,←,↑ and ↓ | Move the cursor from one option to the next. |
| <PgUp> and <PgDn>, <Ctrl><PgUp>, <Ctrl><PgDn> | Modify the default value of the options for the highlighted parameter. If there are fewer than 10 options, <Ctrl><PgUp> and <Ctrl><PgDn> operate like <PgUp> and <PgDn>. <Ctrl> can also be used to increment a setting. |
| <F1> | Displays help. |
| <F2> | Changes background colours. |
| <F3> | Changes foreground colours. |
| <F5> | Restores the values resident when the current Setup session began. These values are taken from the CMOS RAM if it was uncorrupted at the start of the session. Otherwise, the AMIBIOS Setup default values are used. |
| <F6> | Loads all features in the Advanced CMOS Setup/Advanced Chipset Setup with the AMIBIOS Setup defaults. |
| <F7> | Loads all features in the Advanced CMOS Setup/Advanced Chipset with the Power-On defaults. |
| <F10> | Saves all the changes made to Setup and continues the boot process. |

The APEX AMIBIOS Setup main Menu is shown below. The options are selected by using the ↑ and ↓ keys and then pressing <Enter> .

**AMIBIOS SETUP PROGRAM - BIOS SETUP UTILITIES**
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STANDARD CMOS SETUP
ADVANCED CMOS SETUP
ADVANCED CHIP SET SETUP
PERIPHERAL SETUP
AUTO CONFIGURATION WITH DEFAULTS
CHANGE PASSWORD
AUTO DETECT HARD DISK
WRITE TO CMOS AND EXIT
DO NOT WRITE TO CMOS AND EXIT

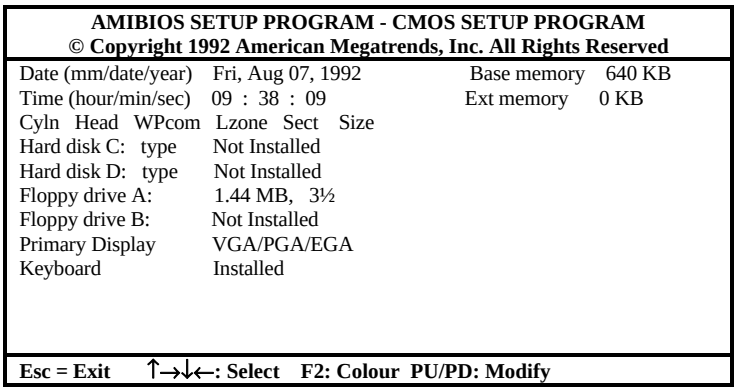
Standard CMOS Setup for changing time, Date, Hard Disk Type, etc.

Each option is described in detail on the pages identified as follows:

| Main Menu Option | Described on Page |
|---|---|
| STANDARD CMOS SETUP | 20 |
| ADVANCED CMOS SETUP | 22 |
| ADVANCED CHIP SET SETUP | 26 |
| CI2 PERIPHERAL SETUP | 31 |
| AUTO CONFIGURATION WITH DEFAULTS | 33 |
| CHANGE PASSWORD | 33 |
| AUTO DETECT HARD DISK | 34 |
| WRITE TO CMOS AND EXIT | 35 |
| DO NOT WRITE TO CMOS AND EXIT | 35 |

## Using the CMOS Setup Program

The default condition for the CMOS Setup Menu is as shown below. This menu sets the basic system parameters, such as date, time, floppy disk and hard disk types. By using the ←↑↓→ keys you can select the parameter to be changed. Once positioned on the parameter to be modified the <PgUp> and <PgDn> keys rotate the available options. The value selected when the menu is exited is the one that will be written to CMOS, should you decide to commit your changes to CMOS.



### Date

This entry allows you to set the Date, Month and Year. Ranges for each value are shown in the lower left corner of the CMOS Setup Screen.

### Time

This entry allows you to set the Hours, Minutes and Seconds. The clock operates in 24 hour mode; that means that for a PM time add 12 to the hour e.g. enter 6:35 PM as 18:35:00.

### Floppy Disk Configuration

The APEX supports None, 360KB, 720KB, 1.2MB, 1.44MB & 2.88MB drives. Two drives are supported A: and B:.

### Hard Disk Configuration

Two hard disk drives are supported directly by the BIOS C: and D:. Each drive can select drive types 1 to 46. In addition type 47 is user definable allowing all parameters for the drive to be customised. Both drives can be set to a different type 47 if required. To set the values for type 47 use the ←,↑,↓ and → keys to select the appropriate field and then type in as required. A complete list of the 46 hard disk type is contained in the APEX-CI 2 manual.

### Display

This entry allows the user to select MDA™, CGA™ or EGA/PGA/VGA display controllers. If your system is to operate without a display then select Disabled. Failure to do this will result in an error being generated during the power-on diagnostics check.

### Keyboard

The APEX keyboard interface is AT compatible. It can be connected to either AT or PS/2 keyboards. The default setting is Enabled. If your system is to operate without a keyboard then select Disabled. Failure to do this will result in an error being generate during *the power-on diagnostics check.*

## Using the Advanced CMOS Setup

The default condition for the Advanced CMOS Setup Menu is as shown below. By using the ←↑↓→ keys you can select the parameter to be changed. Once positioned on the parameter to be modified the <PgUp> and <PgDn> keys rotate the available options. The value selected when the menu is exited is the one that will be written to CMOS, should you decide to commit your changes to CMOS.

**AMIBIOS SETUP PROGRAM - ADVANCED CMOS SETUP**
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| | | | |
|---|---|---|---|
| Typematic Programming | : | Video ROM Shadow C000, 32K | : Enabled |
| Typematic Rate Delay | Disabled | Adaptor ROM Shadow C800, 16K | : Disabled |
| Typematic Rate (Chars/sec) | : 500 | Adaptor ROM Shadow D000, 16K | : Disabled |
| Mouse Support Option | : 15.0 | Adaptor ROM Shadow D800, 16K | : Disabled |
| Above 1 MB Memory Test | : | Adaptor ROM Shadow E000, 16K | : Disabled |
| Memory Parity Error Check | Disabled | Adaptor ROM Shadow E800, 16K | : Disabled |
| Hit <DEL> Message Display | : Enabled | System ROM Shadow F000, 64K | : Enabled |
| Hard Disk Type 47 RAM Area | : Enabled | Boot Sector Virus Protection | : Disabled |
| Wait for <F1> If Any Error | : Enabled | | |
| System Boot Up Num Lock | : 0:300h | | |
| Floppy Drive Seek At Boot | : Enabled | | |
| System Boot Up Sequence | : On | | |
| System Boot Up CPU Speed | : Enabled | | |
| Fast Gate A20 Option | : A:, C: | | |
| Password Checking Option | : High | | |
| | : Enabled | | |
| | : | | |
| | Enabled: | | |

Esc = Exit ↑→↓←: Select (Ctrl) Pu/Pd: Modify F1: Help F2: Colour

F5: Old Values F6: BIOS Setup Defaults F7: Power-on Defaults

### Help Screens

Help can be invoked at any time by pressing <F1>.

### Typematic Rate, Delay and Programming

The control of Typematic rate Programming allows the auto repeat and delay before repeat to be selected. The defaults are as shown above. The Typematic Rate Delay describes the delay before auto repeat starts. The Typematic Rate is the frequency of the key generation once in auto repeat.

### Mouse Support Option

This enables or disables the mouse support. The mouse control is effected by the 8042 keyboard controller on the APEX. It is PS/2 compatible.

### Above 1MB Memory Test

By enabling this test any RAM above 1MB will be exercised by the POST diagnostics thereby taking longer to boot. If your APEX is not fitted with more than 1MB of RAM or you wish to shorten the boot time set this option to disabled.

### Memory Parity Error Check

This option selects whether the parity circuit is active on the system RAM. We strongly recommend that this is set to enabled at all times thereby providing communication of any RAM corruption. If this option is not required select disabled.

### Hit <DEL> Message Display

Disabling this option removes this message from appearing during power-up. This may be required when you do not wish to draw attention to existence of the Setup Menus within the BIOS. The default is enabled.

### Hard Disk Type 47 RAM Area

As described in the CMOS Setup details previously the AMIBIOS supports type 47 user definable input. This data is stored at either:

0:300h in lower system RAM
or
Top 1KB of applications memory

The information will be stored in shadow RAM if shadowing is enabled.

### Wait for <F1> If any Error

If any of the tests run during the POST cause an error then this message will be displayed. If this message is enabled then after displaying it the APEX will halt waiting for <F1> to be pressed. If you expect errors during the POST or do not wish the boot to be halted if any error occurs then disable this option.

### System Boot Up Num Lock

If you wish the numeric keypad to be active after a boot then select ON. If, however, you wish the ←,↑,↓ and → keys instead after power-up then set the option to OFF.

### Floppy Drive Seek at Boot

If enabled, a seek is performed on floppy drive A: at system boot time. The options are Enabled or Disabled. By disabling this option the boot time can be reduced. If very old 360KB drives are used it may be necessary to enable this option to ensure that the heads are recalibrated before the drive is accessed.

### System Boot Up Sequence

The default boot sequence is drive A: and then C:. This would mean that if drive A: is not ready then the boot occurs from C:. The alternative is to boot from drive C: and then A: if C: is not ready. Hence the settings are either: A:, C: or C:, A:.

### System Boot Up CPU Speed

The Setup allows the selection of the CPU at boot time. The default is High speed. The alternative is Low.

### Fast Gate A20 Option

Gate A20 controls the method of accessing memory addresses above 1 MB by enabling or disabling access to the processor line A20. To provide XT compatibility address line A20 must always be low and therefore the option should be Disabled. However, some applications both enter protected mode and shut down through the BIOS. For this software, Gate A20 must be constantly enabled and disabled via the keyboard controller (8042), which slows down the processing.

Fast Gate A20 is another method for handling Gate A20 using the SCATsx internal circuitry. It speeds programs that constantly change from addressing conventional memory to addressing memory addresses above 1MB (from real mode to protected mode and back). Network operating systems in particular benefit from this enhanced circuitry.
The Default is Fast Gate A20 enabled.

### Password Checking Option

This option enables a password check every time the systems boots or Setup is executed. The settings are Always or Setup. If Always is selected the user password prompt appears every time the system is turned on. If Setup (the default) is chosen, the password prompt appears if Setup is executed.

### ROM Shadow

ROM shadow is a technique in which the BIOS code is copied from slower ROM to faster RAM. The BIOS is then executed from the RAM.

For each of the areas of memory identified in the Setup table the option is there to Enable or Disable shadowing for that particular area. The default is that both the Video and System areas are shadowed. Care must be taken where expansion cards are occupying an area that is set for shadowing. If the expansion card has its own internal RAM located at the address that is shadowed then its operation

will be corrupted (examples are network cards). For such cards the setting should be Disabled.

### Boot Sector Virus Protection

When enabled, the BIOS issues a warning when any program or Virus issues a Disk Format command or attempts to write to the boot sector of the hard disk. The settings are Enabled or Disabled.

### Using the Advanced Chipset

The default condition for the Advanced Chipset Setup Menu is as shown below. By using the ←↑↓→ keys you can select the parameter to be changed. Once positioned on the parameter to be modified the <PgUp> and <PgDn> keys rotate the available options. The value selected when the menu is exited is the one that will be written to CMOS, should you decide to commit your changes to CMOS.

**AMIBIOS SETUP PROGRAM - ADVANCED CHIPSET SETUP**
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| | |
|---|---|
| Low CPU Speed | : CXIN/4 |
| Early Ready Mode | : Enabled |
| Bus Clock Speed Select | : CXIN/4 |
| DMA Clock Select | : B/2 |
| Coprocessor Ready Control | : 82C836 |
| Additional RAM Wait State | : Enabled |
| RAS Timeout Feature | : Disabled |
| Video Controller | : Internal |
| Extended Boundary | : None |
| Global EMS | : Disabled |
| EMS I/O Port Access | : Enabled |
| EMS Page Register | : EMS0 |
| Hidden Refresh | : Disabled |
| Refresh On Idle | : Disabled |
| AT Refresh Disable | : No |
| Video BIOS Area Cache (32K) | : Disabled |
| F000 BIOS Area Cache (64K) | : Disabled |

Esc = Exit ↑→↓←: Select (Ctrl) Pu/Pd: Modify F1: Help F2: Colour

F5: Old Values F6: BIOS Setup Defaults F7: Power-on Defaults

### Low CPU Speed

Selects the fraction of the main oscillator frequency to be used for the Low CPU speed. Default is CXIN/4 which for a 25MHz APEX would be: 50MHz / 4 = 12.5mhz operation.

### Early Ready Mode

When enabled allows external devices to assert READY during the first T2 after T1 state to terminate the memory cycle after only two T-states. The default is Enabled.

### Bus Clock Speed Select

The actual Bus Clock Speed is set by this option. The AT standard is 8MHz. We advise a frequency as close to this as possible. However, for applications where the other cards on the backplane are capable of working at a higher speed this option is available. The formula is: CXIN (twice the processor speed) / the setting.

Therefore for a 25MHz APEX: 50MHz / 6 (default) = 8.33MHz.

### DMA Clock Select

The speed of the DMA clock is set by this option. The options are Bus Clock Speed (see above) or Bus Clock Speed/2. We recommend that B/2 is set unless you are sure that your additional cards can operate at the full bus speed.

### Additional RAM Wait State

The Setup allows the RAM to operate with either 0 or 1 wait state. The default is 1 wait state. For improved performance this can be reduced to 0 wait state.

### RAS Timeout Feature

This option is provided to support DRAM that allow a maximum RAS active time of 10 microseconds. If the timeout is Enabled the RAS is not allowed to remain low for more than 9.5 microseconds. With this option disabled the maximum RAS active time is about 15 microseconds, limited by the refresh cycle time.The default setting is Disabled.

### Extended Boundary

This option defines the upper limit of available memory. The options are:

No Limit, 1MB, 1.25MB, 1.5MB, 2MB, 3MB, 4MB, 5MB, 7MB, 8MB, 9MB, 10MB, 11MB, 12MB, 13MB, 15MB.

### Global EMS

This option is used to select whether the EMS hardware is to be operational. If the setting is Disabled then the following EMS setting is ignored. The default is Disabled.

### EMS I/O Port Access

This setting again enables or disables the use of the EMS memory. If you wish to use EMS select enabled. This is the default.

### EMS Page Register

The EMS registers are accessed using three I/O ports. These ports are located at either 208h-20Ah or 218h-21Ah.

This setting selects which block of addresses are used.

Setting EMS0 would enable 208h-20Ah
Setting EMS1 would enable 218h-21Ah

The default is EMS0.

### Hidden Refresh

Enabling this option can improve the APEX performance. However, some applications may not function correctly in this mode. The default is Disabled.

### Refresh On Idle

Enabling this option can improve the APEX performance. However, some applications may not function correctly in this mode. The default is Disabled.

### AT Refresh Disable

The default is No. This option allows the Refresh signal on the AT Bus to be disabled. It should be remembered that some add-on memory cards rely on the bus Refresh signal to maintain their RAM validity.

### Video BIOS Area Cache (32K)

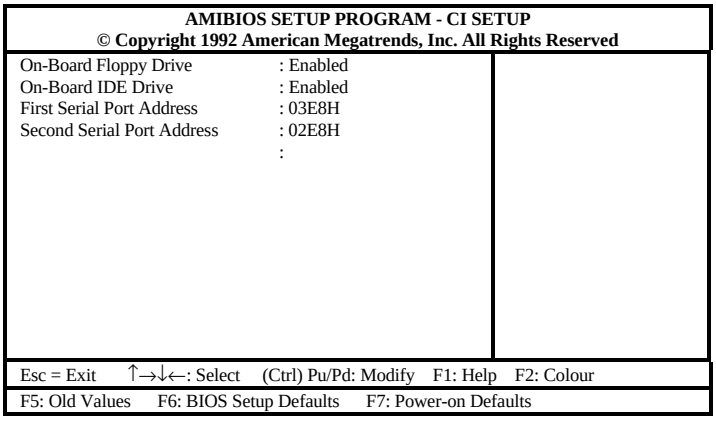
This option enables the caching of the video BIOS.

### F000 BIOS Area Cache (64K)

The default is Disabled. We recommend that this setting is not changed.

## Using the Peripheral Setup

The default condition for the Peripheral Setup Menu is as shown below. By using the ←↑↓→ keys you can select the parameter to be changed. Once positioned on the parameter to be modified the <PgUp> and <PgDn> keys rotate the available options. The value selected when the menu is exited is the one that will be written to CMOS, should you decide to commit your changes to CMOS.




## On-Board Floppy Drive

This option enables the floppy controller on the APEX-CI 2. This setting can either be Enabled or Disabled. The default is Enabled.

### On-Board IDE Drive

This option enables the IDE controller on the APEX-CI 2. This setting can either be Enabled or Disabled. The default is Enabled.

### First Serial Port Address

This option allows the first serial port address on the APEX-CI 2 to be configured as either:

03F8h (Com1), 02F8h (Com2), 03E8h (Com3), or Disabled
Default = 03E8H (Com3)

The interrupt selection will be made automatically to:

Com1 and 3 will be Interrupt 4
Com 2 will be Interrupt 3
Disabled will remove the Interrupt connection.

### Second Serial Port Address

This option allows the second serial port address on the APEX-CI 2 to be configured as either:

03F8h (Com1), 02F8h (Com2), 02E8h (Com4) or Disabled
Default = 02E8H (Com4)

The interrupt selection will be made automatically to:

Com1 will be Interrupt 4
Com 2 and 4 will be Interrupt 3
Disabled will remove the Interrupt connection.

### Auto Configuration with Defaults

By selecting this option you automatically configure the system using the default values. These values are worst case values for system performance, but are the most stable values in the harsh conditions where we expect our products to be used. If you experience any erratic problems with APEX we strongly suggest that you configure with default values and test the system again.

### Change Passwords

The Hi-Flex AMIBIOS has an optional password feature. The system can be configured so that you have to enter a password every time the system boots or when the AMIBIOS Setup is executed.

### Bypassing Password Support

You can bypass the password support by pressing <Enter> when the password prompt appears.

### Enabling Password Support

The password check option is enabled in Advanced CMOS Setup by choosing either Always or Setup. The password, which can be up to 6 characters in length, is stored in CMOS RAM.

### If a Password is Used

You must type correctly the current password when

'enter CURRENT Password'

appears. After the current password has been correctly entered, the user is asked to retype it.

If the password information is incorrect, an error message appears. If the new password confirmation is entered without error, the end user presses <Esc> to return to the Main Setup Menu.

### Password Storage

The password is stored in CMOS RAM after Setup completes. The next time the systems boots, you must enter the password if the password function is present and has been enabled.

### Password Options Control Prompt

Enter CURRENT Password

appears if the Password Option is enabled.

When and if the prompt appears is dependent upon the options chosen in the Advanced CMOS Setup. If Always was set the prompt appears every time the system is powered on. If Setup was set the prompt will not appear when the system is powered on, but is displayed when Setup is run.

### Using a Password

You should keep a record of the new password when the password is changed. If you forget the password and password protection is enabled; the only way to boot the system will be to disable the CMOS RAM. This is achieved on the APEX by removing the battery for approximately two hours to allow the CMOS RAM to clear. After this time reconnect the battery. On power-up the CMOS RAM will be
loaded with default values. Obviously, all previous settings will be lost so it is important that you keep a record of any changes you make to any of the Setup screens each time a new configuration is created so that this information will not be lost forever.

### Auto Detect Hard Disk

This option detects the hard disk parameters for non-standard hard disk drives with RLL, ESDI, IDE or SCSI interfaces. It displays the parameters that it detects and allow the you to accept or reject the parameters. If accepted, these parameters are displayed for the hard disk drive in Standard CMOS Setup. Please note that when an Auto Detect is run on a drive that is not present (drive D: in most systems) then there will be a delay before the test is completed.

### Write to CMOS and Exit

The configuration settings in Standard Setup, Advanced CMOS Setup, Advanced Chipset Setup, Peripheral Setup, Password and AutoDetect Hard Disk are stored in the CMOS RAM when this option is selected. A CMOS RAM checksum is calculated and written to CMOS RAM; control is then passed to the BIOS. You are asked to confirm or deny the action by entering either <Y> or <N>. Press <Y> and <Enter> to save the new system parameters and continue the boot process. Press <N> and <Enter> to return to the Main Menu.

### Do Not Write to CMOS and Exit

This option passes control to the ROM BIOS without writing any changes to the CMOS RAM. Press <Y> and <Enter> to continue the boot process without saving any system parameters changed in Setup. Press <N> and <Enter> to return to the Main Menu.

In addition to the AMI BIOS Setup Utility there is an APEX extended setup option. This option allows the user to configure further Apex 104 CPU and CI2 options. It is invoked by pressing the DEL key after the display message

Hit [DEL] now to run APEX Extended SETUP

The options are selected using the curser key and toggled using thePGUP and PGDN keys.
The Extended setup options are as follows:

**Apex 104 Com1 port :Enabled**
**Apex 104 Com2 port :Enabled**
**Apex 104 LPT port :Enabled**
**CI2 PIO port :Disabled**
**CI2 Com port 1 mode :RS232**
**CI2 Com port 2 mode :RS232**
**Remote disk :Disabled**
**Onboard Flash :Disabled**
**Sign on message :**

**Apex 104 Com1 port**
This option allows the first serial port on the APEX CPU to be enabled ( 03f8h ) or disabled
Interrupt 4 will be assigned to Com1 if the port is enabled

**Apex 104 Com2 port**
This option allows the second serial port on the APEX CPU to be enabled ( 02f8h ) or disabled
Interrupt 3 will be assigned to Com2 if the port is enabled

**Apex 104 LPT1 port**
This option allows the parallel port on the APEX CPU to be enabled ( 0378h ) or disabled
Interrupt 7 will be assigned to LPT1 if the port is enabled

**CI2 PIO port**
This option configures the base address for the CI2 8255 PIO chip. the available options are

IO address 0200h
IO address 0300h
Disabled

**CI2 Com port 1 mode**
This option configures the output drivers for the first serial port on the CI2 card
The available options are:

RS232
RS485/Full Duplex
RS485/Half Duplex

**CI2 Com port 2 mode**
This option configures the output drivers for the second serial port on the CI2 card
The available options are:

RS232
RS485/Full Duplex
RS485/Half Duplex

**Remote Disk**
This option configures the system to boot from a remote disk over the serial port. See the section on REMOTE DISK for a full description of this option.

**Onboard FLASH**
This option configures the flash to be either enabled, memory mapped or disabled. See the section
on FLASH DISK for a full description on the use of this option.

**Sign on message**
This facility allows the user to entera sign on message that will be displaed on the screen during the boot sequence. Upto 31 characters are available for sign on messages.

Note these configuration options are stored in a nonvolatile serial EEPROM on the APEX CPU card and will therefore be retained even if the CMOS battery is removed and the unit is powered down.

## Watchdog Timer

The APEX is fitted with an on-board Watchdog timer. It can be enabled or disabled via software allowing the user to decide whether their application requires protection against processor failure.

The Watchdog is controlled as follows:

| I/O Hex | Access | Operator | Action |
|---|---|---|---|
| 0101 | Write | Bit 0 | 0 - Disable Watchdog operation<br>1 - Enable Watchdog operation |
| 0101 | Read | Byte | Read every 500mS to reset timer |

If the Watchdog is enabled and I/O location 0101H is not ***read*** within 500mS (500mSec to 2Sec variation possible) the Watchdog will generate a Reset to both the APEX and the expansion bus.

The Watchdog is disabled on power-up/reset.

## E²PROM Access

The APEX comes equipped with a serial E²PROM, 64 bytes of which are available for user configuration in formation. Access to the device can be made through the APEX BIOS extensions ( See APEX software utilities section).

| I/O Hex | Access | Operator | Action |
|---|---|---|---|
| 0100 | Write | Bit 0<br>Bit 1<br>Bit 2<br>Bit 3 | E²PROM Chip Select<br>E²PROM Clock Signal<br>E²PROM Write Data |
| 0100 | Read | Bit 0 | Read E²PROM data |

## Flash Access

The Flash device has a capacity of either 128KB, 256KB, 512KB or 1MB (Rev C only). The Flash device is located in memory at E0000H to EFFFFH (64KB). To access all of the Flash device it is necessary to page 64KB sections into the window at E0000H. This is achieved by writing a data byte to 102H thereby accessing the Flash as shown below. It is important to insure that the code being executed is not in Flash when pages are switched. If this were to happen CPU control would be lost. The on-board generated 12 volts will be applied to the Flash when bit 3 is set high (providing J1 is fitted). To program the Flash device the supplied Blue Chip Technology utility "ProgFlash" should be used.

| I/O Hex | Access | Operator | Action |
|---|---|---|---|
| 0102 | Read/Write | Data Bits 0-2,5<br>0000 (128 - 128KB)<br>0001 (128 - 512KB)<br>0010 (256 - 512KB)<br>0011 (256 - 512KB)<br>0100 (512KB - 1MB)<br>0101 (512KB - 1MB)<br>0110 (512KB - 1MB)<br>0111 (512KB - 1MB)<br>1111 (1MB only) | Selects a 64KB page in the Flash device.<br>Selects 00000-0FFFFH in Flash<br>Selects 10000-1FFFFH in Flash<br>Selects 20000-2FFFFH in Flash<br>Selects 30000-3FFFFH in Flash<br>Selects 40000-4FFFFH in Flash<br>Selects 50000-5FFFFH in Flash<br>Selects 60000-6FFFFH in Flash<br>Selects 70000-7FFFFH in Flash<br>Selects 80000-1FFFF in Flash |
| | Read/Write | Data Bit 3 | 0 - Disable Flash Programming Voltage<br>1 - Enable Flash Programming Voltage |
| | Write | Data Bit 4 | 1 - Set user output<br>0 - Reset user output |

Note : J3 is used to select the 512 KB devices only and must be fitted to position 1 in order to access these devices.

The user output on bit 4 can be used to directly drive an LED connected between pins 13 and 14 on connector P4

### On-board Serial and Parallel Ports

The APEX processor card has a 16C452 peripheral device fitted as standard. This offers two serial and one parallel ports. These ports can be disabled via software control.

### Serial Ports

The 16C452 provides two compatible asynchronous serial ports. These are mapped as follows:

| Serial Port | I/O Address | Interrupt | Interface | Connector |
|---|---|---|---|---|
| 1 | 03F8 Hex (COM1) | 4 | RS232 | P8 |
| 2 | 02F8 Hex (COM2) | 3 | RS485 | P9 |

This configuration cannot be changed other than to disable it.

### Parallel Port

The APEX provides one fully compatible uni-directional parallel printer port. It has a fixed configuration as detailed below and can be enabled or disabled using the setup utility.

| Parallel Port | I/O Address | Interrupt | Connector |
|---|---|---|---|
| 1 | 0378 Hex (LPT1) | 7 | P6 |

## Battery

The APEX requires an external battery to be fitted to connector P5. This should have an output of 3.6 volts, capacity of 1.8AH and be fitted with a 10K series resistor for safety. This battery provides power for the Real Time Clock and CMOS RAM when there is no power applied to the board. Under normal conditions the recommended battery should last for several years.

Great care should be taken with this battery; **under NO circumstances should**:

the outputs be shorted
be exposed to temperatures in excess of 100°C
be burned
be immersed in water
be unsoldered
be recharged
be disassembled

If the battery is mistreated in any way there will be a possibility of fire, explosion. and harm.

For battery connector pinouts see page 46.

## Backplane

APEX combines the FULL driving capability of the traditional IBM/AT and the compact physical arrangement of the PC/104 specification. The pinouts are detailed in depth in the connector section.

The PC/104 interface as provided by APEX allows for cards to be stacked on top of one another or optionally to be interfaced to a traditional IBM/AT backplane. This interfacing is achieved by using the APX-PC adaptor card. This configuartion is particularly valuable when in the early stages of a development allowing the APEX processor to directly control current PC/AT cards or prototypes.

The APEX is capable of driving up to an 8 slot multilayer backplane with the appropriate termination.

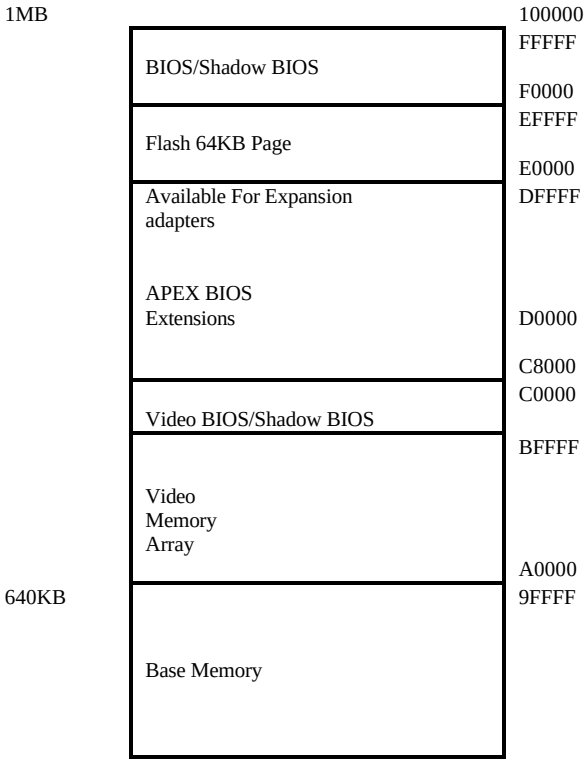
Backplanes are available with three possible types of termination:

| | |
|---|---|
| None | Not recommended for backplanes with more than 2/3 slots |
| Resistive | Recommended for small backplanes (<6 slots) |
| RC | Essential for 8 slot backplanes. |

The actual val ues of termination depend upon the particular installation. Please contact your supplier for assistance.

## Memory Map

### Typical Memory Map for a 1MByte APEX CPU & CI 2



## APEX Configuration Jumpers

| Jumper | Area of Influence | Link | Action |
|---|---|---|---|
| J1 | APEX generated +12 Volts applied to FLASH | None<br><br>Fitted | Not applied - programming disabled<br>Applied - programming enabled |
| J2 | On-board Video BIOS | None<br>Fitted | Enabled<br>Disabled |
| J3 | On-board FLASH selection | Factory Fitted | Position 1 for 512KB only |
| J4 | Select DRAM size | 2M<br><br>8M | 512KByte or 2MB fitted<br>8MB fitted |
| J5 | On-board Serial port RS485 mode | 1<br>2 | Half Duplex selected<br>Full Duplex selected |
| J6 | On-board Serial port RS485 mode | Fitted<br>None | Half Duplex selected<br>Full Duplex selected |

Note

When half duplex RS485 mode is selected, DTR is used to direction control. With DTR asserted in the half duplex mode the RS485 transceiver is transmitting.

## APEX Connector Pinouts

### P1: PC/104 8 bit (64 way)

| A | Signal | B | Signal |
|---|---|---|---|
| 1 | -IOCHCK | 1 | 0 Volts (Ground) |
| 2 | SD7 | 2 | Resetdrv |
| 3 | SD6 | 3 | +5 Volts |
| 4 | SD5 | 4 | IRQ9 |
| 5 | SD4 | 5 | -5 Volts |
| 6 | SD3 | 6 | DREQ2 |
| 7 | SD2 | 7 | -12 Volts |
| 8 | SD1 | 8 | -0WS |
| 9 | SD0 | 9 | +12 Volts |
| 10 | IOCHRDY | 10 | 0 Volts (Ground) |
| 11 | AEN | 11 | -SMEMW |
| 12 | SA19 | 12 | -SMEMR |
| 13 | SA18 | 13 | -IOW |
| 14 | SA17 | 14 | -IOR |
| 15 | SA16 | 15 | -DACK3 |
| 16 | SA15 | 16 | DREQ3 |
| 17 | SA14 | 17 | -DACK1 |
| 18 | SA13 | 18 | DREQ1 |
| 19 | SA12 | 19 | -REF |
| 20 | SA11 | 20 | CLK |
| 21 | SA10 | 21 | IRQ7 |
| 22 | SA9 | 22 | IRQ6 |
| 23 | SA8 | 23 | IRQ5 |
| 24 | SA7 | 24 | IRQ4 |
| 25 | SA6 | 25 | IRQ3 |
| 26 | SA5 | 26 | -DACK2 |
| 27 | SA4 | 27 | T/C |
| 28 | SA3 | 28 | BALE |
| 29 | SA2 | 29 | +5 Volts |
| 30 | SA1 | 30 | OSC |
| 31 | SA0 | 31 | 0 Volts (Ground) |
| 32 | 0 Volts Ground) | 32 | 0 Volts (Ground) |

## P2: PC/104 16 bit (40 way)

| D | Signal | C | Signal |
|---|---|---|---|
| 1 | 0 Volts (Ground) | 1 | 0 Volts (Ground) |
| 2 | -SBHE | 2 | -MEMCS16 |
| 3 | LA23 | 3 | -IOCS16 |
| 4 | LA22 | 4 | IRQ10 |
| 5 | LA21 | 5 | IRQ11 |
| 6 | LA20 | 6 | IRQ12 |
| 7 | LA19 | 7 | IRQ15 |
| 8 | LA18 | 8 | IRQ14 |
| 9 | LA17 | 9 | -DACK0 |
| 10 | -MEMR | 10 | DREQ0 |
| 11 | -MEMW | 11 | -DACK5 |
| 12 | SD8 | 12 | DREQ5 |
| 13 | SD9 | 13 | -DACK6 |
| 14 | SD10 | 14 | DREQ6 |
| 15 | SD11 | 15 | -DACK7 |
| 16 | SD12 | 16 | DREQ7 |
| 17 | SD13 | 17 | +5 Volts |
| 18 | SD14 | 18 | -Master |
| 19 | SD15 | 19 | 0 Volts (Ground) |
| 20 | No Connection | 20 | 0 Volts (Ground) |

## P3: 3½" Disk Drive (4 way header)

| Pin No. | Signal |
|---|---|
| 1 | +5 Volts DC |
| 2 | 0 Volts (Ground) |
| 3 | 0 Volts (Ground) |
| 4 | +12 Volts DC |

## P4: Peripheral (20 way header)

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | Audio +ve | 2 | Audio -ve |
| 3 | Reset +ve | 4 | Reset -ve (Ground) |
| 5 | Turbo LED +ve | 6 | Turbo LED -ve |
| 7 | Keyboard inhibit | 8 | 0 V (Ground) |
| 9 | Power LED +ve | 10 | Power LED -ve (Ground) |
| 11 | Mouse Data | 12 | Mouse clock |
| 13 | 220WPull up | 14 | Reserved |
| 15 | +5V (fused) | 16 | 0 Volts (Ground) |
| 17 | +ve Battery input | 18 | 0 Volts Battery (Ground) |
| 19 | Keyboard Data | 20 | Keyboard Clock |

## P5: Battery (3 way header)

| Pin No. | Signal |
|---|---|
| 1 | +3.6 Volts DC |
| 2 | Not used (key) |
| 3 | 0 Volts (Ground) |
| 4 | 0 Volts (Ground) |

## P6: Parallel (26 way header)

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | -Strobe | 2 | -Auto Feed XT |
| 3 | Data bit 0 | 4 | -Error |
| 5 | Data bit 1 | 6 | -Initialise |
| 7 | Data bit 2 | 8 | -Select (input) |
| 9 | Data bit 3 | 10 | 0 Volts (Ground) |
| 11 | Data bit 4 | 12 | 0 Volts (Ground) |
| 13 | Data bit 5 | 14 | 0 Volts (Ground) |
| 15 | Data bit 6 | 16 | 0 Volts (Ground) |
| 17 | Data bit 7 | 18 | 0 Volts (Ground) |
| 19 | -Acknowledge | 20 | 0 Volts (Ground) |
| 21 | Busy | 22 | 0 Volts (Ground) |
| 23 | Paper Empty | 24 | 0 Volts (Ground) |
| 25 | Select (Output) | 26 | Not Used |

## P7: Co-Processor (36 way header)

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | +5 Volts | 2 | LD14 |
| 3 | +5 Volts | 4 | LD15 |
| 5 | +5 Volts | 6 | -READY |
| 7 | +5 Volts | 8 | -M/IO |
| 9 | LD0 | 10 | PROCLK |
| 11 | LD1 | 12 | RESET |
| 13 | LD2 | 14 | -BUSY |
| 15 | LD3 | 16 | -ADS |
| 17 | LD4 | 18 | -W/R |
| 19 | LD5 | 20 | -NPBUSY |
| 21 | LD6 | 22 | -NPERR |
| 23 | LD7 | 24 | LA23 |
| 25 | LD8 | 26 | LA2 |
| 27 | LD9 | 28 | 386PEREQ |
| 29 | LD10 | 30 | 0 Volts (Ground) |
| 31 | LD11 | 32 | 0 Volts (Ground) |
| 33 | LD12 | 34 | 0 Volts (Ground) |
| 35 | LD13 | 36 | 0 Volts (Ground) |

## P8: Serial 1 RS232 (10 way header)

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | -Data Carrier Detect | 2 | -Data Set Ready |
| 3 | Receive Data | 4 | -Ready To Send |
| 5 | Transmit Data | 6 | -Clear To Send |
| 7 | -Data Terminal Ready | 8 | -Ringing Indicator |
| 9 | 0 Volts (Ground) | 10 | Not used |

## P9: Serial 2 RS485 (10 way header)

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | Full Duplex RX +ve | 2 | 4K7WPull up (+5V) |
| 3 | Full Duplex RX -ve | 4 | RESERVED |
| 5 | TX +ve Full Duplex TX/RX +ve Half Duplex | 6 | NC |
| 7 | TX -ve Full Duplex TX/RX -ve Half Duplex | 8 | NC |
| 9 | 4K7WPull down(0V) | 10 | NC |

## APEX Bus Signal Descriptions

The following is a description of the APEX (ISA) Bus signals. All signal lines are TTL compatible.

**AEN (O)**

'Address Enable' is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus Read command lines (memory and I/O), and the Write command lines (memory and I/O).

**BALE (O) (Buffered)**

'Address latch enable' is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is available to the I/0 channel as an indicator of a valid microprocessor or DMA address (when used with 'AEN'). Microprocessor addresses SA0 through SAl9 are latched with the falling edge of 'BALE. ' 'BALE' is forced high during DMA cycles.

**CLK (O)**

This is the system clock. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

**-DACKO through -DACK3 and -DACK5 through -DACK7 (O)**

-DMA Acknowledge 0 through 3 and 5 through 7 are used to acknowledge DMA requests (DRQ0 through DRQ7). They are active low.

**DRQ0 through DRQ3 and DRQ5 through DRQ7 (I)**

DMA Requests 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). They are prioritized, with DRQ0 having the highest priority and DRQ7 having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding 'DMA Request Acknowledge'(DACK) line goes active. DRQ0

through DRQ3 will perform 8 -bit DMA transfers; 'DRQ5' through DRQ7 will perform l6 bit transfers.

**-I/O CHCK (I)**

'-I/O channel check' provides the system board with parity (error) information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error.

**I/O CHRDY (I)**

'I/O channel ready' is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles. This signal should be held low for no more than 2.5 microseconds.

**-I/O CS16 (I)**

'-I/O 16 bit Chip Select' signals the system board that the present data transfer is a 16 bit, 1 wait state, I/O cycle. It is derived from an address decode. '- I/O CS 16' is active low and should be driven with an open collector or tri-state driver capable of sinking 20mA.

**-IOR (I/O)**

'-I/O Read' instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

**-IOW (I/O)**

'I/O Write' instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is active low.

**IRQ3 to IRQ7, IRQ9 to IRQ12 and IRQ14 to 15 (I)**

Interrupt Requests 3 through 7, 9 through 12, and 14 through 15 are used to signal the microprocessor that an I/0 device needs attention. The interrupt requests are prioritized, with IRQ9 through IRQ12 and IRQ14 through IRQ15 having the highest priority (IRQ9 is the highest) and IRQ3 through IRQ7 having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine).

**LA17 through LA23 (I/O)**

These signals (unlatched) are used to address memory and I/O devices within the system. They give the system up to 16MB of address capability. These signals are valid when 'BALE' is high. LA17 through LA23 are not latched during microprocessor cycles and therefore do not stay valid for the whole cycle. Their purpose is to generate memory decodes for 1 wait- state memory cycles. These decodes should be latched by I/O adapters on the falling edge of 'BALE. ' These signals also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

**-Master (I)**

This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a '- DACK'. Upon receiving the '- DACK', an I/O microprocessor may pull '- Master' low, which will allow it to control the system address, data, and control lines (a condition known as tri-state). After '- Master' is low, the I/O microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15 microseconds, system memory may be lost because of a lack of refresh.

**-MEMCS16 (I)**

'-MEM 16 Chip Select' signals the system board if the present data transfer is a 1 wait-state, 16 bit, memory cycle. It must be derived from the decode of LA17 through LA23. '-MEM CS 16' should be driven with an open collector or tri-state driver capable of sinking 20 mA.

**OSC (O)**

'Oscillator' (OSC) is a high speed clock with a 70 nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50 % duty cycle.

**0WS (I)**

The 'Zero Wait State' (0WS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16 bit device without wait cycles, '0WS' is derived from an address decode gated with a Read or Write command.
In order to run a memory cycle to an 8 bit device with a minimum of two wait states, '0WS' should be driven active on system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to a 8 bit device are active on the falling edge of the system clock. '0WS' is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mA.

**-Refresh (I/O)**

This signal is used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel.

**Reset Drive (O)**

'Reset drive' is used to reset or initialize system logic at power up time or when the power supply drops below its minimum level. This signal is active high.

**SA0 through SAl9 (I/O)**

Address bits 0 through 19 are used to address memory and I/O devices within the system. These twenty address lines, in addition to LA17 through LA23, allow access of up to 16MB of memory. SA0 through SAl9 are gated on the system bus when 'BALE' is high and are latched on the falling edge of 'BALE. '

These signals are generated by the microprocessor or DMA Controller. They also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

**SBHE (I/O)**

'Bus High Enable' (system) indicates a transfer of data on the upper byte of the data bus, SD8 through SD15. 16 bit devices use 'SBHE' to condition data bus buffers tied to SD8 through SD15.

**SD0 through SD15 (I/O)**

These signals provide data bus bits 0 through 15 for the microprocessor, memory, and I/O devices. D0 is the least significant bit and Dl5 is the most significant bit. All 8 bit devices on the I/O channel should use D0 through D7 for communications to the microprocessor. The l6 bit devices will use D0 through D15. To support 8 bit devices, the data on D8 through D15 will be gated to D0 through D7 during 8 bit transfers to these devices. 16 bit microprocessor transfers to 8 bit devices will be converted to two 8 bit transfers.

**-SMEMR (O)- MEMR (I/O)**

These signals instruct the memory devices to drive data onto the data bus. '- SMEMR' is active only when the memory decode is within the low lMB of memory space. '- MEMR' is active on all memory read cycles. '- MEMR' may be driven by any microprocessor or DMA controller in the system. '- SMEMR' is derived from 'MEMR' and the decode of the low lMB of memory. When a microprocessor on the I/O channel wishes to drive '- MEMR', it must have the address lines valid on the bus for one system clock period before driving '- MEMR' active. Both signals are active low.

**-SMEMW (O)- MEMW (I/O)**

These signals instruct the memory devices to store the data present on the data bus. '- SMEMW' is active only when the memory decode is within the low 1 MB of the memory space. '- MEMW' is active on all memory write cycles. '- MEMW' may be driven by any microprocessor or DMA controller in the system. '- SMEMW' is derived from '- MEMW' and the decode of the low lMB of memory. When a microprocessor on the I/O channel wishes to drive '- MEMW', it must have the address lines valid on the bus for one system clock period before driving '- MEMW' active. Both signals are active low.

**T/C (O)**

'Terminal Count' provides a pulse when the terminal count (end of) for any DMA channel is reached.

## I/O Address Map

| Hex Range | Device | Occupied by APEX (default) | Occupied by APEX-CI 2 (default) |
|---|---|---|---|
| 0000 - 00lF | DMA Controller 1 | ✓ | |
| 0020 - 003F | Interrupt Controller 1, Master | ✓ | |
| 0040 - 005F | Timer & Index registers for SCATsx | ✓ | |
| 0060 - 006F | 8042 (Keyboard & Mouse) | ✓ | |
| 0070 - 007F | Realtime Clock, NMI Mask | ✓ | |
| 0080 - 008F | POST, DMA Page Register | ✓ | |
| 00A0 - 00BF | Interrupt Controller 2, Slave | ✓ | |
| 00C0 - 00DF | DMA Controller 2 | ✓ | |
| 00F0 | Clear Maths Coprocessor Busy | ✓ | |
| 00F1 | Reset Maths Coprocessor | | |
| 00F8 - 00FF | Maths Coprocessor | ✓ | |
| 0100H | E²PROM Access | ✓ | |
| 0101H | Watchdog | ✓ | |
| 0102H | FLASH Access | ✓ | |
| 0103H | Peripheral disable | ✓ | |
| 0104H | Serial Port Rs232 or 485/ Half or Full Duplex | | ✓ |
| 0105H | 24 Digital I/O | | ✓ |
| 01F0 - 01F8 | Hard (fixed) Disk Controller | | ✓ |
| 0200 - 0207 | Games port | | |
| 0278 - 027F | Parallel Printer Port 2 | | |
| 0208 - 021A | EMS Page registers ( either 208 or 218, etc) | ✓ | |
| 02E8 - 02EF | Serial Port 4 | | ✓ |
| 02F8 - 02FF | Serial Port 2 | ✓ | |
| 0300 - 031F | Prototype Card/Digital PIO | | ✓ |
| 0360 - 036F | Reserved | | |
| 0378 - 037F | Parallel Printer Port 1 | ✓ | |
| 0380 - 038F | SDLC, Bi-synchronous 2 | | |
| 03A0 - 03AF | Bi-synchronous 1 | | |
| 03B0 - 03DF | Video Adapter | | ✓ |
| 03E8 - 03EF | Serial Port 3 | | ✓ |
| 03F0 - 03F7 | Floppy Diskette Controller | | ✓ |
| 03F8 - 03FF | Serial Port 1 | ✓ | |

## Interrupt Assignments

| Interrupt | Device | Occupied on APEX (default) | Occupied by APEX-CI 2 (default) |
|---|---|---|---|
| NMI | Parity Check (generates IOCHCK on error) | ✓ | |
| 0 | Timer | ✓ | |
| 1 | Keyboard (Output Buffer Full) | ✓ | |
| 2 | Cascaded from Interrupt 9 | ✓ | |
| 3 | Serial Port 2 (also 4, 6 & 8 if sharing interrupts) | ✓ | ✓ |
| 4 | Serial Port 1 (also 3, 5 & 7 if sharing interrupts) | ✓ | ✓ |
| 5 | Parallel Port 2 | | |
| 6 | Floppy Diskette Controller | | ✓ |
| 7 | Parallel Port 1 | ✓ | |
| 8 | Real Time Clock | ✓ | |
| 9 | VGA controller | | |
| 10 | Unassigned | | |
| 11 | Unassigned | | |
| 12 | PS/2 Mouse | ✓ | |
| 13 | Unassigned | | |
| 14 | Hard (Fixed) Disk Controller | | ✓ |
| 15 | Unassigned | | |

## DMA Assignments

| DMA Channel | 8/16 bit Peripherals | Device | Occupied on APEX (default) | Occupied by APEX-CI 2 (default) |
|---|---|---|---|---|
| 0 | 8 bit | Available (usually Refresh but free on APEX) | | |
| 1 | 8 bit | Available | | |
| 2 | 8 bit | Diskette Drive | | ✓ |
| 3 | 8 bit | Available | | |
| 4 | 16 bit | Cascaded to 1st DMA controller | ✓ | |
| 5 | 16 bit | Available | | |
| 6 | 16 bit | Available | | |
| 7 | 16 bit | Available | | |

## POST Error Codes

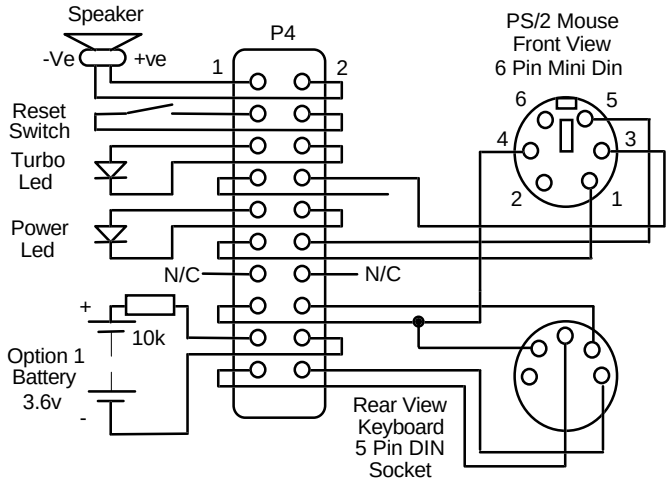
The BIOS performs a **P**ower **O**n **S**elf **T**est after a reset or reboot. During the POST the microprocessor indicates the state of the test by writing codes to the I/O port address 80 hex. The APEX offers on-board decode of this information and can drive the optional POST display without modification. The following codes indicate the progress of the microprocessor during the test.

| Code (Hex) | Description |
|---|---|
| 01 | Processor register test starting. NMI disabled next. |
| 02 | NMI disabled. Power-on delay starting. |
| 03 | Power-on delay complete. Keyboard initialisation. |
| 04 | Keyboard initialisation complete. |
| 05 | Checking soft or cold start via keyboard SYS bit. |
| 06 | Enabled ROM. Calculating BIOS checksum. |
| 07 | Sending BAT command to the keyboard controller. |
| 08 | BAT command sent. |
| 09 | BAT verified. |
| 0A | Keyboard command code byte sent. |
| 0B | Keyboard command data byte sent. |
| 0C | Keyboard controller blocked and unblocked. |
| 0D | Keyboard controller NOP command complete. |
| 0E | CMOS RAM shutdown register test passed. |
| 0F | CMOS RAM checksum complete and the DIAG byte is written. |
| 10 | CMOS RAM initialised. |
| 11 | CMOS RAM status register initialised. |
| 12 | DMA and Interrupt controllers disabled. |
| 13 | Video display disabled. |
| 14 | SCATsx initialisation complete. Auto memory detection complete. |
| 15 | 8254 timer channel 2 test half complete. |
| 16 | 8254 timer channel 2 test complete. |
| 17 | 8254 timer channel 1 test complete. |
| 18 | 8254 timer channel 0 test complete. |
| 19 | Memory refresh started. |
| 1A | Memory refresh toggling test completed. |
| 1B | Memory refresh test at 15uS completed. |
| 20 | Start 64KB base memory test. |
| 21 | Memory address line test completed. |
| 22 | Memory parity toggling completed. |
| 23 | Base 64KB memory read/write test passed. |
| 24 | System configuration before vector initialisation completed. |
| 25 | Interrupt vector initialisation completed. |
| 26 | 8042 input port read. Turbo initialisation completed. |
| 27 | Global data initialisation done. |
| 28 | Initialisation complete. |
| 29 | Monochrome mode is set. |
| 2A | Colour mode set. |
| 2B | Parity toggle completed. |

| | |
|---|---|
| 2C | Initialise for video ROM done. |
| 2D | Video ROM check complete. |
| 2E | Complete video ROM processing. |
| 2F | No EGA or VGA adapter has been found. |
| 30 | Video display read/write test completed. |
| 31 | Video display read/write or retrace test failed. |
| 32 | Alternate video display read/write test passed. |
| 33 | Video display check completed. |
| 34 | Verification of video adapter done. |
| 35 | Video display mode set. |
| 36 | BIOS ROM data area check completed. |
| 37 | Cursor setting for power-on message done. |
| 38 | Display power-on message. |
| 39 | New cursor position has been read and saved. |
| 3A | BIOS identification string displayed. |
| 3B | Hit "DEL" message displayed. |
| 40 | Prepare virtual mode test. |
| 41 | Verifying display memory completed. |
| 42 | Descriptor tables prepared. |
| 43 | Entered virtual mode. |
| 44 | Interrupts are enabled if the diagnostics switch is on. |
| 45 | Data initialised for memory wrap around check. |
| 46 | Memory wrap around check completed. Memory size check completed. |
| 47 | Memory test patterns written to extended RAM. |
| 48 | Memory test patterns written to conventional RAM. |
| 49 | Memory size below 1MB established. |
| 4A | Memory size above 1MB established. |
| 4B | BIOS ROM data area check completed. |
| 4C | Memory below 1MB cleared via a soft reset. |
| 4D | Memory above 1MB cleared via a soft reset. |
| 4E | Memory test started. No soft reset was performed. |
| 4F | Memory size display has begun. The display is updated during the test. |
| 50 | Memory test below 1MB is completed. |
| 51 | Memory size has been adjusted for memory relocation above 1MB. |
| 52 | Memory test above 1MB complete. |
| 53 | CPU registers saved. |
| 54 | CPU in real mode. Shutdown successful. |
| 55 | CPU registers restored. |
| 56 | Gate A20 address line disabled. |
| 57 | BIOS ROM data area check partially complete. |
| 58 | BIOS ROM data area check complete. |
| 59 | "Hit DEL" message has been cleared. |
| 60 | DMA page register test passed. |
| 61 | Display memory test completed. |
| 62 | DMA controller1 test passed. |
| 63 | DMA controller2 test passed. |
| 64 | BIOS ROM data area check partially complete. |
| 65 | BIOS ROM data area check complete. |
| 66 | DMA controllers 1&2 programmed. |
| 67 | 8259 interrupt controller initialisation done. |
| 80 | Keyboard test started. |

| | |
|---|---|
| 81 | Keyboard reset command passed. |
| 82 | Keyboard controller interface test done. |
| 83 | Command byte written and global initialisation complete. |
| 84 | Lock key checking done. |
| 85 | Memory size check done. |
| 86 | Password has been checked. |
| 87 | Programming before Setup complete. |
| 88 | Returned from Setup program and cleared the screen. |
| 89 | Programming after Setup completed. |
| 8A | The power-on screen message is displayed. |
| 8B | The "Wait..." message is displayed. |
| 8C | System and video BIOS shadowing successful. |
| 8D | Setup options are programmed. |
| 8E | Mouse test and initialisation done. |
| 8F | Floppy Disk check identify that the drive needs initialising. |
| 90 | Floppy Disk configuration complete. |
| 91 | Hard Disk presence check completed. |
| 92 | Hard Disk configuration completed. |
| 93 | BIOS ROM data area check partially complete. |
| 94 | BIOS ROM data area check fully completed. |
| 95 | Memory size adjusted because of mouse support and hard disk type 47. |
| 96 | Display memory verified. |
| 97 | Pre-initialisation for expansion ROM operation completed. |
| 98 | Expansion ROM control test completed. |
| 99 | Initialisation for option ROM test completed. |
| 9A | Set timer data area and parallel printer base address. |
| 9B | Set asynchronous base addresses. |
| 9C | Initialisation for coprocessor test completed. |
| 9D | Coprocessor partially initialised. |
| 9E | Coprocessor initialised. |
| 9F | Extended keyboard flags checked. |
| A0 | Keyboard ID command issued. |
| A1 | Keyboard ID flag reset has been done. |
| A2 | Cache memory test completed. |
| A3 | Soft error test completed. |
| A4 | Keyboard typematic rate is set. |
| A5 | Memory wait states set. |
| A6 | Screen cleared. |
| A7 | NMI and parity enabled. |
| A8 | Initialisation before E0000H adapter ROM control invoked. |
| A9 | E0000H adapter ROM control completed. |
| 00 | System configuration displayed. Passing control to INT 19H bootstrap Loader now. |

## Wiring to the Peripheral Connector




Please note that all LED drive outputs have a 220 ohm serial resistor connected to the +5 volt supply rail, and the +5v supply to the keyboard is fused (via a SMD fuse) at 1 Amp.

## Apex BIOS Extensions

The APEX provides a BIOS extension at address C800:0000 which provides the programmer with access to the additional hardware found on the board. The BIOS extension hooks into software interrupt 50. The programmer loads a particular function code into the AH register followed by a specific set of parameters in the other registers before executing the interrupt. Most high level languages allow access to software interrupts through a particular function call. For example, in Quick Basic :-

```
' Read E2 Data via interrupt 50 call
$include:'QB.BI'

DIM INARY%(7),OUTARY%(7)
CONST AX=0,BX=1,CX=2,DX=3,BP=4,SI=5,DI=6,FL=7

INARY%(AX) = &H0400             ' Read e2 data
INARY%(BX) = &h21               ' address &h31
CALL INT86OLD(&h50,INARY%(),OUTARY%()) ' Call the APEX ' service
PRINT "E2 ADDRESS &h31 CONTAINS: ";OUTARY%(DX)
```

Similarly in C :-

```
#include <stdio.h>
#include <dos.h>

#define APEX 0x50

void main(void)
{
  union REGS regs;

  regs.x.ax = 0x0400;  /* read e2 */
  regs.x.bx = 0x31;    /* address 0x31 */
  int86(APEX, &regs, &regs);
  printf("e2 Address 0x31 contains %x\n",regs.x.dx);
}
```

## Flash Memory Functions

The APEX has on-board Flash memory options of 128KB, 256KB, 512KB and 1MB. Flash memory is similar to UV erasable EPROM in that all the memory locations must be erased before it can be reprogrammed. The advantage over EPROM is that Flash can be erased electrically with the device in situ.

The APEX BIOS Extension provides 3 functions which allow the programmer access to
the flash memory, these are:

A. Read one or more FLASH Sectors into RAM

B. Write one or more FLASH Sectors

C. Erase all FLASH

### Read FLASH Sector

Calling Registers:
AH = 00
AL = Device number (00 for internal flash)
CX = Number of sectors to transfer
DX = Start Sector
DS:BX = Pointer to users buffer

Return Registers:
Carry Clear if successful
Carry Set if unsuccessful with error code in AX

This function is provided to allow transfer of data from the internal FLASH EPROM. Each FLASH sector is 512 bytes long. The maximum value for the starting sector is 254.

### Write FLASH Sector

Calling Registers: AH = 01
AL = Device number (00 for internal flash)
CX = Number of sectors to transfer
DX = Start Sector
DS:BX=Pointer to users buffer

Return Registers: Carry clear if successfully

Carry set if unsuccessful

This function is provided to allow transfer of data from a user buffer to the internal FLASH. Each flash sector is 512 bytes long and the maximum value for the starting sector
is 254.

NOTE: Each flash sector can only be programmed once - in order to re-write a sector
the FLASH FORMAT function must be called first.

### FLASH Format

Calling Registers: AH = 02

Return Registers: Carry clear if successful
Carry Set if unsuccessful

This function erases the entire contents of the FLASH. Depending on the age of the FLASH this can take up to 10 seconds to complete.

## E2 Functions

Unlike the FLASH ROM, e2 does not require to be completely erased before a single location is written. It is therefore more useful for storage of configuration information.

The APEX contains 64 16bit words of e2 memory - the lower 32 are reserved for use by Blue Chip Technology for configuration information, the top 32 are available to the user for any purpose.

The APEX BIOS extension provides two functions to allow access to the e2 memory these are:

1. Write to a single e2 memory location

2. Read from a single e2 memory location

### 1. Write to e2 Memory

Calling Registers: AH = 03
BL = Location to write to (0-63)
DX = Data to Write (16 bit value)

Return Registers:

Carry flag clear if successful
Carry flag Set if unsuccessful

### 2. Read e2 Memory

Calling Registers: AH = 04
BL = Location to read (0-63)

Return Registers:
DX = e2 Data

## Watchdog Facility

The APEX contains a simple hardware watchdog function. When enabled, the watchdog will generate a hardware reset if a RESET WATCHDOG function call is not made at least once every 1.5 seconds

Two functions are available to control the watchdog

1. Enable/Disable Watchdog function

2. Reset Watchdog

### 1. Enable/Disable Watchdog

Calling Registers: AH = 05
AL = 00 or 01
if AL is 00, watchdog function is disabled
if AL is 01, watchdog function is enabled

Return Registers: NONE

### 2. Reset Watchdog

Calling Registers: AH = 06

Return Registers: NONE

### System Identification

In order to detect whether software is running on an APEX unit a function has been provided which returns a unique unit identification.

Calling Registers: AH = 09

Return Registers: DX = 4981

The following C routine demonstrates the use of this function

```
*****************************************************************
unsigned int System_ID(void)
{
        // return system ID code

        struct REGPACK          regs;

        reg.r_ax = 0x0900               // Function to return ID code
        reg.r_dx = 0x0000               // Clear DX
        intr(0x50,&reg)

                                        // ID returned in DX
        return reg.r_dx    // APEX returns 0x4981
                                        // Any other system will return 0x0
}

*****************************************************************
******
```

## APEX Utilities

### Remote Disk

The remote disk facility allows the APEX to communicate with floppy diskette drives and hard disk drives through a serial communications link to a PC-based host computer running DOS.

**i. Configuration**
Use the Extended Setup program to configure the remote disk - If the remote is enabled, all other options relating to disks are overridden.

**ii. Making the Connection**
The remote disk requires only RX ,TX and Ground lines from the serial port to operate correctly. Connect the RX line from the serial port on the Host computer to the TX line on the serial port on the APEX ,and the RX line from the APEX to the TX line on the Host

**iii. The Server**
In order for the host computer to operate as a server, two files are required from the APEX UTILITIES disk, these are

REMSVR.SYS - A Device driver
SERVER.EXE - A remote disk monitor program

Copy both of these files onto the host computer, make sure that REMSVR.SYS is copied into the root directory and add the following entry to CONFIG.SYS

DEVICE = REMSVR.SYS

If the host is using a COM port other than COM1 for communication to the APEX add the comport number after REMSVR.SYS on this line.

Reboot the host computer and run SERVER.EXE - if the device driver is installed correctly, the remote disk status screen will be displayed, if not, check the entry in the CONFIG.SYS file.

### iv. Using the Remote Disk

Connect the APEX to the Host computer and reboot the APEX with the Host running the SERVER.EXE program.If all is well the APEX should display:

REMOTE DISK INSTALLED
[Connected]

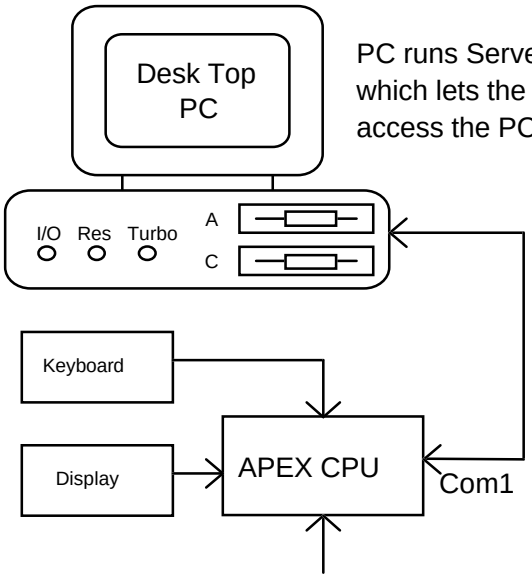
Prior to booting.

The APEX will then attempt to boot from the host's disk, the serial link operates at 115Kbaud - even so, the data transfer rate is typically only 2 or 3 Kbytes per second which is slow even compared to floppy disks, so please be patient!

**WARNING**

The remote disk will only operate correctly with operating systems which rely on the BIOS disk services for disk access - certain operating systems such as WINDOWS which communicate directly with disk hardware will cause the remote disk to hang. In extreme cases data on the disk can be corrupted - Blue Chip Technology accept no responsibility for data corrupted in this way, we recommend that the remote disk is used initially to access floppy drives only, where potential damage is less likely.

**Overview**




PC runs Server Program which lets the APEX CPU access the PC's drive A:

Simple 3 wire RS232 Serial Link. Link Normally on Com1 of the PC to Com1 of the APEX unit

APEX unit runs special Remote Disk program via the BIOS

### Flash Disk

The on-board FLASH can be configured to appear to the system as a read only 720KB or 1.44MB floppy disk. Use the Extended Setup program to enable the FLASH as either drive A or drive B.

In order to copy files onto the FLASH first take a blank
formatted diskette. Copy the files required on the FLASH disk onto this diskette.

Once all the required files are assembled on the diskette run the program PROGFLSH.EXE, found on the APEX UTILITIES disk - the command line for this program is PROGFLASH <src. drive> , where src. drive is the source drive of the floppy diskette containing the files to be copied on the FLASH Disk. PROGFLASH will copy from the diskette onto the FLASH Disk. The FLASH Disk is now ready for use.

For APEX systems which contain no floppy drives, a utility is provided which copies data from a floppy disk on a remote PC.

The program PFREMOTE.EXE operates in exactly the same way as PROGFLAS.EXE except the disk is copied from another computer connected to the APEX via a serial cable.

To use PFREMOTE the host system must be prepared by loading the Remote Disk Server REMSVR.SYS.

Add the line :

DEVICE = REMSVR.SYS <port>

to the CONFIG.SYS file, add ,port. to specify the serial port the host will use to communicate with the APEX.

Now load the program SERVER.EXE on the host system.

Connect COM1 on the APEX to the host serial port (the cable should cross TX and RX, no modem control signal need be connected).

The host is now ready for remote access. To re-program the FLASH disk on the APEX run PFREMOTE.EXT on the APEX (the command line is the same as PROGFLAS.EXE and insert the 720KB disk to copy into the floppy drive of the host system.

# APEX CI-2

## Introduction

The APEX-CI 2 is a member of the APEX 104 family. It stacks to the APEX 104 CPU via the PC/104 compatible interface (P1 & P2). The APEX-CI 2 provides standard computer interfaces by the use of two VLSI devices. These are:

CL-GD6235 which provides VGA compatible video output to both CRT & LCD displays. SMC37C663 which provides floppy, ID & 2 serial ports

For further information on these devices please contact your supplier.

## Specification

## On-board Features

- VGA compatible with CRT resolutions up to 1024 by 768 by 16 colours with 512KByte video memory as standard
- VGA compatible with LCD resolutions up to 640 by 480 driving mono, colour STN, dual scan STN, TFT LCDs & EL displays
- 2 Asynchronous 16C550 compatible software selectable serial ports providing either RS232 or RS485 interfaces
- Dual IDE interface for embedded hard drives
- Dual Floppy Disk controller (UPD72065B compatible) with on-chip Analog data separator
- 24 Channel programmable I/O
- Low power operation
- PC/104 compatible

## Video

The APEX-CI 2 offers a VGA compatible interface with resolutions up to 1024 by 768 by 16 colours. ***The BIOS is resident on the APEX processor card at memory address C0000 to C7FFF hex and is enabled/disabled by J2 on the APEX CPU***. The data highway to APEX is via a 16 bit interface ensuring optimum speed for graphics applications. Connections to a CRT monitor are made via P7 on the APEX CI-2 . This is a 10 way header and requires an custom cable to interface to the standard 15 way condensed D type connector used on most monitors. The CRT output is compatible with VGA mono, colour and multisync monitors.

Connections to the LCD output are made via P4 on the APEX CI-2. This is a 40 way socket. For connection details please refer to the Display connection Appendix at the rear of this manual.

## Serial Ports

Two asynchronous 16C550 compatible interfaces are provided by the APEX-CI. Both serial ports can operate in either RS232 or RS485 modes. When in RS485 mode either half (2 wire) or (4 wire) full duplex operation can be software selected via the Setup menu. DTR is used for direction control. The APEX-CI 2 generates its own RS232 levels on-board allowing 5 volt only operation. The AMI BIOS provides built-in configuration of I/O addresses and interrupt usage.

Note
If the APEX CPU's on-board serial & parallel ports are enabled then COM1, COM2 and LPT1 will already be occuppied. Use Extended Setup Menu to enable and disable the APEX CPU serial ports.

## Digital PIO

The APEX-CI 2 has an on-board 8255 (NEC 71055) I/O device allowing the up to 24 digital (TTL) input/outputs. Connector P8 is a 26 way header providing interfacing for three 8 bit ports and two digital grounds (0 volts). The base address is selectable as 0200 or 0300 Hex and is configured via the Extended Setup Menu.

For full details on programming this device please refer to Appendix A at the rear of this manual.

## Disk Drives

## Floppy

The APEX-CI 2 has built in support for two floppy disk drives. These drives can be any permutation of the following:

| Capacity | Drive Size |
|---|---|
| 360KB | 5¼" |
| 720KB | 3½" |
| 1.2MB | 5¼" |
| 1.44MB | 3½" |
| 2.88MB | 3½" |

The BIOS Setup allows you to configure the drives for your installation.

A standard PC 34 way ribbon cable with twisted lines can be connected to two drives both set as drive 1 (as opposed to 0). This is possible because the IBM convention twists the drive select and motor control lines between the two drive connections. Connection to floppy is made using P9.

Remember that only one drive in the chain should be terminated. That should be the drive furthest from the APEX. Without correct termination drive operation can be unreliable. In high noise environments it may be necessary to use shielded ribbon cable. Do not extend the cable length beyond 1 metre.

## Hard (IDE) Drive

The on-board IDE interface allows the connection of up to two hard drives. These connect to the APEX-CI 2 via P5 which is a 40 way header. The maximum length of ribbon cable to be used for reliable operation is 450mm. Each drive can be one of the following 46 types or alternatively a custom type 47 (i.e. each drive can be a different type 47).

Should problems be experienced with the hard disk operation please check the status of both J4 & J5 on the APEX-CI 2 card. J4 selects whether the ALE (Address Latch Enable) signal is passed through to the hard drive. Where problems are being experienced, especially in electrically noisy environments, try changing the link.

J5 selects whether pin 34 of the IDE interface is grouded or left floating. This should only be changed after consulting your IDE drive data sheet. With the link present ground is applied to pin 34.

### Hard Disk Types

Hard disk drive types are identified by the following parameters:

| Parameter | Description |
|---|---|
| Type | A designation for a hard disk drive with predefined parameters |
| Cylinders | The number of cylinders in the disk drive. |
| Heads | The number of heads. |
| Write Precompensation | The size of a sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write precompensation circuitry difference in sector size by boosting the write current for sectors on inner tracks. This parameter is the track number where write precompensation begins. |
| Landing Zone | The number is the cylinder location where the heads normally park when the system is shut down. |
| Sectors | The number of sectors per track. Hard drives that use MFM have 17 sectors per track. RLL drives have 26 sectors per track. ARLL and ESDI drives have 34 sectors per track. SCSI and IDE drives may have even more sectors per track. |
| Capacity | The formatted capacity of the drive based on the following formula:<br>(Number of heads) * (Number of cylinders) * (Number of sectors per cylinder) * (512 bytes per sector) |

The standard 46 hard disk type are as follows:

| Type | No. of Cylinders | No. of heads | Write Precompen-sation | Landing Zone | No. of Sectors | Size |
|---|---|---|---|---|---|---|
| 1 | 306 | 4 | 128 | 305 | 17 | 10MB |
| 2 | 615 | 4 | 300 | 615 | 17 | 20MB |
| 3 | 615 | 6 | 300 | 615 | 17 | 31MB |
| 4 | 940 | 8 | 512 | 940 | 17 | 62MB |
| 5 | 940 | 6 | 512 | 940 | 17 | 47MB |
| 6 | 615 | 4 | 65535 | 615 | 17 | 20MB |
| 7 | 462 | 8 | 256 | 511 | 17 | 31MB |
| 8 | 733 | 5 | 65535 | 733 | 17 | 30MB |
| 9 | 900 | 15 | 65535 | 901 | 17 | 112MB |
| 10 | 820 | 3 | 65535 | 820 | 17 | 20MB |
| 11 | 855 | 5 | 65535 | 855 | 17 | 35MB |
| 12 | 855 | 7 | 65535 | 855 | 17 | 50MB |
| 13 | 306 | 8 | 128 | 319 | 17 | 20MB |
| 14 | 733 | 7 | 65535 | 733 | 17 | 43MB |
| 15 | | | | | | |
| 16 | 612 | 4 | 0 | 663 | 17 | 20MB |
| 17 | 977 | 5 | 300 | 977 | 17 | 41MB |
| 18 | 977 | 7 | 65535 | 977 | 17 | 57MB |
| 19 | 1024 | 7 | 512 | 1023 | 17 | 60MB |
| 20 | 733 | 5 | 300 | 732 | 17 | 30MB |
| 21 | 733 | 7 | 300 | 732 | 17 | 43MB |
| 22 | 733 | 5 | 300 | 733 | 17 | 30MB |
| 23 | 306 | 4 | 0 | 336 | 17 | 10MB |
| 24 | 925 | 7 | 0 | 925 | 17 | 54MB |
| 25 | 925 | 9 | 65535 | 925 | 17 | 69MB |
| 26 | 754 | 7 | 754 | 754 | 17 | 44MB |
| 27 | 754 | 11 | 65535 | 754 | 17 | 69MB |
| 28 | 699 | 7 | 256 | 699 | 17 | 41MB |
| 29 | 823 | 10 | 65535 | 823 | 17 | 68MB |
| 30 | 918 | 7 | 918 | 918 | 17 | 53MB |
| 31 | 1024 | 11 | 65535 | 1024 | 17 | 94MB |
| 32 | 1024 | 15 | 65535 | 1024 | 17 | 128MB |

| | | | | | | |
|---|---|---|---|---|---|---|
| 33 | 1024 | 5 | 1024 | 1024 | 17 | 43MB |
| 34 | 612 | 2 | 128 | 612 | 17 | 10MB |
| 35 | 1024 | 9 | 65535 | 1024 | 17 | 77MB |
| 36 | 1024 | 8 | 512 | 1024 | 17 | 68MB |
| 37 | 615 | 8 | 128 | 615 | 17 | 41MB |
| 38 | 987 | 3 | 987 | 987 | 17 | 25MB |
| 39 | 987 | 7 | 987 | 987 | 17 | 57MB |
| 40 | 820 | 6 | 820 | 820 | 17 | 41MB |
| 41 | 977 | 5 | 977 | 977 | 17 | 41MB |
| 42 | 981 | 5 | 981 | 981 | 17 | 41MB |
| 43 | 830 | 7 | 512 | 830 | 17 | 48MB |
| 44 | 830 | 10 | 65535 | 830 | 17 | 69MB |
| 45 | 917 | 15 | 65535 | 918 | 17 | 114MB |
| 46 | 1224 | 15 | 65535 | 1223 | 17 | 152MB |

## APEX-CI 2 Configuration Jumpers

| Jumper | Area of Influence | Link | Action |
|---|---|---|---|
| J1 | Serial port 1 RS485 Duplex termination | None<br>Fitted | No termination on-board<br>100R & 100nF in circuit |
| J2 | Serial port 2 RS485 Duplex termination | None<br>Fitted | No termination on-board<br>100R & 100nF in circuit |
| J3 | LCD Mode Select | 3 2 1<br>0 0 0<br>0 0 1<br>0 1 0<br>0 1 1 | **See Table below**<br>Panel Class 0<br>Panel Class 1<br>Panel Class 2<br>Panel Class 3 |
| J4 | IDE interface | None<br>Fitted | Removes ALE from IDE<br>Connects ALE to IDE |
| J5 | IDE interface | None<br>Fitted | Pin 34 floats<br>Pin 34 is grounded |
| J6 | Video Controller selection | DIS<br>EN | Disable<br>Enable |

**LCD Table:** **Note: 0 = link present, 1 = no link present**

Class 0: 8 colour, single panel, single scan, 16 bit
Class 1: Monochrome, 2 shade, dual panel, dual scan, 8 bit
Class 2: 8 colour, dual panel, dual scan, 16 bit
Class 3: 256K colour,single panel, 18 bit
and 4096 colour, single panel, 12 bit
and 512 colour, single panel, 9 bit

## APEX-CI 2 Connector Pin-outs

### P1: PC/104 8 bit (64 way)

| A | Signal | B | Signal |
|---|---|---|---|
| 1 | -IOCHCK | 1 | 0 Volts (Ground) |
| 2 | SD7 | 2 | Resetdrv |
| 3 | SD6 | 3 | +5 Volts |
| 4 | SD5 | 4 | IRQ9 |
| 5 | SD4 | 5 | -5 Volts |
| 6 | SD3 | 6 | DREQ2 |
| 7 | SD2 | 7 | -12 Volts |
| 8 | SD1 | 8 | -0WS |
| 9 | SD0 | 9 | +12 Volts |
| 10 | IOCHRDY | 10 | 0 Volts (Ground) |
| 11 | AEN | 11 | -SMEMW |
| 12 | SA19 | 12 | -SMEMR |
| 13 | SA18 | 13 | -IOW |
| 14 | SA17 | 14 | -IOR |
| 15 | SA16 | 15 | -DACK3 |
| 16 | SA15 | 16 | DREQ3 |
| 17 | SA14 | 17 | -DACK1 |
| 18 | SA13 | 18 | DREQ1 |
| 19 | SA12 | 19 | -REF |
| 20 | SA11 | 20 | CLK |
| 21 | SA10 | 21 | IRQ7 |
| 22 | SA9 | 22 | IRQ6 |
| 23 | SA8 | 23 | IRQ5 |
| 24 | SA7 | 24 | IRQ4 |
| 25 | SA6 | 25 | IRQ3 |
| 26 | SA5 | 26 | -DACK2 |
| 27 | SA4 | 27 | T/C |
| 28 | SA3 | 28 | BALE |
| 29 | SA2 | 29 | +5 Volts |
| 30 | SA1 | 30 | OSC |
| 31 | SA0 | 31 | 0 Volts (Ground) |
| 32 | 0 Volts Ground) | 32 | 0 Volts (Ground) |

## P2: PC/104 16 bit (40 way)

| D | Signal | C | Signal |
|---|---|---|---|
| 1 | 0 Volts (Ground) | 1 | 0 Volts (Ground) |
| 2 | -SBHE | 2 | -MEMCS16 |
| 3 | LA23 | 3 | -IOCS16 |
| 4 | LA22 | 4 | IRQ10 |
| 5 | LA21 | 5 | IRQ11 |
| 6 | LA20 | 6 | IRQ12 |
| 7 | LA19 | 7 | IRQ15 |
| 8 | LA18 | 8 | IRQ14 |
| 9 | LA17 | 9 | -DACK0 |
| 10 | -MEMR | 10 | DREQ0 |
| 11 | -MEMW | 11 | -DACK5 |
| 12 | SD8 | 12 | DREQ5 |
| 13 | SD9 | 13 | -DACK6 |
| 14 | SD10 | 14 | DREQ6 |
| 15 | SD11 | 15 | -DACK7 |
| 16 | SD12 | 16 | DREQ7 |
| 17 | SD13 | 17 | +5 Volts |
| 18 | SD14 | 18 | -Master |
| 19 | SD15 | 19 | 0 Volts (Ground) |
| 20 | No Connection | 20 | 0 Volts (Ground) |

## P3: RS422/485 Serial (10 way header)

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | +ve Receive Data 1 | 2 | 10KWpull up (+5V) |
| 3 | -ve Receive Data 1 | 4 | +ve Receive Data 2 |
| 5 | +ve Transmit Data 1 | 6 | -ve Receive Data 2 |
| 7 | -ve Transmit Data 1 | 8 | +ve Transmit Data 2 |
| 9 | 10KWpull down (0V) | 10 | -ve Transmit Data 2 |

## P4: LCD Interface (40 way socket)

| Pin No. | Description | Pin No. | Description |
|---|---|---|---|
| 2 | LCDRST | 1 | FPVDCLK |
| 4 | NPD | 3 | MOD |
| 6 | FVSYNC | 5 | LFS |
| 8 | FHSNYC | 7 | LLCLK |
| 10 | STANBY | 9 | R5 |
| 12 | SUSPEND | 11 | R4 |
| 14 | DE | 13 | R3 / SUD7 |
| 16 | FPBACK | 15 | R2 / SUD6 |
| 18 | FPVCC | 17 | G5 / SUD5 |
| 20 | FPVEE | 19 | G4 / SUD4 |
| 22 | VCC (APEX) | 21 | G3 / SUD3 |
| 24 | GND (APEX) | 23 | B5 / SUD2 |
| 26 | GND (APEX) | 25 | B4 / SUD1 |
| 28 | GND (APEX) | 27 | B3 / SUD0 |
| 30 | GND (APEX) | 29 | R1 / SLD7 / UD3 |
| 32 | N/C | 31 | R0 / SLD6 / UD2 |
| 34 | B1 / SLD1 / LD1 | 33 | G2 / SLD5 / UD1 |
| 36 | B0 / SLD0 / LD0 | 35 | G1 / SLD4 / UD0 |
| 38 | VCC (APEX) | 37 | G0 / SLD3 / LD3 |
| 40 | N/C | 39 | B2 / SLD2 / LD2 |

## P5: IDE/Hard Drive (40 way header)

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | -Reset | 2 | 0 Volts DC (Ground) |
| 3 | Data bit 7 (HD) | 4 | Data bit 8 (HD) |
| 5 | Data bit 6 (HD) | 6 | Data bit 9 (HD) |
| 7 | Data bit 5 (HD) | 8 | Data bit 10 (HD) |
| 9 | Data bit 4 (HD) | 10 | Data bit 11 (HD) |
| 11 | Data bit 3 (HD) | 12 | Data bit 12 (HD) |
| 13 | Data bit 2 (HD) | 14 | Data bit 13 (HD) |
| 15 | Data bit 1 (HD) | 16 | Data bit 14 (HD) |
| 17 | Data bit 0 (HD) | 18 | Data bit 15 (HD) |
| 19 | 0 Volts DC (Ground) | 20 | Not used |
| 21 | Not used | 22 | 0 Volts DC (Ground) |
| 23 | -IO Write (HD) | 24 | 0 Volts DC (Ground) |
| 25 | -IO Read (HD) | 26 | 0 Volts DC (Ground) |
| 27 | Not used | 28 | ALE (HD) |
| 29 | Not used | 30 | 0 Volts DC (Ground) |
| 31 | IRQ14 | 32 | IOCS16 |
| 33 | Address 1 (HD) | 34 | Ground/Float (via link) |
| 35 | Address 0 (HD) | 36 | Address 2 (HD) |
| 37 | -Chip Select 0 (HD) | 38 | -Chip Select 1 (HD) |
| 39 | IDE LED Drive | 40 | 0 Volts DC (Ground) |

## P6: Digital I/O Port (26 way header)

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | PA0 | 2 | PB0 |
| 3 | PA1 | 4 | PB1 |
| 5 | PA2 | 6 | PB2 |
| 7 | PA3 | 8 | PB3 |
| 9 | PA4 | 10 | PB4 |
| 11 | PA5 | 12 | PB5 |
| 13 | PA6 | 14 | PB6 |
| 15 | PA7 | 16 | PB7 |
| 17 | PC0 | 18 | PC4 |
| 19 | PC1 | 20 | PC5 |
| 21 | PC2 | 22 | PC6 |
| 23 | PC3 | 24 | PC7 |
| 25 | 0 Volts (Ground) | 26 | 0 Volts (Ground) |

## P7: Video (10 way header)

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | Analogue RED | 2 | 0 Volts (Ground) |
| 3 | Analogue GREEN | 4 | 0 Volts (Ground) |
| 5 | Analogue BLUE | 6 | 0 Volts (Ground) |
| 7 | Horizontal Sync | 8 | 0 Volts (Ground) |
| 9 | Vertical Sync | 10 | 0 Volts (Ground) |

## P8: Serial 1 (10 way header)

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | -Data Carrier Detect | 2 | -Data Set Ready |
| 3 | Receive Data | 4 | -Ready To Send |
| 5 | Transmit Data | 6 | -Clear To Send |
| 7 | -Data Terminal Ready | 8 | -Ringing Indicator |
| 9 | 0 Volts (Ground) | 10 | Not used |

## P9: Floppy (34 way header)

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | 0 Volts (Ground) | 2 | +RPM/Low Current |
| 3 | 0 Volts (Ground) | 4 | Not used |
| 5 | 0 Volts (Ground) | 6 | Not used |
| 7 | 0 Volts (Ground) | 8 | -Index |
| 9 | 0 Volts (Ground) | 10 | -Motor 0 |
| 11 | 0 Volts (Ground) | 12 | -Drive select 1 |
| 13 | 0 Volts (Ground) | 14 | -Drive select 0 |
| 15 | 0 Volts (Ground) | 16 | -Motor 1 |
| 17 | 0 Volts (Ground) | 18 | +Direction |
| 19 | 0 Volts (Ground) | 20 | -Step |
| 21 | 0 Volts (Ground) | 22 | -Write Data |
| 23 | 0 Volts (Ground) | 24 | -Write Gate |
| 25 | 0 Volts (Ground) | 26 | -Track 0 |
| 27 | 0 Volts (Ground) | 28 | -Write Protect |
| 29 | 0 Volts (Ground) | 30 | -Read Data |
| 31 | 0 Volts (Ground) | 32 | +Head Select |
| 33 | 0 Volts (Ground) | 34 | +Disk Change |

## P10: Serial 2 (10 way header)

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | -Data Carrier Detect | 2 | -Data Set Ready |
| 3 | Receive Data | 4 | -Ready To Send |
| 5 | Transmit Data | 6 | -Clear To Send |
| 7 | -Data Terminal Ready | 8 | -Ringing Indicator |
| 9 | 0 Volts (Ground) | 10 | Not used |

## P11: IDE Activity LED (2 way header)

| Pin No. | Signal |
|---|---|
| 1 | IDE LED +ve |
| 2 | IDE LED -ve |

## I/O Address Map

| Hex Range | Device | Occupied by APEX (default) | Occupied by APEX-CI 2 (default) |
|---|---|---|---|
| 0000 - 00lF | DMA Controller 1 | ✓ | |
| 0020 - 003F | Interrupt Controller 1, Master | ✓ | |
| 0040 - 005F | Timer & Index registers for SCATsx | ✓ | |
| 0060 - 006F | 8042 (Keyboard & Mouse) | ✓ | |
| 0070 - 007F | Realtime Clock, NMI Mask | ✓ | |
| 0080 - 008F | POST, DMA Page Register | ✓ | |
| 00A0 - 00BF | Interrupt Controller 2, Slave | ✓ | |
| 00C0 - 00DF | DMA Controller 2 | ✓ | |
| 00F0 | Clear Maths Coprocessor Busy | ✓ | |
| 00F1 | Reset Maths Coprocessor | | |
| 00F8 - 00FF | Maths Coprocessor | ✓ | |
| 0100H | E²PROM Access | ✓ | |
| 0101H | Watchdog | ✓ | |
| 0102H | FLASH Access | ✓ | |
| 0103H | Peripheral disable | ✓ | |
| 0104H | Serial Port Rs232 or 485/ Half or Full Duplex | | ✓ |
| 0105H | 24 Digital I/O | | ✓ |
| 01F0 - 01F8 | Hard (fixed) Disk Controller | | ✓ |
| 0200 - 0207 | Games port | | |
| 0278 - 027F | Parallel Printer Port 2 | | |
| 0208 - 021A | EMS Page registers ( either 208 or 218, etc) | ✓ | |
| 02E8 - 02EF | Serial Port 4 | | ✓ |
| 02F8 - 02FF | Serial Port 2 | ✓ | |
| 0300 - 031F | Prototype Card/Digital PIO | | ✓ |
| 0360 - 036F | Reserved | | |
| 0378 - 037F | Parallel Printer Port 1 | ✓ | |
| 0380 - 038F | SDLC, Bi-synchronous 2 | | |
| 03A0 - 03AF | Bi-synchronous 1 | | |
| 03B0 - 03DF | Video Adapter | | ✓ |
| 03E8 - 03EF | Serial Port 3 | | ✓ |
| 03F0 - 03F7 | Floppy Diskette Controller | | ✓ |
| 03F8 - 03FF | Serial Port 1 | ✓ | |

## APEX 104-CI 2 Extended I/O Port Map

**104Hex:** Serial Com port mode select register (write only)
(As per DX Rev B)

Data bit 0: primary port RS485 Full/half duplex.(0=full, 1= half)
Data bit 1: secondary port RS485 Full/half duplex.(0=full, 1= half)
Data bit 2: primary port RS232/485.(0=232, 1= 485)
Data bit 3: secondary port RS232/485.(0=232, 1= 485)

**Note: The power on default is all bits = 0.**

**105Hex:** 8255 enable/address select (write only)

Data bit 0: Base address select 0=200H, 1= 300H
Data bit 1: Enable/ disable 8255 0=disable, 1= enable

**Note : The power on default value for each of the above is 0.**

## Interrupt Assignments

| Interrupt | Device | Occupied on APEX (default) | Occupied by APEX-CI 2 (default) |
|---|---|---|---|
| NMI | Parity Check (generates IOCHCK on error) | ✓ | |
| 0 | Timer | ✓ | |
| 1 | Keyboard (Output Buffer Full) | ✓ | |
| 2 | Cascaded from Interrupt 9 | ✓ | |
| 3 | Serial Port 2 (also 4, 6 & 8 if sharing interrupts) | ✓ | ✓ |
| 4 | Serial Port 1 (also 3, 5 & 7 if sharing interrupts) | ✓ | ✓ |
| 5 | Parallel Port 2 | | ✓ |
| 6 | Floppy Diskette Controller | | ✓ |
| 7 | Parallel Port 1 | ✓ | |
| 8 | Real Time Clock | ✓ | |
| 9 | VGA controller | | |
| 10 | Unassigned | | |
| 11 | Unassigned | | |
| 12 | PS/2 Mouse | ✓ | |
| 13 | Unassigned | | |
| 14 | Hard (Fixed) Disk Controller | | ✓ |
| 15 | Unassigned | | |

## DMA Assignments

| DMA Channel | 8/16 bit Peripherals | Device | Occupied on APEX (default) | Occupied by APEX-CI 2 (default) |
|---|---|---|---|---|
| 0 | 8 bit | Available (usually Refresh but free on APEX) | | |
| 1 | 8 bit | Available | | |
| 2 | 8 bit | Diskette Drive | | ✓ |
| 3 | 8 bit | Available | | |
| 4 | 16 bit | Cascaded to 1st DMA controller | ✓ | |
| 5 | 16 bit | Available | | |
| 6 | 16 bit | Available | | |
| 7 | 16 bit | Available | | |

# Appendix A - Using the Digital PIO

## Introduction

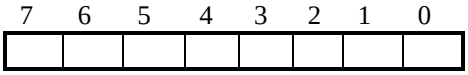
The CI card contains one 8255 chip. The chip has three 8 bit ports which can be programmed as input or output by writing a control word to the control port. (See Table 3). Port A and B must be all input or all output. Port C may be split into two 4 bit sections each of which may be input or output.

The chip occupies 4 read/write addresses in the IBM-PC port map.

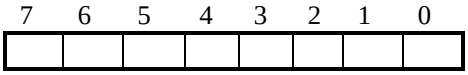
Address

| | |
|---|---|
| Base + 0 | Port A |
| Base + 1 | Port B |
| Base + 2 | Port C |
| Base + 3 | Command Port |

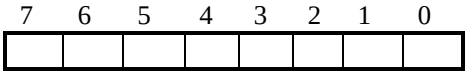
### Output Ports



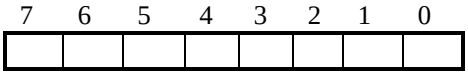

DATA (8255 PORT A)




DATA (8255 PORT B)




DATA (8255 PORT C)




CONTROL

### Control Bit Operations

| | | | | |
|---|---|---|---|---|
| Bit 0 | = | Port C (Lower) | 0 = Output | 1 = Input |
| Bit 1 | = | Port B | 0 = Output | 1 = Input |
| Bit 2 | = | Mode Selection | 0 = Mode 0 | 1 = Mode 1 |
| Bit 3 | = | Port C (Upper) | 0 = Output | 1 = Input |
| Bit 4 | = | Port A | 0 = Ouput | 1 = Input |
| Bit 5,6 | = | Mode Selection | 00 = Mode 0<br>1X = Mode 2 | 01 = Mode 1 |
| Bit 7 | = | Mode Set Flag | 0 = Inactive | 1 = Active |

See Table 3 for Quick Set-up Guide

# Electrical Options

## Input Conditioning

The 8255 has high impedance inputs. In electrically noisy environments it is advised to terminate the input lines with resistors. The termination may be pull up (to 5V) or pull down to 0V).

## Input/Output Connections

A 26 way insulation displacement connector (IDC) is provided (P6) on the CI board for I/O channel signal connection. If access to individual channels is required, a 26 way IDC ribbon cable may be used to connect the I/O channels to screw terminal blocks or other similar output connectors.

### Connector Pin Details (P6)

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | PA0 | 2 | PB0 |
| 3 | PA1 | 4 | PB1 |
| 5 | PA2 | 6 | PB2 |
| 7 | PA3 | 8 | PB3 |
| 9 | PA4 | 10 | PB4 |
| 11 | PA5 | 12 | PB5 |
| 13 | PA6 | 14 | PB6 |
| 15 | PA7 | 16 | PB7 |
| 17 | PC0 | 18 | PC4 |
| 19 | PC1 | 20 | PC5 |
| 21 | PC2 | 22 | PC6 |
| 23 | PC3 | 24 | PC7 |
| 25 | 0 Volts (Ground) | 26 | 0 Volts (Ground) |

## Programming Guide

The state of the input lines may be determined by using either of the following methods :

(a) Microsoft BASIC A or GW BASIC

X = INP (P)

Returns the byte from port P and assigns this value to the variable, X.

(b) 8088/8086 Assembly Language

```
PORT EQU 0300H

GETDAT :

        MOV   DX, PORT
        IN    AL,DX
        RET
```

The state of the output lines may be modified by using either of the following methods :-

(a) Microsoft BASIC A or GW BASIC

OUT P,D

Outputs the byte D to port P.

(b) 8088/8086 Assembly Language

```
PORT EQU 0300H

PITDAT :

        MOV DX, PORT
        MOV AX, DATA
        OUT DX,AL
        RET
```

The following table gives a summary of the most commonly used 'control words' which must be written to the control port to configure the 8255 before using this module.

The 8255 can operate in one of 3 modes (Mode 0-2).

In the first mode (mode 0) the 8255 provides simple I/O for 3, 8 bit ports. Data is simply written to or read from a specified port (A, B or C) without the use of handshaking. The following Control Code Table (3) assumes mode 0 is required.

Mode 1 enables the transfer of data to or from a specified 8 bit port (A or B) in conjunction with strobes or handshaking signals.

In mode 2 data is transferred via one bi-directional 8 bit port (A) with handsheskes (Port C).

| Control Word (Hex) | Control Word Decimal | Sets All of Port A | Sets All of Port B to | Sets High 4 Bits of Port C to | Sets Low 4 Bits of Port C to |
|---|---|---|---|---|---|
| 80 | 128 | Output | Ouput | Output | Output |
| 81 | 129 | Output | Output | Output | Input |
| 82 | 130 | Output | Input | Ouput | Output |
| 83 | 131 | Output | Input | Ouput | Input |
| 88 | 136 | Output | Output | Input | Output |
| 89 | 137 | Output | Output | Input | Input |
| 8A | 138 | Output | Input | Input | Output |
| 8B | 139 | Output | Input | Input | Input |
| 90 | 144 | Input | Ouput | Output | Output |
| 91 | 145 | Input | Output | Output | Input |
| 92 | 146 | Input | Input | Output | Output |
| 93 | 147 | Input | Input | Output | Input |
| 98 | 152 | Input | Output | Input | Output |
| 99 | 153 | Input | Ouput | Input | Input |
| 9A | 154 | Input | Input | Input | Output |
| 9B | 155 | Input | Input | Input | Input |

Table 3 - Control Word Table

### Example Program

The following program written in Microsoft QBASIC will test the operation of the PIO if a loopback is connected.

The loopback connector should loop all bits of port A to all bits of port B and the bottom four bits of port C to the top four bits of port C.

```
REM ****** APEX PIO LOOP BACK TEST PROGRAM *********

REM Set base address of PIO
BASEADDR = &H300

REM Set PORT A to OUTPUT, PORT B to INPUT
REM Low 4 bits of PORT C to OUTPUT, High 4 bits of PORT C to INPUT
OUT BASEADDR + 3, &H83

errnum = 0
REM ** First check ports A and B **
outval = 0
errnum = 0
REM output to port A
DO
    OUT BASEADDR, outval
    REM Check the value on port B
        IF INP(BASEADDR + 1) <> outval THEN
            PRINT "PORT A-B Failed"
            outval = 256
            errnum = 1
    ELSE
        outval = outval + 1
    END IF
LOOP UNTIL outval = 256
IF errnum = 0 THEN PRINT "PORT A-B Passed"2


REM ** Now check port C **
outval = 0
errnum = 0
DO
    REM Output to port C
```

```
    OUT BASEADDR + 2, outval
    IF (INP(BASEADDR + 2) / 16) <> outval THEN
        PRINT "PORT C Failed"
        outval = 15
        errnum = 1
    ELSE
        outval = outval + 1
    END IF
LOOP UNTIL outval = 15
IF errnum = 0 THEN PRINT "PORT C Passed"

END
```

## Application Notes for Interfacing to the 8255 I/O Port

The signals present at ports A, B and C on either the NMOS or CMOS 8255 are TTL (Transistor Transistors Logic) compatible, that is they will interface into standard 74LS logic. However, TTL has limitations when interfacing to other circuitry.

The following should be considered when attempting to interface to the 8255 I/O Port.

1. The 8255 cannot drive high capacitances.

2. The 8255 cannot sink loads greater than 2.5mA and retain an output voltage that is TTL compatible.

3. The 8255 cannot source loads greater than - 200uA (1-400uA for CMOS version) and retain an output voltage that is TTL compatible.

4. The 8255 cannot interface to any voltage greater than VCC (VDD) + 0.5 or lower than -0.5V.

5. The 8255 cannot drive long lengths of cable into other TTL compatible devices. TTL is a standard for on-board interfacing primarily and is too susceptible to interference and noise to be used with long cable runs.

## General TTL Requirement

| LOW | HIGH |
|---|---|
| Input 0.5 - 0.8V | 2.0 - Vcc (VDD) |
| Output 0 - 0.45V | 2.4 - Vcc (VDD) |

Characteristics :

| DC Parameter | Symbol | 8255 MIN MAX LIMITS | 82C55/71055 MIN MAX LIMITS |
|---|---|---|---|
| Input Voltage High | VIH | 2 VCC | 2.2 VDD+0.3V |
| Input Voltage Low | VIL | -0.5V 0.8V | -0.5V 0.8V |
| Output Voltage High | V0H | 2.4V @-20uA | 3.5 IOH=400uA |
| Output Voltage Low | VOL | IOL=1.7MA 0.45V | IOL=2.5MA 0.4V |
| Input Leakage Current High | ILIH | VI=VCC 10uA | VI=VDD 10uA |
| Input Leakage Current Low | ILIL | -10uA | VI-0V -10uA |
| Output Leakage Current High | IL0H | 10uA | VO=VDD 10uA |
| Output Leakage Current Low | IL0L | -10uA | VO = 0V -10uA |
| Supply Current (Dynamic) | IDD1 | 120mA | 15MA |
| Supply Current (Standby) | IDD2 | 120mA | 15MA |

## PIO Glossary

VIH High level input voltage - the minimum and maximum voltages that can be applied (reference to 0V) for a high to be recognised.

VIL Low level input voltage - the minimum and maximum voltages that can be applied (reference to 0V) for a low to be recognised.

VOH High level output voltage - the minimum voltage that will be presented at the output as a high at a given maximum current source current.

VOL Low level output voltage - the maximum voltage that will be presented at the output as a low at a given maximum current load.

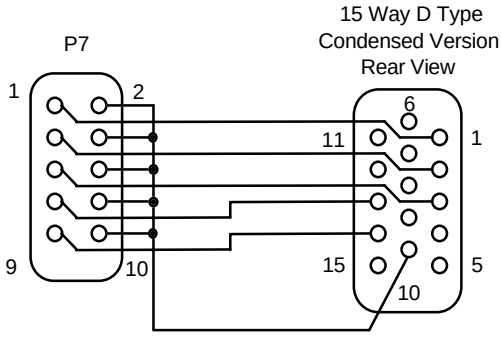
# Appendix B - Connecting to Displays & Peripherals

## Connecting to the CRT display Header

The specifications of the types of CRT displays you can use via this connector are listed in the Technical Hardware Section, but as a good starting point use either a standard VGA or SVGA PC compatible screen.

Locate the connector P7 on the PCB and either :-

a. connect the optional cable labelled CRT to this connector
or
b. wire the connector as per the details below :-

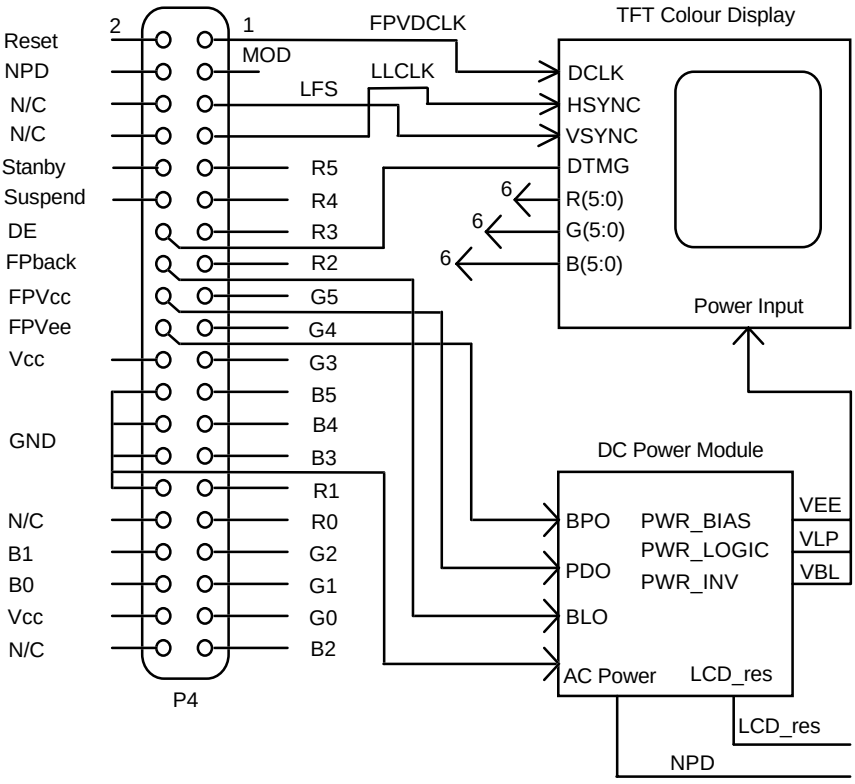



Please note that the pinout of P7 is incompatible with normal condensed 15 way D type connector used to drive CRT displays and that the above translation is required.

## Connecting to the LCD Display Header (P4)

The specifications of the types of LCD displays you can use via this connector are listed in the Technical Hardware Section, but as a good starting point use a standard VGA TFT screen.

Locate the connector P4 on the PCB and wire the connector as follows :-




Note
The cable is not supplied for this connector due to the varied nature of LCD display interfaces and pin outs.

## Video Outputs

The APEX-CI 2 unit offers dual output video drive capability. By using the new CIRRUS LOGIC CL-GD6235 video controller the APEX-CI 2 unit is capable of driving both CRT and LCD displays in various modes. Connected to the video controller is 512KBytes of VRAM in the form of a single 256K x 16 bit memory IC. This device offer the user a wide range of display types giving excellent display features.
A full specification of the CIRRUS LOGIC CL-GD6235 IC is obtainable via from your supplier. However we have listed in the following sections some of the more important features which we think will be of use and interest in helping you get the most from this APEX-CI 2 unit.

## CRT Display Mode

The CRT output is capable of driving VGA displays with resolutions upto 1024 x 768 pixels by 16 colours and 800 x 600 with 256 colours.
The 16 bit local-bus interface is used to connect to the microprocessor.
Using the SimulSCAN™ feature (a technique introduced by CIRRUS LOGIC for achieving simultaneous CRT and LCD output) it is possible to develop your application on a desktop PC screen and then to convert over to an LCD display with the smallest of effort. The fact that you can run both displays together can greatly ease the the display formating process for LCDs.

## CRT Displays

The Cirrus Logic 6235 display driver can drive many different CRT display configurations. The following table shows the most popular formats. If the CRT type you require is not shown please call your supplier for further details.

# CRT Display Types

## IBM Standard Video Modes

| Mode No. | VESA No. | Colours | Char v Row | Char Cell | Screen Format | Display Mode | Horiz Freq KHz | Vert Freq Hz |
|---|---|---|---|---|---|---|---|---|
| 0,1 | 0,1 | 16/256K | 40 x 25 | 9 x 16 | 360 x 400 | Text | 31.5 | 70 |
| 2,3 | 2,3 | 16/256K | 80 x 25 | 9 x 16 | 720 x 400 | Text | 31.5 | 70 |
| 4,5 | 4,5 | 4/256K | 40 x 25 | 8 x 8 | 320 x 200 | Graphics | 31.5 | 70 |
| 6 | 6 | 2/256K | 80 x 25 | 8 x 8 | 640 x 200 | Graphics | 31.5 | 70 |
| 7 | 7 | Mono | 80 x 25 | 9 x 16 | 720 x 400 | Text | 31.5 | 70 |
| D | D | 16/256K | 40 x 25 | 8 x 8 | 320 x 200 | Graphics | 31.5 | 70 |
| E | E | 16/256K | 80 x 25 | 8 x 14 | 640 x 200 | Graphics | 31.5 | 70 |
| F | F | Mono | 80 x 25 | 8 x 14 | 640 x 350 | Graphics | 31.5 | 70 |
| 10 | 10 | 16/256K | 80 x 25 | 8 x 14 | 640 x 350 | Graphics | 31.5 | 70 |
| 11 | 11 | 2/256K | 80 x 30 | 8 x 16 | 640 x 480 | Graphics | 31.5 | 60 |
| 12 | 12 | 16/256K | 80 x 30 | 8 x 16 | 640 x 480 | Graphics | 31.5 | 72 |
| 13 | 13 | 256/256K | 40 x 25 | 8 x 8 | 320 x 200 | Graphics | 31.5 | 70 |

## Cirrus Logic Extended Video Modes

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 14 | - | 16/256K | 132 x 25 | 8 x 16 | 1056 x 400 | Text | 31.5 | 70 |
| 54 | 10A | 16/256K | 132 x 43 | 8 x 8 | 1056 x 350 | Text | 31.5 | 70 |
| 55 | 109 | 16/256K | 132 x 25 | 8 x 14 | 1056 x 350 | Text | 31.5 | 70 |
| 58,6A | 102 | 16/256K | 100 x 37 | 8 x 16 | 800 x 600 | Graphics | 35.2 | 56 |
| 58,6A | 102 | 16/256K | 100 x37 | 8 x 16 | 800 x 600 | Graphics | 37.8 | 60 |
| 58,6A | 102 | 16/256K | 100 x 37 | 8 x 16 | 800 x 600 | Graphics | 48.1 | 72 |
| 5C | 103 | 256/256K | 100 x 37 | 8 x 16 | 800 x 600 | Graphics | 35.2 | 56 |
| 5C | 103 | 256/256K | 100 x 37 | 8 x 16 | 800 x 600 | Graphics | 37.9 | 60 |
| 5C | 103 | 256/256K | 100 x 37 | 8 x 16 | 800 x 600 | Graphics | 48.1 | 72 |
| 5D | 104 | 16/256K | 128 x 48 | 8 x 16 | 1024 x 768 | Graphics | 35.5 | 87 |
| 5D | 104 | 16/256K | 128 x 48 | 8 x 16 | 1024 x 768 | Graphics | 48.3 | 60 |
| 5D | 104 | 16/256K | 128 x 48 | 8 x 16 | 1024 x 768 | Graphics | 56 | 70 |
| 5D | 104 | 16/256K | 128 x 48 | 8 x 16 | 1024 x 768 | Graphics | 58 | 72 |
| 5F | 101 | 256/256K | 80 x 30 | 8 x 16 | 640 x 480 | Graphics | 31.5 | 60 |
| 5F | 101 | 256/256K | 80 x 30 | 8 x 16 | 640 x 480 | Graphics | 37.9 | 72 |
| 60 | 105 | 256/256K | 128 x 48 | 8 x 16 | 1024 x 768 | Graphics | 35.5 | 87 |
| 60 | 105 | 256/256K | 128 x 48 | 8 x 16 | 1024 x 768 | Graphics | 48.3 | 60 |
| 60 | 105 | 256/256K | 128 x 48 | 8 x 16 | 1024 x 768 | Graphics | 56 | 70 |
| 60 | 105 | 256/256K | 128 x 48 | 8 x 16 | 1024 x 768 | Graphics | 58 | 72 |
| 64 | 111 | 64K | - | - | 640 x 480 | Graphics | 31.5 | 60 |
| 64 | 111 | 64K | - | - | 640 x 480 | Graphics | 37.9 | 72 |
| 65 | 114 | 64K | - | - | 800 x 600 | Graphics | 35.2 | 56 |
| 65 | 114 | 64K | - | - | 800 x 600 | Graphics | 37.8 | 60 |
| 66 | 110 | 32K | - | - | 640 x 480 | Graphics | 31.5 | 60 |
| 66 | 110 | 32K | - | - | 640 x 480 | Graphics | 37.9 | 72 |
| 67 | 113 | 32K | - | - | 800 x 600 | Graphics | 31.5 | 56 |
| 6C | 106 | 16/256K | 160 x 64 | 8 x 16 | 1280 x 1024 | Graphics | 48 | 87 |
| 6D | - | 256/256K | 160 x 48 | 8 x 16 | 1280 x 1024 | Graphics | 48 | 87 |
| 71 | 112 | 16M | 80 x 30 | 8 x 16 | 640 x 480 | Graphics | 31.5 | 60 |
| 74 | - | 64K | - | - | 1024 x 768 | Graphics | 35.5 | 87 |

✞ denotes INTERLACED modes
▯ denotes 32K Direct-Colour/256 colour Mixed Mode
Shaded modes required 2MBytes of video memory fitted.

### Video Drivers

Blue Chip Technology provide drivers for a wide range of operating systems and popular applications. Diskettes containing drivers required for DOS & Windows are located at the rear of this manual. For other operating systems please contact BCT.

## LCD Display Modes

The LCD output is capable of driving the following display types :-

- Dual-Scan Monochrome
- Dual-Data Monochrome
- Passive-matrix Monochrome
- Colour TFT
- Colour STN
- Dual Scan STN

Grayscale mapping is provided by AutoMap™ which maps 256 colours into a monochrome image; the colours then appear either in 16 shades of grey with greyscale enhancement, or 64 shades of grey in 256-colour mode. There are also four greyscale mapping options available through register control:

- NTSC weighted
- DAC Look-up table "green' output
- 4 or 6 bit video data direct
- Attribute Controller 64-shade colour data

A colour STN panel can be driven by either 8 or 16 bit interfaces, and give 256 simultaneous colours from a palette of 256K.

A colour TFT panel can support 9, 12, 15 or 18 bit panels and give 256 simultaneous colours from a palette of 256K.

The CL-GD6235 offers true packed-pixel addressing, colour expansion for 8 bit-per-pixel graphics, and a hardware cursor, thus improving Windows performance.

## Power Management

The family also offers Standby and Suspend power-management modes which reduce the power consumption when the system is not in active use. The internal Standby Counter initiates Standby mode without software intervention. During this reduced-power mode, the LCD panel is turned off while the video memory can still be accessed and modified.

The CL-GD6235 provides efficient power management of the display system by turning-off, or shutting-down the LCD flat panel and CRT when not being used. The device offers both hardware methods (using device pins) and software methods (using programmable timers and on-chip registers) to control the LCD panel and or CRT display.

In **NORMAL MODE** the LCD is being used, and the following occur :

- Display is active and receives power
- Full-screen refresh occurs
- CPU and access :
  - Video memory
  - RAMDAC
  - I/O registers
- Refresh is provided to the video memory

In **STANDBY MODE** the controller stops power to the LCD panel. As a result the following occurs :

- LCD panel power-down sequence occurs automatically when this mode is entered
- VCLK oscillator is stopped
- MCLK is divided by six
- No clock is provided to the CRT controller
- Video DAC is in lower power mode
- Video display memory refresh is maintained
- CPU can access and modify the video memory
- When standby mode is terminated the previous state is restored

## LCD Connector (P4) Pin out Details

The following table shows the pin out for the LCD connector together with a description for each pin. **Note the connector is a female type** and the table shows **looking down on top** of the connector from the main component side of the PCB.

| Pin No. | Description | Pin No. | Description |
|---|---|---|---|
| 2 | LCDRST | 1 | FPVDCLK |
| 4 | NPD | 3 | MOD |
| 6 | FVSYNC | 5 | LFS |
| 8 | FHSNYC | 7 | LLCLK |
| 10 | STANBY | 9 | R5 |
| 12 | SUSPEND | 11 | R4 |
| 14 | DE | 13 | R3 / SUD7 |
| 16 | FPBACK | 15 | R2 / SUD6 |
| 18 | FPVCC | 17 | G5 / SUD5 |
| 20 | FPVEE | 19 | G4 / SUD4 |
| 22 | VCC (APEX) | 21 | G3 / SUD3 |
| 24 | GND (APEX) | 23 | B5 / SUD2 |
| 26 | GND (APEX) | 25 | B4 / SUD1 |
| 28 | GND (APEX) | 27 | B3 / SUD0 |
| 30 | GND (APEX) | 29 | R1 / SLD7 / UD3 |
| 32 | N/C | 31 | R0 / SLD6 / UD2 |
| 34 | B1 / SLD1 / LD1 | 33 | G2 / SLD5 / UD1 |
| 36 | B0 / SLD0 / LD0 | 35 | G1 / SLD4 / UD0 |
| 38 | VCC (APEX) | 37 | G0 / SLD3 / LD3 |
| 40 | N/C | 39 | B2 / SLD2 / LD2 |

## LCD Signal Descriptions

**B[5:0]**

BLUE BITS [5:0]. These bits contain the BLUE colour data for TFT colour flat panel displays.

**DE**

DISPLAY ENABLE. For those flat panels that require an external display enable, this pin is used to provide a data enable. For the CL-GD6235 it is the second Shift Clock output for STN single-scan dual-clock colour panels.

**FPVDCLK**

FLAT PANEL VIDEO CLOCK. This signal is used to drive the flat panel shift clock which is designated as CP0 by some panel manufactures.

**G[5:0]**

GREEN BITS [5:0]. These bits contain the GREEN colour data for TFT colour flat panel displays.

**LD[3:0]**

LOWER DATA [3:0]. The lower Data bits [3:0] are typically used with monochrome dual-scan flat panels to provide 4-bit parallel data for the lower portion of the panel.

**LFS**

LCD FRAME START. This output provides a pulse to start a new frame on flat panels.

**LLCLK**

LCD LINE CLOCK. This output is used to drive the LCD panel line clock. This signal is also designated as LP or CP by some panel manufactures.

**MOD**

MODULATION. This output provides AC inversion. It should be connected to the MOD, FR or DF inputs of the panel, and is appropriate. Some panel manufactures provide this function in the panel circuitry.

**R[5:0]**

RED BITS [5:0]. These bits contain the RED colour data for TFT colour flat panel displays.

**SLD[7:0]**

STN LOWER DATA [7:0]. The lower Data bits [7:0]are for use with colour STN LCD panels and are only available on the CL-GD6225/'35 chips.

**SUD[7:0]**

STN UPPER DATA [7:0]. The Upper Data bits [7:0] are for use with colour STN LCD panels and are only available on the CL-GD6225/'35 chips.

**UD[3:0]**

UPPER DATA. The Upper Data bits [3:0] are typically used with monochrome dual-scan flat panels to provide 4-bit parallel data for the upper portion of the panel.

**LCDRST**

LCD Reset. This active low signal is an optional LCD display reset input. Any logic high to low transistion on this input will clear both the LCD and CRT Enable bits in the Power Management register (CR20[6:5]). This will initiate the LCD-panel power down sequence, and will stop video memory refresh.

The logic high to low transistion on this pin does NOT restore the CRT or LCD Enable bits. These bits MUST be restored by writing to the appropriate registers.
This pin has an internal pull-up resistor and when not used it should not be connected to.

**STANDBY (Input or Output function pin)**

When the panel is on and this input is driven high, the power down sequence will start to put the system into Standby Mode. Standby Mode terminates when this pin goes low, as long as CR20[4] =' 0 ' and the standby timer has been reset.

Please ask for more detailed information if your application needs to make use of this function.

**SUSPEND**

This input pin can be used in one of two ways :

To initiate the Hardware-Suspend mode. If the SUSPEND pin is used to control Suspend Mode, CPU access will not be allowed.

To turn off the LCD display for a 'closed cover' type condition. In a closed cover type condition, CPU access is allowed, and the CRT outputs remain active.

Please ask for more detailed information if your application needs to make use of this function.

**FPBACK (Output pin)**

Flat Panel Backlight. This output pin is part of the panel power sequencing, and it should be connected to the panels backlight enable pin.

**FPVCC (Output pin)**

Flat Panel VCC. This output pin is part of the panel power sequencing, and it should be connected to the panels logic power enable input pin.

**FPVEE (Output pin)**

Flat Panel VEE. This output is pin part of the panel power sequencing, and it should be connected to the panels power enable input pin.

**NPD (Input pin)**

NO POWER-DOWN. This pin, when 'high', stops the power-down counters from decrementing. This pin is used to inhibit automatic power-down, when for example the system is supplied from an AC power source.

**FVSYNC**

VERTICAL SYNC. This is a copy of the vertical sync line as output on the CRT display connector, and would not be used in normal LCD flat panel operation.

**FHSYNC**

HORIZONTAL SYNC. This is a copy of the horizontal sync line as output on the CRT display connector, and would not be used in normal LCD flat panel operation.

## LCD Power Sequencing

The internal logic of the 6235 controls the sequencing of the LCD contrast voltage, logic power, data input and control pins. To minimise the possibility of damage to the LCD display, the 6235 provides the recommended power-up/down sequences shown below. These sequences meet most panel manufactures specifications.

It should be noted however that not all LCD display panels provide direct input channels for power sequencing control. Please ask your panel supplier for this information. If the panel you intend to use does not support power sequencing directly then a custom circuit will be needed to carry out these functions.

Blue Chip Technology can supply suitable PC/104 add on boards at extra cost.

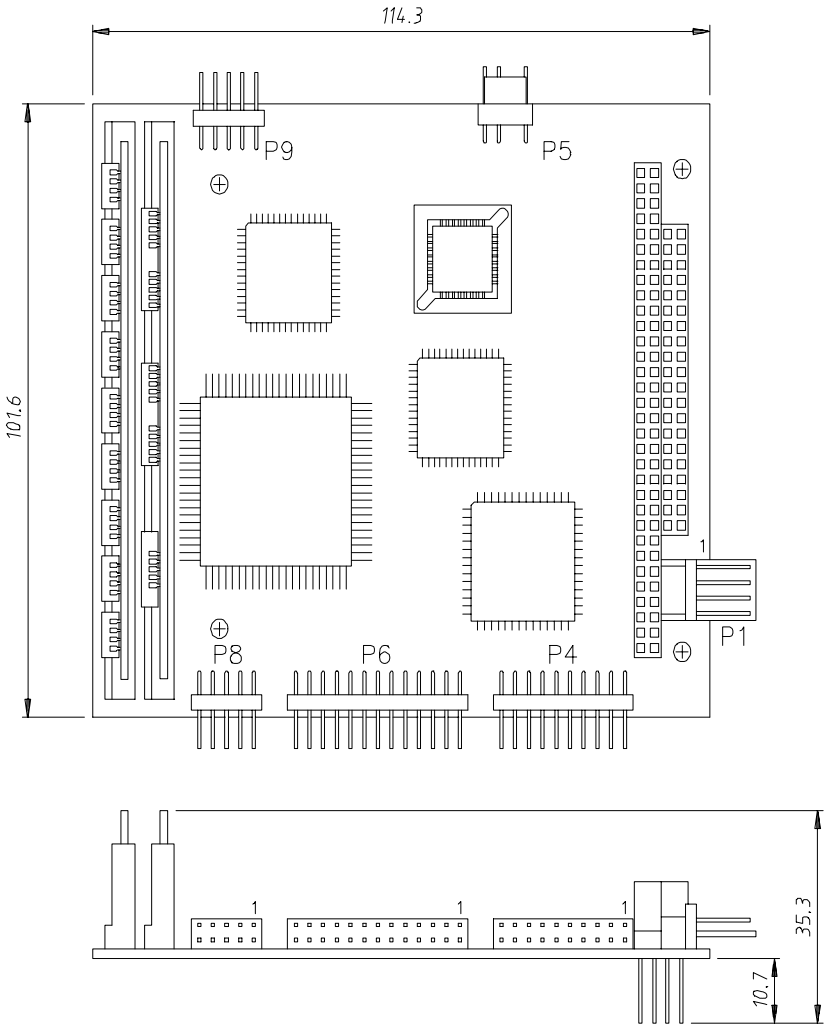
## LCD Panel Power-Down Sequence

1) Shut off FPVEE and FPBACK
2) Wait 96 - 128 ms
3) Force all 6235 panel control signals low
4) Wait 32 ms
5) Shut off FPVCC
6) Shut off internal VCLK

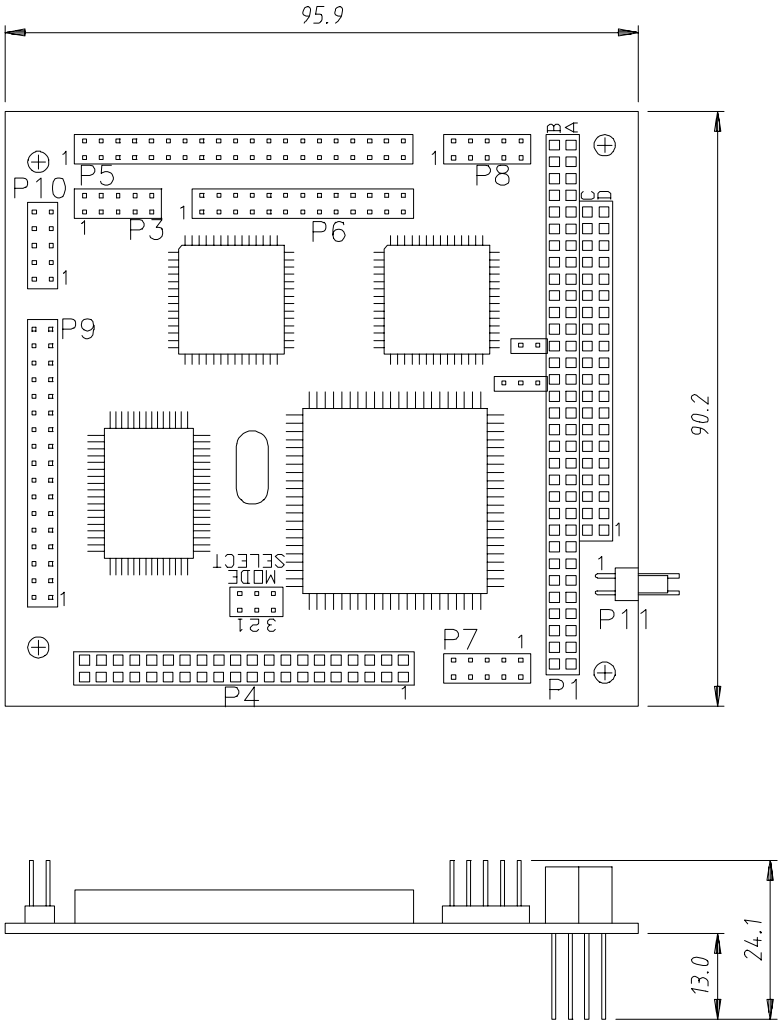
## LCD Panel Power-Up Sequence

1) Turn on VCLK increase MCLK frequency
2) Wait 32 ms
3) Enable FPVCC
4) Wait 32 ms
5) Enable 6235 panel control signals
6) Enable FPVEE and FPBACK

## APEX 104 CPU Board Layout



## APEX 104 CI-2 Board Layout



## Electromagnetic Compatibility (EMC)

This product meets the requirements of the European EMC Directive (89/336/EEC) and is eligible to bear the CE mark.

It has been assessed in a representative enclosure for an embedded application. However, because the board is designed to be installed in a variety of enclosures, certain conditions have to be applied to ensure that the compatibility is maintained. It meets the requirements for an industrial environment (Class A product) subject to those conditions.

- The board must be installed in a conductive housing which provides screening suitable for the industrial environment. Avoid holes wherever possible, where they are essential keep them as small as possible. Many small holes are preferable to a few large ones. All covers should be earthed and not create slots in the housing.

- The board must be securely screwed to the chassis to ensure good contact at the fixing holes. Cutting washers are essential.

- The power supply must be capable of filtering mains-borne transients, and must not create mains interference.

- Most EMC problems are caused by the external cabling to boards. Intermediate connectors at the chassis are strongly recommended rather than connecting external cables direct to the board. Keep internal wiring as short and direct as possible. Where practicable run internal cables against the metal chassis.

- It is imperative that any external cabling to the board is totally screened, and that the screen of the cable connects to the metal chassis and hence to earth. This facilitates shunting interference to earth rather than allowing it onto the board.

- It is recommended that round screened cables with a braided wire screen are used in preference to those with a foil screen and drain wire. Use metal connector shells which connect around the full circumference of the screen; they are far superior to those which earth the screen by a simple “pig-tail”.

- If a display is incorporated it must be compatible with the EMC requirements.

- The keyboard will play an important part in the compatibility of the processor card since it is a port into the board. A fully compatible keyboard must be used otherwise the keyboard itself may radiate or behave as if keys are pressed when subject to interference. Under these circumstances it may be beneficial to add a ferrite clamp on the keyboard lead as close as possible to the connector. A suitable type is the Chomerics type H8FE-1004-AS.

- Ensure that the screens of any external cables are bonded to a good RF earth at the remote end of the cable.

Failure to observe these recommendations may invalidate the EMC compliance.

| Warning |
| --- |
| This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures. |

## EMC Specification

The card meets the following specification when installed in a suitable representative housing:

Emissions

EN 55022:1995

| | |
|---|---|
| Radiated | Class A |
| Conducted | Class A & B |

Immunity

EN 50082-1:1992 incorporating:

| | | |
|---|---|---|
| Electrostatic Discharge | IEC 801-2:1984 | Performance Criteria B |
| Radio Frequency Susceptibility | IEC 801-3:1984 | Performance Criteria A |
| Fast Burst Transients | IEC 801-4:1988 | Performance Criteria B |