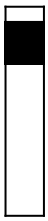

AP450GX MP Server Board Set Technical Product Specification

Order Number 282964-001

July 1996

Enterprise Server Group

0Revision History

Revision	Revision History	Date
-001	Preliminary release of the Alder Board Set Technical Product Specification.	7/96

This product specification applies only to standard AP450GX MP Server board set with BIOS identifier CD0. Information in this version of the specification applies to the BIOS 1.00.04CD0. Different versions of the BIOS may look and behave differently.

Changes to this specification will be published in the AP450GX MP Server Board Set Specification Update before being incorporated into a revision of this document.

Note: If printing this document from an electronic file, use a post script printer with the appropriate post script print driver to insure the drawings print clearly.

The AP450GX MP Server Board Set may contain design defects or errors known as errata. Current characterized errata are available upon request.

Technical updates should be obtained by calling Intel Literature or writing:

Intel Corporation
P.O. Box 7641
Mt. Prospect, Il 60056-7641

or call in North America 1-800-879-4683, Europe 44-0-1793-431-155, France 44-0-1793-421-777, Germany 44-0-1793-421-333, Japan (fax only) 81-0-120-478-832, other Countries 708-296-9333

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1 Board Set Description

1.1 Overview

The AP450GX MP Server board set is a modular, high performance server system capable of supporting up to four Pentium® Pro processors. The board set includes the system baseboard, one or two processor modules, a memory module, and an optional bus terminator module.

Board set feature	Description
Multi-processing support	Two expansion slots for processor modules; up to four Pentium Pro microprocessors (two on each module). The system may include one processor module and one terminator module, or two processor modules.
Upgradable memory	One expansion slot for a memory module, supporting up to 1GB of memory using 64 MB SIMMs. The module will support up to 2GB of memory using 128MB SIMMs when they become available. An alternate memory module will be available later to support up to 4GB of memory using 128MB DIMMs.
Bus Termination Module	Required per the GTL+ processor bus specification if only one processor module is installed in the system.
PCI bus support	Two PCI “peer” buses, each with three 32-bit PCI slots on the system base baseboard.
EISA bus support	Four dedicated EISA bus master slots on the system baseboard.
SCSI controller	Two PCI based, integrated AIC-7880 controllers; fast and wide SCSI-2 support. (At this time, Fast 20/Ultra SCSI support is not available)
Integrated Drive Electronics (IDE) interface	Provides access to two IDE hard drives; ISA-based controller. One controller on the baseboard. A second controller may be added via an add-in card.
BIOS	Basic Input/Output System (BIOS) stored in enhanced 512 KB (4Mbit) Paged Flash memory device.
Video controller	Integrated ISA based CL-GD5424 super VGA controller shipped with 512 KB of video memory (expandable to 1 MB).
External device connectors	Onboard connectors for 2 serial ports, parallel port, PS/2-compatible keyboard and mouse, and VGA monitor.
Clock	Real-time clock/calendar (RTC) chip with 8 KB of NVRAM.
Flash memory	Contains Power-on Self Test (POST), BIOS core and Setup utilities.
System hardware monitoring	Detects chassis intrusion and contains sensors for temperature, voltage, and fan failure.
I2C Bus Support	I2C bus connects all major system components together for diagnostic information
Configuration utilities	System Configuration Utility (SCU) and SCSISelect Utility

The following diagram shows the functional blocks and system architecture.

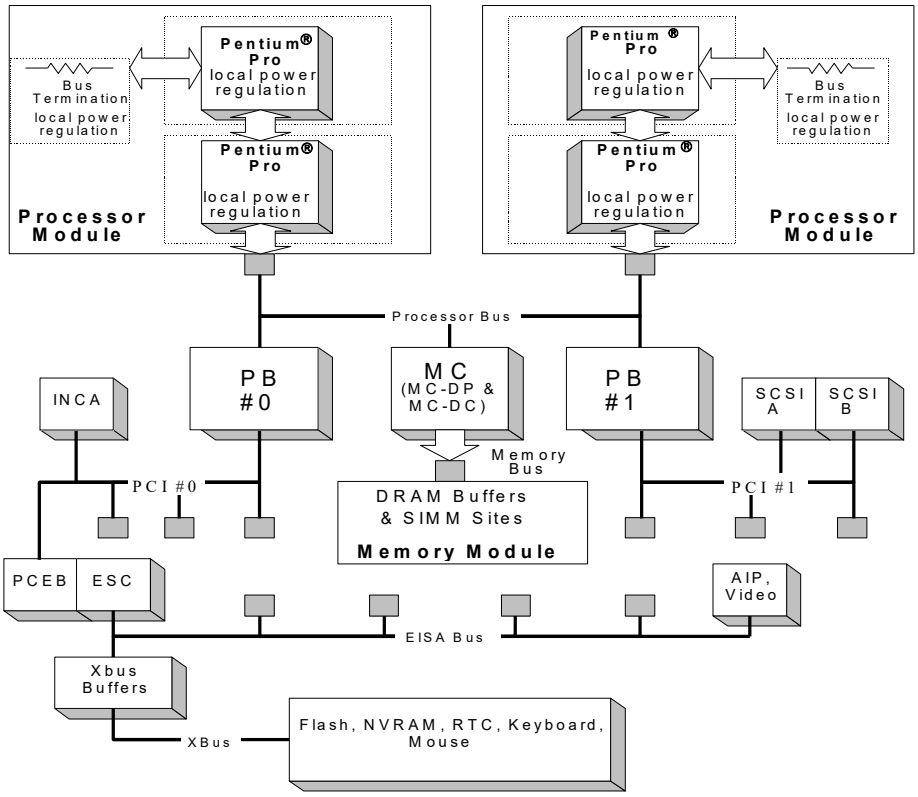


Figure 1.1 System Block Diagram

1.2Board Set Options

The server design allows expanded processor and memory capacity.

- Baseboard has two slots for processor modules and one slot for the memory module.
- Each processor module may contain one or two processors, for a configurable range from one to a maximum of four processors.
- A bus termination module is available to terminate the processor bus if only one processor module is installed in the system. Both processor slots must be filled to correctly terminate the processor bus.
- The memory module supports SIMMs up to 1 GB of memory using 64MB SIMMs.
- The memory module will support up to 2GB of memory when 128MB SIMMs have been qualified.
- A future memory module with 32 DIMM connectors will be available which will support up to 4GB of memory using 128MB DIMMs.
- The video memory is expandable up to 1MB with a 512KB memory component.

1.3Form Factor

The board set is designed to fit into a custom form factor chassis. Currently Intel's chassis, code named Poca, is the only Intel designed chassis qualified for the AP450GX board set.

1.4Placement Diagrams

The following diagram shows the placement of major components and connector interfaces on the system baseboard, and the modules. See Chapter 5 for complete mechanical drawings.

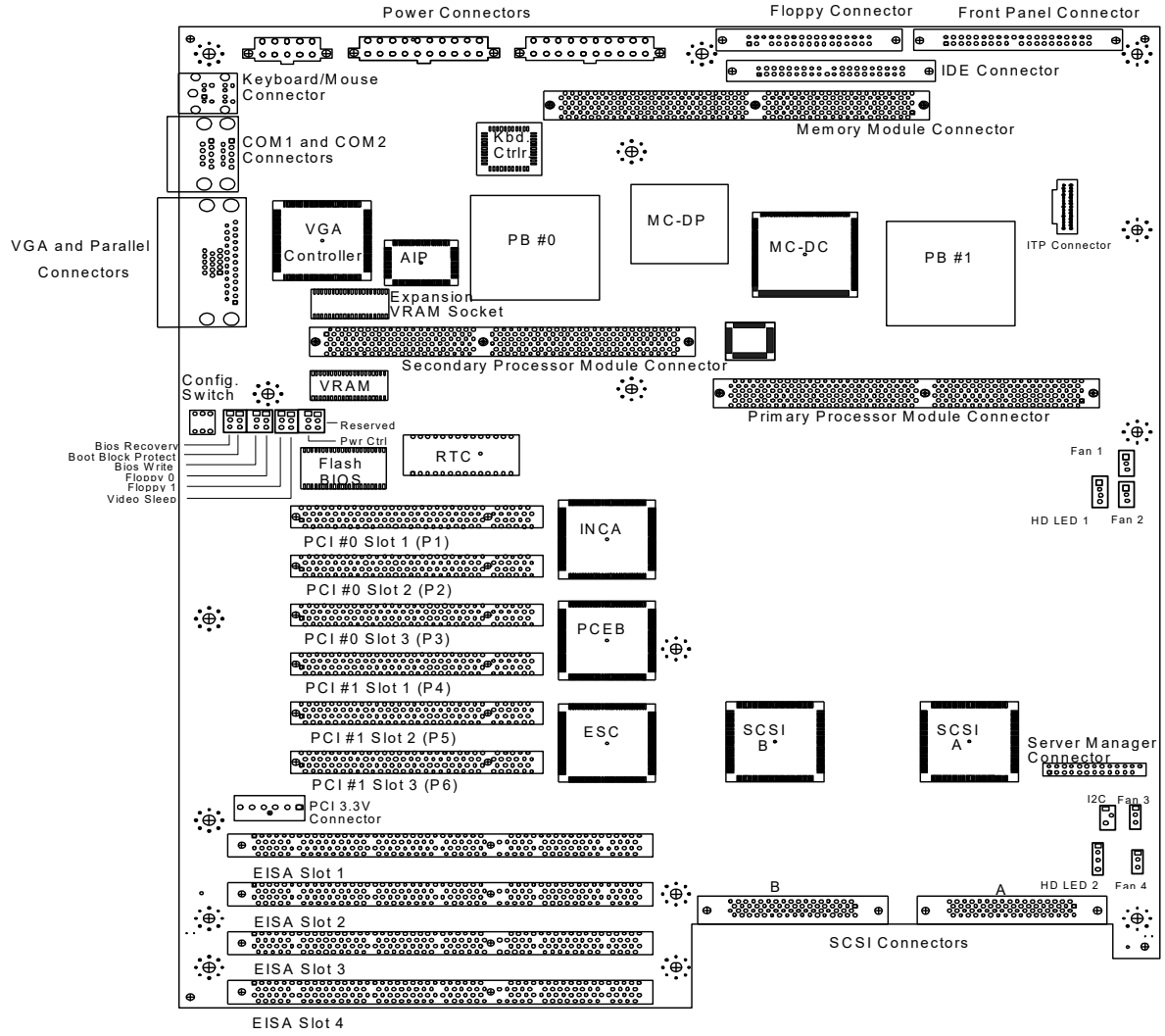


Figure 1.2 Baseboard Layout

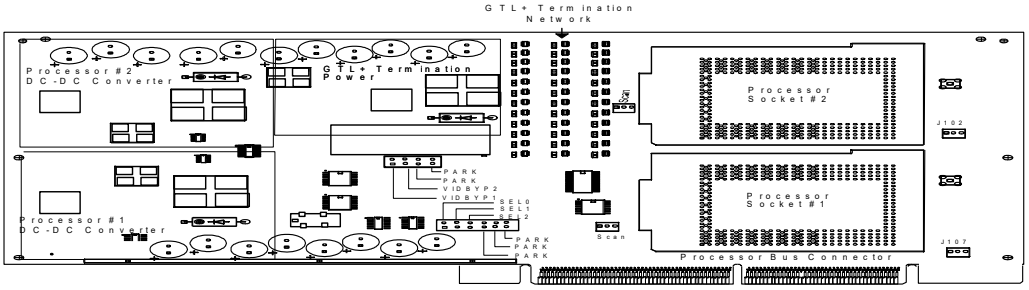


Figure 1.3 Processor Module Layout

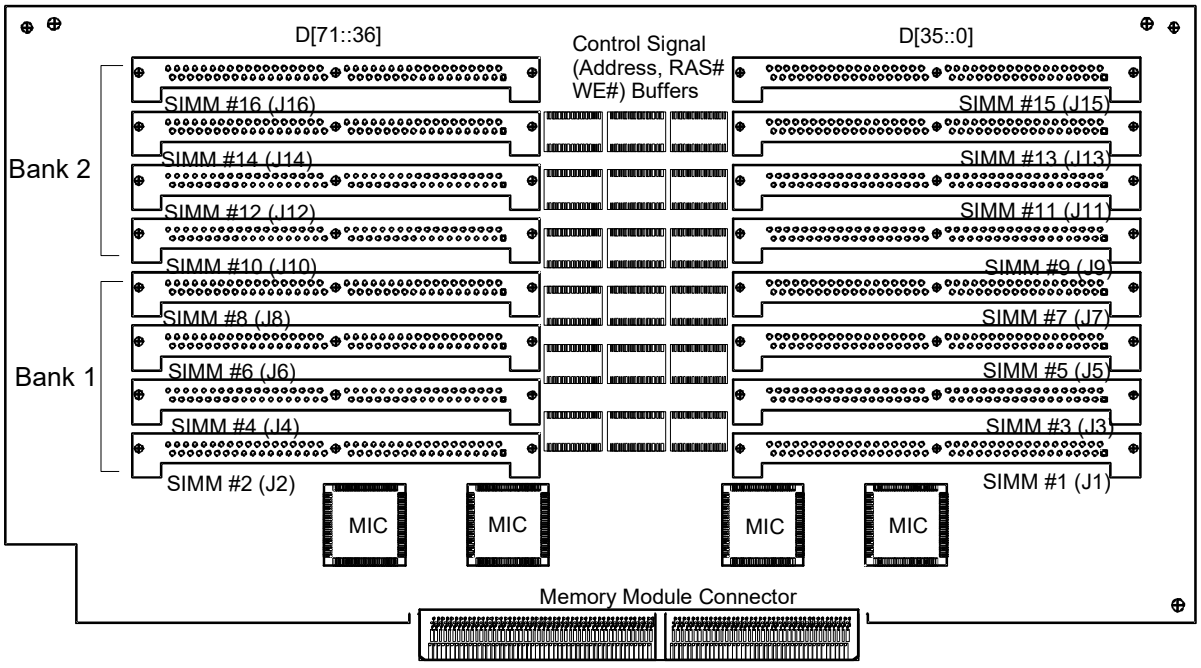


Figure 1.4 Memory Module Layout

1.5Connector Locations

Baseboard connector locations are shown in the figure below. See Appendix C for the connector pinouts.

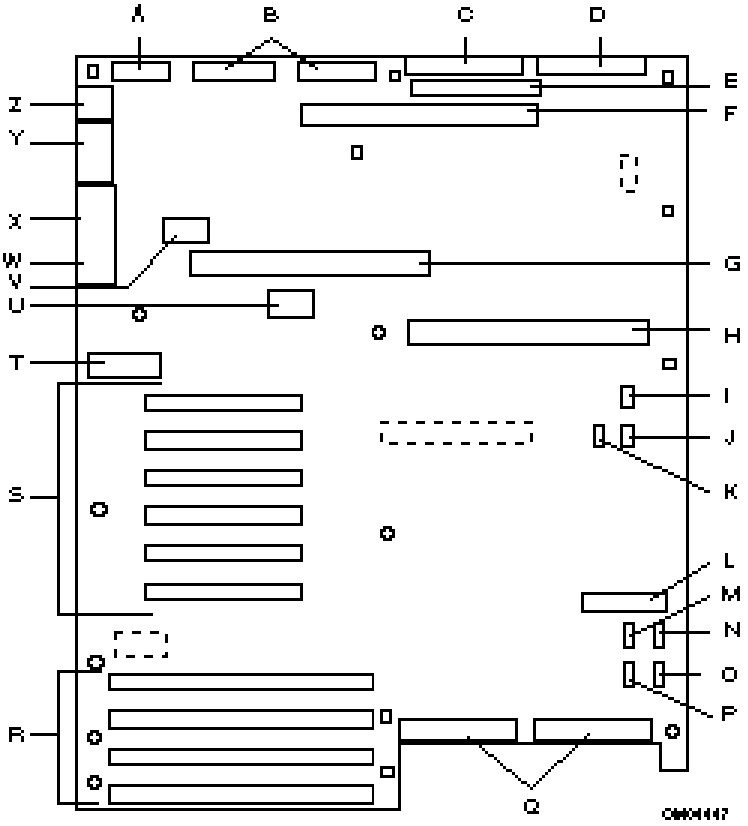


Figure 1.5 AP450GX Board Set Connectors

**	*Comments in italics are applicable when the board set is installed into Intel's Poca chassis.*
A	Power control and status connector (PS3)
B	+5V, +12V, and 3.3V power connectors (PS1 and PS2) (identical)
C	Diskette drive connector
D	Front panel connector
E	IDE drive connector
F	Memory module connector
G	Secondary processor module (or termination module) connector
H	Primary processor module connector
I	Fan 1 connector (*not used*)
J	Fan 2 connector *(inner chassis fan*)
K	Hard drive LED 1 connector (*not used*)
L	Connector for optional Server Management Module (SMM)
M	I^2C connector (*not used*)
N	Fan 3 connector (*upper outer chassis fan*)

O	Fan 4 connector (*lower outer chassis fan*)
P	Hard drive LED 2 connector (*not used*)
Q	SCSI bus connectors: Channel A to the right, Channel B to the left
R	EISA slots 1 - 4 for add-in boards (slot 1 toward top, 4 toward bottom)
S	PCI slots 1 - 6 for add-in boards (slot 1 toward top, 6 toward bottom: PCI Bus 0 = slots 1 - 3; PCI Bus 1 = slots 4 - 6)
T	Configuration switches and jumpers
U	Real-time clock
V	Video DRAM expansion socket
W	VGA monitor connector (bottom)
X	Parallel port connector (Top)
Y	Serial port connectors -- Port 1 (top), Port 2 (bottom)
Z	PS/2-compatible keyboard and mouse connectors (interchangeable)

Three connectors are shown in the board drawing as dotted-line boxes. They are not used in this system configuration. Their functions are as follows:

- ITP (In-target Probe) A located near the upper right corner of the baseboard for low level system debug.
- PCI test connector A Blue connector near middle of board (not used)
- 3.3V PCI power connector Located near the lower left corner, below the PCI slots.

1.6Microprocessor

The Pentium Pro processor is a 387-pin dual-cavity PGA package. The package contains two devices: a 5.5 million transistor processing core with 8 KByte primary cache, and 32 million transistor 512 KB secondary cache (L2 cache).

The AP450GX board set operates with Pentium® Pro processors whose voltage may range from 2.1V to 3.5V and are Voltage ID (VID) enabled (i.e. the processors have the ability to ask for a certain voltage). A voltage regulator circuit on the processor module makes use of the VID capabilities to automatically adjust its voltage output to match that of the installed processor. The board set also has jumpers allowing processors ranging from 133 to 266 MHz to be installed. It should be noted, however, that there will be limitations on which processors will be supported. Refer to future specification updates for this information. In general, **all processors in the system must be running at the same frequency and be the same stepping and level 2 cache size**. The initial board set will be validated only with the 166MHz/512KB processor.

An approved Pentium Pro processor heatsink (Intel part #644591-002) is necessary for proper thermal dissipation. The processor/heatsink assembly must be securely fastened to the socket by two clips (Intel part #637886-002). These clips fit over the heatsink assembly and attach to the outer wide tabs of the socket assembly. The heat sink must use thermal grease for proper heat dissipation for any processor greater than 35W (i.e. the 200MHz/512KB). “Foil pads” with grease on them will not properly cool a >35W processor. A heat sink kit is available that contains the proper heatsink, two clips and a tube of thermal grease. The current Intel order code is

ALCPUUPKIT. However this order code will soon be superseded by a new order code, ALHSINKKIT.

The Pentium Pro processor maintains full backward compatibility with the 8086, 80286, Intel386™, Intel486™ and Pentium processors. It also has a numeric coprocessor that significantly increases the speed of floating point operations, while maintaining backward compatibility with the i486DX math coprocessor and complying with ANSI/IEEE standard 754-1985.

CAUTION

Do not use the older style of bail-wire clips for securing the heatsink assembly. These clips have been found to cause damage when installed or removed incorrectly.

1.6.1 Processors and Processor Modules

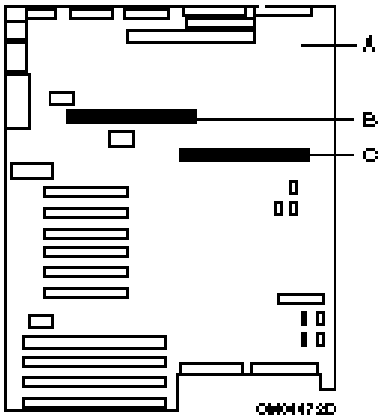
The processor module will support up to two Pentium® Pro processors. The two processor sites are ZIF socketed, so that only one might be installed at the time of shipment with upgrades to be added later. The ZIF sockets are compatible with Intel's Socket 8 specification. Each processor module contains termination circuitry required by the GTL+ signaling environment, DC to DC converters for proper power to each processor, an I^2C controller, and logic for I^2C support and clock ratio programming. Each processor module has three DC-DC converters; one for the 1.5V GTL+ termination voltage, and two identical converters for the processors. The processor converters are supplied from the +12V supply. The GTL+ converter is supplied from the +12V supply on early processor modules (identified as 647428-xxx), or from the 3.3V supply on more recent processor modules (identified as 659506-xxx). The newer processor modules will support up to a 40W processor (i.e. the 200MHz/512KB). The older module will only supply enough current for up to a 35W processor (i.e. the 166MHz/512KB or 200MHz/256KB).

1.7 Bus Termination Module

This module is required when only one processor module is installed in the system. The terminator module provides GTL+ signal termination and voltage regulation. When used, this module must be installed in the secondary processor module slot on the system. The terminator module contains a single DC-DC converter which provides the 1.5V termination voltage. This converter is driven from the +12V supply.

1.8Processor Population Order

The system baseboard has a primary processor module connector and a secondary processor module connector. A processor module can have one or two Pentium Pro processors installed. The tables that follow show the different supported population orders for 1, 2, 3 or 4 processors. Other processor configurations are not supported.



Processor board connectors on system baseboard

A System baseboard

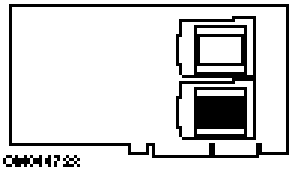
B Connector for secondary processor module or bus termination module

C Connector for primary processor module

Figure 1.6 Processor Module Connector Locations

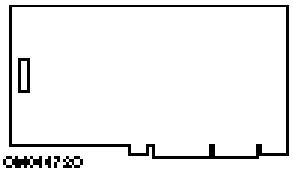
PRIMARY connector on system baseboard

1st processor module, one processor in lower socket

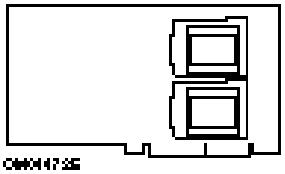


Plus one of the following in the **SECONDARY connector on system baseboard:**

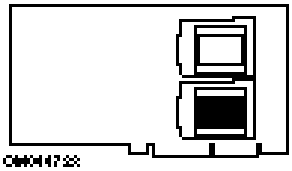
Termination module



2nd processor module, no processors

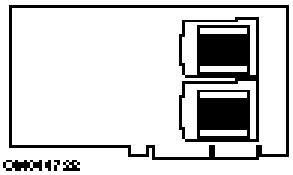


2nd processor module, one processor in lower socket



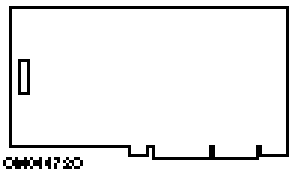
PRIMARY connector on system baseboard

1st processor module, two processors

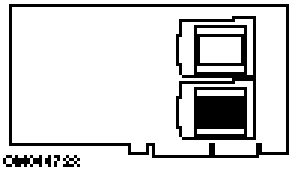


Plus one of the following in the **SECONDARY connector on system baseboard:**

Termination module



2nd processor module, one processor in lower socket



2nd processor module, two processors

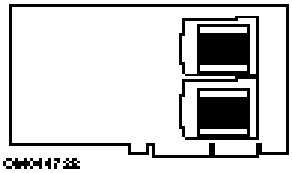


Figure 1.7 Processor Configuration Models

Refer to section 1.21 for the processor module jumper configurations.

1.9Memory

1.9.1System Memory

The memory subsystem consists of the memory chip set, the memory module connector on the system baseboard, and the memory module itself. The system baseboard contains the data path and data control portions of the chip set. The memory module contains the buffer devices from the chip set and 16 SIMM sites for up to 1 GB of system memory (using 64MB SIMMs). When the 128MB SIMMs are available and qualified, the memory module will support up to 2GB of memory. DRAM SIMMs on the module are organized as two 72-bit wide, 1-, 2-, or 4-way interleaves and 1 or 2 banks. The 1-way interleave is only supported in a memory downsizing condition (see below for more detail). SIMM sites accept 72-pin single- or double-sided SIMMs (60 or 70ns SIMMs only). SIMM sites must be populated using identical SIMMs in each bank.

Memory error checking and correction is supported via ECC logic in the chip set while using standard parity SIMM/DIMMs. The chip set will detect double bit errors and correct single bit errors. Errors may be generated by a defective memory module or soft errors. When a bad SIMM/ DIMM is detected (i.e. a double bit error), the BIOS will automatically downsize memory to eliminate the bad SIMM/DIMM.

The 1GB memory module is available in two versions. Both are functionally identical except for the type of metal used in the SIMM connector and the type of capacitors used. One version has tin lead SIMM connectors and must be used with tin lead SIMMs. The other version is available with Gold lead SIMM connectors and must be used with Gold lead SIMMs. The Gold lead module also has fused tantalum capacitors. The Tin lead version simply has non-fused tantalum capacitors. There are separate order codes for each version. See Appendix B for the specific order codes.

✎ **NOTE**

Only use SIMMs approved for use in this system. See Appendix A for a partial list of qualified SIMMs. Contact your Intel representative for an updated list of Qualified SIMMs and DIMMs.

1.9.2Memory Installation Options (1GB Memory Module)

The following SIMM interleaving options are supported:

- Two-way interleave, J1 through J4;
- Four-way interleave, single bank, J1 through J8
- Four-way interleave, dual bank, J1 through J16.

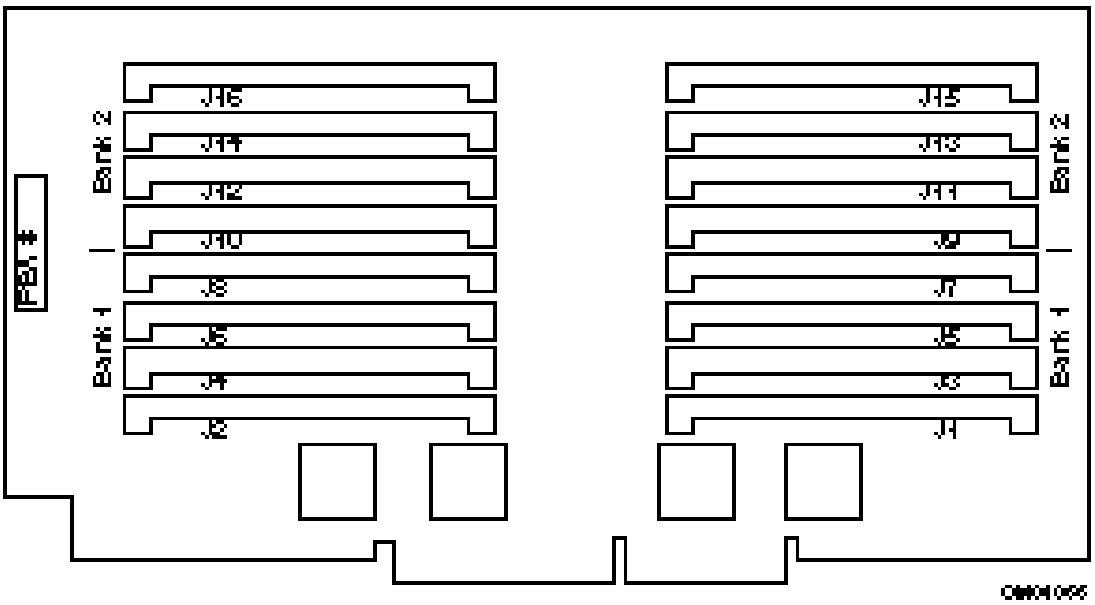


Figure 1.8 Memory Configurations

The 1GB memory module has 16 SIMM sockets, arranged in two banks. The system automatically detects system memory installed, so jumpers do not need to be set to specify memory size although the SCU must be run after you change the memory configuration. See chapter 3 for details.

Table 1.1 Supported Memory Options

Memory size	Bank installation	SIMM type
Minimum memory configuration is 64 MB of DRAM (with four 16 MB SIMMs installed in J1, J2, J3, and J4). Maximum memory configuration is 1GB of DRAM (with 64 MB SIMMs installed in each socket, J1 through J16). Maximum memory configuration is 2GB with 128MB SIMMs.	Always begin with the bottom SIMM sites (lowest number is J1) as you fill the board sockets. All SIMMs in a bank must be identical (same size and speed). SIMMs in bank 1 may differ in size from the SIMMs in bank 2, but may not differ in speed. Number of SIMMs supported: 4, 8, or 16 only.	Use 16 MB or 64MB single-sided SIMMs or 32 MB double-sided SIMMs. (or 128MB double-sided SIMMs when available) Use only 36-bit, 72-pin, 60 or 70ns fast page mode SIMMs with tin-lead alloy plated edge connectors, single- or double-sided. (Single-sided refers to the addressing method, not to the physical layout of the SIMM.) Use JEDEC-compatible SIMMs. Contact customer service representative for list of approved SIMMs.

1.9.3Memory Performance Hints

Memory performance, and thus system performance, can be increases by changing the number of interleaves, number of banks and the speed of memory installed. While not all applications will behave the same way, below are some rules of thumb for increasing memory performance. Note the performance increases are approximate and based on certain applications. Your results may vary.

- More memory is better (i.e. 1GB is better than 512KB)
- 4-way interleave is faster than 2-way interleave (by ~18-30%)
- 2 banks of memory is usually faster than one bank
- 60ns SIMMs are better than 70ns SIMMs (by ~5%)

1.9.44GB Memory Module

A memory module will be made available at a later date that will support up to 4GB of memory using 128MB DIMMs. This module fits into the same memory module connector the 1GB module fits into and has the same mechanical form factor. The additional memory capacity is accomplished with the use of TOSP DRAM's packaged in JEDEC standard 16Mx72 DIMMs (Dual In-line Memory Module) 60ns DIMMs only. The 4GB module contains 32 DIMM sockets, which when populated in groups of 4 DIMMs, offers memory capacity options of 0.5GB through 4GB in 0.5GB increments. Memory on the module is organized in 4 banks and supports 1, 2 or 4-way interleaves. 4-way interleave is the default for all memory sizes. 1 and 2-way interleaves are only supported in memory downsizing conditions. Availability of the 4GB memory module is targeted for the Q4 1996 time frame. Only the 128MB DIMM will be supported.

1.10Intel 82450GX PCIset

The Intel 82450GX PCIset consists two functional groups, the PCI controller and the memory controller. The PCI controller consists of a single 82454GX PCI Bridge (PB) component. Two of 82454GX components are on the system baseboard, each supporting a single PCI (peer) bus. The memory controller consists of six components; the 82452GX (DP) Data Path component, 82453GX (DC) Data path Controller, and the 82451GX (MIC) Memory Interface Controller. The DP and DC each reside on the system baseboard. Four of the MIC components are located on the memory module.

1.11Onboard SCSI Controllers

The baseboard includes two embedded wide SCSI-2 controllers (Adaptec AIC-7880, channels A and B) integrated as PCI bus masters. The controllers support data path widths of 8-bit (narrow SCSI) at a data transfer rate of 10 MB/sec and 16-bit (wide fast SCSI) at a data transfer rate of 20 MB/sec. As PCI bus masters, these controllers support data transfer rates of 133 MB/sec.

You can connect up to seven 8-bit narrow SCSI devices or up to fifteen 8-bit narrow and/or 16-bit wide SCSI devices and one controller (maximum of seven 8-bit narrow devices) to each channel. Devices can be tape drives, printers, optical media drives, and other devices.

Active termination must be provided on the far end of the SCSI bus to ensure proper termination of the bus. The baseboard provides active termination at the near end.

Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus and avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SCSI output drivers can directly drive a 48 mA, single-ended SCSI bus with no additional drivers.

Although the 7880 controller is designed to support Ultra SCSI mode (also known as Fast-20 mode), the AP450GX board set has not yet been validated to support this mode. Watch for specification updates, or contact your field support personal for an update on when this mode has been fully validated.

1.12EISA Expansion Slots

The baseboard has four EISA bus slots. The EISA bus is an extension of the Industry Standard Architecture (ISA) bus. Because EISA is fully backward-compatible with ISA, you can install EISA or ISA add-in boards and software in your server. This compatibility is handled by the PCEB and ESC chip set components on the system baseboard.

The EISA bus provides:

- 32-bit memory addressing
- Type A transfers at 5.33 MB per second
- Type B transfers at 8 MB per second
- Burst transfers at 33 MB per second
- 8-, 16-, or 32-bit data transfers
- Automatic translation of bus cycles between EISA and ISA masters
- Interrupt sharing

All four slots have the capability of being bus masters. When EISA masters arbitrate for the bus, the following pairs of slots share arbitration requests: 1 and 2, 3 and 4. Therefore, in the round-robin scheme of letting EISA masters take over the bus, ownership of it occurs in the following sequence: 1, 2, 3, 4, 1, 2, 3, 4, etc.

1.13PCI Expansion Slots

The system baseboard has six, 32 bit, PCI 2.1 compliant bus slots. The PCI subsystem consists of two I/O bus segments. PCI #0 is the primary or compatibility bus segment, running always at 33 MHz. PCI #0 connects the processor bus to the INCA (Intel's Interrupt Controller ASIC), a PCI/EISA bridge, and three PCI connectors. PCI #1 connects the processor bus to two embedded wide SCSI controllers and three PCI connectors. PCI #1 also always runs at 33MHz. The architecture supports Host-to-PCI, PCI-to-Memory, PCI-to-EISA, EISA-to-Memory, and PCI-to-PCI transfers. The PCI bus provides:

- 32 and 64-bit memory addressing
- +5 V and + 3 V signaling environments
- Burst transfers at 133 MB per second
- 8-, 16-, or 32-bit data transfers
- Plug-and-play configuration
- PeerBus to maximize throughput

The INCA device provides these features:

- PCI clock generation: 14 PCI clocks (7 per PCI segment)
- Three buffered clocks
- Interrupt control
- Arbitration support for six PCI masters on PCI #1
- General purpose I/O ports: two 8-bit I/O ports for control or status
- 3-mode diskette control support
- DMA steering for IDE and parallel port to 1 of 4 DRQs/DACKs
- Keyboard emulation
- Support for front panel interface and LCD
- Security features: watchdog timer (software start/reset) resets system if it expires; monitors keyboard/mouse; monitors system baseboard voltage (+12V, -12V, +5V, -5V, +3.3V); monitors baseboard temperature and chassis door switch

1.14Boot Order

When the system boots, it will look for a bootable device in a certain order. The system will then boot off the first bootable device it finds. Below is the order in which the system will look for bootable devices.

1. Floppy Drive
2. IDE Drive
3. E1 (EISA bus slot #1)
4. E2 (EISA bus slot #2)
5. E3 (EISA bus slot #3)
6. E4 (EISA bus slot #4)
7. P1 (PCI Bus#0, slot 1)
8. P2 (PCI Bus#0, slot 2)
9. P3 (PCI Bus#0, slot 3)
10. P4 (PCI Bus#1, slot 1)
11. SCSI A (On-board AIC-7880 SCSI controller)
12. SCSI B (On-board AIC-7880 SCSI controller)
13. P5 (PCI Bus#1, slot 2)
14. P6 (PCI Bus#1, slot 3)

Notes:

- The actual boot order on the EISA bus may change depending on how the devices installed on the EISA bus are configured, but the EISA bus will always be scanned for bootable devices before the PCI buses.
- If a PCI-to-PCI bridge device (P2P) is installed in the system, the boot order will change and may vary depending on the configuration. Typically, if a P2P is installed in P2, for example, the boot order will likely look for a bootable device on the P2P before looking at P3. However under some circumstance, the system may actually go to P3 before looking for a bootable device on the P2P.

1.15Super VGA Controller

The onboard, integrated Cirrus Logic CL-GD5424 super VGA controller (ISA based) is fully compatible with these video standards: CGA, EGA, Hercules Graphics, MDA, and VGA. The standard system configuration comes with 512 KB of onboard 70ns video memory. You can optionally expand the onboard video memory buffer size to 1 MB by adding one 40-pin 256 K x 16, 70 ns fast-page DRAM. See Appendix A for a list of qualified Video DRAM. The SVGA controller supports only analog monitors (single and multiple frequency, interlaced and noninterlaced) with a maximum vertical retrace interlaced frequency of 87 Hz.

The BIOS will automatically disable the onboard video if another add-in video adapter is installed into the system baseboard. Note, however, the BIOS will only support add-in video adapters in the first PCI bus (slots P1-P3). Video adapters placed in the second PCI bus (slots P4-P6 will not be recognized).

- Supported with 512 KB memory: Pixel resolutions of 640 x 480 and 800 x 600 in 256 colors, and 1024 x 768 x 16 colors.
- Supported with 1 MB memory (optional): 132-column text modes and high resolution graphics with 1280 x 1024 x 16 colors. Depending on the environment, the controller displays up to 64,000 colors in some video resolutions.

Table 1.2 Standard VGA Modes

Mode(s) in Hex	Colors (number /palette size)	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
0, 1	16/256K	360 X 400	14	31.5	70
2, 3	16/256K	720 X 400	28	31.5	70
4, 5	4/256K	320 X 200	12.5	31.5	70
6	2/256K	640 X 200	25	31.5	70
7	Mono	720 X 400	28	31.5	70
D	16/256K	320 X 200	12.5	31.5	70
E	16/256K	640 X 200	25	31.5	70
F	Mono	640 X 350	25	31.5	70
10	16/256K	640 X 350	25	31.5	70
11	2/256K	640 X 480	25	31.5	60
12	16/256K	640 X 480	25	31.5	60
12+	16/256K	640 X 480	31.5	37.5	75
13	256/256K	320 X 200	12.5	31.5	70

Table 1.3 Extended VGA Modes

Mode(s) in Hex	Colors (number /palette size	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
14, 55	16/256K	1056 X 400	41.5	31.5	70
54	16/256K	1056 X 350	41.5	31.5	70
58, 6A	16/256K	800 X 600	40	37.8	60
58, 6A	16/256K	800 X 600	49.5	46.9	75
5C	256/256K	800 X 600	36	35.2	56
5C	256/256K	800 X 600	40	37.9	60
5C	256/256K	800 X 600	49.5	46.9	75
5D	16/256K (interlaced)	1024 X 768	44.9	35.5	87
5D	16/256K	1024 X 768	65	48.3	60
5D	16/256K	1024 X 768	75	56	70
5D	16/256K	1024 X 768	78.7	60	75
5F	256/256K	640 X 480	25	31.5	60
5F	256/256K	640 X 480	31.5	37.5	75
60	256/256K (interlaced)	1024 X 768	44.9	35.5	87
60*	256/256K	1024 X 768	65	48.3	60
60*	256/256K	1024 X 768	75	56	70
60*	256/256K	1024 X 768	78.7	60	75
64*	64K	640 X 480	25	31.5	60
64*	64K	640 X 480	31.5	37.5	75
65*	64K	800 X 600	36	35.2	56
65*	64K	800 X 600	40	37.8	60
65*	64K	800 X 600	49.5	46.9	75
66*	32K Direct/256 Mixed	640 X 480	25	31.5	60
66*	32K Direct/256 Mixed	640 X 480	31.5	37.5	75
67*	32K Direct/256 Mixed	800 X 600	40	37.8	60
67*	32K Direct/256 Mixed	800 X 600	49.5	46.9	75
6C*	16/256K (interlaced)	1280 X 1024	75	48	87
6C*	16/256K	1280 X 1024	108	65	60
6D*	256/256K (interlaced)	1280 X 1024	75	48	87
6D*	256/256K	1280 X 1024	108	65	60
71*	16M	640 X 480	25	31.5	60
72*	16M 32-bit/pixel	800 X 600	40	37.8	60
73*	16M 32-bit/pixel (interlaced)	1024 X 768	44.9	35.5	87
74*	64K (interlaced)	1024 X 768	44.9	35.5	87
74*	64K	1024 X 768	65	48.3	60
74*	64K	1024 X 768	75	56	70
74*	64K	1024 X 768	78.7	60	75
75*	64K (interlaced)	1280 X 1024	75	48	87
76*	16M 32-bit/pixel	640 X 480	25	31.5	60
76*	16M 32-bit/pixel	640 X 480	31.5	37.5	75

* Requires 1MB video memory option.

1.16Keyboard and Mouse

The 8742 keyboard controller is PS/2-compatible. The system may be locked automatically if there is no keyboard or mouse activity for a predefined length of time, as specified through the Setup utility. The default keystroke combination to enable this feature is <Ctrl + Alt + Backspace>. Once the inactivity timer has expired, the keyboard or mouse does not respond until the previously stored password in the keyboard controller is entered. The keyboard LED will blink until the password is entered.

The mouse is disabled on power-up; in this state, interrupt IRQ12 is available for use by add-in boards, and the mouse clock input to the keyboard controller is connected to the mouse clock output, with no connection to the external mouse.

1.17Advanced Integrated Peripheral (AIP)

The AIP resides on the EISA bus and contains a floppy disk controller (FDC), 2 serial ports, a multi-function parallel port and an IDE interface.

1.17.1Floppy Drive Support

The FDC on the AIP is functionally compatible with the 82077SL, 82077AA and 8272A floppy disk controllers and can provide a data rate up to 2MB/s. The FDC will support up to two floppy disk drives.

1.17.2Serial Ports

Two 9-pin serial ports are provide in a single stacked housing (ports 1 and 2). Port 1 is located on the top, port 2 on the bottom. Both serial ports are 16550 compatible with 16-byte FIFO's. Each serial port can be set to 1 of 4 different COM ports (via the BIOS setup), and can be enabled separately. When enable, each port can be programmed to generated edge or level sensitive interrupts. When disabled, serial port interrupts are available to adapter cards.

1.17.3Parallel Port

A single PS/2 compatible 25-pin bi-directional parallel port is provided. The parallel port supports Extended Capabilities Port (ECP) protocol with DMA, EPP protocol and IEEE 1284 protocol for PS/2 bi-directional compatibility. The parallel port can be enabled or disabled via the BIOS setup. When disabled, the interrupt is available to adapter cards.

1.17.4IDE Support

IDE is an 8-bit or 16-bit interface for intelligent disk drives with AT disk controller electronics onboard. AC timing constraints allow only Type 2 IDE drives in the CAM specification (or faster) to be supported. The processor can transfer data from the IDE interface at a maximum transfer rate of 2.4Mbytes per second. This IDE implementation will also support DMA to the IDE device, which has a maximum transfer rate of 4.2Mbytes per second. Typical IDE devices can access data a peak rate of 1.2Mbytes per second. Therefore, the usage of DMA will significantly reduce the

bus utilization (with respect to IDE device access), and will significantly improve system performance.

The BIOS will support both a primary and a secondary IDE controller, although only a single controller is provided by the board set. The second controller must be installed as an adapter card.

The IDE interface can be disabled. It is disabled on reset; in this state, the I/O address space and interrupt IRQ14 are available for add-in modules. The system BIOS may disable the interface when it finds the registers of another hard disk controller.

1.18Miscellaneous Functions

The board set provides the additional miscellaneous functions listed below:

- I2C Diagnostic bus
- Server Management Connector
- System Fan Interface
- Hard Drive LED Interface

1.18.1I2C Diagnostic Bus

The baseboard has an integral I2C (Inter-Integrated Circuit) bus which can be used for general purpose system management such as providing module revision or status information from anywhere in the system. This bus is routed to processor and memory modules, the front panel and power supply connectors, the Server Management Connector and a single “user” connector on the baseboard.

A Philips PCF8584 I2C controller is mapped into EISA I/O space and can be used by system software to access the I2C bus. The 8584 appears at addresses CA0h and CA1h. the interrupt from the 8584 is routed to input PCI8 on the INCA component.

The baseboard, processor, memory and terminator modules have PCF8574 and PCF8474A I/O devices on them. These are 8-bit devices that connect the I2C bus and provide system information from each module. Below is the I2C base address for each component.

Baseboard I2C Address:	0x40
Primary Processor Module Slot I2C Address:	0x70
Secondary Processor Module Slot I2C Address:	0x72
Memory Module I2C Address:	0x42

The information available from each module when accessed via the I2C bus is listed below along with the bit definitions.

Table 1.4 Baseboard I2C Bit Map

Bit	Bit Name	Description
2:0	BRDREV(2:0)	Baseboard board revision ID 001 = Fab 1 010 = Fab 2 011 = Fab 3
6:3	RESERVED	Reserved
6:3	FANFAIL(3:0)	A zero (0) indicates a failed fan. Bits 6:3 are valid as FANFAIL when bit 7 = “1”. bit 3 = fan 4 (Outer chassis fan, lower) bit 4 = fan 3 (Outer chassis fan, upper) bit 5 = fan 2 (Inner chassis fan) bit 6 = fan 1 (Not used in Poca chassis)
7	FANFAILSEL	When “1”, bits 6:3 are fan fail When “0”, bits 6:3 are Reserved

Table 1.5 Processor Module I2C Bit Map

Bit	Bit Name	Description
2:0	P6ID(2:0)	Pentium® Pro processor core/bus frequency ID 000 = 150/60 MHz 001 = 180/60 MHz 010 = 210/60 MHz 011 = 240/60 MHz 100 = 166/66 MHz 101 = 200/66 MHz 110 = 233/66 MHz 111 = 266/66 MHz
4:3	Reserved	
5:3	BRDREV(0:2)	Processor Module Board Revision ID 000 = Fab 3 Bits 5:3 are valid as BRDREV when bit 7 = “1”. All previous processor module revisions are not compatible with Fab 3 which is why the numbering starts with 000.
6:5	Reserved	
7	BRDREVSEL	When “1”, bits 5:3 indicate the board revision, bit 6 is reserved When “0”, bit 6:3 are reserved.

Table 1.6 1GB Memory Module I2C Bit Map

Bit	Bit Name	Description
1:0		Board Revision ID 00 = 1GB Module (Fab1 or Fab2) 01 = 1GB Module (Fab3) 10 = Reserved 11 = 4GB Module
3:2		Bank 0 SIMM Speed 00 = 50ns (bank 0) 01 = 80ns (bank 0) 10 = 70ns (bank 0) 11 = 60ns (bank 0)
5:4		Bank 1 SIMM Speed 00 = 50ns (bank 1) 01 = 80ns (bank 1) 10 = 70ns (bank 1) 11 = 60ns (bank 1)
6		Reserved
7		RAS/CAS Multiplexing for Address Bit permuting 0 = Enabled 1 = Disabled

Table 1.7 Termination Module I2C Bit Map

Bit	Bit Name	Description
2:0	BRDREV(2:0)	Alder Terminator Module revision ID 000 = Fab 3 All previous terminator module revisions are not compatible with Fab 3 which is why the numbering starts with 000.
6:3	N/C	These signals are not used.
7	GROUND	Hard wired to ground. To differentiate between a terminator module and a processor module, write a one “1” to bit 7 then do a read of bit 7. If a one “1” is read back, the board is a processor module. If a zero “0” is read back, the board is a terminator module.

1.18.2Server Management Connector

A 26-pin connector is provide to interface with an emergency management adapter card. It is designed for Intel's Server Monitor Module which allows the user to manage (monitor and control) the server from a remote console, but could be used by other similar implementations. The connector provides access to the I2C bus, power on/off signals, power good from the power supply and a host of other signals. Refer to the connector pin-out in Appendix C for a list of all signals.

1.18.3System Fan Interface

There are four fan connectors on the system baseboard. The connector pin-out is listed in Appendix C. These connectors provide a ground, 12V power to the fan and a fan-fail input from the fan. The system will be able to detect the failure and will report it via Intel's LANDesk Server Control Software. All four fan-fail inputs are tied to A/D channel 8 for monitoring by the INCA component. The current BIOS does have the ability to distinguish between the four fans. It simply knows if one fan has failed. Future versions of the BIOS will address this issue. If one or more of the fan connectors is not used in a particular application, pins 1 (GND) and 3 (Fan Fail) on the connector must be connected together. This connection is required to prevent an erroneous failed fan indication.

1.18.4Hard Drive LED Interface

There are two Hard Drive LED interface connectors on the baseboard (locking polarized, 4 position, single in-line, .025 in square pin). See Appendix C for the pinout. Pin 2 of both connectors is tied together as well as to the IDE connector (pin 39), the SCSI A LED signal and the front panel signal HD1_LED_ACT# (pin 10). They are tied together so that any of these sources can activate a light on the front panel to indicate hard drive access..

Likewise pin 3 of both connectors is tied together as well as to the SCSI B LED signal and the front panel signal HD2_LED_ACT# (pin 11).

The purpose of the connectors themselves is to provide a way for a front panel LED to be driven from an add-in disk controller. Note Intel's Poca chassis does provide LED's on its front panel that can be driven by either of these signals.

1.19Control Signals

1.19.1Remote Sensing

Remote sensing exists on the +5.1 Vdc, +12 Vdc, and +3.3 Vdc outputs. The -12 Vdc, -5 Vdc, and +5 V standby outputs are referenced to the negative (-) remote sense point. Only voltage drops exterior to the power supply are included. The loss of a remote sense connection will not cause the power supply to go into a high output voltage condition. Intel strongly recommends using the signals for remote sense. Without remote sense capabilities, it will be difficult to keep the power rails within the board set specifications.

Table 1.8 Amount of Drop to Regulate

Output voltage	Maximum voltage drop
+5.1 Vdc	0.3V
+12 Vdc	0.2V
+3.3 Vdc	0.2V
Ground	0.2V

1.19.2Power Good Signal

The PWRGOOD signal must be driven to the baseboard (pin 10, PS3) by the power supply and indicates that all outputs have reached operating state. The PWRGOOD signal is held low until the +5.1 Vdc output voltage reaches a minimum of 4.75 Vdc. The turn on delay for the PWRGOOD signal is between 5 and 50 milliseconds. The PWRGOOD signal must be deasserted for a minimum of 1 mS before any of the output voltages fall below the regulation limit.

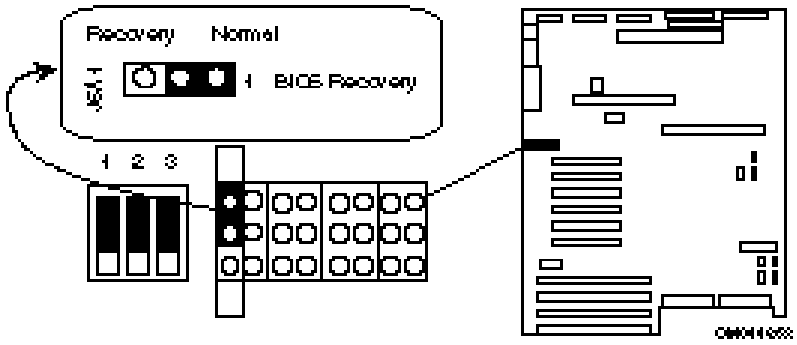
1.20 Baseboard Jumper Settings

Table 1.9 Jumper Configuration, Baseboard

Baseboard configuration jumper summary (listed by block number on board)	Pins	Description
J6A1, BIOS Recovery	1-2*	Normal BIOS boot block
	2-3	Recovery BIOS boot block
		If the normal BIOS gets corrupted, and you are unable to reload a new BIOS from floppy disk, install the jumper into recovery mode which will allow the system to boot from the recovery BIOS.
J6A1, Boot Block Protect	1-2*	BIOS boot block is write-protected
	2-3	BIOS boot block is programmable
		The programmable mode should only be enabled under carefully controlled circumstances. Incorrect programming of the boot block will render the system unbootable
J6A4, BIOS write	1-2	Disables BIOS update of flash memory
	2-3*	Enables BIOS update of flash memory with special utility
		Install the jumper in the enable mode when updating the system BIOS.
J6A4, Floppy 0	1-2	For 1.44 MB diskette drive size or autodetection. Disables 2.88 MB size detection
	2-3*	For forced 2.88 MB diskette drive size
J6A2, Floppy 1	1-2	For 1.44 MB diskette drive size or autodetection. Disables 2.88 MB size detection
	2-3*	For forced 2.88 MB diskette drive size
J6A2, Video Sleep	1-2	Video Sleep Register resides at 03C3H
	2-3*	Video Sleep Register resides at 46E8H
J6A3, Power Control	1-2	Disables RTC power supply control
	2-3*	Enables power supply control using RTC
		Under certain conditions the RTC can be programmed via the BIOS setup to turn off the system. Installing the jumper in the enable mode allows the RTC to use this feature.

* Factory default setting

1.20.1BIOS Recovery Jumper, J6A1



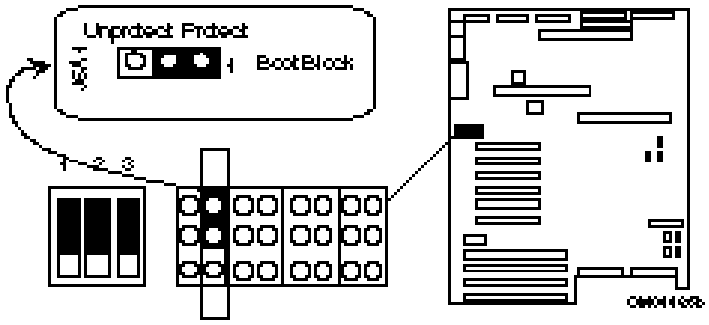
1-2 Normal BIOS boot block, factory default

2-3 Recovery BIOS boot block

Figure 1.9 BIOS Recovery Jumper

This jumper enables the recovery mode for the BIOS flash memory. This mode is important because the system BIOS can be corrupted—for example, when the update procedure is aborted due to a power outage. The flash memory contains a protected area that cannot be corrupted. Code in this area is used to boot the computer from a diskette in drive A when the BIOS has been corrupted. After booting, the Flash Memory Update utility is used to automatically recover the system BIOS from the BIOS recovery files on the diskette. (For normal operation, it is important to keep the jumper on pins 1 and 2.) When the recovery procedure is run, another jumper, BIOS Write at J6A4, must also be in its default position (pins 2 and 3 jumpered).

1.20.2Boot Block Jumper, J6A1



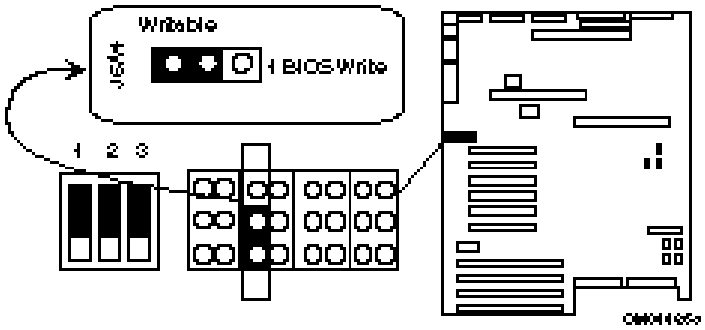
1-2 BIOS boot block is write-protected, factory default

Figure 1.10 Boot Block Jumper

CAUTION, leave at factory-default setting, pins 1 and 2

Always leave the Boot Block jumper installed in the factory-default position, on pins 1 and 2, to protect the BIOS boot block from being overwritten. Do not mistake this jumper block for the ones on either side.

1.20.3BIOS Write Jumper, J6A4



2-3 Enables BIOS update of flash memory with special utility, factory default

1-2 Disables BIOS update of flash memory (cannot overwrite the BIOS)

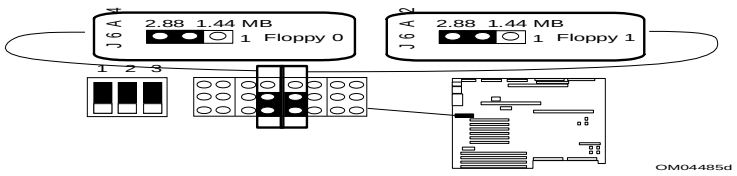
Figure 1.11 BIOS Write Jumper

CAUTION, updating the BIOS requires special utility

Changing this jumper should be done only by a qualified technical person, because updating the BIOS requires a special utility.

This jumper enables updating the BIOS in flash memory with a special utility. The factory default is to leave this function enabled so that you can update the BIOS from a bootable diskette without needing to open the system and change the jumper. For a copy of the utility to update the BIOS, contact your customer service representative.

1.20.4Floppy 0 Jumper at J6A4; Floppy 1 Jumper at J6A2



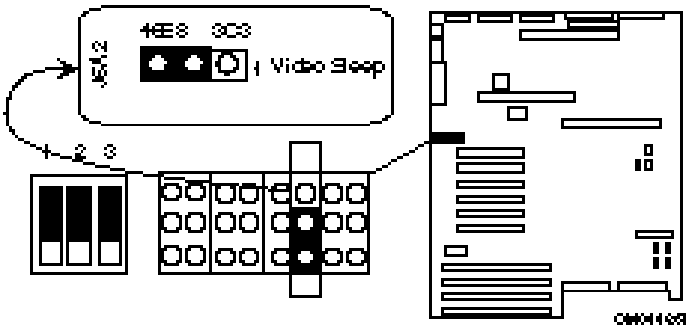
2-3 For forced 2.88 MB diskette drive size, factory default

1-2 For 1.44 MB drive size or autodetection; disables 2.88 MB size detection

Figure 1.12 Floppy Jumpers

The Floppy 0 and Floppy 1 functions are set at separate jumper blocks, but the descriptions are identical. These jumpers configure the floppy drive port to force 2.88 MB drive size or to support automatic size detection.

1.20.5Video Sleep Jumper, J6A2



2-3 Video Sleep register resides at 46E8H, factory default

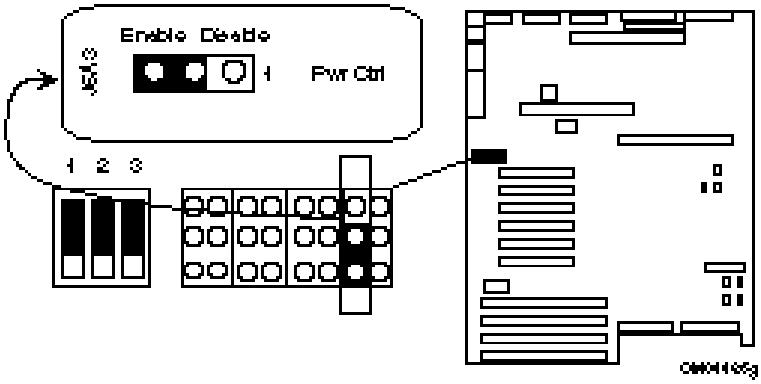
1-2 Video Sleep register resides at 03C3H

Figure 1.13 Video Sleep Jumper

The video address jumper determines which I/O port the onboard Cirrus Logic CL-GD5424 super VGA controller uses for its internal AT mode setup port. The starting address of the default port is 046E8H.

If there is no keyboard activity after a specified time-out period (1 to 128 minutes as specified by using the SCU), the video sleep register blanks out the monitor screen. When this happens, you must enter a password to reactivate the monitor and the keyboard.

1.20.6Power Control Jumper, J6A3



2-3 Enables power supply control using the RTC, factory default

1-2 Disables RTC power supply control

Figure 1.14 Power Control Jumper

This jumper (PWR CTRL) enables power supply control using the real-time clock. Power control from the RTC is typically used for Automatic Server Recovery. An alarm is set in the RTC by the BIOS or a utility program to power the system on or off at a predetermined time.

1.21 Processor Module Jumper Settings

Table 1.10 Jumper Configuration, Processor Module

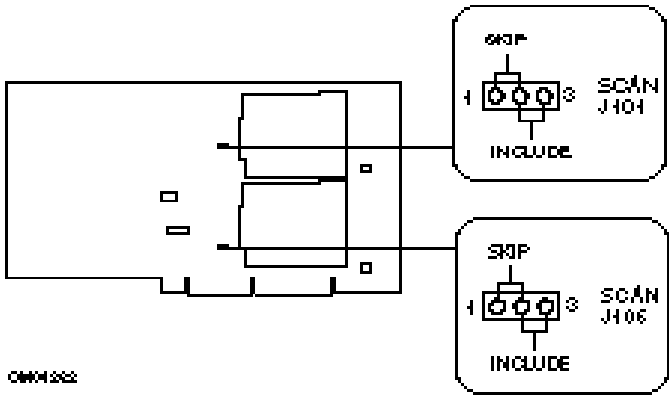
Processor board jumper summary	Pins	Description
J101 and J106, scan for processor (SCAN)	1-2*	Processor not installed in adjacent socket**
	2-3	Processor installed in adjacent socket
J103, voltage identification (VID)***	1-2	If jumper is installed, VID is disabled, processor 2. If not installed, VID is enabled, processor 2.
	3-4	If jumper is installed, VID is disabled, processor 1. If not installed, VID is enabled, processor 1.
	5-6*	Park - not connected
	7-8*	Park - not connected
J105, processor frequency select (SEL) (see table in section 1.21.3)	1-2*	SEL0
	3-4	SEL1
	5-6	SEL2
	7-8	Park - not connected
	9-10	Park - not connected
	11-12	Park - not connected

* Factory default setting.

** The pins at J101 and J106 are only useful when using the ITP. During normal operation they have no effect on the system.

*** J103 block may not be present on all versions of the processor module. If not present, then VID is enabled and is not selectable.

1.21.1SCAN Jumpers, J101 and J106



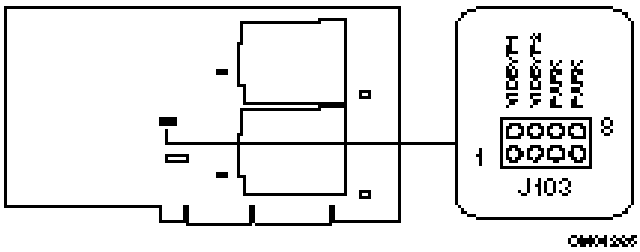
1-2 Processor not installed in adjacent socket (SKIP position), factory default

2-3 Processor installed in adjacent socket (INCLUDE position)

Figure 1.15 SCAN Jumpers

There are two SCAN jumper blocks, one for each processor socket. These are used to determine if a processor is installed in the socket adjacent to a given jumper block. In normal operation, these jumpers have no function and are useful only during low-level processor ITP bus debugging.

1.21.2VID Jumpers, J103



1-2 VID bypass 1; 3-4 VID bypass 2

5-6 Park, factory default; 7-8 Park, factory default

Figure 1.16 VID Jumpers

The settings at J103 depend on whether processors are voltage-ID-ready or not. In general, voltage identification (VID) is default-enabled; that is, the unused jumpers are placed in the Park locations. The J103 block is present only on early versions of the processor board; later versions have VID enabled at all times.

To disable VID for processor 2, move a jumper to pins 1 and 2 (VIDBYP1).

To disable VID for processor 1, move a jumper to pins 3 and 4 (VIDBYP2). (This is the correct description: VIDBYP1 refers to processor 2, and VIDBYP2 to processor 1.)

Note: J103 block may not be present on all versions of the processor module. If not present, then VID is enabled and is not selectable.

1.21.3Processor Frequency Select Jumpers, J105

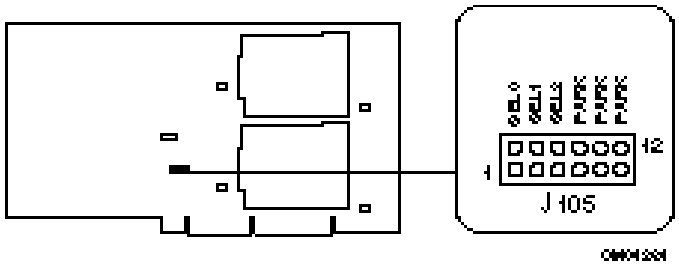


Figure 1.17 Processor Frequency Jumpers

CAUTION, select the actual frequency setting

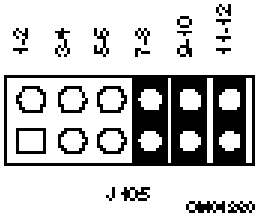
Damage to the processor may occur if you select a jumper setting frequency that is greater than the actual frequency of the processor.

Use this jumper block to select the processor core/bus frequency. The selection must match the frequency of the processor being installed in the system. Be sure that both boards are programmed to the same frequency. Install jumpers for the desired frequency as shown in the following table. Place any unused jumpers in the Park locations (pins 7-8; 9-10; 11-12).

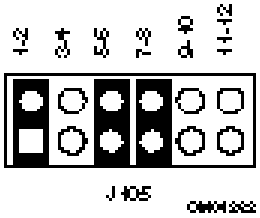
Table 1.11 Frequency Jumper Configurations

Frequency	SEL0 Pins 1-2	SEL1 Pins 3-4	SEL2 Pins 5-6
150/60 MHz	No jumper	No jumper	No jumper
180/60 MHz	Jumper	No jumper	No jumper
210/60 MHz	No jumper	Jumper	No jumper
240/60 MHz	Jumper	Jumper	No jumper
166/66 MHz	No jumper	No jumper	Jumper
200/66 MHz	Jumper	No jumper	Jumper
233/66 MHz	No jumper	Jumper	Jumper
266/66 MHz	Jumper	Jumper	Jumper

Example, jumpering for 150/60 MHz



Example, jumpering for 200/66 MHz



1.21.4Processor Board Fan Sink Connectors, J102 and J107

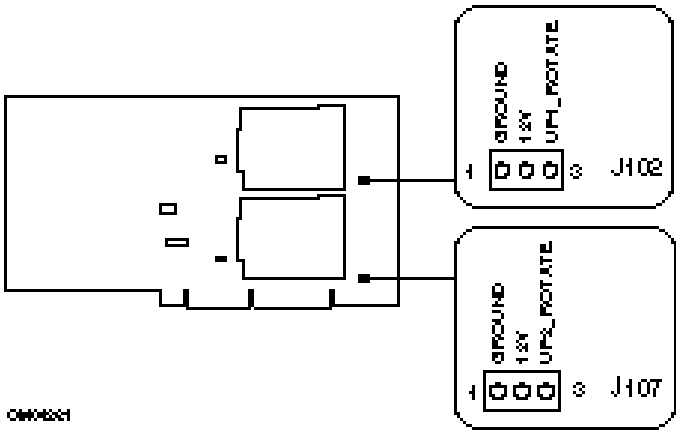


Figure 1.18 Fan Sink Connectors

J102 and J107 are connectors to provide power for optional fan sinks to cool the processors while the board set is being tested outside of the chassis on a test bench. Each fan sink comes with a 3-pin connector wire. The connectors are not used in normal system operation.

1.21.5Power Supply Considerations

The AP450GX MP Server board set is designed to operate with 2 or 3 420W custom power supply when installed in Intel's Poca chassis. Refer to Chapter 5 for the actual power requirements. Intel strongly recommends using the signals provided for remote sense. Without remote sense capabilities, it will be difficult to keep the power rails within the board sets specifications.

1.22Regulatory Compliance

Table 1.12 Regulatory Specifications

Board	Specification
Safety	UL 1950 CSA 22.2 No. 950 -M93 by cUL EN 60950 by TÜV IEC 950 by TÜV EN 60950 and Nordic deviations by NEMKO
Electromagnetic Emissions	Certified to FCC 47 Class B Tested, CISPR 22/85 Class B, EN 55022 Registered with VCCI
	Declaration of the Manufacturer or Importer: We hereby certify that this product is in compliance with EU Directive 89/336/EEC, using the EMC standards EN55022, EN61000-3-2 and EN50082-2.
Electromagnetic Immunity	Verified to comply with EN 50082-2

1.23Product Certification Markings

1.23.1European CE Marking

Marking on the board or shipping container.

1.23.2UL Recognition

UL Recognized Marking consists of UL File No. E139761 on component side of board PB No. on solder side of board. Board material flammability is 94V-1 or -0.

1.23.3Canadian Compliance

Marking consists of small c followed by a stylized backward UR on component side of board.

1.23.4Installation Requirements

CAUTION

To avoid an adverse impact on the compliance with safety or regulatory requirements due to installation of this board assembly, the following guidelines must be followed.

Follow Installation Instructions

Be sure to read and adhere to all of these instructions, and the instructions supplied with the host system and associated modules. If the instructions of the host system appear to be incompatible with these instructions or the instructions of any associated modules, contact the suppliers' technical support organization for the products involved to determine the appropriate action for continued safety and regulatory compliance of the resultant system. Failure to read and follow instructions provided by host system and module suppliers may result in increased safety risk and non-compliance with regional laws and regulations.

Assure Host System Compatibility

For electromagnetic compatibility, the host system enclosure and power supply should have passed electromagnetic compatibility testing using a board with a microprocessor from the same family as the microprocessor on this board, operating at the same or higher microprocessor speed. Also, only peripherals (computer input/output devices, terminals, printers, etc.) that are CE Marked and certified by the FCC to comply with Class B limits may be attached to this board. Pay particular attention to the installation instructions of the host system and other modules, particularly concerning certifications, external I/O cable shielding and filtering, mounting, grounding and bonding requirements to assure appropriate shielding effectiveness. Otherwise electromagnetic compatibility testing must be repeated on a representative sample of the complete system.

For safety, if mis-mating of connectors could result in a hazard, assure that all connectors are sufficiently keyed to prevent mis-mating.

Use Only In Intended Applications

This product was evaluated for use in systems installed in offices, homes, schools, computer rooms or similar applications. Other applications, such as medical, industrial, alarm systems and test equipment may necessitate a re-evaluation of the product suitability.

Assure Host System & Accessory Certifications

Assure that the host system, any other subassemblies such as board & drive assemblies being added in, and internal or external wiring, are properly certified for the region(s) the end-product will be used in. Proof of certification can be determined by the marks on the product. For example:

1.23.4.1Europe

The CE Marking signifies compliance with all relevant EU requirements. If the host system does not bear the CE Marking, obtain a supplier's Declaration of Conformity to the appropriate standards required by the European EMC Directive and Low Voltage Directive. Other Directives,

such as the Machinery and Telecommunications Directives, may also apply depending on the type of product. No regulatory assessment is necessary for low voltage DC wiring used internally, or wiring used externally when provided with appropriate overcurrent protection. Appropriate protection is achieved by max. 8 Amp current limiting circuit or a max. 5 Amp fuse or Positive Temperature Coefficient Resistor (PTC). All Intel baseboards presently have PTC's on all external ports which provide DC power externally.

1.23.4.2U.S.

For safety, a certification mark by a Nationally Recognized Testing Laboratory (NRTL) such as UL, CSA or ETL. External wiring must be UL Listed and suitable for the use. Internal wiring must be UL Listed or Recognized and rated appropriately for the voltages and temperatures involved. For electromagnetic interference, the FCC mark: Class A for commercial or industrial only; or Class B for all applications other than described above.

1.23.4.3Canada

For safety, a nationally recognized certification mark such as CSA or cUL. No regulatory assessment is necessary for low voltage DC wiring used internally, or wiring used externally when provided with appropriate overcurrent protection. Appropriate protection is achieved by max. 8 Amp current limiting circuit or a max. 5 Amp fuse or Positive Temperature Coefficient Resistor (PTC). All Intel baseboards presently have PTC's on all external ports which provide DC power externally.

1.23.5Installation Precautions

During installation and initial test, use caution to avoid personal injury and damage to wiring due to sharp pins on connectors and printed circuit assemblies, rough chassis edges and corners, and hot components. Adhere to warnings and limitations regarding accessibility into areas designated only for authorized technical personnel.

1.23.6Battery Marking

There is insufficient space on this board product to provide the required replacement and disposal instructions for the battery. The following marking must be placed permanently and legibly on the host system as near as possible to the battery:

CAUTION

Danger of explosion if battery is incorrectly replaced.

Replace with only the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

1.23.7Overload Protection

Unless the power supply is provided with inherent overcurrent protection, use caution to avoid overloading the power supply output. This can be accomplished by assuring that the calculated total current load of all the modules within the system is less than the output current rating of the power supply. Failure to accomplish this could result in overheating in the power supply, which

could result in a fire or could cause damage to insulation separating hazardous AC line circuitry from low-voltage user accessible circuitry. If the load drawn by a particular module cannot be determined by the markings and instructions supplied with the module, contact the module supplier's technical support organization.

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2 System Resources

2.1Memory Map

Table 2.1 Memory Addressing

Address Range (hex)	Amount	Function
0000_0000H – 0007_FFFFH	512 KB	Base system memory (fixed)
0008_0000H – 0009_FFFFH	128 KB	Base system memory or ISA memory enabled in Setup
000A_0000H – 000B_FFFFH	128 KB	ISA video buffer
000C_0000H – 0007_FFFFH	160 KB	Video BIOS, AIC-7880 SCSI BIOS, other option ROMs. All these can be shadowed
000E_8000H – 000F_FFFFH	96 KB	System BIOS and data areas (fixed)
0010_0000H – 00EF_FFFFH	14 MB	System memory or unused
00F0_0000H – 00FF_FFFFH	1 MB	System memory or EISA memory
0100_0000H – FEBF_FFFFH	4060 MB	System memory or add-in cards or unused
FEC0_0000H – FEC0_0FFFH	4 KB	I/O APIC #1
FEC0_1000H – FEC0_1FFFH	4 KB	I/O APIC #2
FEC0_2000H – FEC0_7FFFH	24 KB	Unused
FEC0_8000H – FEC0_8FFFH	4 KB	Local APIC
FEC0_9000H – FFF7_FFFFH	4939 KB	Add-in card or unused
FFF8_0000H – FFFF_FFFFH	512 KB	System BIOS (fixed)

2.2I/O Map

Table 2.2 I/O Addressing

I/O address	Resource
0000 – 001F	DMA controller 1
0020 – 0021	Interrupt controller 1
0022 – 0023	EISA bridge configuration space access ports
0040 – 005F	Programmable Timer
0060 – 0064	Keyboard Controller
0061	NMI Status & Control Register
0070	NMI Mask (bit 7) & RTC Address (bits 6:0)
0071	Real-time Clock (RTC)
0080 – 0081	PCEB BIOS Timer
0080 – 008F	DMA Low Page Register
0092	System Control Port A (PC-AT control Port)
00A0 – 00BF	Interrupt Controller 2
00C0 – 00DF	DMA Controller 2
00F0	Clear NPX error
00F8 – 00FF	x87 Numeric Coprocessor
0102	Video Display Controller
0170 – 0177	Secondary Fixed Disk Controller (IDE)
01F0 – 01F7	Primary Fixed Disk Controller (IDE)
0278 – 027F	Parallel Port 2 (relocatable)
02E8 – 02EF	Serial Port 4 (relocatable)
02F8 – 02FF	Serial Port 2 (relocatable)
0370 – 0377	Secondary Floppy
0378 – 037F	Parallel Port 1 (relocatable)
03B4 – 03BA	Monochrome Display Port
03BC – 03BF	Parallel Port 3
03C0 – 03CF	Enhanced Graphics Adapter
03D4 – 03DA	Color Graphics Controller

System I/O Map, continued

I/O address	Resource
03E8 – 03EF	Serial Port (relocatable)
03F0 – 03F7	Floppy Disk Controller
03F8 – 03FF	Serial Port 1 (relocatable)
0400 – 043F	DMA Controller 1, Extended Mode Registers
0461	Extended NMI / Reset Control
0462	Software NMI
0464	Last EISA Bus master granted
0480 – 048F	DMA High Page Register
04C0 – 04CF	DMA Controller 2, High Base Register
04D0 – 04D1	Interrupt Controllers 1 and 2 Control Register
04D4 – 04D7	DMA Controller 2, Extended Mode Register
04D8 – 04DF	Reserved
04E0 – 04FF	DMA Channel Stop Registers
0C80 – 0C83	EISA System Identifier Registers
0C84	Board Revision Register
0CF8	PCI CONFIG_ADDRESS Register
0CFC	PCI CONFIG_DATA Register
n000 –n0FF	EISA Slot n I/O Space (n = 1 to 4)
x100 – x3FF	ISA I/O slot alias address
n400 – n4FF	EISA Slot n I/O Space (n = 1 to 4)
x500 – x7FF	ISA I/O slot alias address
n800 – n8FF	EISA Slot n I/O Space (n = 1 to 4)
x900 – xBFF	ISA I/O slot alias address
nC00 – nCFF	EISA Slot n I/O Space (n = 1 to 4)
xD00 – xFFF	ISA I/O slot alias address

2.3PCI Configuration Space Map

Table 2.3 PCI Configuration Space Map

Bus Number (hex)	Dev Number (hex)	Function Number (hex)	Description
00	C8	00	Intel 82454GX (PB) PCI Bridge - Bus 0 (Compatibility)
00	D0	00	Intel 82454GX (PB) PCI Bridge - Bus 1
00	A0	00	Intel 82453GX (DC) Memory Controller
00	78	00	INCA
00	70	00	PCEB
00	58	00	P1 (PCI Bus 0, slot 1)
00	60	00	P2 (PCI Bus 0, slot 2)
00	68	00	P3 (PCI Bus 0, slot 3)
01	60	00	On-board SCSI controller, Channel B
01	58	00	On-board SCSI controller, Channel A
01	50	00	P4 (PCI Bus 1, slot 1)
01	68	00	P5 (PCI Bus 1, slot 2)
01	70	00	P6 (PCI Bus 1, slot 3)

2.4DMA Channels

Table 2.4 DMA Channel Mapping

Channel	Device
0	(add-in board)
1	(add-in board)
2	Diskette drive
3	IDE hard disk drive
4	Reserved
5	(add-in board)
6	(add-in board)
7	(add-in board)

2.5Interrupts

Table 2.5 Interrupt Mapping

IRQ	Device
NMI	Parity error
0	Interval timer
1	Keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	Onboard serial port B (COM2) or add-in board
4	Onboard serial port A (COM1) or add-in board
5	Parallel port LPT2 or add-in board
6	Onboard diskette (floppy) controller, if enabled
7	Parallel port LPT1 or add-in board
8	Real-time clock (RTC)
9	(add-in board)
10	(add-in board)
11	(add-in board)
12	Onboard PS/2 mouse port or add-in board
13	Math coprocessor error
14	IDE hard drive controller, if enabled
15	(add-in board)

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3 BIOS, Setup, SCU and SCSISelect™ Utilities

3.1Introduction

The Alder board set uses an Intel BIOS, which is stored in Flash memory and easily upgraded using a floppy disk-based program. In addition to the Intel BIOS, the Flash memory also contains the Setup utility, Power-On Self Tests (POST), the PCI auto-configuration utility, and Windows 95 ready Plug-N-Play 1.0a. This board set also supports system BIOS shadowing, allowing the BIOS to execute from 64-bit on-board write-protected DRAM. The Setup and SCU utilities are used to change configuration values in Flash memory. In addition, the SCSISelect utility is provided to configure the on-board AIC-7880 SCSI controllers. All three utilities are be described in more detail in this chapter.

3.2BIOS

The BIOS displays a sign-on message during POST identifying the type of BIOS and a five-digit revision code. The initial production BIOS in the baseboard will be identified as 1.00.04.CD0

3.2.1BIOS Flash Memory Organization

The Intel 4Mb Flash component is organized as 512K x 8 (512 KB). The Flash device is divided into seven areas, as described in Table 3.1.

Table 3.1 Flash Memory Organization

System Address		FLASH Memory Area
FFFF0000H	FFFFFFFFH	64 KB Main BIOS
FFFEC000H	FFFEFFFFH	16 KB Boot block (Not FLASH erasable)
FFFEA000H	FFFEBFFFH	8 KB ESCD Area (Plug-N-Play data storage area)
FFFE9000H	FFFE9FFFH	4 KB Reserved for BIOS
FFFE8000H	FFFE8FFFH	4 KB OEM Logo Area
FFFE0000H	FFFE7FFFH	32 KB Reserved for BIOS
FFFD0000H	FFFDFFFFH	64 KB Reserved for BIOS
FFFC0000H	FFFCFFFFH	64 KB Reserved for BIOS

3.2.2BIOS Upgrades

Flash memory makes distributing BIOS upgrades easy. A new version of the BIOS can be installed from a diskette. BIOS upgrades are available the secure section on the Intel bulletin board or from Intel's field representative.

The disk-based Flash upgrade utility, FMUP.EXE, has three options for BIOS upgrades:

- The Flash BIOS can be updated from a file on a disk;
- The current BIOS code can be copied from the Flash memory to a disk file as a backup in the event that an upgrade cannot be successfully completed; or

- The BIOS in the Flash device can be compared with a file to ensure the system has the correct version.

The upgrade utility ensures the upgrade BIOS extension matches the target system to prevent accidentally installing a BIOS for a different type of system.

3.2.3ISA IDE Support

The ISA based IDE connector with independent I/O channel support are setup up automatically by the BIOS if the user selects "Autoconfiguration" in setup. The IDE interface supports PIO Mode 3, and Mode 4 hard drives and recognition of ATAPI CD-ROMs, tape drives, and any other ATAPI devices. The BIOS will determine the capabilities of each drive and configure them to optimize capacity and performance. For the high capacity hard drives typically available today, the drive will be automatically configured for Logical Block Addressing (LBA) for maximum capacity and to PIO Mode 3 or 4 depending on the capability of the drive. The user is able to override the auto-configuration options by using the manual mode setting. The ATAPI Specification Revision 2.5 recommends that an ATAPI device be configured as shown in the table below.

Table 3.2 Recommendations for Configuring an ATAPI Device

Primary Cable		Secondary Cable		
Drive 0	Drive 1	Drive 0	Drive 1	
ATA				Normal, no ATAPI
ATA		ATAPI		Disk and CD-ROM for enhanced IDE systems
ATA	ATAPI			Legacy IDE System with only one cable
ATA		ATAPI	ATAPI	Enhanced IDE with CD-ROM and a tape or two CD-ROMs

3.2.4PCI Auto-Configuration

The PCI auto-configuration utility operates in conjunction with the system Setup utility to allow the insertion and removal of PCI cards to the system without user intervention (Plug-N-Play). When the system is turned on after adding a PCI add-in card, the BIOS automatically configures interrupts, I/O space, and other parameters. PCI interrupts are distributed to available ISA interrupts that have not been assigned to an ISA card, or system resources. Those interrupts left set to "available" in the CMOS setup will be considered free for PCI add-in card use.

The PCI Auto-Configuration function complies with version 2.10 of the PCI BIOS specification. System configuration information is stored in ESCD format. The ESCD data may be cleared by setting the CMOS clear jumper to the ON position.

PCI specification 2.1 for add-in card auto-configuration is also a part of the Plug-N-Play BIOS. Peer-to-peer hierarchical PCI Bridge 1.0 is supported, and by using an OEM supplied option ROM or TSR, a PCI-to-PCMCIA bridge capability is possible as well.

3.2.5ISA Plug-N-Play

The BIOS incorporates ISA Plug-N-Play capabilities as delivered by Plug-N-Play Release 1.0A (Plug-N-Play BIOS V.. 1.0A, ESCD V.. 1.03). When used in conjunction with the EISA

Configuration Utility (ECU) for DOS, the system allows auto-configuration of Plug-N-Play ISA cards, PCI cards, and resource management for legacy ISA cards. Because the BIOS supports configuring devices across PCI bridges, release 1.41 or greater of the ICU must be used with the baseboard to properly view and change system settings. System configuration information is stored in ESCD format. The ESCD data may be cleared by setting the CMOS clear jumper to the ON position.

The BIOS also has a setup option to support the Windows 95 run time Plug-N-Play utilities. When this option is selected, only devices critical to booting are assigned resources by the BIOS. Device Node information is available for all devices to ensure compatibility with Windows 95.

Note: copies of the IAL Plug-N-Play specification may be obtained via the Intel BBS , or via CompuServe by typing Go PlugPlay.

3.2.6Language Support

The BIOS setup screen and help messages are supported in 32 languages. There are five languages available at this time: American English, German, Italian, French, and Spanish. Translation to other languages may become available at a later date.

3.2.7Boot Options

Booting from CD-ROM is supported in adherence to the "El Torito" v. 1.0 bootable CD-ROM format specification developed by Phoenix Technologies and IBM. Under the *Boot Options* field in setup, *CD-ROM* is one of four possible boot devices which are defined in priority order. The default setting is for floppy to be the primary boot device and hard drive to be the secondary boot device. If CD-ROM is selected, it must be the first device. The third and fourth devices are set to *disabled* in the default configuration. The user can add also select *network* as a boot device. The network option allows booting from a network add-in card with a remote boot ROM installed.

✎ **NOTE**

A copy of "El Torito" v. 1.0 is available on the Phoenix Web page (http://www.ptltd.com/techs/specs.html).

3.2.8Console Redirection

The BIOS supports redirection of both the video and keyboard via a serial port (COM 1 or COM 2).. When console redirection is enabled, keyboard input and video output is transferred not only through the normal keyboard and video connections, but also via the serial port (i.e. keyboard inputs from both sources are considered valid and video is displayed to both sources). If you choose, the system can be operated without a keyboard or monitor attached to the system and run entirely via the remote console. Both Setup and the SCU can be used while console redirection is enabled.

When connecting a modem up to the COM port, it should be configured in both auto-answer and the modems reaction to DTR must be to switch to command state.

Keystroke Mappings

During console redirection, the **remote** terminal (which may be a dumb terminal or a system with a modem running a package such as ProComm) sends keystrokes to the **local** server, which then passes video back. For keys which have an ASCII mapping (such as A and Ctrl-A), the ASCII character is sent For keys which do not have an ASCII mapping (such as F1 and Alt-A), a string of characters as defined in the tables below is sent.

The strings are based on the ANSI BBS and vt100 terminal standards. Since these terminals do not support all the keys on the standard 101 key U.S. keyboard, some strings were added (such as F5 - F12, Page Up, and Page Down.) Alt key combinations were created by adding the prefix **^[}** to the character (both ^[}a and ^[}A will be interpreted at the local server as alt-a.). In addition, ^[{ will be interpreted as a screen refresh.

Since the mappings for non-ASCII keys are done via table lookup, the decision was made not to support unusual combinations such as Ctrl-F1. This saves a little bit of space in BIOS, as well as a good deal of coding to interpret these sequences.

Table 3.3 Non-ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
ESC	^[	NS	NS	NS
F1	^[OP	NS	NS	NS
F2	^[OQ	NS	NS	NS
F3	^[OR	NS	NS	NS
F4	^[OS	NS	NS	NS
F5	^[OT	NS	NS	NS
F6	^[OU	NS	NS	NS
F7	^[OV	NS	NS	NS
F8	^[OW	NS	NS	NS
F9	^[OX	NS	NS	NS
F10	^[OY	NS	NS	NS
F11	^[OZ	NS	NS	NS
F12	^[O1	NS	NS	NS
Print Screen	NS	NS	NS	NS
Scroll Lock	NS	NS	NS	NS
Pause	NS	NS	NS	NS
Insert	^[[L	NS	NS	NS
Delete	(7Fh)	NS	NS	NS
Home	^[[H	NS	NS	NS
End	^[[K	NS	NS	NS
Pg Up	^[[M	NS	NS	NS
Pg Down	^[[2J	NS	NS	NS
Up Arrow	^[[A	NS	NS	NS
Down Arrow	^[[B	NS	NS	NS
Right Arrow	^[[C	NS	NS	NS
Left Arrow	^[[D	NS	NS	NS
tab	(09h)	NS	NS	NS

NS = Not supported, (xxh) = ASCII character xx

Table 3.3 ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
backspace	(08h)	(08h)	(7Fh)	^[}(08h)
(accent) `	`	(tilda) ~	NS	^[}`
1	1	!	NS	^[}1
2	2	@	NS	^[}2
3	3	#	NS	^[}3
4	4	$	NS	^[}4
5	5	%	NS	^[}5
6	6	^	NS	^[}6
7	7	&	NS	^[}7
8	8	*	NS	^[}8
9	9	(	NS	^[}9
0	0	)	NS	^[}0
(dash) -	-	(under) _	(1Fh)	^[}-
=	=	+	NS	^[}=
a to z	a to z	A to Z	(01h) to (1Ah)	^[}a to ^[}z
[	[	{	(1Bh)	^[}[
]	]	}	(1Dh)	^[}]
\	\	|	(1Ch)	^[}\
(semi-colon) ;	;	(colon) :	NS	^[};
(apostrophe) '	‘	(quote) "	NS	^[}'
(comma) ,	,	<	NS	^[},
(period) .	.	>	NS	^[}.
/	/	?	NS	^[}/
(space)	(20h)	(20h)	(20h)	^[}(20h)

NS = not supported, (xxh) = ASCII character xx

Limitations

Console redirection can only be used in “Real Mode”. It will not work in “Protected Mode. Console redirection only works with text based video, and will not work with graphics based video applications. For keyboard redirection to work, the application on the local server must use the INT 16 keyboard services normally to receive keystrokes. If the program uses INT 9 and INT 15 services instead, the redirection will not work. For example, the DOS edit program cannot be used remotely due to the way it gets keys in the menu code and WordPerfect will not work due to its extensive use of Shift-F1, Ctrl-F1 and other “special” keystrokes.

3.3Setup Menu Screens

This section describes the BIOS Setup options. The Setup utility stores configuration values in flash memory and in the battery-backed memory of the real-time clock (RTC). Values you enter in Setup are overwritten when you run the SCU.

For a number of options, the settings are made by using the SCU, not Setup. The values are simply displayed in the Setup screens. To see the descriptions of such options, refer to the SCU section later in this chapter.

Setup has four major menus and several sub-menus. To move between the major menus, use the ← → keys. To display the sub-menus, press <Enter> when the prompt is displayed beside an option name.

When you see this on the screen:	What it means
On screen, an option is grayed out. In the tables in this chapter, the phrase "Display only" appears in the "Choice" column.	You cannot change or configure the option through Setup. You must use (1) a different Setup screen or (2) the SCU. In some cases, the option may be auto-configured or auto-detected.
On screen, the phrase <Press Enter> appears next to the option, and, in the tables here, in the "Default/next menu" column.	Press <Enter> to display a sub-menu (either a separate full-screen menu or a small pop-up menu with one or several choices).
"Default/next menu" appears as a column header in the tables here.	The column shows either the default option setting, a grayed-out "display only" setting, or a "Press Enter" prompt that leads to a separate menu.

3.3.1When to Run Setup

... if you get a boot-time prompt that says to do so.

... if you need to enable or properly configure your diskette drive.

... if you do not have access to a diskette drive.

Much of the system configuration is done through the SCU, not Setup. Because the SCU is provided on diskette, a diskette drive needs to be connected and enabled. After configuring the system, you may prefer to secure it against casual or unauthorized access by someone using diskettes. Therefore, you can

- run Setup to enable the diskette drive
- then use Setup or the SCU to configure the system
- run Setup again to disable the diskette drive for security

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Main Menu

Option	Default	Choices
System Date	Month xx, 1995	Default is current date.
System Time	xx:xx:xx	Default is random.
Floppy Options	Press Enter	
Primary IDE Master	Press Enter	Display menu.
Primary IDE Slave	Press Enter	Display menu.
Secondary IDE Master	Press Enter	Display menu.
Secondary IDE Slave	Press Enter	Display menu.
Language	English (US)	Display menu. Default is English.
Boot Options	Press Enter	Display boot option menu.
Video Mode	EGA / VGA	Display only. Go to SCU to select.
Mouse	Installed	Display only. Go to SCU to select.
Base Memory	640KB	Display only. Go to SCU to select.
Extended Memory	32678KB	Display only. Go to SCU to select.

System Date and System Time—to change, type in the correct date and time and press <Enter>.

Floppy Options—displays a menu that lists the type of diskette drive connected. If one is not connected, you will see the word "Disabled."

✎ **You can use Floppy Options menu to limit access to drive**

Use this menu to specify whether access to the diskette drive is Read/Write or Read Only.

Primary IDE Master—a separate menu screen appears for EACH of the IDE devices. For each IDE drive, if the system has already been configured, you will see the name of the device or the phrase "Not installed."

Language—step through the language choices available for the BIOS prompts. If you change the default (English), you will not see any change until you exit the SCU and enter Setup. Only the BIOS prompts and menus appear in the selected language. The SCU screens remain in English.

Boot Options—a separate menu screen appears.

Video Mode—displays the mode selected in the SCU.

Mouse—displays the mode selected in the SCU.

Memory—displays the amount of base and extended memory detected.

The most stable system will be achieved if you use the recommended default settings, although you are free to try other options. Keep the settings for the primary and secondary IDE masters and slaves.

3.3.2Main Menu: IDE Device

Each IDE device, primary or secondary, master or slave, has a separate menu screen. To display each, select the item from the main menu and press <Enter>.

Option	Default	Choices*
IDE Device Configuration	Auto Configured	**Auto Configured** User Definable
Number of Cylinders	1057	If autoconfigured, display only.
Number of Heads	16	If autoconfigured, display only.
Number of Sectors	63	If autoconfigured, display only.
Maximum Capacity	520 MB	If autoconfigured, display only.
IDE Translation Mode	Auto Detected	Standard CHS addressing Extended CHS Logical block **Auto Detected**
Multiple Sector Setting	Auto Detected	**Auto Detected** 4 Sectors per block 8 Sectors per block Disabled
Fast Programmed I/O Modes	Auto Detected	**Auto Detected** Disabled

* Choices shown in **bold** are factory default.

IDE Device Configuration—when Auto Configured, the BIOS automatically senses and configures any IDE drives in the system. The User Definable option lets you specify the IDE drive parameters.

Number of Cylinders—if Auto Configured, the value is display-only.

Number of Heads—if Auto Configured, the value is display-only.

Number of Sectors—if Auto Configured, the value is display-only.

Maximum Capacity—if Auto Configured, the value is display-only.

IDE Translation Mode—select the translation mode for the IDE hard disk:

Standard CHS addressing: cylinder count of 1024 or less

Extended CHS: cylinder count greater than 1024

Logical block: if supported by disk

Auto Detected: selects proper method based on information from the hard disk

Multiple Sector Setting—set IDE programmed I/O cycles so that multiple sectors are transferred with a single interrupt.

Fast Programmed I/O Modes— the BIOS queries an IDE hard disk connected to the PCI IDE bus and uses the fastest PIO protocol supported by the hard disk/controller pair. Can be disabled.

3.3.3Main Menu: Boot Options

Option	Default	Choices*
First Boot Device	{Name of device}	**Floppy**/Disabled/Hard Disk/CD-ROM/Network
Second Boot Device	{Name of device}	**Hard Disk**/Disabled/Floppy/Network
Third Boot Device	{Name of device}	**Disabled**/Floppy/Hard Disk/Network
Fourth Boot Device	{Name of device}	Network/**Disabled**/Floppy/Hard Disk
CD-ROM Image Type	Floppy	Floppy/Hard Disk
System Cache	Enabled	Enabled/Disabled
Boot Speed	Turbo	Turbo/Deturbo
Num Lock	Off	Off/On
Setup Prompt	Enabled	Enabled/Disabled
Typematic Rate Programming	Default	Default/Override

* Choices shown in **bold** are factory default.

Boot Devices—selects the order in which the system checks drives to find an operating system to boot from.

CD-ROM Image Type—selects either Floppy or Hard Disk for the type.

System Cache—when system cache is enabled, the cache controllers in all Pentium Pro processors are initialized consistently (a) among all such processors in a multiprocessor system and also (b) between the Pentium Pro processors and the chip set. When system cache is disabled, system performance will decrease significantly.

Boot Speed—selects CPU speed. When set to Deturbo, system performance will decrease significantly.

Num Lock—sets the initial state of the Num Lock keyboard feature when the system boots. When set to Off, the numeric keypad is not locked on at boot-time.

Setup Prompt—enables/disables the screen prompt to enter Setup utility.

Typematic Rate Programming—when set to Default, the Rate Delay = 250 ms, and the Rate = 15 characters per second. When set to Override, the Rate Delay and Rate can be reprogrammed.

3.3.4Advanced Menu

On the Advanced menu, the type and speed of processor(s) are displayed (not selected). The Advanced menu leads to three separate configuration menus: Peripheral, Advanced Chipset, and Plug and Play. Press <Enter> to display each in turn.

Option			Default	Choices
Slot 1:	Processor 1	Type	Pentium Pro processor	
	Processor 1	Speed	166 MHz	
	Processor 2	Type	Pentium Pro processor	
	Processor 2	Speed	166 MHz	
Slot 2:	Processor 1	Type	Absent	
	Processor 1	Speed	Absent	
	Processor 2	Type	Absent	
	Processor 2	Speed	Absent	
		Cache Size	512K	
	Peripheral Configuration		Press Enter	Go to Peripheral Configuration.
Advanced Chipset Configuration			Press Enter	Go to Advanced Chipset Configuration.
	Plug and Play Configuration		Press Enter	Go to Plug and Play Configuration.

3.3.5Peripheral Configuration

Option	Default	Choices
Configuration Mode	Auto	Auto / Manual:
Standard IDE Interface	Enabled	Enabled/Disabled
Floppy Interface	Enabled	Enabled/Disabled
Serial Port 1 Address	COM1, 3F8h	Disabled/COM1, 3F8h/COM3, 3E8h/COM4, 2E8h
Serial Port 2 Address	COM2, 2F8h	Disabled/COM2, 2F8h/COM3, 3E8h/COM4, 2E8h
Parallel Port Address	LPT1, 378h	Disabled/LPT3, 3BCh/LPT1, 378h/:LPT2, 278h
Parallel Port Mode	ISA Compatible	ISA Compatible/PS/2 Compatible/EPP Compatible/ECP Compatible
Parallel Port ECP-DMA	Disabled	Disabled/DMA 3/DMA 5/ DMA 6
Serial Port 1 IRQ	IRQ4	
Serial Port 2 IRQ	IRQ3	
Parallel Port IRQ	IRQ7	
Onboard SCSI-A ROM Scan	Enable	Enable/Disable
Onboard SCSI-B ROM Scan	Enable	Enable/Disable
Console Redirection	Disable	Disable/Port 1/Port 2

Configuration Mode—when set to Auto, system peripherals are automatically configured during power up. When set to Manual, system peripherals must be explicitly confirmed.

Standard IDE Interface—enables or disables the onboard standard IDE hard disk controller.

Floppy Interface—enables or disables the onboard floppy disk controller.

Serial Port 1 Address—enables the onboard serial port and configures the COM number and I/O address.

Serial Port 2 Address—enables the onboard serial port and configures the COM number and I/O address.

Parallel Port Address—enables the onboard parallel port and configures the LPT number and I/O address.

Parallel Port Mode—compatible mode is the AT-spec output only mode. Extended mode set the port to the extended capabilities mode.

Onboard SCSI-A ROM Scan—SCSI device gets all other resources including IRQ and memory, even if the ROM scan is disabled.

Onboard SCSI-B ROM Scan—SCSI device gets all other resources including IRQ and memory, even if the ROM scan is disabled.

Console Redirection—enables the console redirection to a serial port.

3.3.6Advanced Chip set Configuration

Option	Default	Choices
Base Memory Size	640KB	512KB / 640KB
VGA Buffer Attributes	Uncacheable	Uncacheable / USWC
SMM	Disable	Enable / Disable
MPS version	1.1	1.1/1.4
Second I/O APIC	Disable	Enable / Disable
Cache Mode	Write Back	Write Back / Write Through
IOQ Depth	Auto Configure	Auto Configure / 1 / 8
Outbound Posting	Disable	Enable/Disable
PCI Line Prefetch	Enable	Enable/Disable
Addr Bit Permuting	Disable	Enable/Disable
Fast String	Disable	Enable/Disable
Bus Performance	Auto Configure	Auto Configure / Low / 82450A / 82450B
BINIT Mode	Enable	Enable / Disable
AERR Mode	Enable	Enable / Disable
BERR Mode	Enable	Enable / Disable
EERR Mode	Disable	Enable / Disable
MERR Mode	Enable	Enable / Disable
PERR Mode	Disable	Enable / Disable

Base Memory Size—use to set the amount of baseboard base memory.

VGA Buffer Attributes—select Uncacheable Speculative Write Combined (USWC) to allow the processor to perform speculative combining while writing to the VGA frame buffer. Select Uncacheable for adapters that do not support USWC mode.

SMM—enable system management mode, including event logging and ECC memory support.

MPS Version—choose a multiprocessing specification version number for the BIOS to use when building the MPS table. Select 1.4 for Windows NT†, and select 1.1 for all other operating systems.

Second I/O APIC—If disabled, the BIOS does not report the second I/O APIC in the MPS tables. The operating system will not be able to use it. Enable this feature only if the operating system is capable of supporting the second I/O APIC.

Cache Mode—set the processor's L1 and L2 caches to use either write back or write through mode.

IOQ Depth—configure the In-order Queue to support either 1 or 8 outstanding pipelined transactions on the host (processor) bus.

Outbound Posting—enable the posting of writes to the PCI bus from the host (processor) bus.

PCI Line Prefetch—enable the prefetching of up to three additional cache lines in response to PCI Line Read and PCI Read Multiple commands.

Address Bit Permuting—when enabled, the memory controller will swap the high order row selection bits with some low order bits when computing the effective address. In some applications this can increase performance by decreasing the precharge penalties when accessing system memory.

Bus Performance—this setting turns on and off certain performance features in the chip set based on the revision level of the hardware. The Auto Configuration setting allows the BIOS to detect your hardware and set the appropriate level. Although you can override this and hard-code the system to a given level, overriding may cause the system to become unstable.

BINIT Mode—if enabled, the host (processor) bus will attempt to reinitialize in response to a noncorrectable error. Disabling this will prevent the system from trying to recover from the noncorrectable error.

AERR Mode—enable the detection of Address Parity Errors on the host (processor) bus.

BERR Mode—BERR is used to signal any error condition on the host (processor) bus that will not impact the future reliability of the bus. If enabled, the operating system error handler will attempt to correct the error. If disabled, then the BERR will be ignored.

EERR Mode—enable the reporting of EISA bus time-out errors.

MERR Mode—enable ECC error correction on the host (processor) bus.

PERR Mode—enable the detection of PCI bus protocol violations.

3.3.7Plug and Play Configuration

Latency Timer (PCI Clocks)	Ensures that a PCI card can access the PCI bus within the specified number of PCI clocks.

3.3.8Security Menu

Option	Default	Choices
Set User Password	Press Enter	
Set Administrative Password	Press Enter	
Unattended Start	Disabled	Disabled/enabled
Security Hot Key (CTRL-ALT-)		
Keyboard Inactivity Timer	10	0 - 10 - 128
Video Blanking	Disabled	Disabled/enabled
Floppy Writes	Disabled	Disabled/enabled
Reset and Power Switch Locking	Enabled	Disabled/enabled

If you enter a user password, the following items will appear:

```
User password is enabled.

Administrative password is disabled.
```

Set User Password—user password controls access to the system at boot. The password can be up to seven characters.

Set Administrative Password—administrative password controls access to the Setup utility and the SCU. The password can be up to seven characters.

Unattended Start—if feature is enabled, the system can boot before a password is required. The keyboard and mouse remain locked until the user password is entered.

Security Hot Key—secure the system immediately, rather than wait for the inactivity time-out period, use a hot-key combination that you set through the SCU or Setup.

Keyboard Inactivity Timer—specify a keyboard/mouse inactivity time-out period of 1 to 128 minutes (in 1-minute increments). If the timer is enabled, and no keyboard or mouse action occurs for the specified period, keyboard and mouse input will be inhibited.

Video Blanking—if feature is enabled, the monitor display will go blank after the specified inactivity time-out period occurs.

Floppy Writes—if feature is enabled, the diskette drive will be write-protected after the specified inactivity time-out period occurs.

Reset and Power Switch Locking—if feature is enabled, the power switch and reset button will be locked when the system is in secure mode.

3.3.9Exit Menu

Exit saving changes	Save Setup information to CMOS and exit the utility.
Exit discarding changes	Exit the utility without saving the Setup information to CMOS.
Load Setup defaults	Default Setup values are loaded and displayed by the utility.
Discard changes	Discard the changes made in the current Setup session but do not exit the utility.

3.4System Configuration Utility (SCU)

The system configuration utility (SCU) is the main tool to configure the system or to check or change the configuration. Most system settings can be entered from either the SCU or Setup, but the SCU provides conflict resolution as well as access to information about ISA, ISA Plug-N-Play, EISA, and PCI adapters.

✎ **System must have a diskette drive**

Your system must have a diskette drive present and enabled to use the SCU, because it is provided on a diskette. If a drive is present but is disabled or improperly configured, use the BIOS Setup utility to enable or configure the diskette drive. Then make a bootable SCU diskette and use the SCU to configure the system.

3.4.1When to Run the SCU

...when you first set up and configure your system

...if you get a configuration error message at power-on
...each time you add, remove, or move an EISA or ISA add-in board
...each time you add or remove memory

Running the SCU is also recommended for Plug-N-Play and PCI add-in boards.

3.4.2Where the SCU Gets Information

Information comes from	Description
Configuration (.CFG) *or* overlay (.OVL) files	For the baseboard, we provide these files. For EISA and some ISA add-in boards, each comes with a diskette that contains a .CFG file (and an optional .OVL file) supplied by the device manufacturer. The file describes the board's characteristics and the system resources it requires.
Configuration registers	The configuration registers on PCI and Plug-N-Play add-in boards contain the same type of information that an EISA .CFG file does. The SCU is PCI and Plug-N-Play aware, and it complies with the EISA Specification (version 3.12) and ISA Plug-N-Play Specification (version 1.1).
Your option selections	The SCU stores your information by modifying ISA CMOS and EISA nonvolatile RAM (NVRAM). It stores most of the values in the battery-maintained memory of the real-time clock (RTC); it stores the rest of the values in flash memory.

3.4.3Checking the Configuration at Power-on

At power-on or rebooting, the BIOS POST routines and the Plug-N-Play Auto Configuration Manager check and configure the hardware. POST checks the values that have been stored against the actual hardware configuration; if the values do not agree, you will get an error message. You must then run the SCU to correct the configuration before the system boots.

3.4.4How to Use the SCU

First make a bootable diskette, and copy the file HIMEM.SYS onto it.

1. Turn on your video display monitor and system.
2. There are three ways to start and run the SCU:

   - From diskette: insert the System Configuration Disk in drive A, and then press the reset button or type <Ctrl+Alt+Del> to reboot the system.
   - From a DOS directory that you have copied onto your hard drive, type SCU. Press <Enter>. If you use this method, you need to load HIMEM.SYS into the AUTOEXEC.BAT and CONFIG.SYS files.
   - From diskette in drive A: change to drive A and type SCU at the MS-DOS† prompt. Press <Enter>.

     Whether or not you can use the second and third ways depends on how much main memory is used by drivers you have loaded on the system.

The SCU has four major configuration menus and several sub-menus. From the main menu, select "Step 1: About System Configuration" for information about setting up your computer.

To navigate the screens	Press key	or use mouse
Change between major menus	← or →	
From main menu, press up or down arrow to highlight an item	or ↓	Point to item
Select an item	<Enter>	Double-click left button
Get help	<F1>	Point to help on toolbar
Enter numbers and symbols	numeric keypad keys	
To change options	Enter Administrator password if this is enabled	

✎ **To run the SCU faster on a DOS-based system**

To run the SCU faster on a DOS-based system, copy to a directory on your hard drive, and run it from there. The SCU may not run properly unless HIMEM.SYS is loaded and there is approximately 600 KB of conventional system memory available.

3.4.5Configuring the System

There are six steps to configure your system. These steps are accessed from the main menu:

- Step 1: About System Configuration
- Step 2: Add and Remove Boards
- Step 3: Change Configuration Settings
- Step 4: Save Configuration
- Step 5: View Switch/Jumper Settings
- Step 6: Exit

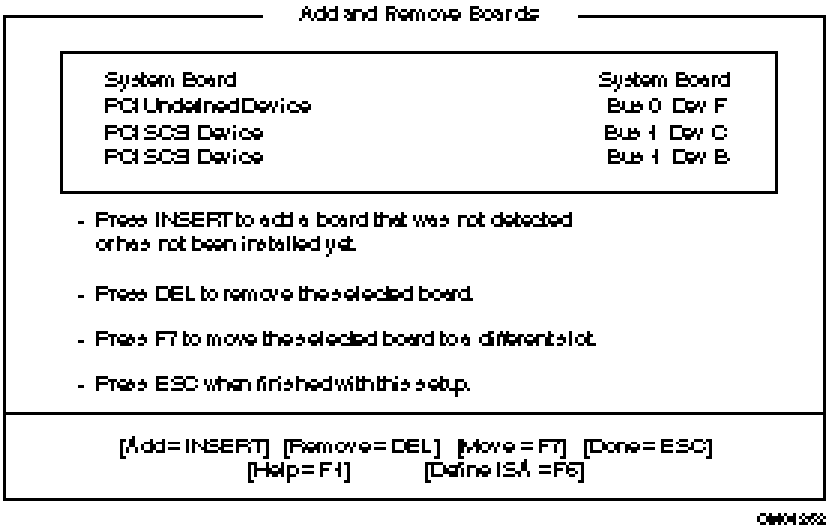
The SCU has three major menus and multiple sub-menus. Follow the screen prompts to move between the major menus, display sub-menus, and make selections.

About System Configuration

This step provides basic information for configuring expansion devices. More experienced users can skip this step.

Add and Remove Boards

Use this step to add, delete, or move boards. Most boards are automatically detected and added by the SCU once you enter this step. However, if the SCU did not detect a board, you can add a board manually.



To add a board:

1. Press Insert.
2. From the Select the Board to Add dialog box, select the board's .CFG file and press Enter.

To delete an existing board:

1. Use the arrow keys to select the board that you want to delete.
2. Press Delete.
3. Confirm that you want to delete the board.

To move a board from one slot to another:

1. Use the arrow keys to select the board that you want to move.
2. Press F7.

✎ **If you add, move, or remove boards**

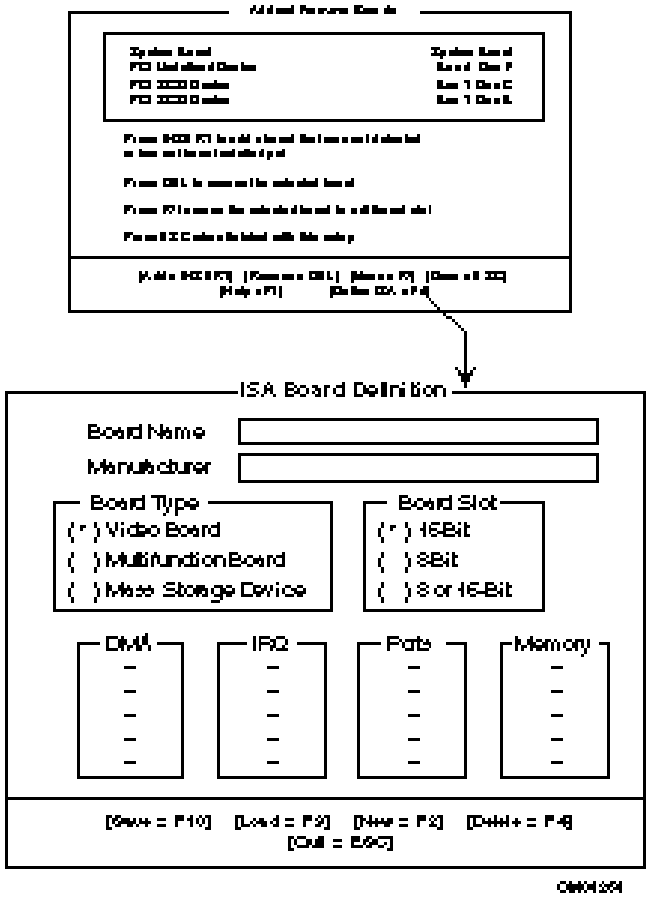
Manually verify the resource settings of these adapters, and any other adapters that are not locked, before saving your configuration.

To define an ISA board:

Press F6 to display the ISA Board Definition dialog box. Refer to the section below for details.

Define an ISA Board

To define an ISA board that has no .CFG file, press F6 while viewing the Add and Remove Boards screen. The ISA Board Definition dialog box will appear. It is necessary to define a board to prevent other boards in the system from using the same IRQ levels, DMA channels, I/O addresses, or memory addresses as that of the ISA board.



To define an ISA board:

1. In the Board Name box, type a description of the board.
2. In the Manufacturer box, type the name of the board manufacturer.
3. From the Board Type box, choose the type of board.
4. From the Board Slot box, choose the type of slot.
5. In the DMA box, define up to four DMA channels.
6. In the IRQ box, define up to seven IRQ levels.
7. In the Ports box, define up to eight ranges of I/O ports.
8. In the Memory box, define up to eight memory address ranges.

9. Press F10 to save the ISA board definition.

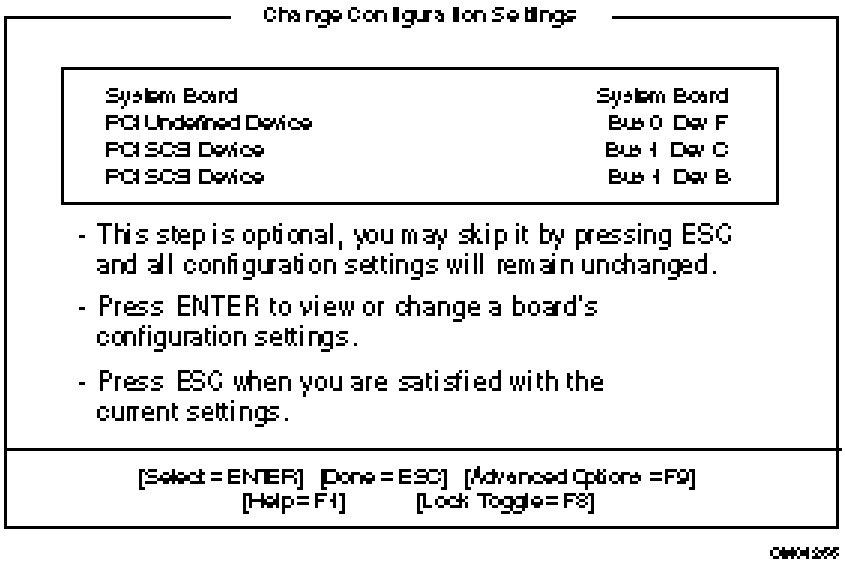
You can load an existing ISA board in order to modify the board definition.

To load an existing ISA board: Press F9.

To delete an ISA board: Press F9, and confirm that you intend to delete the ISA definition.

Change Configuration Settings

Use this step to view or change the configuration settings for any board in the system. You can verify that the baseboard and adapter board resources are set properly.



To view or change the settings for a board:

1. Use the arrow keys to select the board.
2. Press Enter.
3. When you are satisfied with the current settings, press ESC to return to the Main Menu.

Advanced Options

The Advanced Options menu is intended for advanced users. These are the options available:

Use this option	To see this
Global resource map	A list of allocated resources (DMA, IRQ, ports, and memory)
Board details	Detailed information for individual boards
System details	Information on the entire system and the current configuration
Physical board ID map	IDs of boards present in the system

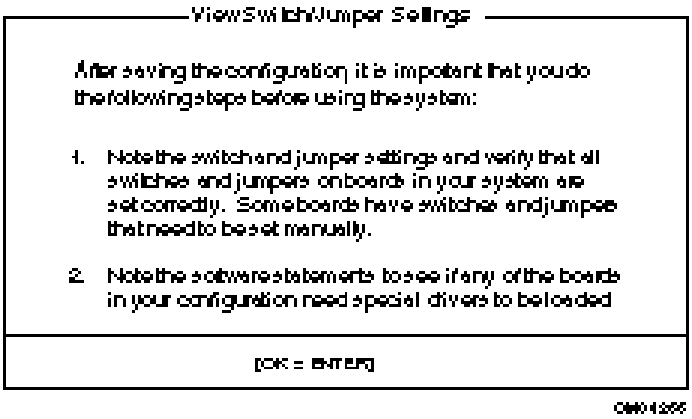
To view the Advanced Options menu: from the Change Configuration Settings dialog box, press F9.

Save Configuration

This step saves the configuration settings to nonvolatile RAM as well as to a backup file (.CMS file). You must save your settings once they have been configured.

View Switch/Jumper Settings

Use this step to view manufacturer's instructions about setting dip switches and jumpers, and how to run utilities to ensure correct configuration of each adapter.



Exit

This step exits to the operating system. If any configuration settings were changed, you will be prompted to restart your system to see the changes.

3.4.6About the Options

The rest of this chapter lists SCU groups as they display on screen after you select System Board from the Change Configuration Settings screen. These are the groups: Systems Group, Peripheral Configuration Group, LCD Display, Management Subsystem, and System Management.

After each group, some of the option choices are described. Not all of them are described because (a) a few are not user-selectable but are displayed for your information, and (b) many of the option choices are relatively self-explanatory.

3.4.7System Group

System Identification and Version Information		
System Identification String	N/A	Display only
Config and Overlay Version	N/A	Display only
BIOS Version String	N/A	Display only
MP Spec. Version	**1.1**/1.4	
System Processor Modules		
Display Processor Type(s) and Speed based on position	N/A	Display only
System Processor Status		
Processor Status for each processor	**No Failures Detected**/ Failures Detected	The status automatically changes to *Failures Detected* if the BIOS detects a processor failure. Unless there is only one processor in the system, a failed processor remains disabled in next boots until you use the SCU to change the status to *No Failures Detected*.
System Performance		
Power-On Speed	**Fast** / Slow	BIOS programs the SLOW timer before boot.
Secondary IOAPIC control	Enable / **Disable**	
Memory Subsystem		
Base Memory Option	512 / **640** KB	
Shadowing ISA ROMs Options	MENU	Shadowing at C0000, C4000, C8000, CC000, D0000, D4000, D8000, DC000, E0000, E4000
Extended Memory Options (Cache, 1 MB ISA Hole)	MENU	Cache mode **enable**/disable ISA hole enable/**disable**

3.4.8ROM Shadowing

All onboard adapter ROM (stored in compressed form in the system flash ROM) and PCI adapter ROM will be shadowed into RAM in the ISA-compatible ROM adapter memory space between C0000h to E7FFFh. Any BIOS found on ISA or EISA devices that can be shadowed will be shadowed into adapter memory space in the same range after initialization. ISA cards that require memory-mapped read/write accessibility should be located into the 15M-16M ISA space, or the 512KB-640KB space, which may be enabled individually via the SCU. Shadowing for ISA devices can be disabled for various regions via the SCU. A PCI BIOS is always shadowed.

3.4.9Peripheral Configuration Group

Onboard Disk Controllers		
Onboard Floppy Controller	**Enable /** Disable	
Onboard IDE Controller	**Enable /** Disable	
Onboard Communications Devices		
Serial Port 1 Configuration	Serial port 1 Address and IRQ	
Serial Port 2 Configuration	Serial Port 2 Address and IRQ	
Parallel Port Configuration	Parallel Port Address and IRQ	
Parallel Port Mode	Parallel Port Mode	
Parallel Port DMA	Valid only with ECP mode	
Floppy Subsystem Group		
Floppy drive A Options	Size and capacity	The system automatically detects diskette drive type and size.
Floppy drive B Options	Size and capacity	
IDE Subsystem Group		
ISA IDE DMA Transfers	**Auto Configured /** Disable	
IDE Configuration	MENU	
Multi-sector transfer selection	**Auto Configured /** 4 Sector / 8 Sector / Disable	
Translation Mode	Standard CHS / Logical Block Addressing / Extended CHS / **Auto Configured**	
Fast Programmed I/O modes	**Auto Configured** / Disable	

Language Support Group		
Language Support options	Languages supported	
KB/Mouse Subsystem Group		
NumLock Options	On at Boot/ **Off at Boot**	
Typematic Speed	**Auto** / Slow / Medium / Fast	
Mouse Control option	Auto detected	
Console Redirection		
COM port for redirection	**Disable** / COM 1/COM 2	
Baud rate	2400/ 9600/ 19.2k/ **115.2k**	
Hardware Flow Control	**None** / CTS/RTS / CTS/RTS & Xoff/Xon	
Terminal Type	**ANSI**	Display only
Security Subsystem		
Administrative Password	Enable / **Disable**	Enabled is implied by entering a password.
User Password	Enable / **Disable**	Enabled is implied by entering a password.
Hot-Key Option	Enable / **Disable**	
Lockout Timer	1 through 127 min. / **10 min.**	
Secure Boot Mode	Enable / **Disable**	
Video Blanking	Enable / Disable	
Floppy Writes	Enable / **Disable**	

Boot Subsystem Group	
First Boot Drive	Boot Disabled / **Boot Floppy** / Boot Hard Disk / Boot IDE CD-ROM Floppy Image / Boot IDE CD-ROM Hard Drive Image / Boot Network
Second Boot Drive	Boot Disabled / Boot Floppy / **Boot Hard Disk** / Boot Network
Third Boot Drive	**Boot Disabled** / Boot Floppy / Boot Hard Disk / Boot Network
Fourth Boot Drive	**Boot Disabled** / Boot Floppy / Boot Hard Disk
Display “<F1> for Setup” message during POST	**Enable** / Disable
Require user interaction on POST errors	Enable / **Disable**

SCSI ROM BIOS Options Group		
SCSI A ROM BIOS scan	**Enable**/Disable	SCSI A is fully configured, but the ROM scan is skipped if this is disabled.
SCSI B ROM BIOS scan	**Enable**/Disable	SCSI B is fully configured, but the ROM scan is skipped if this is disabled.

3.4.10 Language Support Group

BIOS prompts are displayed in English as the factory default. To select a different display language, the preferred way is to use Setup. However, the SCU also includes a Language Support option in the Peripheral Configuration menu. Select the Language Support option and step through the language choices until you see the one you want. After you select a language, the Setup menus and other BIOS information will display in that language. However, any change you make by using the SCU does not show an immediately visible result. The SCU menu screens continue to display in English no matter which language is selected, and you will need to exit the SCU and enter Setup to see whether the language change took effect (which it should have automatically). The available language choices are listed in the option menu. When more language files become available, they can be flashed into the system BIOS by using FMUP.

✎ **Updating the BIOS overwrites language files**

Although you do not have to update the BIOS to select a different display language, a system BIOS update does overwrite language files. Thus, if you have created a custom language file, you must flash it into the BIOS again after updating the BIOS.

3.4.11 Automatic Detection and Enabling of IDE Hard Drives

During POST, if an IDE controller is detected, the BIOS does the following:

- Determines the types of IDE drives attached
- Sets the drive parameters for the best performance
- Maps each device into memory and I/O space
- Assigns IRQs and DMA channels as needed so that there are no conflicts

If you choose parameters for your drive that are different from the drive's native parameters, your definitions will be programmed into the drive controller.

3.4.12 Security

The BIOS includes security features to prevent unauthorized access to or tampering with the system. Once the security features are enabled, access is allowed only after the correct password has been entered.

3.4.13 Boot Subsystem Group

Besides the sequence that you specify on the menu in the Boot Subsystem Group, the boot device sequence is also affected by whether the system is in secure mode or not.

System is NOT in secure mode:	• Boots from diskette drive A:, or if no diskette is present, boots from hard disk C:. • Boots from hard disk C:, or if no bootable OS is present on C:, boots from diskette drive A:. • Boots from hard disk C: only. • Boots from diskette A: only.
• **System IS in secure mode:**	• Boots from hard disk C: if present. After booting, system remains in secure mode. Even if the power cycles off and on for an unattended system, it still comes up in secure mode. • Boots from a diskette ONLY if the correct password is entered. Without the password, the system will not boot from diskette. Once a password is entered, the system is no longer in secure mode.

Onboard SCSI devices are scanned before PCI slots 5 and 6.

3.4.14LCD Subsystem Group

LCD Display String	**Enable** / Disable	
LC Display String Before OS Boot	**MENU**	Default
	(user-defined string or default)	"N x PID Speed System Ready " where N is the number of processor PID is the processor ID string Speed is what the processor is running in MHz

3.4.15LCD

In a system with an LC display panel, you can choose to have the panel display informative messages. If the system supports server control monitoring software and features, the LCD can display status messages about the monitoring process.

If you do not want to display messages, use the SCU to disable the LCD option.

During POST, the BIOS displays on the LCD the BIOS revision number, current POST countdown value, POST error codes, and the sizes of base and extended memory.

3.4.16LCD Display String Before Boot

Just before the OS is booted, the BIOS can display (a) the default message, consisting of the processor type and speed, number of processors, and POST error codes, or (b) your custom message string. This string can be 32 characters long, displayed as two lines of 16 characters each. To return to the default string, enter a blank message.

3.4.17Management Subsystem

Temperature/Voltage Limit Control	MENU
A to D Channel Enable switch	MENU
Speaker Options	**Enable** / Disable
Scan user FLASH area	Enable / **Disable**

The options in the Management Subsystem group are used to

- Set up system board voltage and temperature scanning by determining the appropriate thresholds
- Scan a particular A/D channel
- Scan the flash memory area for binaries that extend or alter critical event logging

3.4.18System Management Options

System Management Mode	Enable / **Disable**	
SMM Time Stamp Source	**Post capture** / Real time Clock	
Event Logging	Enable / **Disable**	Controls onboard event logging.
Reserve VGA resources	**Reserve VGA memory** / Disable onboard video	

If event logging is enabled, the BIOS can log critical and informational events to nonvolatile flash memory. Critical events are those that normally result in the system being shut down to prevent catastrophic side-effects from propagating to other parts of the system:

- Operating system outside of the range of set temperature and voltage limits
- Multi-bit and parity errors in the memory subsystem
- Most errors that normally generate a Nonmaskable Interrupt (NMI) (including I/O channel check, EISA bus time-out, EISA fail-safe timer expiration, software generated NMI, and PCI SERR and PERR events)

When these errors are detected, the system management interrupt (SMI) routines will log the error or event (transparently to the OS) and will then cause an NMI to be generated for certain fatal events (for example, certain NMIs and uncorrectable ECC errors).

If the OS device driver is using the watchdog timer to detect software or hardware failures, and that timer happens to expire, an Asynchronous System Reset (ASR) will be generated. This is equivalent to a hard reset, except that the limit registers are not reset. POST will detect this event as the system reboots and will log the event to the logging area. Failure of a processor during POST will also be logged in flash memory during POST.

3.4.19Worksheets for SCU Settings

Record your SCU settings on the worksheets, especially if your settings differ from the defaults. If the default values ever need to be restored to CMOS (after a CMOS-clear, for example), you would need to run the SCU again; referring to the worksheets could make your reconfiguration task easier.

Circle your options or write in the values.

Table 3.1 System Group Worksheet

System Identification and Version Information	
System Identification String	N/A
Config and Overlay Version	N/A
BIOS Version String	N/A
MP Spec. Version	1.1/1.4
System Processor Module	
Display Processor Type(s) and Speed based on position	N/A
System Processor Status	
Processor Status, 1st processor, module 1	No Failure Detected / Failure Detected
Processor Status, 2nd processor, module 1	No Failure Detected / Failure Detected
Processor Status, 3rd processor, module 2	No Failure Detected / Failure Detected
Processor Status, 4th processor, module 2	No Failure Detected / Failure Detected
System Performance	
Power-On Speed	Fast / Slow
Secondary IOAPIC control	Enable / Disable
Memory Subsystem	
Base Memory Option	512 / 640 KB
Shadowing ISA ROMs Option	MENU
Extended Memory Options	MENU

Table 3.2 Peripheral Configuration Worksheet

Onboard Disk Controllers		
Onboard Floppy Controller	Enable / Disable	
Onboard IDE Controller	Enable / Disable	
On-board Communications Devices		
Serial Port 1 Configuration	(Serial port 1 Address and IRQ)	
Serial Port 2 Configuration	(Serial Port 2 Address and IRQ)	
Parallel Port Configuration	(Parallel Port Address and IRQ)	
Parallel Port Mode	(Parallel port Mode)	
Parallel Port DMA	(Valid only with ECP mode)	
Floppy Subsystem Group		
Floppy drive A Options		(Size and capacity)
Floppy drive B Options		(Size and capacity)
IDE Subsystem Group		
ISA IDE DMA Transfers	Auto Configured / Disable	
IDE Configuration - Primary Master	MENU	
Multi-sector transfer selection	Auto Configured / 4 Sector / 8 Sector / Disable	
Translation Mode	Standard CHS / Logical Block Addressing / Extended CHS / Auto Configured	
Fast Programmed I/O modes	Auto Configured / Disable	
IDE Configuration - Primary Slave	MENU	
Multi-sector transfer selection	Auto Configured / 4 Sector / 8 Sector / Disable	
Translation Mode	Standard CHS / Logical Block Addressing / Extended CHS / Auto Configured	
Fast Programmed I/O modes	Auto Configured / Disable	
IDE Configuration - Secondary Master	MENU	
Multi-sector transfer selection	Auto Configured / 4 Sector / 8 Sector / Disable	
Translation Mode	Standard CHS / Logical Block Addressing / Extended CHS / Auto Configured	
Fast Programmed I/O modes	Auto Configured / Disable	

Continued

Table 3.2 Peripheral Configuration Worksheet, continued

IDE Configuration - Secondary Slave	MENU
Multi-sector transfer selection	Auto Configured / 4 Sector / 8 Sector / Disable
Translation Mode	Standard CHS / Logical Block Addressing / Extended CHS / Auto Configured
Fast Programmed I/O modes	Auto Configured / Disable
Language Support Group	
Language Support options	
KB/Mouse Subsystem Group	
NumLock Options	On at Boot / Off at Boot
Typematic Speed	Slow / Medium / Fast
Mouse Control option	Auto detected
Console Redirection	
COM port for redirection	Disable / COM 1/ COM 2
Serial Port baud rate	2400/ 9600/ 19.2k/ 115.2k
Hardware Flow Control	None / CTS/RTS / CTS/RTS & Xoff/ Xon
Terminal Type	ANSI
Security Subsystems	
Administrative Password	Enable / Disable
User Password	Enable / Disable
Hot-Key Option	Enable / Disable
Lockout Timer	1 through 127 min. / 10 min.
Secure Boot Mode	Enable / Disable
Video Blanking	Enable / Disable
Floppy Writes	Enable / Disable
Boot Subsystem Group	
Boot Sequence Control	Boot Disabled / Boot Floppy / Boot Hard Disk / Boot IDE CD-ROM Floppy Image / Boot IDE CD-ROM Hard Drive Image / Boot Network
Display “<F1> for Setup” message during POST	Enable / disable
Require user interaction on POST errors	Enable / disable
Onboard SCSI Subsystem	
SCSI A ROM BIOS scan	Enable/Disable
SCSI B ROM BIOS scan	Enable/Disable

Table 3.3 LCD Display Worksheet

LCD display string	Enable / Disable	
LC Display String Before OS Boot	MENU	(user-defined string or default)

Table 3.4 System Management Options Worksheet

System Management Mode	Enable / Disable
SMM time stamp Source	Post capture / Real time Clock
Event Logging	Enable / Disable
Reserve VGA Resources	Reserve VGA memory / Disable onboard video

Table 3.5 Management Subsystem Worksheet

A to D Channel Enable switch	MENU
Speaker Options	Enable / Disable
Scan user FLASH area	Enable / Disable
Temperature/Voltage Limit Control	MENU
+5 V Upper Warning Level	0.02 - 5.4 V in 0.02 V steps
+5 V Lower Warning Level	0.02 - 5.4 V in 0.02 V steps
+5 V Upper Critical Level	0.02 - 5.4 V in 0.02 V steps
+5 V Lower Critical Level	0.02 - 5.4 V in 0.02 V steps
+12 V Upper Warning Level	0.1 - 14.9 V in 0.1 V steps
+12 V Lower Warning Level	0.1 - 14.9 V in 0.1 V steps
+12 V Upper Critical Level	0.1 - 14.9 V in 0.1 V steps
+12 V Lower Critical Level	0.1 - 14.9 V in 0.1 V steps
+3.3 V Upper Warning Level	0.02 - 3.74 V in 0.02 V steps
+3.3 V Lower Warning Level	0.02 - 3.74 V in 0.02 V steps
+3.3 V Upper Critical Level	0.02 - 3.74 V in 0.02 V steps
+3.3 V Lower Critical Level	0.02 - 3.74 V in 0.02 V steps
-12 V Upper Warning Level	-16.7 to -5.9V in .1V steps
-12 V Lower Warning Level	-16.7 to -5.9V in .1V steps
-12 V Upper Critical Level	-16.7 to -5.9V in .1V steps
-12 V Lower Critical Level	-16.7 to -5.9V in .1V steps
Temperature Probe #1 Upper Warning Level	0 °C to 200 °C in 2 °C steps
Temperature Probe #1 Lower Warning Level	0 °C to 200 °C in 2 °C steps
Temperature Probe #1 Upper Critical Level	0 °C to 200 °C in 2 °C steps
Temperature Probe #1 Lower Critical Level	0 °C to 200 °C in 2 °C steps
Temperature Probe #2 Upper Warning Level	0 °C to 200 °C in 2 °C steps
Temperature Probe #2 Lower Warning Level	0 °C to 200 °C in 2 °C steps
Temperature Probe #2 Upper Critical Level	0 °C to 200 °C in 2 °C steps
Temperature Probe #2 Lower Critical Level	0 °C to 200 °C in 2 °C steps

3.5SCSI*Select*™ Utility

The SCSI*Select* utility detects the number of SCSI AIC-78xx host adapters in your system. Use the utility to start, format, and verify SCSI drives or to explicitly configure the SCSI host adapter to settings other than defaults.

The utility is menu-driven. Follow the screen prompts and information about moving around through the menus and selecting options.

3.5.1To Start up SCSI*Select*

1. Turn on or reboot the system. During boot-up, the following prompt is displayed at the time the SCSI BIOS is loaded:

   ```
   <<< Press <CTRL><A> for SCSISelect™ Utility! >>>
   ```

   To enter the SCSI*Select* utility, press <Ctrl-A> when you see the prompt.

2. When the utility appears, choose the bus:device that you want to configure; each bus accepts up to 15 devices.

3.5.2Main Menu

Feature	Option	Comment
Bus:Device	01:0Bh	Select this option to configure the SCSI devices on SCSI Channel A.
	01:0Ch	Select this option to configure the SCSI devices on SCSI Channel B.

3.5.3Bus: Device 01:0Bh/01:Ch Menu

Feature	Option	Comment
Bus:Device 01:XXh	Configure/View Host Adapter Settings	See Configuration Menu.
	SCSI Disk Utilities	See SCSI Disk Utilities Menu.

3.5.4Configuration Menu

Feature	Option*	Comment
SCSI Bus Interface Definitions		
Host Adapter SCSI ID	0–**7**–15	
SCSI Parity Checking	**Enabled** Disabled	
Additional Options		
Boot Device Options	Press <Enter>	See Boot Device Options Menu.
SCSI Device Configuration	Press <Enter>	See SCSI Device Configuration Menu.
Advanced Configuration Options	Press <Enter>	See Advanced Configuration Options Menu.

* Options shown in **bold** are factory default.

3.5.5Advanced Configuration Options

Feature	Option*	Comment
Plug and Play Support	Enabled **Disabled**	Option appears only if the BIOS is configured to include SCAM-1 support.
Host Adapter BIOS (Configuration Utility Reserves BIOS Space)	**Enabled** Disabled	No effect if BIOS is disabled.
Support Removable Disks Under BIOS as Fixed Disks	**Boot Only** All Disks Disabled	**CAUTION** Do not remove media from a removable media drive if drive is under BIOS control. No effect if BIOS is disabled.
Extended BIOS Translation for DOS Drives > 1 GByte	**Enabled** Disabled	No effect if BIOS is disabled.
Display <Hot><Key> Message During BIOS Initialization	**Enabled** Disabled	
Multiple LUN Support	Enabled **Disabled**	LUN = logical unit number.
BIOS Support for More Than 2 Drives (MS-DOS 5.0 and above)	**Enabled** Disabled	
BIOS Support for Bootable CD-ROM	**Enabled** Disabled	
BIOS Support for Int13 Extensions	**Enabled** Disabled	

Support for Ultra SCSI Speed	Enabled **Disabled**

* Options shown in **bold** are factory default.

3.5.6SCSI Device Configuration Menu

SCSI Device ID	0–15 Option*	Comment
Initiate Sync Negotiation	**yes** no	
Maximum Sync Transfer Rate	**20.0** 8.0 6.7 5.0	
Enable Disconnection	**yes** no	
Initiate Wide Negotiation	**yes** no	
Send Start Unit Command	**yes** no	No effect if BIOS is disabled. Needs to be YES for hot-swap drives.

* Options shown in **bold** are factory default.

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4 Error Messages and Beep Codes

4.1BIOS Beep Codes

Table 4.1 Beep Codes

Beep Count	Port 80 Codes	Error Condition
1	71h	Refresh failure
2	72h	Parity cannot be reset
3	73h	First 64 KB memory failure
4	74h	Timer not operational
5	75h	Processor failure
6	76h	8042 Gate A20 is off (v_mode)
7	77h	Exception interrupt error
8	78h	Display memory R/W error
9	79h	ROM checksum error
10	7Ah	Shutdown reg. R/W error
11	7Bh	I2C Error

4.2POST Codes and Countdown Codes

At power-on, after the video adapter has been initialized, the BIOS indicates the current testing phase by sending a 2-digit hex code to I/O location 80h. The current countdown code will be displayed on the LCD panel, once the panel is initialized.

4.2.1 Recovery Port-80 Codes and Countdown Codes Displayed

During BIOS recovery, the diskette in drive A is booted, and a BIOS image is automatically installed.

Table 4.2 Recovery Port-80 Codes

Port 80 Code	Countdown Code	Reason
02h		Disable internal cache
08h		Disable DMA controller #1, #2, disable interrupt controller #1, #2, reset video display
13h		Initialize all chip set registers (Enable LCD display here)
15h	900	Initialize system timer
1Bh	800	Real mode base 64 KB test
20h	700	16 KB base RAM test
23h	650	Setup interrupt vectors
40h	600	Test memory in virtual mode
65h	500	Initialize 8237 DMA controller
67h	400	8259 interrupt controller test
80h	300	Unmask diskette, keyboard and timer interrupts
88h	200	Floppy unit initialization
A0h	100	Cache enable
00h	000	Boot OS

4.2.2Standard Port-80 Codes and Countdown Codes Displayed

Table 4.3 Standard Port-80 Codes

Port 80 Code	Countdown Code	Reason
D0h		Early MP Initialization
D1h		Power On Initialization
D2h		Disable NMI
D3h		Reset video controller
D4h		Enter real mode
D5h		Checksum the 8 KB loader BIOS
D6h		Loader BIOS checksum good
D7h	900	Check if Keyboard Controller (KBC) buffers are free
D8h		Issue BAT (basic assurance test) command to KBC
D9h		Read BAT results
DAh		Check if keyboard controller passed BAT
DBh	820	Keyboard Initialization Passed
DDh		Disable keyboard and auxiliary devices
DFh		Disable both DMA controllers
E0h	780	Preliminary initialization of PICs
E1h		Enter real big mode and initialize chip set, size memory
E2h		Initialize timer 2 for speaker
E3h	760	Initialize timer channel 0 for system timer
E4h		Clear any pending parity errors
E6h	740	Test RAM from 0-640 KB
E7h		Test and initialize 2 MB memory
E8h		RAM failure, remap memory partitions and test again

Continued

Port 80 Code	Countdown Code	Reason
E9h		RAM test complete, passed. Clear parity errors
EAh	730	Set up stack at 30:100, enable cache and shadow BIOS
EBh		Initialize code dispatcher
ECh		Make F000h DRAM R/W Enabled
EDh		Dispatch POST
23h	700	Initializations before setting up vector table
24h		Setup interrupt vector table
0Dh		Check CMOS clear jumper
0Eh	690	Check validity of CMOS
0Fh		Force CMOS defaults if required
10h		CMOS initialization complete
25h		Nothing
28h		Set monochrome mode
29h		Set color display
2ah		Clear parity status if any, initialize warm reset flag
2bh		Video autoconfiguration and initialization
F0h		EISA Slot Initialization
F1h		Enable extended NMI sources
F2h		Test extended NMI sources
2ch	580	Conventional video option ROM search
2dh		Scan user flash
2eh	570	Initialize monochrome display if no other video present
2fh	560	Test buffer memory for monochrome
30h		Check vertical and horizontal retrace

Continued

Port 80 Code	Countdown Code	Reason
31h		Test for color display memory if no external video BIOS found
32h		Check vertical retrace
34h		Sign on message
36h		Initialize Messaging Services and clear screen
37h	500	Custom sign on display
80h	370	Keyboard/mouse port check
81h		Keyboard controller initialization and testing
83h		Check if keyboard is locked
F5h	330	Initialize mouse
39h		Keyboard, mouse and other signons
3bh		Prepare for memory test
43h	290	Decide memory size from chip set
4Fh		Disable cache, test memory and display memory size on screen
52h		Initialize for the other processors in MP system, reset DMA controller
61h	250	DMA register tests
62h		DMA test OK
65h		Initialize 8237 DMA controller
66h		Clear DMA write request register and mask set/reset register
67h	220	8259 Interrupt controller test
F4h		Enable extended NMI sources
8Ch	140	Initialize remaining Plug-N-Play devices (i.e., other than video), initialize IPL, initialize IDE controller

Continued

Port 80 Code	Countdown Code	Reason
8Fh	130	Floppy Initialization
92h		Set printer, RS-232 time-out
96h		Optional ROM scan and initialize above C800h
97h	080	Scan User flash and conventional option ROM scan
98h		Scan User flash area
9Ah		Clear soft reset flag, complete MP Table
9Dh	070	Timer data area initialization
A0h		Printer setup
A1h		RS-232 setup
A2h		Check for stuck key
ABh		Before NPX test and initialization
ACh	060	NPX test and initialization
ADh		Update coprocessor information in CMOS and recalculate checksum
Aeh		Set typematic rate
AFh	050	Keyboard read ID command
B0h		Wait for READ ID response
A3h		Display POST errors
A6h		Before Setup
A7h	030	Call Setup if required, prompt for password if enabled
B1h		Enable Cache for boot
B3h		Setup display mode set
B4H		Jump to pre-OS code
BBh	020	Initialize SMI code, prepare for boot
00h	000	Execute BOOT

4.3POST Error Codes and Messages

The BIOS indicates errors as follows:

- By writing an error code to the PS/2-standard logging area in the Extended BIOS Data Area
- By displaying a POST Error Code and message on the screen.

Table 4.4 POST Error Codes

Number	Error message
0002	Primary Boot Device Not Found
0010	Cache Memory Failure, Do Not Enable Cache
0015	Primary Output Device Not Found
0016	Primary Input Device Not Found
0041	EISA ID Mismatch for Slot
0043	EISA Invalid Configuration for Slot
0044	EISA config NOT ASSURED!
0045	EISA Expansion Board Not Ready in Slot
0047	EISA CMOS Configuration Not Set
0048	EISA CMOS Checksum Failure
0049	EISA NVRAM Invalid
0060	Keyboard Is Locked ... Please Unlock It
0070	CMOS Time & Date Not Set
0080	Option ROM has bad checksum
0083	Shadow of PCI ROM Failed
0084	Shadow of EISA ROM Failed
0085	Shadow of ISA ROM Failed
0131	Floppy Drive A:
0132	Floppy Drive B:
0135	Floppy Disk Controller Failure

Continued

Number	Error message
0140	Shadow of System BIOS Failed
0171	CPU Failure - Slot 1, CPU # 1
0172	CPU Failure - Slot 1, CPU # 2
0173	CPU Failure - Slot 2, CPU # 1
0174	CPU Failure - Slot 2, CPU # 2
0171	Previous CPU Failure - Slot 1, CPU # 1
0172	Previous CPU Failure - Slot 1, CPU # 2
0173	Previous CPU Failure - Slot 2, CPU # 1
0174	Previous CPU Failure - Slot 2, CPU # 2
0175	CPU modules are incompatible
0180	Attempting to boot with failed CPU
0191	CMOS Battery Failed
0195	CMOS System Options Not Set
0198	CMOS Checksum Invalid
0289	System Memory Size Mismatch
0295	Address Line Short Detected
0297	Memory Size Decreased
0299	ECC Error Correction failure
0301	ECC Single bit correction failed, Correction Disabled
0302	ECC Double bit Error
0305	PCI-to-PCI bridge found, IO Queue Depth set to 1,setup value overridden
0310	ECC Memory Size Changed, Bank # 1
0311	ECC Memory Size Changed, Bank # 2
0312	ECC Memory Size Changed, Bank # 3
0370	Keyboard Controller Error
0373	Keyboard Stuck Key Detected
0375	Keyboard and Mouse Swapped

Continued

Number	Error message
0380	ECC SIMM failure, Board in slot 1 SIMM #
0392	ECC SIMM failure, Board in slot 2 SIMM #
0430	Timer Channel 2 Failure
0440	Gate-A20 Failure
0441	Unexpected Interrupt in Protected Mode
0445	Master Interrupt Controller Error
0446	Slave Interrupt Controller Error
0450	Master DMA Controller Error
0451	Slave DMA Controller Error
0452	DMA Controller Error
0460	Fail-safe Timer NMI Failure
0461	Software Port NMI Failure
0465	Bus Time-out NMI in Slot
0467	Expansion Board NMI in Slot
0501	PCI System Error
0510	PCI Parity Error
0710	System Board Device Resource Conflict
0711	Static Device Resource Conflict
0800	PCI I/O Port Conflict
0801	PCI Memory Conflict
0802	PCI IRQ Conflict
0803	PCI Error Log is Full
0810	Floppy Disk Controller Resource Conflict
0811	Primary IDE Controller Resource Conflict

Continued

Number	Error message
0812	Secondary IDE Controller Resource Conflict
0815	Parallel Port Resource Conflict
0816	Serial Port 1 Resource Conflict
0817	Serial Port 2 Resource Conflict
0820	Expansion Board Disabled in Slot
0900	NVRAM Checksum Error, NVRAM Cleared
0903	NVRAM Data Invalid, NVRAM Cleared
0905	NVRAM Cleared By Jumper
0982	I/O Expansion Board NMI in Slot
0984	Expansion Board Disabled in Slot
0985	Fail-safe Timer NMI
0986	System Reset caused by Watchdog Timer
0987	Bus Time-out NMI in Slot

5 Electrical, Environmental and Mechanical Specifications

This chapter specifies the operational parameters and physical characteristics for the processor, memory, and termination modules and the baseboard. This is a board-level specification only. System specifications are beyond the scope of this document.

5.1 Absolute Maximum Ratings

Operation at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 5.1 Absolute Maximum Board Level Ratings

Operating temperature for board set	0°C to +55°C Note: Chassis design must meet the Pentium Pro processor maximum case temperature as specified in the *Pentium Pro EMTS*.
Storage temperature	-55°C to +150°C
Voltage on any signal with respect to VSS	-0.3 to supply voltage + 0.3 V
Supply voltage with respect to VSS	-0.3 to +5.5 V (VCC only)

Further topics in this chapter specify normal operating conditions.

5.2 Electrical Specifications

Below is a summary of the power requirements for the AP450GX MP server board set.

Table 5.2 Voltage and Current Specifications

Voltage	Specification	Min Current	Max Current	Max di/dt	Suggested Bulk Capacitance (in power supply)	Notes
+3.3V	3.3V ± 5%	---	28A	14A/300uS	80,000uF	1,2,3,4,5
+5V	5.0V ± 5%	---	40A	14A/300uS	80,000uF	1,2,3,5
+12V	12.0V ± 5%	---	18.5A	0.2A/uS	10,000uF	1,2,5
-5V	-5.0V ± 5%	---	0.25A	---	---	1,2
-12V	-12.0V ± 10%	---	1A	---	---	1,2

Notes:

1. All values are specified at the power supply connector on the baseboard.
2. di/dt is the maximum rate of change of current the power supply must be able to supply to the board set while keeping the voltage within tolerance.
3. Bulk Capacitance is a suggestion only. The system integrator is looked upon to make the appropriate determination.
4. Max values for +3.3V will only be achieve if the 4GB Memory Module is installed, which uses 3.3V DIMMs.
5. Remote sense capabilities should be used to ensure proper regulation

Table 5.3 Voltage Sequencing Specifications

Parameter	Description	Specification	Notes
T_{rise}	Voltage Rise Time	50mS	1
T_{fall}	Voltage Fall Time	None	2
$T_{sequence-on}$	Voltage Sequencing During Power On	None	3
$T_{sequence-off}$	Voltage Sequencing During Power Off	None	3
PwrGood	PowerGood Assertion	Min = 5mS Max = 50mS	4
$T_{powerGood\ Rise}$	PowerGood Rise Time	0.5V/ns	Typical value

Notes:

1. Voltage rise time is the time it takes for all voltages input to the baseboard (+3.3V, +5V, +12V, -5V, -12V) to be within their specified value as noted in Table 1. This time is measured from the time the voltages begin their rise from ground (0 Volts).
2. Voltage fall time is the time it takes for all voltages input to the baseboard to drop to 0V from the time the power supply is turned off.
3. There are no voltage sequencing requirements during power on or power off. All voltages can come up in any order, but they all must be within their specified value within 50mS as defined by T_{rise}.
4. PwrGood must be asserted no sooner that 5mS, but not longer than 50mS after all voltages are within their specified values as defined by T_{rise}. The rise time of the Power Good

5.3Environmental

Table 5.4 Board Set Environmental Specifications

Environmental Condition		Specification
Temperature	nonoperating	-40° to 70°C (-40° to 158°F)
	operating	0° to 55°C (to 131°F)
Temperature, thermal map		Must not exceed maximum IC junction temperature as specified in the component data sheets.
Thermal shock	nonoperating	-40° to 70°C (-40° to 158°F)
Humidity	nonoperating	92% relative humidity (noncondensing) at 55°C (131°F)
	operating	85% relative humidity (noncondensing) at 55°C (131°F)
Vibration	nonoperating	Random input, 0.01 g2/Hz at 5 Hz, sloping to 0.02 g2/Hz at 20 Hz, and maintaining 0.02 g2/Hz from 20 Hz to 500 Hz.
Shock	nonoperating	50 g, 11 ms, 1/2 sine
	operating	Not applicable
Altitude	nonoperating	To 50,000 ft (15,240 m)
	operating	To 10,000 ft (3,048 m)
Electrostatic discharge (ESD)	operating	Tested to 25 kV; no component damage
EMI	operating	Tested as part of system; required to meet EMI emission requirements

5.4Cooling Requirements

Below are the cooling requirements for the board set; specifically the processors. The first table specifies cooling requirements for the primary processor module. The second table is for the secondary processor module. Both tables assume both processor sockets on each module are populated. Ambient temperature is measured just before it passes over the processor module.

Table 5.5 Primary Processor Module Cooling Requirements

30W Processor		35W Processor		40W Processor	
Air Flow (LFM)	Max Ambient Temp (°C)	Air Flow (LFM)	Max Ambient Temp (°C)	Air Flow (LFM)	Max Ambient Temp (°C)
100	30.7	100	20.3	100	16.3
200	42.9	200	33.7	200	29.9
300	51.2	300	44.2	300	39.6
400	56.2	400	50.8	400	46.7
500	59.6	500	55	500	50.4

Table 5.6 Secondary Processor Module Cooling Requirements

30W Processor		35W Processor		40W Processor	
Air Flow (LFM)	Max Ambient Temp (°C)	Air Flow (LFM)	Max Ambient Temp (°C)	Air Flow (LFM)	Max Ambient Temp (°C)
100	28.3	100	24.3	100	17.3
200	41.5	200	37.5	200	29.9
300	49.3	300	46.1	300	40.6
400	55.6	400	51.6	400	46.8
500	59.2	500	55.2	500	50.9

5.5Power Budget

All power for the Pentium Pro processors on the processor module is provided by DC-DC converters powered from the +12V supply. There is also a DC-DC converter used for the GTL+ termination voltage reference. The efficiency of the converters is 80%.

I^2C components are powered from +5 volts.

All power numbers are given for worst case conditions, not nominal. See the *Pentium Pro Processor Data Sheet* for details of Pentium Pro processor power requirements.

Voltage tolerance is ± 5%.

The numbers below are for the baseboard, processor, and memory modules. The system integrator is looked upon to make cost / performance / market tradeoffs to determine how much power to dedicate for add-in slots.

Table 5.7 Example Power Budget in Watts (Maximum Values)

	-12V	+12V	+3.3V	+5V
Processor Module	0	99.2	0.2*	1.4
Termination Module	0	10.9	0	0.9
Memory Module (1GB)	0	0	3.9	75.3
Baseboard (no add-in cards)	1.2	1.2	7.0	10.0
Total Watts	300.2			
Assumptions: **two processor modules, four 35W processors (166/512KB), 1GB of memory no add-in cards**				

* The Pentium Pro processor pinout also specifies power at +3.3V. These numbers assume the Pentium Pro processor does not use that voltage. Refer to the *Pentium Pro Processor Data Sheet* for details.

5.6Mechanical Drawings

The following diagrams show the mechanical specifications of the baseboard, processor module, termination module, and memory module. All dimensions are given in inches, as per ANSI Y15.4M. Maximum primary-side component height is .550" unless otherwise noted. Connectors are dimensioned to pin 1. Refer to "Connector Specifications" after the diagrams for more information.

5.6.1Processor and Terminator Module Mechanical Specifications

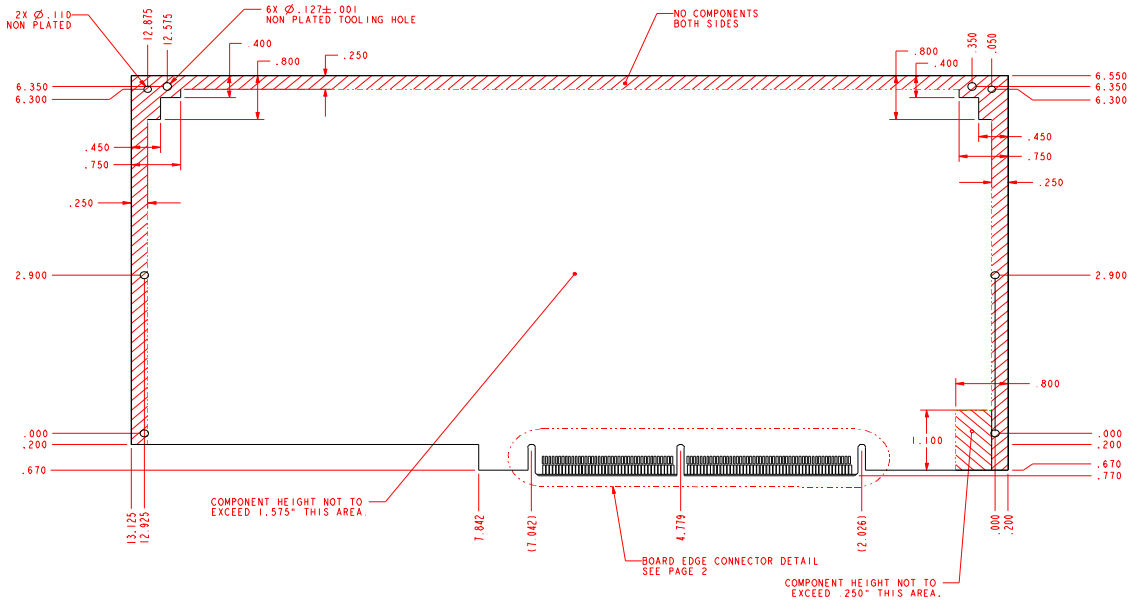

Figure 5.1 Processor and Terminator Module Mechanical Specifications

5.6.2Memory Module Mechanical Specifications

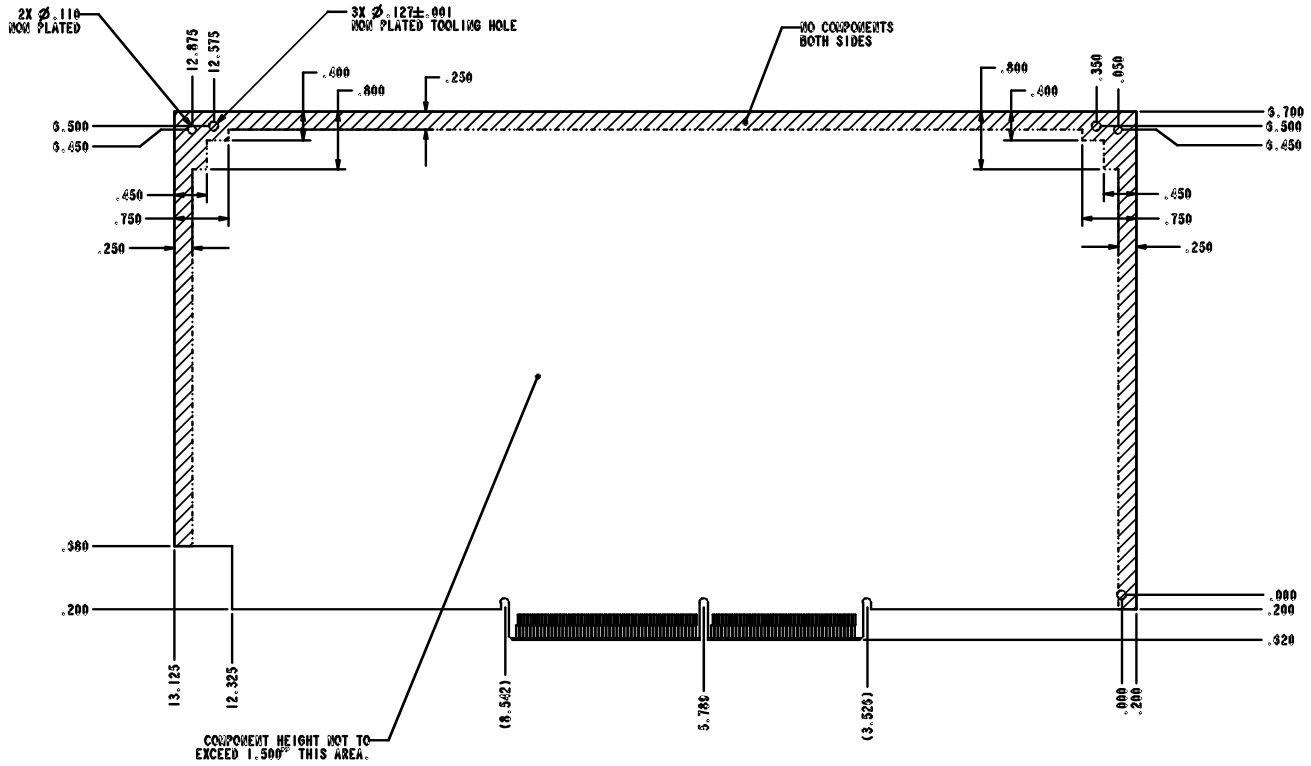

Figure 5.2 Memory Module Mechanical Specifications

5.6.3Baseboard Mechanical Specifications

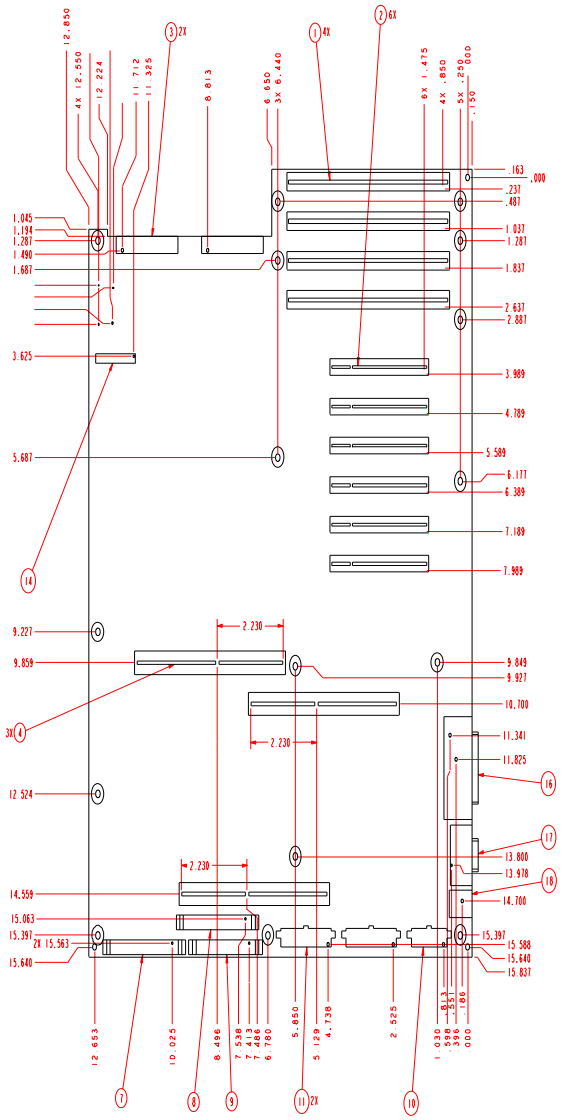

Figure 5.3 Baseboard Mechanical Specifications

5.6.4Module Insertion/Extractor Handle Specifications

The card ejection lever shown below is a requirement for the processor and memory modules in the Pentium Pro processor server system. The cards must be seated into the baseboard connector at no more than a 5° deviation from perpendicular to avoid damage to the baseboard. Using the ejection lever ensures that these modules are completely seated, and eases the insertion /extraction force needed to correctly

In addition to the ejection levers, card guides and a hold down rail are required to keep the cards from moving around and becoming displaced during shipping or handling.

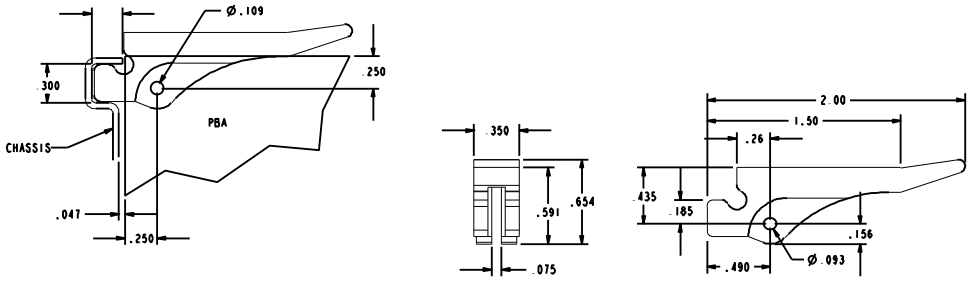

Figure 5.4 Module Insertion/Extractor Handle

5.7Connector Specifications

The following table shows reference designators, quantity, and the manufacturer's part numbers for connectors on the baseboard and processor module. Item numbers reference the circled numbers on the baseboard mechanical drawing. Refer to manufacturers' documentation for more information.

Table 5.1 Connector Specifications

Item	Ref. Designator(s)	Qty	Mfr(s) and Part #	Description
1	J1A1, J1A2, J2A1, J2A2	4	Burndy CB2E188SC-13Z14	EISA bus add-in card connector
2	J5A2, J5A3, J4A2, J4A1, J3A2, J3A1	6	AMP 646255-1	PCI add-in card connector
3	J1F1, J1G1	2	AMP 74931-7	68-pin SCSI connector
4	J6D1, J7D1, J9C1	3	AMP 145238-1	Processor and memory bus connectors
7	J9F1	1	3M 3432-Z00044	LCD front panel display connector
8	J9E1	1	3M 2450-60Y2UB or G	IDE connector
9	J9E2	1	3M 2534-60V2UG	Floppy connector
10	J9A2	1	Molex 39-29-9144	Power control connector (PS3)
11	J9D1, J9B1	2	Molex 39-29-9202	20-pin power connector (PS1 & PS2)
14	J3G1	1	Fox Conn/Hon Haj HC11131-KD6	Server Management feature connector
16	J7A1	1	AMP 750433-2	VGA and Parallel port connector
17	J8A1	1	Fox Conn/Hon Haj DM10156-73	Dual serial port connector
18	J9A1	1	Fox Conn/Hon Haj MH11063-D0	Keyboard and mouse connector
	J5G3, J2G4, J2G3, J5G2, J107, J102	6	AMP640456-3	System & CPU Fan Connector (3 pin) (J107 & J102 on processor module)
	J2G1, J5G1	2	AMP 640456-4	Hard Disk LED Connector (4 pin)

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Appendix A -- Supported Environments

The AP450GX MP Server has been validated with the leading network operating systems, adapter cards and SIMM combinations. Below is a summary of them. Not all configurations have been validated and there may be limitations to their interoperability. The list will change as more environments are validated. Contact your Intel technical representative for as updated list.

A.1 Validated Operating Systems

The table below lists which O/S each particular adapter was tested with.

- Level 1 - Heavy testing done in Intel's Server Validation Lab
- Level 2 - Minimal testing done in one of Intel's compatibility labs

MP = Multi-Processing, UP = Uni-Processing

Level	Operating System	Version	MP/UP	Certified
1	Windows NT	Versions 3.51 (Build 1057) Advanced Server (w/Service Pack 3)	MP & UP	OEM must certify w/Microsoft
1	Novell NetWare	4.1 SMP (patches 410pt3 & 410it6 installed on UP prior to installing MP)	MP & UP	In Progress
1	IBM OS/2	IBM OS/2 2.11 SMP w/LanServer 4.0 (Fix Pack s.630)	MP & UP	In Progress
1	SCO UnixWare	Beta 2.1 (Eiger 8.4) (Version will be 2.03 certified)	MP & UP	OEM must certify w/SCO
2	Banyon	5.5.4	UP	Will not certify
2	Banyon	6.0	UP	In Progress
2	IBM OS/2	WARP 3.0	UP	In Progress
2	MS DOS	6.22	UP	N/A
2	Novell NetWare	3.12	UP	In Progress
2	SCO UNIX	ODT 3.0	UP	OEM must certify W/SCO
2	SCO UNIX	ODT 5.0	UP & MP	OEM must certify W/SCO
2	Solaris	2.5	UP	In Progress

A.2 Validated Adapter Cards

The table below lists which O/S each particular adapter was tested with.

- Level 1 - Heavy testing done in Intel's Server Validation Lab
- Level 2 - Minimal testing done in one of Intel's compatibility labs

Level	PCI Adapters	Driver and/or O/S tested
	LAN Adapters	
1	Intel EtherExpress Pro/100B	NT-1.63, NW-1.08, OS/2-1.25
1	3COM 3C595-TX	NT-1.03, NW-4.01k, OS/2-1.0ab
1	SMC 9332DST	NT-2.42, NW-1.13, OS/2-2.03, UW-1.06f
2	Zynx ZX312 Combo	NT
2	3COM 3C590 Combo	DOS
	SCSI Hard Disk Adapters	
1	Adaptec 7880 - On board (Operating in 7870 compatible mode)	1.2s3 (NT, NW, OS/2, UW)
1	Adaptec AHA-2940W	1.2s3 (NT, NW, OS/2, UW)
1	Mylex DAC960PL-2A RAID (Firmware 2.6)	NT-3.05, NW-3.08, OS/2-3.07, UW
1	Symbios 8251S	3.0 (NT, NW, OS/2, UW)
2	Adaptec AHA-2940	NT, NW, OS/2, UW
2	Mylex DAC960PL (Firmware 2.6)	NT, NW, OS/2, UW
2	Mylex DAC960P	NT, NW, OS/2
2	NCR NCR8251S	NT, NW, OS/2
2	NCR NCR8250S	Win95
	Token Ring Network Interface Adapters	
2	IBM Auto LAN Streamer PCI	NT, OS/2
2	Olicom Olicom 16/4	NT, OS/2

Level	PCI Adapters (continued)	Driver and/or O/S tested
	Video Adapters	
2	ATI MACH 64 (Graphics Pro Turbo VRAM)	Win 95
2	Orchid Fahrenheit Pro 64	DOS
2	#9 GXE64 (D2-P)	DOS
2	#9 GXE64Pro (2MB)	DOS
2	#9 Imagine 128 (V4-P)	DOS
2	#9 Imagine 128 (V4-P-16)	DOS

Level	EISA/ISA Adapters	Driver and/or O/S Tested
	LAN Adapters	
2	Intel Pro100/Rev F	NT
2	Intel NE3200	NT, NW, OS/2
2	3COM 3C579 (EL-III)	NT
	SCSI Hard Disk Adapters	
1	Adaptec AHA-2740	2.1 (NT, NW, OS/2)
1	Mylex DAC960 EISA RAID	NT-3.05, NW-3.08, OS/2-3.07
2	Bus Logic BTBT946C	NT
	Token Ring Network Interface Adapters	
2	IBM Token Ring Auto 16/4I	NT
2	Intel TokenExpress 16s	NT
2	Intel TokenExpress 32	NT
	Server Management Adapters	
1	Intel Server Monitor Module (ISA)	NT

A.3 Qualified SIMM/DIMMs

The following table list SIMM/DIMM devices known to be compatible with the AP450GX MP Server platform. In general, SIMM devices which are faster than those specified for a given platform will work although no extra performance will be realized. The memory devices shown are categorized according to four levels of qualification:

1. **Intel Tested and Approved**: The SIMM/DIMM device has been electrically tested by Intel engineering and is known to be compatible with the server baseboard or associated memory module. Rigorous environmental testing, voltage margin, shock, and vibration testing were conducted on these SIMM/DIMM devices. In addition, the vendor has met or exceeded Intel's product change, quality control, and availability requirements. The SIMM/DIMM device is on the Intel Approved Manufacturing List and has an Intel part number associated with the device.

2. **Intel Tested**: The SIMM/DIMM device has been electrically tested by Intel engineering and is known to be compatible with the server baseboard or associated memory module. Rigorous environmental testing, voltage margin, shock, and vibration testing were conducted on these SIMM/DIMM devices. The vendor has met Intel's product change, quality control, and availability requirements. The SIMM/DIMM device is not on the Intel Approved Manufacturing List, but maybe listed in the tables below.

3. **Paper Qualification**: The SIMM/DIMM device have been analyzed by the data sheet and have been electrically tested. A small sample (normally 12 SIMMs) have been tested by either Intel engineering, OEM engineering or the SIMM manufacturer across voltage and temperature margins on the baseboard and/or memory modules. The SIMM/DIMM devices are not on the Approved Manufacturing list and are not listed on the tables below.

4. **Customer Tested**: The SIMM/ DIMM has been electrically tested by an OEM customer and is reported to be compatible with the server platform system. The SIMM/DIMM devices are not on the Approved Manufacturing list, and are not listed on the tables below.

Intel recommends that SIMMs listed as (1) *Intel Approved and Tested* or (2) *Intel Tested* be used to ensure reliable system operation. SIMM/DIMM devices not listed or listed as (3) *Customer Tested* can be used; but, in the event of unreliable system operation, the SIMM/DIMM devices should be replaced with SIMMs tested by Intel (1 or 2) to determine whether the SIMM/DIMM devices are causing the problem.

Note: The 1GB memory module is available in two different versions. One version has Tin lead SIMM connectors. The other version has Gold lead SIMM connectors. The Tin lead module must be used with Tin lead SIMMs. Similarly the Gold lead module must be used with Gold lead SIMMs. Mixing metals will result in unknown results.

Intel only qualifies Tin lead SIMMs in the Tin lead memory module. However if a SIMM is identical to one on the Intel qualified list in every way except it has gold leads, it is considered to be a qualified SIMM for the Gold lead memory module.

AP450GX MP Server
Intel Approved and Qualified SIMM Modules

Manufacturer	Part number	Intel Part #'s	SIMM Type	Size	Date Qualified
Hyundai	HYM536410AM-70	644926-001	4Mx36	16MB	03-22-1996
Micron	MT12D436DM-70	644926-001	4Mx36	16MB	05-08-1996
Texas Inst.	TM497MBK36Q-70	644926-001	4Mx36	16MB	06-09-1996
Samsung	KMM5364103AK-60	644926-002	4Mx36	16MB	03-22-1996
Texas Inst.	TM497MBK36Q-60	644926-002	4Mx36	16MB	04-19-1996
Samsung	KMM5368103BK-70	644925-001	8Mx36	32MB	05-08-1996
Mitsubishi	MH8M36BNJ-70	644925-001	8Mx36	32MB	06-14-1996
Samsung	KMM5368103AK-60	644925-002	8Mx36	32MB	03-22-1996
Toshiba	THM3680G0BS-60	644925-002	8Mx36	32MB	04-18-1996
Simple Tech.	I3616100H3-6THBHBA		16Mx36	64MB	04-26-1996

AP450GX MP Server
Intel Approved and Qualified DIMM Modules

Manufacturer	Part number	Intel Part #'s	DIMM Type	Size	Date Qualified
None	None				None

A.4 Qualified Video DRAM

The following table list Video DRAM devices known to be compatible with the AP450GX MP Server. All are devices are in the SOJ package.

AP450GX MP Server Intel Approved and Qualified Video DRAM					
Manufacturer	**Part number**	**Intel Part #'s**	**DRAM Type**	**Size**	**Date Qualified**
Mitsubishi	M5M44260AJ-7-T10 OR -6		256KBx16	512KB	
Samsung	KM416C256AJ-6T		256KBx16	512KB	
Samsung	KM416C256BLJ-7T OR -6		256KBx16	512KB	
Samsung	KM416C256BJ-6T		256KBx16	512KB	
Hyundai	HY514260BJC-60 TAPE/REEL		256KBx16	512KB	
NEC	UPD424260LE-70 ITR OR-60		256KBx16	512KB	
Hitachi	HM514260AJ-7T OR -6		256KBx16	512KB	
Fujitsu	MB814260-70PJRD OR -60		256KBx16	512KB	
Toshiba	TC514260BJ-70 OR-60		256KBx16	512KB	
Micron	MT4C16257DJ-7TR OR -6		256KBx16	512KB	
Oki	MSM514260A-70JSTR		256KBx16	512KB	
Hyundai	HY514260BJC-70 TAPE/REEL		256KBx16	512KB	
Siemens	HYB514171BJ-70		256KBx16	512KB	
Siemens	HYB514171BJ-60 TAPE/REEL		256KBx16	512KB	
Samsung	KM416C256BJ-7T OR -6		256KBx16	512KB	
Samsung	KM416C256AJ-7T OR -6		256KBx16	512KB	

Appendix B -- Product Codes

Below is a list of Intel product codes currently available and a brief description of each. Contact your sales representative for availability and pricing.

Product Code	Description
ALBBRD	AP450GX MP Server Baseboard with B0 82450GX silicon (Fab 3.5)
ALCPU0X	Processor Module with no processors[1]
ALCPU0XA	Processor Module with no processors[2]
ALCPU1X166512	Processor Module with 1 processor & heat sink installed (166MHz/512KB Cache)[1]
ALCPU2X166512	Processor Module with 2 processors & heat sinks installed (166MHz/512KB Cache) [1]
ALCPA1X166512	Processor Module with 1 processor & heat sink installed (166MHz/512KB Cache)[2]
ALCPA2X166512	Processor Module with 2 processors & heat sinks installed (166MHz/512KB Cache) [2]
ALTRMBRD	Termination Module
ALMEM1GBM0	1GB Memory Module (16 SIMM sites, 0MB Memory, non-fused tantalum capacitors, Tin lead SIMM connectors)
ALMEM1GBM0TG	1GB Memory Module (16 SIMM sites, 0MB memory, fused tantalum capacitors, Gold lead SIMM connectors)
ALMEM4GBM0	4GB Memory Module (32 DIMM sites, 0MB memory,
ALCPUUPKIT	Heat sink kit (contains 1 heat sink, 2 heat sink clips and thermal grease) Does not contain a processor.

NOTES:

1. This processor module will **NOT** support a 200/512KB Pentium® Pro processor
2. This processor module will support a 200/512KB Pentium® Pro processor

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Appendix C -- Connector Pinouts

Below is the pinout for each connector on the AP450GX MP server board set.

C.1 Power Connectors PS1 and PS2, Baseboard

The baseboard receives power at PS1 and PS2 from connectors J6 and J7 on the power distribution board. PS1 and PS2 are identical; J6 and J7 are identical.

Table 2.6 Power Connectors

Pin	Signal	Pin	Signal
1	+5 VDC	11	+12 VDC
2	GND	12	GND
3	+5 VDC	13	+12 VDC
4	GND	14	GND
5	+5 VDC	15	+3.3 VDC
6	GND	16	GND
7	+5 VDC	17	+3.3 VDC
8	GND	18	GND
9	+5 VDC	19	+3.3 VDC
10	GND	20	GND

C.2 Power Status/Control Signal Connector PS3, Baseboard

The baseboard receives power status and control signals at PS3 from connector J11 on the power distribution board.

Table 2.7 Power Status/Control Signal Connector

Pin	Signal	Pin	Signal
1	-12 VDC	8	+5 V standby
2	-5 VDC	9	GND
3	PWR_ON	10	PWRGOOD
4	I2C-SDA (Data)	11	GND
5	I2C-SCL (Clock)	12	I2C_PRESENT
6	+5V remote sense (+)	13	+3.3V remote sense (+)
7	+12V remote sense (+)	14	Ground remote sense (-)

C.3 Diskette Drive Connector, Baseboard

Table 2.8 Diskette Drive Connector

Pin	Signal	Pin	Signal
1	GND	18	Head direction
2	Density select	19	GND
3	GND	20	Step
4	Not connected	21	GND
5	Key (pin missing)	22	Write data
6	Extended density in	23	GND
7	GND	24	Write enable
8	Index	25	GND
9	GND	26	Track 0
10	Motor A on	27	GND
11	GND	28	Write protect
12	Drive B select	29	Extended density out
13	GND	30	Read data
14	Drive A select	31	GND
15	GND	32	Head select side 1
16	Motor B on	33	High density out
17	GND	34	Disk change

C.4 Front Panel Connector, Baseboard

Table 2.9 Front Panel Connector

Pin	Signal name	Type	Function
1	SPKRDAT	Out	Drives standard PC-AT speaker
2	VCC5	Out	5 V power supply
3	5VSTANDBY	Out	5 V power supply standby
4	PS_ON	I/O	Power supply on/off switch connection
5	FP_RESET #	In	Active-low front panel reset switch connection
6	GND		Ground
7	FP_NMI #	In	Connects to FP_NMI driver
8	GND		Ground
9	HD1_LED_VCC		Hard Drive #1 LED Activity indicator return
10	HD1_LED_ACT#		Hard Drive #1 LED Activity indicator
11	HD2_LED_ACT#		Hard Drive #2 LED Activity indicator
12	HD2_LED_VCC		Hard Drive #2 LED Activity indicator return
13	KEYLOCK#		Keyboard lock signal
14	GND		Ground
15	SECURE	Out	Secure mode indicator
16	VCC5	Out	LCD Display controller power
17	KEY		Not connected
18	VCC5	Out	5 V power supply
19	I2C-SDA	I/O	I^2C interface data signal
20	CHASIS_SWT_RET	In	Chassis intrusion detection switch return
21	LCD_SD	I/O	Serial I/O data to LCD controller
22	H_PWROFF#	Out	Host power control (from Server Management board)

Continued

Front Panel Connector, Baseboard, continued

Pin	Signal name	Type	Function
23	LCD_SCLK	Out	Clock for LCD serial I/O
24	I2C_SCL	I/O	I^2C interface clock signal
25	LCD_PCLK	Out	LCD controller processor clock
26	GND		Ground
27	EN	Out	LCD enable
28	GND		Ground
29	RW	Out	LCD Read/Write strobe
30	VCC3		3.3 V power supply
31	RS	Out	LCD reset
32	PWR#	Out	RTC power control indication
33	LCD_GND	Out	LCD display ground connection
34	GND		Ground
35	FAN_FAIL#	Out	Indicates failure of at least one cooling fan
36	GND		Ground
37	I2C_PRES		I^2C control signal
38	RESERVED		Reserved
39	Vcc		Vcc
40	RESERVED		Reserved

- Out: driven by system baseboard. In: driven by front panel.
- # at the end of a signal name indicates an active low signal

C.5 IDE Drive Connector, Baseboard

Table 2.10 IDE Drive Connector

Pin	Signal	Pin	Signal
1	IDERST#	2	GND
3	ID7 (data bit 7)	4	ID8 (data bit 8)
5	ID6 (data bit 6)	6	ID9 (data bit 9)
7	ID5 (data bit 5)	8	ID10 (data bit 10)
9	ID4 (data bit 4)	10	ID11 (data bit 11)
11	ID3 (data bit 3)	12	ID12 (data bit 12)
13	ID2 (data bit 2)	14	ID13 (data bit 13)
15	ID1 (data bit 1)	16	ID14 (data bit 14)
17	ID0 (data bit 0)	18	ID15 (data bit 15)
19	GND	20	Keyed (pin missing)
21	IDEDRQ (DMA request 3)	22	GND
23	IDEIOW# (I/O write)	24	GND
25	IDEIOR# (I/O read)	26	GND
27	CHRDY (I/O channel ready)	28	SPSYNC (address latch enable)
29	IDEDAK# (DMA acknowledge 3)	30	GND
31	IDEIRQ14 (interrupt request 14)	32	IDEIO16 # (I/O channel size 16)
33	IDESA1 (address bit 1)	34	PDIAG #
35	IDESA0 (address bit 0)	36	IDESA2 (address bit 2)
37	IDECS0# (host chip select 0)	38	IDECS1# (host chip select 1)
39	IDEHDACT#/DRVPRES# disk activity/drive present)	40	GND

C.6 Fan Connector, Baseboard & Processor Module

Table 2.11 Fan Connectors

Pin	Function
1	GND
2	+12V
3	Fan fail sensor

C.7 Hard Drive LED Connectors, Baseboard

Table 2.12 Hard Drive LED Connectors

Pin	Function
1	not connected
2	HD1_ACTIVE#
3	HD2_ACTIVE#
4	not connected

C.8 I2C Connector, Baseboard

Table 2.13 I2C Connector

Pin	Function
1	I2C_SDA (Data)
2	GND
3	I2C_SCL (Clock)

C.9 3.3V PCI Power Connector, Baseboard

Table 2.14 3.3V PCI Power Connector

Pin	Function
1	GND
2	GND
3	GND
4	+3.3V PCI
5	+3.3V PCI
6	+3.3V PCI

C.10 Server Monitor Module Connector, Baseboard

Table 2.15 Server Monitor Module Connector

Pin	Signal	Type	Description
1	SMI#	Input	System management interrupt
2	I2C_CLK	Output	I^2C clock (8 MHz)
3	GND	Power	Ground
4	Reserved		No connection
5	PWROFF#	Output	Power supply off (active low)
6	I2CDATA	I/O	I^2C data signal
7	LPOK	Input	Host line power okay
8	KEYUNLK#	Input	Keyboard unlock
9	NMI	Input	Nonmaskable interrupt
10	3.3 V	Input	3.3 V power
11	RESET#	Output	Reset system board
12	GND	Power	Ground
13	GND	Power	Ground
14	Reserved		No connection
15	SECURE	Input	Host in secure mode
16	GND	Power	Ground
17	INTRUD	Input	Chassis is open
18	Reserved		No connection (reserved for future use)
19	Reserved		No connection
20	GND	Power	Ground
21	Reserved		No connection
22	Reserved		No connection
23	POWERGD		Power to system is within specification
24	Reserved		No connection
25	Reserved		No connection, pin missing
26	Reserved		No connection

C.11 SCSI Channel A and B Connectors, Baseboard

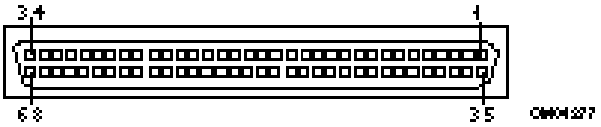


Table 2.15 68-pin Wide SCSI connector

Signal name	Connector contact	SCSI bus conductor	SCSI bus conductor	Connector contact	Signal name
GND	1	1	2	35	DB(12) #
GND	2	3	4	36	DB(13) #
GND	3	5	6	37	DB(14) #
GND	4	7	8	38	DB(15) #
GND	5	9	10	39	DB(P1) #
GND	6	11	12	40	DB(0) #
GND	7	13	14	41	DB(1) #
GND	8	15	16	42	DB(2) #
GND	9	17	18	43	DB(3) #
GND	10	19	20	44	DB(4) #
GND	11	21	22	45	DB(5) #
GND	12	23	24	46	DB(6) #
GND	13	25	26	47	DB(7) #
GND	14	27	28	48	DB(P) #
GND	15	29	30	49	GND
GND	16	31	32	50	GND
TERMPWR	17	33	34	51	TERMPWR
TERMPWR	18	35	36	52	TERMPWR
Reserved	19	37	38	53	Reserved
GND	20	39	40	54	GND
GND	21	41	42	55	ATN #
GND	22	43	44	56	GND
GND	23	45	46	57	BSY #
GND	24	47	48	58	ACK #
GND	25	49	50	59	RST #
GND	26	51	52	60	MSG #
GND	27	53	54	61	SEL #
GND	28	55	56	62	CD #
GND	29	57	58	63	REQ #
GND	30	59	60	64	I/O #
GND	31	61	62	65	DB(8) #
GND	32	63	64	66	DB(9) #
GND	33	65	66	67	DB(10) #
GND	34	67	68	68	DB(11) #

C.12 PCI Connectors, Baseboard

The baseboard PCI connectors adhere to the requirements in the PCI Specification 2.0.

C.13 VGA Video Port, Baseboard

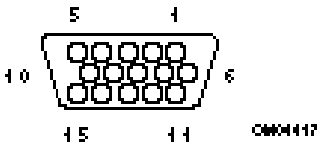


Table 2.16 VGA Video Port

Pin	Signal	Pin	Signal
1	Red	9	Not connected
2	Green	10	GND
3	Blue	11	Not connected
4	Not connected	12	Not connected
5	GND	13	HSYNC (horizontal sync)
6	GND	14	VSYNC (vertical sync)
7	GND	15	Not connected
8	GND		

C.14 Parallel Port Connector, Baseboard

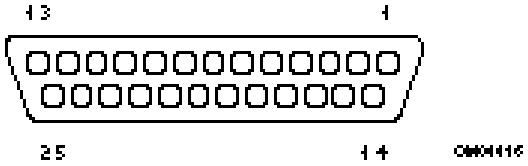


Table 2.17 Parallel Port Connector

Pin	Signal	Pin	Signal
1	Strobe #	10	ACK (acknowledge) #
2	Data bit 0	11	Busy
3	Data bit 1	12	PE (paper end)
4	Data bit 2	13	SLCT (select)
5	Data bit 3	14	AUFDXT (auto feed) #
6	Data bit 4	15	Error #
7	Data bit 5	16	INIT (initialize printer)
8	Data bit 6	17	SLCTIN (select input) #
9	Data bit 7	18–25	GND

C.15 Serial Port Connectors 1 and 2, Baseboard

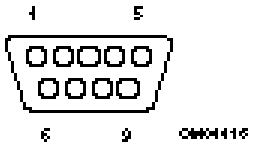
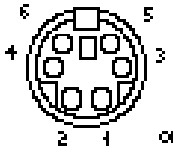


Table 2.18 Serial Port Connectors

Pin	Signal
1	DCD (data carrier detect)
2	RXD (receive data)
3	TXD (transmit data)
4	DTR (data terminal ready)
5	GND
6	DSR (data set ready)
7	RTS (request to send)
8	CTS (clear to send)
9	RIA (ring indicator)

C.16 Keyboard and Mouse Connectors, Baseboard



These identical PS/2-compatible connectors share a common housing.

Table 2.19 Keyboard and Mouse Connectors

Pin	Keyboard signal
1	KEYDAT (keyboard data)
2	Not connected
3	GND
4	FUSED_VCC (+5 V)
5	KEYCLK (keyboard clock)
6	Not connected

Pin	Mouse signal
1	MSEDAT (mouse data)
2	Not connected
3	GND
4	FUSED_VCC (+5 V)
5	MSECLK (mouse clock)
6	Not connected

Appendix D - Customer Support

D.1 FAXBack

- Product descriptions and technical data sent to any fax machine from a touch-tone phone
- Information on End-of-Life products
- Available worldwide through direct dial

U.S. Toll Free 800-628-2283 (Americas: 916-356-3105)

Europe 44-793-496646

D.2 Intel Application Support

Contact Your Local Technical Representative

The customer's number one asset is the local representative. For all technical issues, first contact your Field Application Engineer.

Hotline

A direct link to highly qualified and well trained technical personnel.

- Toll-free access to Intel support engineers for problem resolution
- Responses within 24 hours Monday-Friday
- Expert assistance geared to the special needs of OEMs and VARs

1-800-628-8686

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A full service bulletin board with product information and more.

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Europe	**44-793-496340**

- FLASH BIOS upgrade files
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A full service World Wide Web location with product information and more.

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- FLASH BIOS upgrade files
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