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AP-757
Application Note

Embedded Processor Module
Design Guide

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Embedded Processor Module Design Guide

FIGURES

TABLES

1.0   Introduction

The Intel Embedded Processor Module was developed to assist system designers with the challenges of high speed design by taking care of the high speed processor interface. This allows the system designer to concentrate on the I/O subsystems and PCI-bus interface.

This document is a supplement to the *Intel Embedded Processor Module* datasheet (Order No. 273105). The contents of this design guide assist in the development of a system-level platform that uses the Intel Embedded Processor Module.

In this document, the term "system board" refers to the system-level platform (baseboard or motherboard) that the Embedded Processor Module plugs into. Note that the 82371SB (PIIX3) must be used in the system board design.

1.1   Related Documents

Document	Intel Order Number
Intel 430HX PCIset Design Guide	297467
Intel Embedded Processor Module datasheet	273105
PCI Local Bus Specification, Revision 2.1	

2.0   Electrical Layout Considerations

Increasing bus frequencies with fast edge rates place additional demands on system designers. Designing a reliable system requires the use impedance-controlled boards, equalized clock trace lengths, optimized component layout and trace routing, and proper termination.

2.1   Clocks

The Embedded Processor Module contains a Cypress CY2254A* clock synthesizer. The clock synthesizer is fed by a 14.318 MHz crystal oscillator. The clock synthesizer generates four buffered copies of the 66 MHz processor clock, six buffered copies of the 33 MHz PCI clock, a 12 MHz clock, a 24 MHz clock, and two 14.318 MHz reference clocks.

The clocks lines are of matched length to minimize any skew between the processor, the system controller, and the pipeline-burst SRAMs (PBSRAMs). The host clocks are series terminated on the module with 66.5 Ω resistors. The 66 MHz clocks are not routed to the connector.

The six 33 MHz PCI clocks are routed to the 120-pin connector and are of equal length. The PCI clock traces are series terminated with 33.2 Ω resistors. One of the six PCI clocks must be routed back into the Embedded Processor Module through the PCICLK_IN pin on the 120-pin connector. The PCICLK_IN signal is used to drive the 82439HX System Controller PCI interface. The PCICLK_IN trace must be matched with the other PCI clocks on the system board to minimize skew between the Embedded Processor Module and the system board.

Clocks are series terminated on the Embedded Processor Module; the designer must ensure that the system board supports AC termination at the signal destination.

Table 1 lists trace lengths for the Embedded Processor Module clock signals.

Table 1. Clock Trace Lengths on the Intel Embedded Processor Module

Clock Trace	Length
CPU Host Clock	9.35″
PCI Onboard Clocks	2.60″
PCICLK_IN	1.60″

Based on the trace lengths provided in Table 1, the system board requirements are:

Minimum PCI trace length on system board
      = CPU Host Clock – PCI Onboard Clock

PCI min = 9.35″ – 2.60″
        = 6.75″

All PCI Clock traces on the system board must be of equal length ($\pm$ 250 mils) and at least 6.75″ long to maintain the proper relationship between PCI devices and between PCI and host clocks.

The line length of the PCI clock routed back to the Embedded Processor Module must be 1.60″ shorter than

the other five PCI clock lines to maintain the proper clock relationships:

PCICLK_IN trace length
= PCI max length (system board) – 1.60"

The Embedded Processor Module also supplies clocks of 24 MHz, 12 MHz, and 14.318 MHz for system use. These clocks are not terminated on the Embedded Processor Module. The system board must provide proper termination of these clock signals.

Summary of key points:

- PCI Clock circuits are series terminated on the Embedded Processor Module. The system board must support AC termination.

- All PCI clocks routed on the system board must be at least 6.75" long.

- The trace length of the PCICLK_IN input to the Embedded Processor Module must be 1.60" shorter than the other PCI clocks on the system board. The minimum length required is 5.15".

- The impedance at the connector of the system board should be approximately 65 Ω to match the impedance on the Embedded Processor Module connector.

- Use point-to-point routing topologies whenever possible.

- To minimize EMI concerns, terminate unused PCI and system clocks on the system board.

- Future embedded modules may support higher processor clock frequencies, but the processor bus and PCI bus frequencies will remain the same:

  — Processor I/O bus = 66 MHz

  — PCI Bus = 33 MHz

  — Processor Core = Processor I/O × Ratio;
  Ratio= 2 (EMBMOD133)
  or 2.5 (EMBMOD166)

These frequencies are hardwired into the Embedded Processor Module and are not selectable.

2.2   Memory Bus

Follow the design guidelines for the 82439HX system controller when integrating the Embedded Processor Module into a system solution.

The RAS[7:0]# and CAS[7:0]# lines are terminated with 22 Ω resistors on the Embedded Processor Module. Termination need not be integrated on the system board.

Other design considerations regarding the memory bus include:

- External buffering of the MA[11:2], MAA/B[1:0] and MWE# signals is required when more than four SIMM slots are supported.

- The 430HX supports ECC or Parity when x72-bit memory devices are used.

NOTE: The Embedded Processor Module supports both fast page mode (FPM) and extended data out (EDO) memory types. Synchronous DRAM is not supported by the Embedded Processor Module.

- Mixed EDO and FPM memory types are not allowed in the same bank. Mixing of memory types between banks is allowed.

For more information on the System Controller design, refer to the *Intel 430HX PCIset Design Guide* (Order No. 297467).

2.3   PCI Interface

The Embedded Processor Module communicates with the system board using a 32-bit PCI bus. The PCI bus conforms to the *PCI Local Bus Specification*, Revision 2.1. The module itself represents 1.5 electrical loads on the PCI bus.

The REQ[3:0]# signals are pulled up to 5 V by 2.7 KΩ resistors on the Embedded Processor Module. The following signals must be pulled to 5 V on the system board: PIRQ[A:D]#, FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, PERR#, and SERR#. Pins REQ64# and ACK64# on the PCI connector must also be pulled to 5 V.

The GNT[3:0]# signals are pulled up to 3.3 V on the Embedded Processor Module by 2.7 KΩ resistors. The PHLDA# must be pulled up on the system board through a 2.7 KΩ resistor. These signals are outputs of the 82439HX system controller.

The 82439HX System Controller supports up to four PCI masters with its REQ[3:0]# and GNT[3:0]# signals.

For more information on the PCI interface design, see the *Intel 430HX PCIset Design Guide* (Order No. 297467).

2.4   Voltage Regulation

The Embedded Processor Module integrates a Linear Technology, Inc. LTC1435* voltage regulator on-board to provide the core voltage of the Pentium® Processor.

The input to the voltage regulator is the 5 V power plane on the Embedded Processor Module. Because the 5 V plane also supplies 5 V to the 82439HX system controller the tolerance on the power supply must be within ±5% (under a maximum current load). Refer to the applicable processor datasheet for maximum current requirements. The system board must supply a minimum voltage of 4.75 V.

Since the 3.3 V supply is not regulated on the Embedded Processor Module, the system board must provide a minimum of 3.135 V and a maximum of 3.6 V to meet the specifications for components integrated on the Embedded Processor Module.

The frequency of the switching regulator used on the Embedded Processor Module is approximately 165 KHz.

Bulk and high frequency decoupling capacitance is provided on the module; however, the system board should provide additional bulk and high frequency capacitance near the connectors of the Embedded Processor Module. The additional capacitors ensure that "clean" power is provided to the Embedded Processor Module. The amount of capacitance required on the system board depends on many factors, including power supply design, system board layout, and board impedance. Table 2 lists the minimum recommended configuration.

Table 2. Voltage Plane Capacitance Requirement

Voltage Plane	Location	Capacitance	Rating
V_5V	Connector	100 µF, 0.1 µF, 0.01 µF	35 V
V_3	Connector	100 µF, 0.1 µF	6 V

The Embedded Processor Module provides bulk decoupling for the processor, the 82439HX system controller, and the PBSRAMs. The bulk capacitance

minimizes voltage drop when the power supply does not have time to react to a large current change in a relatively short period of time (50–300 ns). Table 3 lists the bulk capacitance for the processor on the Embedded Processor Module.

Table 3. Processor Bulk Decoupling Capacitance

2.9 V Core Decoupling	4 x 100 µF Low ESR/ESL Ceramic
3.3 V I/O Decoupling	1 x 33 µF Low ESR/ESL Ceramic

Additional bulk capacitance is implemented on the Embedded Processor Module for the System Controller and SRAM devices.

The Embedded Processor Module also provides high frequency decoupling capacitors to minimize the effects of high-frequency transient currents during device operation.

The Embedded Processor Module has a COREV_SENSE signal output to indicate that the core power supply is at the correct voltage. This signal should be used by the system designer to communicate the power good status to the overall system. The COREV_SENSE signal is detected by a comparison circuit, and the output is routed to the PWROK signal on the 82371SB (PIIX3). When this signal is received by the PIIX3, the system can be reset.

There is no overcurrent/overvoltage protection circuitry on the Embedded Processor Module, except for the input protection circuitry on the individual components. Never insert or remove the Embedded Processor Module while the power is on. Permanent damage to the module may result.

2.5   Embedded Processor Module Pullup/Pulldown Resistor Requirements

Table 4 lists the Embedded Processor Module signals that have pullup or pulldown resistors and the required resistor values:

Table 4. Signals with Pullups or Pulldowns

Signal	PU / PD	Resistor Values (Ω)	Voltage (V)
DP[7:0]	PU	4.7 K	3.3
STPCLK#	PU	8.2 K	3.3
AP	PU	8.2 K	3.3
WB/WT#	PU	8.2 K	3.3
FLUSH#	PU	1.0 K	3.3
PEN#	PU	4.7 K	3.3
R/S#	PU	8.2 K	3.3
REQ[3:0]#	PU	2.7 K	5.0
GNT[3:0]#	PU	2.7 K	3.3
EWBE#	PD	0	GND
HOLD	PD	0	GND
PHLD#	PU	10 K	5.0
PHLDA#	PU	10 K	3.3

2.6   System Board Pullup/Pulldown Resistor Requirements

The system designer must provide pullup resistors on the system board for the signals listed in Table 5.

Table 5. System Board Pullup/Pulldown Requirements

Signal	PU/PD	Resistor Value (Ω)	Strapping Voltage (V)
INTR	PU	4.7 K	3.3
FERR	PU	4.7 K	3.3
NMI	PU	4.7 K	3.3
SMI#	PU	4.7 K	3.3
IGNNE#	PU	4.7 K	3.3
CPURST	PU	3.3 K	3.3
PLOCK#	PU	2.7 K	5.0
DEVSEL#	PU	2.7 K	5.0
TRDY#	PU	2.7 K	5.0
IRDY#	PU	2.7 K	5.0
FRAME#	PU	2.7 K	5.0
SERR#	PU	2.7 K	5.0
STOP#	PU	2.7 K	5.0
PAR	PU	2.7 K	5.0
A20M#	PU	4.7 K	3.3
INIT	PU	330	3.3

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3.0   Mechanical Considerations

3.1   Space Constraints

The Embedded Processor Module is designed to fit into a single CompactPCI* slot or into other space-constrained environments. The Embedded Processor Module integrates a thermal solution and provides adequate signal integrity at the connector interface.

The module does *not* provide a thermal solution that is adequate for *all* environmental conditions. The thermal characteristics of the Embedded Processor Module are currently being evaluated.

3.2   Reserved Areas

The area beneath the Embedded Processor Module module should be considered reserved, with the exception of 0805 footprint and smaller passive components. If the system board uses this area, the system designer must ensure that there is no interference between the Embedded Processor Module and the system board.

3.3   Module Mechanical Description

The following sections the physical characteristics of the Embedded Processor Module.

3.3.1   General Description

The Embedded Processor Module has components on both sides. Components on the bottom may extend to within 100 mils of the system board surface, except for the board-to-board connectors. The lead guard for the Tape Carrier Package (TCP) is not removable. Any attempt to remove it may result in damage to the TCP device. Components on the top side of the PCB (including the Heat sink) do not exceed 540 mils. Heights are relative to the PCB surface.
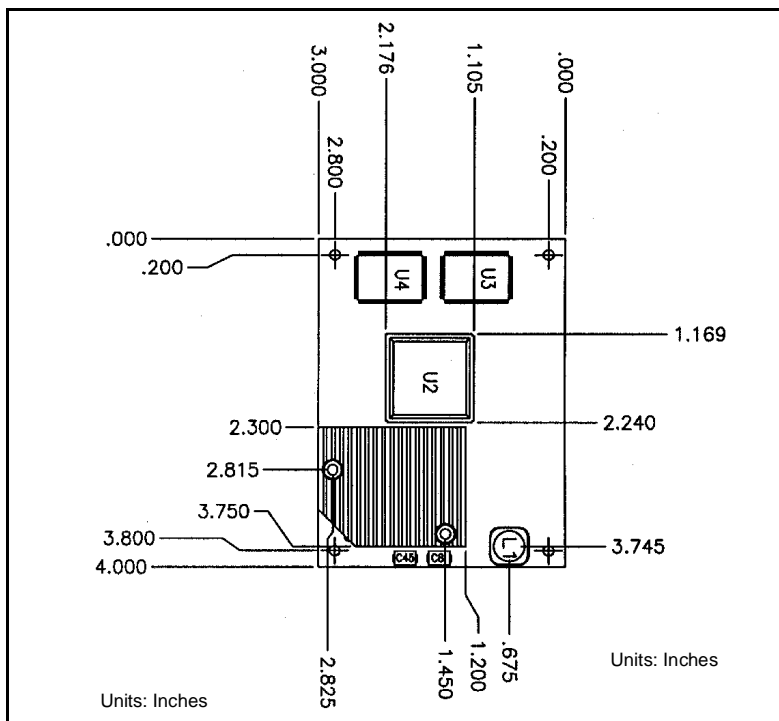

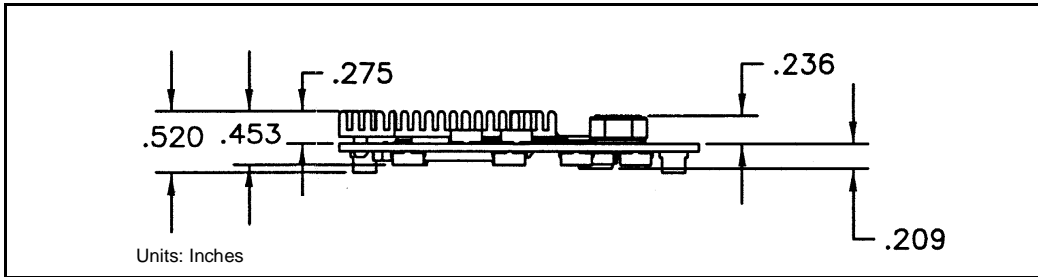**Figure 1. Module Dimensions — Top Side View**
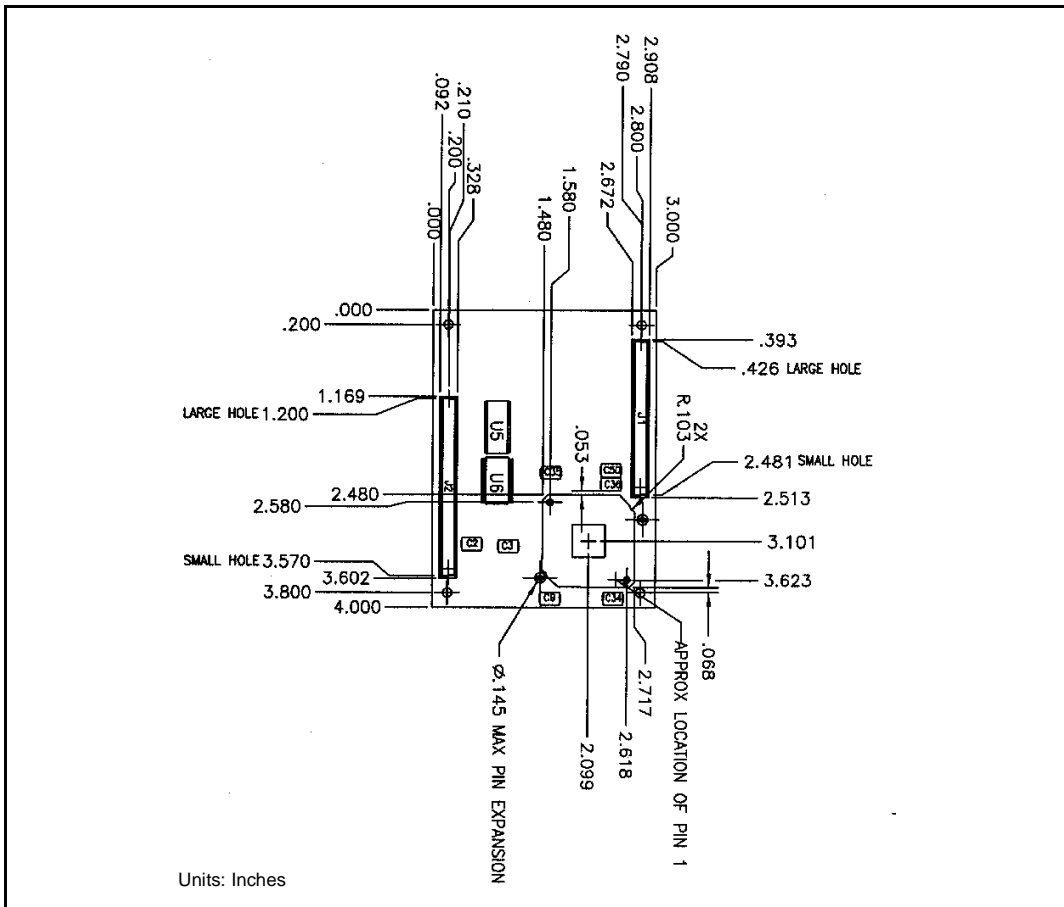
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Figure 2. Module Dimensions — Side View

Figure 3. Module Dimensions — Bottom (Connector) Side View

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3.3.2   Mounting Hole Locations and Size

There are four holes in the corners of the Embedded Processor Module for attachment to the system board. The diameter of the four mounting holes is 125 mils, nominal. The mounting holes accept a size 4 screw. Figure 4 shows the location of the holes from the edges of the PCB (all values are nominal).
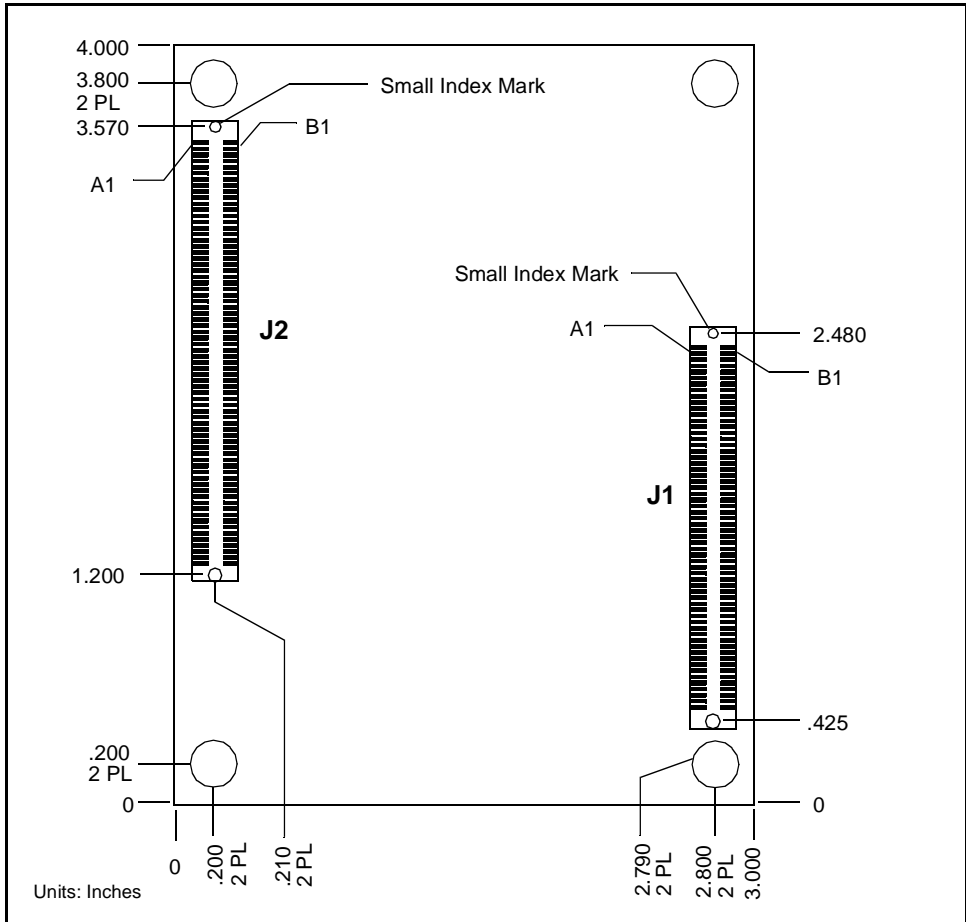

Figure 4. Mounting Hole Diagram

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3.3.3 Ground Ring

The mounting holes are electrically tied to ground (GND) on the Embedded Processor Module. The ground ring around the mounting holes are 450 mils in diameter.

3.3.4 Module Mass

The mass of the module is currently a total of 63 grams, including the heatsink. It is recommended that the system board design be able to accommodate a mass of 100 grams to support possible future changes in module material.

3.4 Recommended Module Mounting Technique

The system manufacturer must use the mounting locations to attach the Embedded Processor Module to the system board. Attachment using the board-to-board connectors alone does not provide an adequate or reliable connection between the Embedded Processor Module and the system board over time.

It is recommended that the Embedded Processor Module be grounded to the system board through the standoffs. These standoffs must be able to withstand the manual insertion force of the Embedded Processor Module into the system board. In addition, the standoffs must be able to withstand the shock and vibration requirements of the system. Connection via the standoffs provides a low impedance ground path from the Embedded Processor Module.

The mounting holes accept a size 4 screw. When attaching the processor module to the system board, the appropriate screw, washer and lock washer should be used to properly attach the module. A size 4 screw should not be used without appropriate washers.

4.0 Surface Mount Connectors

The Embedded Processor Module connects to the system board via two low profile, high density connectors. The two connectors are segregated into functional categories: the PCI Bus interface and the DRAM interface. Refer to the *Intel Embedded Processor Module* datasheet for detailed information on the module pinout and signal descriptions. The connectors are available from multiple vendors with identical designs. The part numbers for two

of the vendors are listed below. Mating pairs can be mixed between vendors.

Figure 5. Connector Part Numbers

Manufacturer	Part Number	Type
AMP	177983-5	120-pin receptacle[†]
AMP	177983-6	140-pin receptacle[†]
AMP	177984-5	120-pin header
AMP	177984-6	140-pin header
BERG	61082-12100X	120-pin receptacle[†]
BERG	61082-14100X	140-pin receptacle[†]
BERG	61083-12100X	120-pin header
BERG	61083-14100X	140-pin header

[†]The receptacle part numbers are part of the Embedded Processor Module assembly and are listed for reference only.

4.1 Connector Specifications

A subset of the connector specifications is listed in the Embedded Processor Module datasheet; however, refer to the connector vendor for a detailed specification.

5.0 Implementing the ITP Port on the Embedded Processor Module

The module accommodates the attachment of the Intel Test Port (ITP), which allows in-circuit emulation. To attach the ITP, the following components must be added to the module:

Table 6. Additional Components for ITP

Location	Component	Footprint
U8	74LVQ04 Hex Inverter	14LSOIC
R41	1.0 KΩ Resistor	0805
R42	0Ω Resistor	0805

See Figure 6 for the location of the test port. Figure 7 shows the location of the additional components required for the ITP to function.
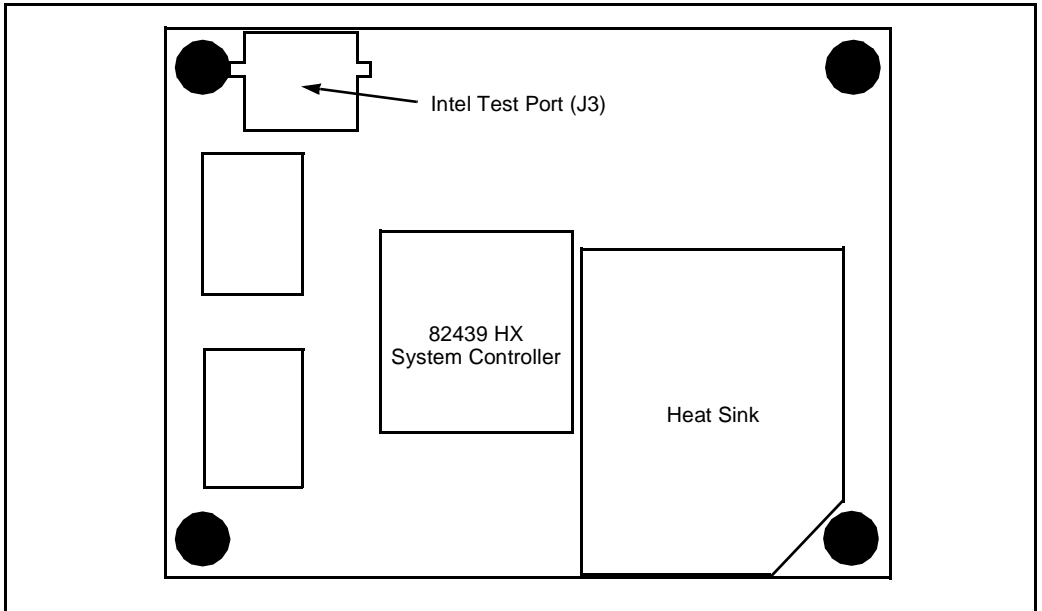
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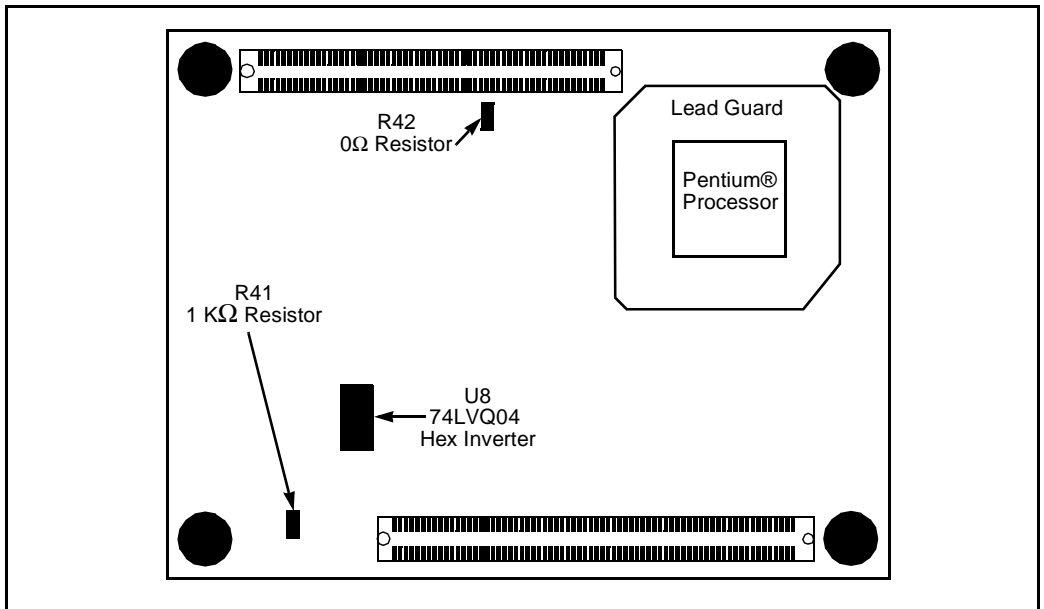**Figure 6. Intel Test Port Mounting Location**

Figure 7. Additional Components Required for ITP

6.0   Regulatory Compliance

6.1   Safety

The fabricated printed wiring board is UL Recognized with a 94V-0 flame classification.

6.2   EMI/EMC

Compliance with applicable EMI/EMC regulations must be evaluated in the end use product.

7.0   Features not Supported by the Embedded Processor Module

These Pentium processor features are not implemented on the Embedded Processor Module:

*   The Cypress CY2254ASC-1* does not support gating of the CPU or PCI clocks. Therefore, the Embedded Processor Module cannot fully support the power management features available on the Pentium processor.

*   The Embedded Processor Module does not support dual processing capability.

*   The Embedded Processor Module does not support Functional Redundancy Checking mode.

*   The Embedded Processor Module does not support synchronous DRAM (SDRAM) memory.