ALTServer
Baseboard & Platform

Preliminary Technical Product Summary

(SUBJECT TO CHANGE)

Version 0.6

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Order Number 281657-001

ALTServer
Technical Product Summary

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281657-001

Introduction

The ALTServer baseboard and platform have been clearly designed to meet the needs of the server marketplace, and continue a tradition of performance and reliability set by Intel's Xpress technology. In contrast with the Xpress modular architecture, ALTServer offers a 'flat' design with the processor and memory subsystems residing on the main baseboard. The ALTServer design uses members of the Intel 82430 Neptune PCIset to provide high performance and a highly integrated system at multiple price/performance levels.

Two Zero Insertion Force (ZIF) sockets for Pentium™ processors provide scalability using Symmetric MultiProcessing (SMP) operating systems, such as UnixWare*, SCO UNIX, Solaris*, OS/2*, and WindowsNT*. The ALTServer's multiprocessing capabilities comply with the Intel Multiprocessing Specification v1.1. Additional simple and cost-effective performance upgrades are available through a variety of plug-in cache module options.

The ALTServer's expansion capabilities meet the needs of file and application servers for high performance I/O by providing a combination of PCI local bus and EISA connectors. The baseboard offers two dedicated PCI slots, five dedicated EISA slots, and one shared PCI/EISA slot. The high-performance PCI local bus allows the adoption of newer networking technology, such as ATM and 100 MB/second Ethernet NICs, with a minimum of effort and without concern for I/O bottlenecks. The PCI local bus offers a 133 MB/second bandwidth and has been a proven high-speed solution on the desktop. The ALTServer's architecture, as shown in the diagram below, brings these benefits to servers:

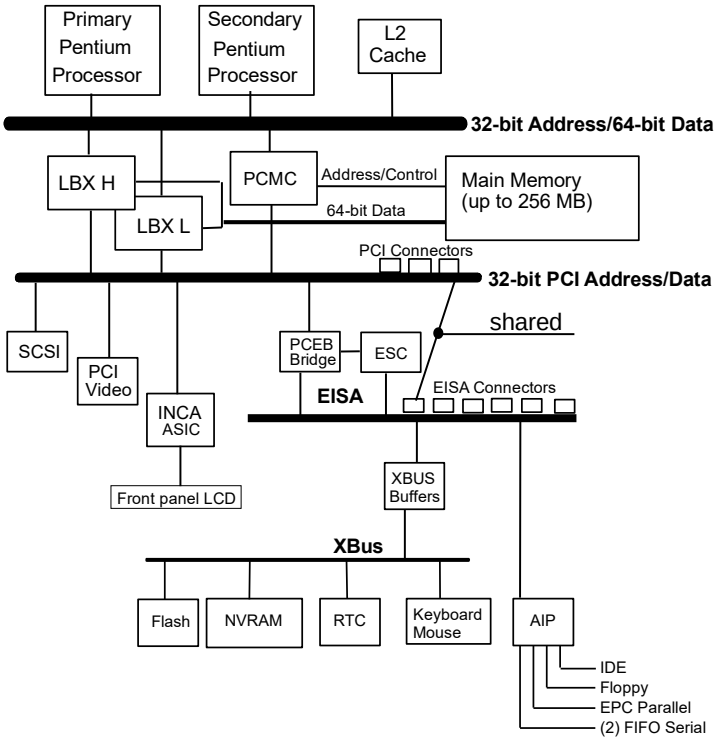


Figure 1. ALTServer block diagram

This combination of PCI and EISA expansion offers continuing support for existing special function EISA add-in boards, such as X.25 Multiport Serial cards. All of the add-in slots are available to the user because the high-performance PCI fast SCSI-2 interface and a PCI graphics controller are integrated on the baseboard.

A number of security, reliability, and management features also have been incorporated into the ALTServer's design to meet vital server needs. These features can be further enhanced with accessory products like the Intel Server Monitor Module and either intelligent EISA or PCI RAID controllers.

AT FORM FACTOR

The ALTServer baseboard measures 12” by 13” and is designed to fit into a standard AT-style chassis. Maximum chassis flexibility is provided by a special baseboard header which allows the connection of a riser with any of the following configurations of standard external I/O connections (keyboard, mouse, serial ports, etc.):

1. Wide SCSI internal to chasis
2. Wide SCSI external to chasis
3. Narrow SCSI external to chasis
4. Standard AT form factor

The following diagram shows the dimensions and mounting hole locations.

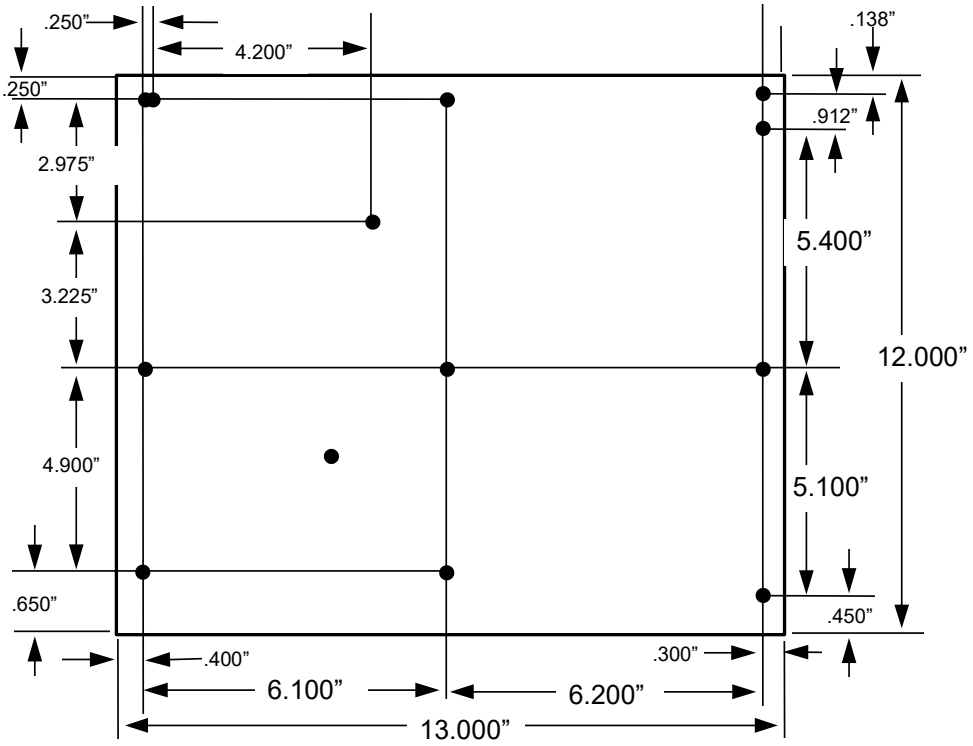
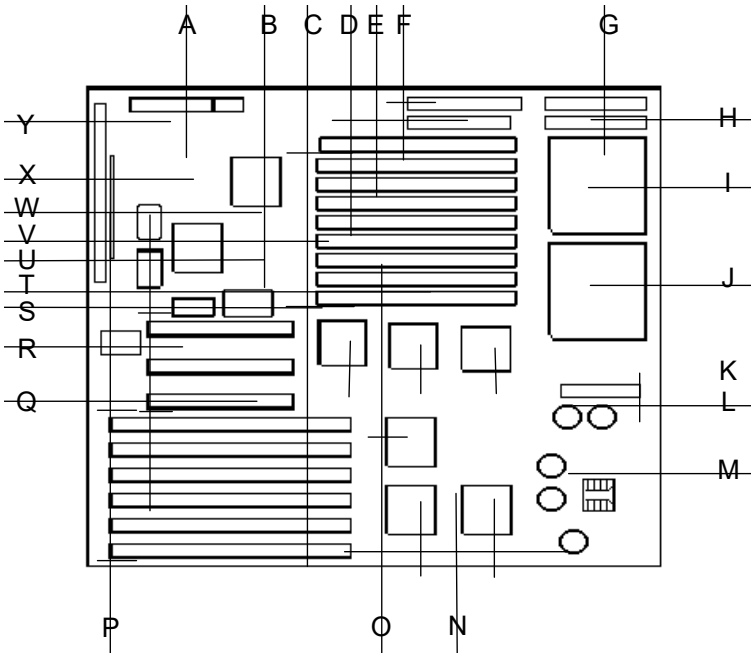


Figure 2. ALTServer board dimensions

Board Level Features



A – Primary power connector
B – Adaptec 7870 PCI SCSI Controller
C – SIMM sockets for up to 256 MB system memory
D – Socket for second level cache
E – PCI IDE connector
F – PCI SCSI connector (termination adjacent)
G – Floppy drive connector
H – Front panel LCD connector
I – Primary Pentium processor
J – Second Pentium processor socket
K – Intel Neptune PCIset
L – Server Monitor feature connector
M – Voltage regulation circuitry
N – EISA bus bridge chip set
O – Interrupt Control ASIC (INCA component)
P – EISA expansion slot connectors
Q – PCI expansion slot connectors
R – Flash memory component holding BIOS
S – 3.3 volt PCI power connector
T – Real Time Clock and battery
U – Socket for video memory upgrade to 1 MB
V – Cirrus Logic 5430 PCI Graphics controller
W – 512 KB video memory
X – Termination for SCSI devices connected to riser(all 3 removed for wide devices, first two removed for narrrow devices)
Y – Header for I/O riser connector

Figure 3. ALTServer board features

PENTIUM PROCESSORS

The ALTServer baseboard is designed to operate with 75 MHz, 90 MHz, 100 MHz or 120 MHz Pentium processors and is shipped with a single processor installed in the main Zero Insertion Force (ZIF) socket. A second ZIF socket is provided to upgrade to a dual processor SMP configuration. When two processors are installed, both should be of the same frequency, stepping and voltage specifications to ensure correct operation.When upgrading to dual processing, care should be taken to ensure the second processor is correctly oriented in the ZIF socket next to the primary processor.

The Pentium processor has an internal speed of 75, 90, or 100 MHz and an external speed of 50, 60, or 66 MHz respectively and is backward-compatible with the Intel486™ processor. The Pentium processor supports both read

and write burst mode bus cycles and includes a 16 KB on-chip cache core (8 KB for code and 8 KB for data caches) employing a write-back policy. Also integrated into the Pentium processor is an advanced numeric coprocessor which significantly increases the speed of floating point operations, while maintaining backward compatibility with the i486™DX math coprocessor and complying with ANSI/IEEE standard 754-1985. Based on 0.6 micron processes, the Pentium processor is powered by 3.3 volts and supports Intel's System Management Mode (SMM) power-management operation.

3.3 VOLT REGULATION

A patented onboard voltage regulator circuit provides the required 3.3 volts to the processor from the 5 volts provided by a standard power supply. This allows the ALTServer baseboard to be used with a 'standard' PC supply, instead of more costly supplies with 3.3V outputs. It should be noted that the onboard 3.3 volt regulator provides power for the processor(s) and not the PCI slots. When 3.3V PCI cards are used, the baseboard's 3.3 volt connector for the PCI slots must be used with a separate 3.3 volt power supply or with an external voltage converter.

SYMMETRIC MULTIPROCESSING (SMP) SOFTWARE CONSIDERATIONS

The ALTServer Baseboard and BIOS comply with the Intel MultiProcessor (MPS) Specification, revision 1.1. This standard defines a method of constructing systems in which two or more processors operate concurrently. These processors operate in a tightly coupled architecture in which each processor has the same 'view' of the system, and in which each processor can interrupt any other processor. This architecture has the following features:

- Each processor sees the same memory and I/O space, requiring only one copy of the operating system.
- Any task can run on any processor, reducing the chance that the failure of one or more processors will render the system unusable. Tasks can be written generically, without regard for which processor they will be executing on.

The use of an Advanced Programmable Interrupt Controller (APIC) is specified for interrupt detection and notification. This reduces the load on the system bus, since the APICs use a serial bus to transmit and receive interrupts.

SMP Operating System Requirements

To obtain the benefits from using a second processor on the ALTServer platform, it is essential to use an operating system that is capable of Symmetric MultiProcessing and which has driver support for the Intel MultiProcessor Specification, version 1.1. This allows the software load to be distributed across the processors and for the operating system and application process to be shared efficiently. Most server operating systems now have this functionality. However, DOS and Microsoft Windows 3.1, 3.11 and Windows '95 do not have this capability and will see no performance increase from adding a second processor.

The following table shows which server operating systems support Intel MPS v1.1 and ALTServer:

Operating System	*Version*
Microsoft Windows NT	3.1, 3.5
Novell UnixWare	2. 0
Novell USL/USG	System V.4.2 MP
IBM OS/2*	2.11 SMP
SunSoft Solaris for x86	2.4
SCO OpenServer + MPX	3.1
Banyan Vines*	5.54

Table 1. MultiProcessing operating system support

SECOND LEVEL (L2) CACHE

To provide a cost effective solution using standard chip set components, the ALTServer offers an upgradeable second level cache using Integrated Device Technology (IDT) or Corsair cache devices. This provides five options

and price/performance points: No cache, 256 KB or 512 KB asynchronous cache, 256 KB or 512 KB Burst Synchronous cache.

The performance of each option depends on many factors, such as operating system, number of processors, amount of system memory, and other variables. However, as a general rule, overall system performance increases with larger cache sizes. The use of a Burst Synchronous cache should provide even higher performance than the equivalent size Asynchronous cache device.

The second level cache may be *Enabled* or *Disabled* using the BIOS Configuration Utility. When *Enabled,* the caching policy is always write-back mode to support the internal (L1) 16 KB cache of the Pentium processor. With a burst cache device installed, the processor read and write clock latencies are 3-1-1-1. With the Asynchronous modules, the processor read latency is 4-2-2-2 and the write latency is 3-1-1-1.

The single cache resource is shared in SMP configurations where two Pentium processors are installed. Cache coherency and control is provided by the 82434NX PCI/Cache Memory Controller.

SYSTEM MEMORY

The main system memory is provided by eight 72-pin SIMM sockets for up to 256 MB of memory expansion on the baseboard. The eight 90° angled sockets support 256K x 36 (1 MB), 512K x 36 (2 MB), 1M x 36 (4 MB), 2M x 36 (8 MB), 4M x 36 (16 MB), and 8M x 36 (32 MB) SIMMs. The minimum memory size is 2 MB and the maximum memory size, using eight 32 MB SIMMs, is 256 MB. Memory timing requires 70 ns fast page devices. Parity generation/checking is provided for each byte, but parity generation/checking can be disabled using the System Configuration Utility (SCU) to allow for use of non-parity 32-bit SIMMs.

The eight SIMM sockets are arranged as four banks (Bank 0, 1, 2, and 3) with each bank consisting of two sockets and providing a 64-bit wide data path and 8 parity bits. The memory array is controlled by the Intel 82434NX PCMC and data buffering is provided by two Intel 82433NX Local Bus Extension devices. Both SIMMs in a bank must be of the same memory size and type, although separate banks may have different sizes and types of memory installed. Any (or all) banks may be populated to provide the required system memory. In some instances, for electrical reasons only, it may be essential to populate Bank 0 first.

System memory begins at address 0 and is contiguous (flat addressing) up to the maximum amount of system memory installed. The only places where system memory is non-contiguous is in the ranges from 00080000 - 000FFFFF (the DOS compatibility region) and 00F00000 - 00FFFFFF (the system BIOS region). Memory regions holes at any other location may result in DRAM beyond that hole unusable.

EXPANSION SLOTS (PCI AND EISA)

The ALTServer baseboard allows the addition of up to eight I/O expansion cards, and provides interfaces to the the ISA bus, the EISA bus, and the PCI loca bus. There are six EISA bus expansion connectors and three PCI expansion connectors. One expansion slot is shared by connectors which will accommodate either an EISA or a PCI expansion card, but not both at the same time. All three PCI expansion slots accept PCI master cards and fully support the PCI 2.0 specification. The six EISA bus expansion connectors will accept either EISA or ISA add-in cards. All six slots will accept either EISA/ISA bus masters or EISA/ISA slave cards.

The PCI bus on the ALTServer runs at half the external bus speed of the installed processor. For example, the external bus speed of the 100 MHz processor is 66 MHz, and the PCI bus is clocked at 33MHz. By dividing the PCI bus clock by either 3 or 4, the EISA bus clock can be derived. The table below shows an example:

Processor Clock Speed	*External Bus Speed*	*PCI Bus Speed*	*Divisor*	*EISA Clock*
75 MHz	50 MHz	25 MHz	3	8.33 MHz
90 MHz	60 MHz	30 MHz	4	7.5 MHz
100MHz	66 MHz	33 MHz	4	8.33 MHz

Table 2. ALTServer clock frequencies and bus speeds

PERIPHERAL COMPONENT INTERCONNECT (PCI) CHIP SET

The baseboard's two dedicated PCI expansion slots and one PCI/EISA combination slot are controlled by the Intel Neptune PCIset. The ALTServer uses one 82434NX PCI/Cache/Memory Controller (PCMC) and two 82433NX Local Bus Extension (LBX) devices. Together they provide a PCI interface, as well as DRAM memory and cache controller functions, including:

- Processor reset control
- Processor L1 cache control
- Processor burst mode control
- Processor interface control
- Integrated second level write-back cache controller with tag comparator
- Fast Page-mode DRAM controller
- Burst memory read/write control logic
- Data bus conversion to PCI
- Parity generation/detection to memory

82434NX PCI/CACHE/MEMORY CONTROLLER (PCMC)

The 82434NX provides all control signals necessary to drive a second level cache and the DRAM array, including multiplexed address signals. It also controls system access to memory and generates snoop controls to maintain cache coherency. The PCMC integral memory controller manages up to 256 MB of SIMM DRAM and controls either a Burst or Asynchronous Cache of either 256 KB or 512 KB. It also maintains full cache coherency between the Cache and main memory when both processors are installed.

82433NX LOCAL BUS EXTENSION (LBX)

There are two 82433NX components which provide data bus buffering and dual port buffering to the memory array, LBX-H and LBX-L. LBX-H decodes the 64-bit data lines (16:31) & data lines (48:63), while LBX-L decodes the other data lines (0:15) & (32:47). The use of two 82433NX components provides a 64-bit data path from the processors to main memory. Controlled by the 82434NX, the 82433NX devices add one load each to the PCI bus and perform all the necessary byte and word swapping required. Memory and I/O write buffers are included in these devices.

HOST-TO-PCI BRIDGE

The PCI control section of the PCMC and the two LBX components form a Host-to-PCI bridge subsystem. This subsystem provides the interface between the processors and the PCI bus, providing for a transfer rate of up to 132 MB/second and full concurrence between processor Host bus and PCI bus transactions. Five integral Write Posting and Read Prefetch buffers increase PCI Master add-in performance.

The PCMC/LBX Host-to-PCI bridge is designed to conform to the *PCI Local Bus Specification 2.0*, and guidelines in the *PCI System Design Guide*.

PCI/EISA BRIDGE (PCEB)

The baseboard has five dedicated and one shared 32-bit EISA I/O expansion slots. The 82375EB PCI-EISA Bridge (PCEB) and 82374EB EISA System Component (ESC) provide a bridge between the PCI local bus and the EISA bus. The PCEB has the following features:

- Address, data paths, and bus protocol translation for PCI-EISA transfers
- Extensive data buffering in both directions that increases system performance and allows concurrence between the PCI bus and EISA bus
- Bus parity checking and error reporting

The ESC provides support for an EISA-compatible I/O subsystem, including:

- EISA (master and slave) interface
- EISA bus controller and arbitration
- Enhanced 7-channel DMA controller with scatter/gather support
- 14-channel interrupt controller, five programmable timer/counters, and NMI logic.
- Support logic for Xbus buffer and devices, including chip selects for Flash BIOS, Real time Clock (RTC), NVRAM and keyboard/mouse controller.

INTERRUPT CONTROL ASIC (INCA) COMPONENT

The Interrupt Control ASIC (INCA) collects many functions into a single component to enhance functionality, reduce part count, and reduce system cost. The main functions include providing both PCI interrupt control and unique security and server management features.

The following INCA features are used on the ALTServer baseboard:

- Interrupt control:
- I/O Advanced Programmable Interrupt Controller (APIC)
- Serial port interrupt steering to any ISA interrupt
- IDE interrupt steering to any ISA interrupt
- PCI interrupt steering for the PCI auto-configuration
- Security and Server Monitoring features:
- Watchdog timer (software start/reset) will reset system if it expires
- Keyboard/mouse inactivity; if detected, blanks video and locks floppy, requires password to re-enable
- Baseboard voltage (12V, -12V, 5V, -5V, 3.3V) monitoring.
- Baseboard temperature monitoring for out of range
- Chassis door switch or improper entry monitoring
- PCI Clock generation - 14 PCI clock drivers
- General purpose I/O bits, used for 3-mode (720KB, 1.44MB, 2.88MB) floppy control, and other functions
- DMA steering for IDE and parallel port to one of four possible ISA DRQs/DACKs
- Support for front panel interface and LCD display

INTERRUPT HANDLING

This important element of the ALTServer design provides great flexibility in interrupt routing. Interrupt sources come from the PCI and EISA/ISA slots and onboard devices and need to be routed to either a single or dual processor. The following diagram illustrates the interrupt structure on the ALTServer Baseboard.

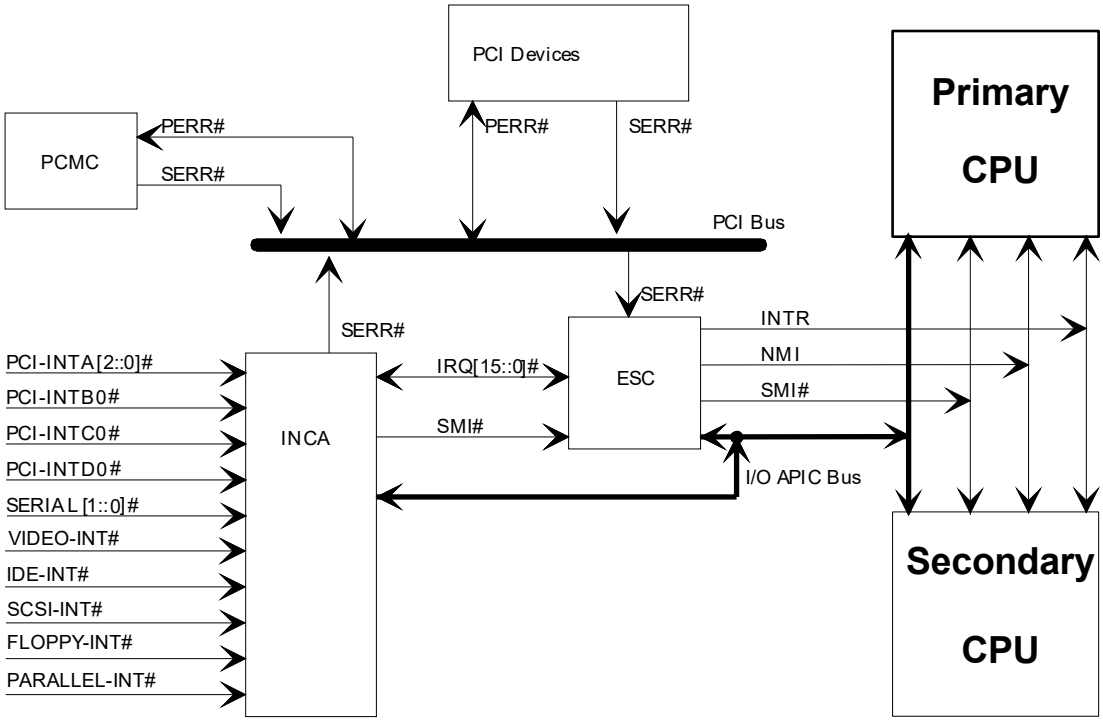


Figure 4. ALTServer interrupt structure

Dual Pentium Processor (SMP) Operation

In the dual processor configuration, the interrupt routing is performed by the Advanced Programmable Interrupt Controller (APIC) bus. Each processor has an on-chip local APIC device that can receive interrupts driven onto the APIC bus by I/O APIC devices. Both the INCA and 82374EB EISA System Component (ESC) incorporate I/O APICs that drive individual interrupts onto the APIC bus. All of the EISA/ISA interrupts are routed to the ESC component and all PCI interrupts are routed to the INCA component. This allows any external interrupt to be routed to the processor. For further details, refer to the operating system documentation and the Intel 82489 APIC data sheet.

Single Processor Operation

All EISA/ISA interrupts are routed to the ESC component and all PCI interrupts from onboard PCI devices and PCI slots are routed to the INCA component. Under software control, the PCI interrupts can be routed from the INCA inputs to any of the ESC interrupt inputs. This allows PCI interrupts to be 'patched' into the standard PC interrupt structure. This routing is done dynamically at power-on by the Plug and Play BIOS by examining each device, assigning an interrupt to it, and programming the INCA device accordingly.

ERROR INTERRUPTS

The traditional server platform will typically generate a Non-Maskable Interrupt (NMI) whenever a memory or bus error occurs. Traditional sources for an NMI are memory system parity error, EISA bus master time-out, or IOCHK#. The PCI bus adds two new sources of error detection which must be managed: PCI bus parity and PCI system error (SERR).

PCI bus parity is performed by the PCI source of the transaction which generates the bus parity while the destination checks it. If a parity error occurs (PERR# asserted one clock after the offending bus cycle), the current PCI bus master manages the error. The master may retry the transfer or may pulse SERR#. An asserted SERR# causes the ESC to generate an NMI. The PCMC manages the SERR# assertion for various conditions.

SYSTEM MANAGEMENT INTERRUPT (SMI) SUPPORT

The EISA System Component (ESC) has added an SMIin# (pin 185). This pin is under software control and if enabled, asserts SMI# to the Processor. SMI# is of higher priority than NMI or INTR to the Pentium Processor. Assertion of SMIin# causes an SMI# and the processor switches memory space and begins execution of the SMM handler. SMM creates a secure memory space that the processor can use for ALTServer fault management.

CRITICAL EVENT LOGGING

During POST, the BIOS will initialize the SMI RAM with code to log errors into non-volatile memory. Each processor will have a private area of SMI RAM dedicated to it for SMI processing. The INCA and PCEB/ESC will be programmed to generate SMI for memory errors, bus parity errors, PCI SERR and PERR, EISA bus time-outs, EISA software generated NMI, I/O channel check, and EISA watchdog time-out. When these errors are detected, the SMI routines will log the error or event, and then will cause an NMI to be generated, so that operating systems can respond appropriately.

If the OS is using the INCA watchdog timer to detect software or hardware failures, and that timer expires, an Asynchronous System Reset (ASR) will be generated, which is equivalent to a hard reset, except that the watchdog timer status will not be reset. The POST portion of the BIOS will detect this event as the system reboots, and will log this event to the logging area.

The System Management Log Area will be a minimum of 8192 bytes of non-volatile memory space. The format of the System Management Log Area will be based on the Xpress Server Management Critical Event Logging area format. The event logs will be a superset of the Xpress event logs. For more detail, please refer contact your Intel sales representative for the BIOS Extrernal Product Specification.

SECURITY AND SERVER MONITORING FEATURES

Incorporated into the ALTServer design are a number of features that enhance the reliability and security of the platform and meet the needs for high availability servers. Most of the hardware functionality is incorporated into the INCA device, which provides the following monitoring features:

- Watchdog timer (software start/reset) will reset system if it expires
- Keyboard/mouse inactivity; if detected, blanks video and locks floppy, requires password to re-enable
- Baseboard voltage (12V, -12V, 5V, -5V, 3.3V); if out of range, generates System Management Interrupt
- Baseboard temperature and chassis door switch monitoring for out of range or illegal entry

In addition the BIOS incorporates further security and monitoring functionality:

- Front panel push-button that disables keyboard and mouse input when activated
- User password - when specified must be entered to allow system boot
- Administrative password - when specified it must be entered to enter the System Configuration Utility (SCU) and change the configuration of the system
- Inactivity timer - if there is no keyboard or mouse activity within a specified time then the screen blanks and the User password must be entered to resume operation
- Hot key activation - allows the Inactivity timer to be activated by using a definable ‘Hot Key’ sequence

GRAPHICS SUBSYSTEM

The SVGA subsystem is based on the Cirrus Logic 5430 PCI graphics controller. The Cirrus 5430 supports backward software compatibility with MDA, CGA, Hercules Graphics, EGA, and VGA graphics standards.

The standard configuration includes 512 KB of graphics DRAM soldered on the ALTServer baseboard. Graphics memory can be upgraded to a total of 1 MB by adding a 256 KB x 16 fast page mode 70 ns DRAM to the SOIC socket on the baseboard. The upgrade will allow higher display resolutions and performance. The display RAM is paged into 128 KB of RAM located between A0000H and BFFFFh. The 15-pin VGA Connector appears on the I/O riser board. Graphics VRAM vendors and the VGA connector pinout is listed in the Appendix.

GRAPHICS DRIVERS AND UTILITIES

Graphics drivers and utilities for Windows 3.1, WIN-NT 3.1, MS-DOS software applications and OS/2 2.1 are shipped with the ALTServer platform. Additional drivers for other common applicationsmay be available from the Intel Applications Support BBS. Drivers for SCO* and Interactive UNIX* should be obtained from the respective UNIX vendor.

PCI SCSI INTERFACE

The ALTServer platform integrates an Adaptec AIC-7870 SCSI controller, which supports both narrow SCSI-2 (10 MB/s) and wide SCSI-2 (20 MB/s). The AIC-7870 supports processor-to-PCI and PCI-to-PCI transfers, with an embedded 8 MIPs processor and 256 byte FIFO. As a PCI bus master, the SCSI controller supports burst data transfer rates of up to 133 MB/second at a 66 MHz bus speed. Transfer rates are 120 MB/second at 60 MHz and 100 MB/second at 50 MHz bus speeds.

Although the board supports both narrow and wide devices, there is a limit to how many devices can be connected at one time and identified by the BIOS. The table below shows the allowed narrow/wide configurations:

Device ID	*Wide Devices*	*Narrow devices*
1-15	15	0
1-7	6	1
1-7	5	2
1-7	4	3
1-7	3	4
1-7	2	5
1-7	1	6
1-7	0	7

Table 3. Allowed narrow/wide SCSI configurations

PCI SCSI CONNECTORS

The baseboard contains a 50-pin Fast/Narrow SCSI-2 connector for narrow SCSI-2 peripherals such as disk drives, CD-ROMs, and tape drives that are installed within the system chassis. Signals for both narrow and wide SCSI interfaces are routed to the header for the I/O riser. A selection of I/O risers offers a variety of combinations of either narrow or wide SCSI connections.

For wide SCSI devices, I/O riser cards are available that provide either an internal or external SCSI connection. The internal I/O riser for wide SCSI has the connector on the opposite side of the video and serial port connectors. This allows wide SCSI cabling to wide SCSI disk drives mounted inside the system chassis. The external version is similar to the narrow SCSI riser and could be used, for example, to connect with an external disk drive unit.

SCSI TERMINATION

Termination for all SCSI devices attached to the ALTServer baseboard must be done manually. The baseboard design includes passive termination at one end of the SCSI channel and passive termination at the device. If any SCSI devices are connected to the bus, the passive terminators for that end of the chain must be removed. See the appendix for jumper locations, and the Board Level Features section on page 7 forterminator settings of various narrow/wide devices.

STANDARD I/O AND ADVANCED INTEGRATED PERIPHERAL (AIP) COMPONENT

The EISA bus on the ALTServer baseboard supports the Intel Advanced Integrated Peripheral (AIP) component for standard I/O devices. The AIP contains a floppy disk controller (FDC), two serial ports, a multi-function parallel port, an IDE interface, and a game port on a single chip. The high integration provides low-cost, low-power consumption, and minimal impact on board real estate. The FDC is an 82078 core with a data rate of up to 2 MB/second. The serial ports are 16550-compatible with 16-byte FIFOs. The parallel port supports the Enhanced Capabilities Port (ECP) protocol with DMA, EPP protocol, and IEEE-1284 protocol for PS/2 bi-directional compatibility. The IDE interface supports 8- or 16-bit I/O and 16-bit DMA. The AIP host interface is 8-bit ISA.

IDE INTERFACE

IDE is an interface for intelligent disk drives with onboard AT disk controller electronics. The 16-bit IDE interface consists of address decode (provided by the AIP), address, command, and data buffers, 40-pin connector, and 4-pin hard disk activity LED connector. The AIP selects the IDE device and enables the data buffers between the IDE cable and the bus. When IDE is disabled via the BIOS configuration utility, the I/O address space and interrupt (IRQ14) are available for use by add-in cards. The system BIOS may disable the interface when it finds the registers of another hard disk controller. When IDE DMA is enabled by the AIP and INCA, the IDE hard disk is then accessible through the DMA channel configured in the INCA. The standard I/O logic accommodates both compatible and Type F DMA cycles to IDE. AC timing constraints allow support for only Type 2 IDE drives in the CAM specification (or faster).

KEYBOARD AND MOUSE INTERFACE

An Intel 8242 surface mount microcontroller contains the AMI-based PS/2 compatible keyboard/mouse PE controller code. PS/2-style keyboard and mouse connectors are located on the I/O riser that connects at the back panel side of the baseboard. The 5V line on this connector is protected with a PolySwitch* circuit which acts much like a self-healing fuse, re-establishing the connection after an over-current condition is removed. While this device eliminates the possibility of having to replace a fuse, care should be taken to turn off the system power before installing or removing a keyboard.

The 8242 microcontroller code supports Power-On/Reset (POR) password protection. The POR password is set via the System Configuration Utility. The keyboard controller also provides for the following "hot key" sequences:

- CTRL-ALT-DEL: System software reset. This sequence performs a software reset of the system by jumping to the beginning of the BIOS code and running the POST operation.
- CTRL-ALT+ and CTRL-ALT-: Turbo mode selection. CTRL-ALT- sets the system for de-turbo mode and CTRL-ALT+ sets the system for turbo mode (normal operation). Changing the Turbo mode may be prohibited by an operating system or application software.
- HOT Key X (Immediate Secure): Disables mouse and keyboard immediately. It also disables the power down timer, but it does not place the system into a powered down state. This hot key will work only if a password is enabled in the BIOS.

DALLAS DS12887 REAL TIME CLOCK, CMOS RAM AND BATTERY

The Real Time Clock (RTC) is implemented using a Dallas DS1587 device. The DS1587 is accurate to within 13 minutes/year and requires no external support. The oscillator and battery are integrated into the device and the estimated life-span of the battery is 10 years. The RTC can be set via the System Configuration Utility (SCU). CMOS memory supports the standard 128-byte battery-backed RAM, fourteen bytes for clock and control registers, and 114 bytes of general purpose non-volatile CMOS RAM. All CMOS RAM is reserved for BIOS use. The CMOS RAM can be set to specific values or cleared to the system default values using the SCU. Also, the CMOS RAM values can be cleared to the system defaults by using a hardware jumper.

I/O RISER BOARD

I/O connectors appear on a riser, not on the ALTServer baseboard. This allows great flexibility in chassis design and external I/O connector types, whether the customer desires PS/2 style keyboard and mouse connectors or an AT-style DIN keyboard connector.

The I/O riser also can provide either a Wide or Narrow SCSI connection to the SCSI-2 controller on the baseboard. The SCSI connector may be on either side of the I/O Riser, allowing for cabling to external SCSI peripherals or

internal peripherals. The use of an internal Wide SCSI connector is appropriate because the baseboard itself provides only a Narrow SCSI connector.

A number of I/O riser options are available. The following diagram is an example of a riser that provides PS/2 style keyboard/mouse connectors and an external Narrow SCSI connector.

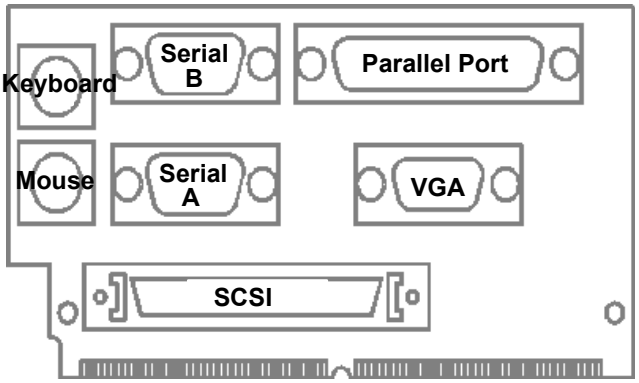


Figure 5. Example of I/O riser board

The I/O riser uses a 144-pin connector that is mechanically similar to a 72-bit SIMM module connector, but has 144-pins. The appendix details the pin-out of this connector.

SYSTEM BIOS

The ALTServer baseboard uses an American Megatrends Incorporated (AMI) ROM BIOS, which is stored in an Intel Flash memory device and can be easily upgraded using a floppy disk-based program. The baseboard has an Intel 28F004BX-T 4 Mb FLASH component organized as 512 KB (512kbit x 8). This Flash memory device contains the following software elements:

- The AMI BIOS code
- The System Configuration Utility (SCU)
- Power-On Self Tests (POST)
- Update recovery code
- On-board Video BIOS
- On-board SCSI BIOS
- The PCI auto-configuration utility
- ISA Plug-N-Play software

The BIOS displays a sign-on message during POST identifying the type of BIOS and a five-digit revision code. This ASCII string has the following format:

- **BIOSÿVersionÿx.yy.aa.pphvv**
- ÿ - indicates an ASCII space character.
- X - The major revision as assigned by AMI (1). If this is an Alpha or Beta BIOS, this number will be '0'.
- YY - The minor revision as assigned by Intel. The minor revision will be ZERO for all production and Alpha BIOS versions, and will be the level of Beta for all Beta BIOS versions.
- AA - The release level of the BIOS.
- PP - The product identifier ('AD')
- H - The hardware revision level. This starts at 0 for the first fab and is revised each time a hardware change is made that requires a BIOS change.
-

Information on BIOS functions can be found in the *IBM PS/2 and Personal Computer BIOS Technical Reference* published by IBM, and the *ISA and EISA Hi-Flex AMIBIOS Technical Reference* published by AMI. Both manuals are available at most technical bookstores.

FLASH IMPLEMENTATION

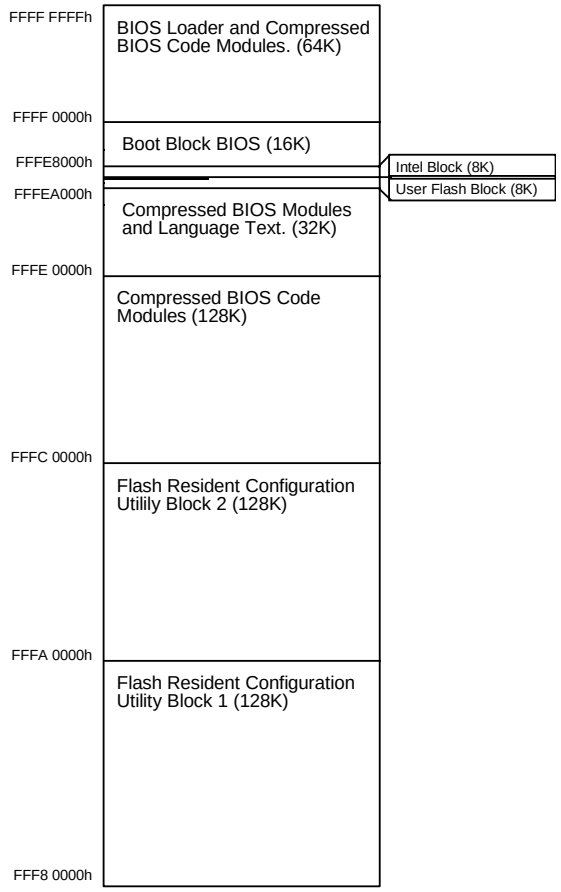


Figure 6. Flash memory implementation

SYSTEM CONFIGURATION UTILITY (SCU)

The System Configuration Utility (SCU) is stored in the BIOS FLASH ROM and is a combination of the functionality previously contained in the EISA Configuration Utility (ECU) and the BIOS Setup utility.

The SCU, system configuration (CFG), and overlay (OVL) files are compressed and stored in the system BIOS ROM. Up to 256 KB of ROM is available for storage of the SCU and CFG/OVL files. Any additional files are maintained on floppy disk in DOS format. The SCU is decompressed into RAM and executed during POST if the user elects to reconfigure the system. This is activated by the user when the F1 key is typed in response to the BIOS prompt.

The SCU conforms to the version 3.12 of the EISA standard and version 1.1 of the ISA Plug and Play Specification. It can be used with any compliant CFG or OVL files that are supplied by an add-in peripheral device manufacturer. The ALTServer platform contains the PCI overlay (OVL) and PCI configuration (CFG) files for the embedded controllers on the system baseboard.

The SCU modifies the ISA CMOS and EISA NVRAM, under direction of the user. The actual hardware configuration is accomplished by the BIOS Power-On-Self-Test routines and the ISA Plug and Play Auto Configuration Manager.

The appendix lists the features that may be configured with the SCU and the defaults as shipped.

POWER-ON SELF TESTS (POST)

The system BIOS performs a Power On Self Test (POST) to confirm the correct operation of the baseboard hardware. Error messages are displayed on the video screen after the video subsystem has been tested and initialized. Prior to video initialization, beep codes are used to inform the user of errors. The POST error codes are logged into NVRAM and the Extended BIOS data area, according to the IBM PS/2 standard and are displayed on the LCD display. Refer to the Appendix for POST error codes and messages, POST beep codes, and their definitions

UPDATE RECOVERY CODE

A Flash Memory Update (FMUP) Utility is supplied, allowing the system BIOS and the System Configuration Utility to be updated from a diskette and without the need to open the chassis or remove any hardware.

GRAPHICS AND SCSI BIOS

The System BIOS contains the video BIOS for the Cirrus PCI graphics subsystem and also the SCSI BIOS for the on-board Adaptec PCI SCSI subsystem.

THE PCI AUTO-CONFIGURATION UTILITY

The PCI auto-configuration utility operates in conjunction with the System Configuration Utility to allow the insertion and removal of PCI cards without user intervention. When the system is turned on after adding a PCI add-in card, the BIOS automatically configures interrupts, DMA channels, I/O space, and other parameters. The user does not have to configure jumpers or worry about potential resource conflicts. Since PCI cards use the same interrupt resources as ISA cards, the user must specify the interrupts used by ISA add-in cards in the BIOS configuration utility. The PCI Auto-Configuration function complies with version 2.0g of the PCI BIOS specification.

ISA PLUG & PLAY CAPABILITY

The BIOS will incorporate ISA Plug and Play capabilities as delivered by Intel Architecture Labs Plug and Play Release 1.2. This will allow auto-configuration of Plug and Play ISA cards, and of older non Plug and Play ISA cards.

System Level Features

CHASSIS

The ALTServer offers the expansion capabilities required by server applications with ten peripheral bays, expansion slots for up to seven add-in cards, a 230 watt power supply and an additional fan to cool a fully-loaded server configuration. Four of the peripheral bays (including the standard 3.5” floppy drive) can be accessed from the front of the chassis. The ALTServer also meets stringent environmental requirements.

PERIPHERAL BAYS

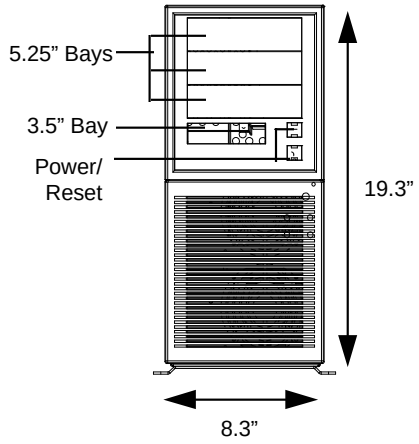


Figure 7. ALTServer front panel

Ten expansion bays are available for peripherals, including hard drives, tape drives, CD-ROMs, and other devices. These include three 5¼" half-height bays and one 3½" one-inch bay accessible from the front panel (filled in system configurations with a floppy drive). Six internal 3½" one-inch bays are located in a peripheral carrier than is hinged and swings out from the chassis for easy access and integration.

FAN

The ALTServer has two fans to keep the system cool. One fan within the power supply provides 28 cfm of air movement. The second fan, located at he chassis front, provides up 500lfmcacross the add-in cards and the processor. The second fan receives 12 Vdc directly from the baseboard.

EXPANSION SLOTS

The ALTServer has eight expansion card slots, all of which are intended for use with full-length cards. Five of the slots are dedicated for use with EISA or ISA cards and two of the slots are dedicated for use with PCI add-ins. One slot is shared by connectors for either an EISA/ISA or PCI card, but not both at the same time.

FRONT PANEL

The ALTServer front panel consists of a power switch, reset switch, a power-on LED and a hard disk access LED. Four peripheral bays also can be accessed from the front panel, as shown in Figure 7.

BACK PANEL

The back panel consists of access panels for the expansion slots (one location is unused), a 115/230 voltage switch, a power supply input, an auxiliary power output and the power supply fan. Access also is provided for any of the ALTServer riser boards, which provide connections to the baseboard I/O devices and interfaces, including the parallel port, serial ports, video, keyboard, mouse, and narrow or wide SCSI-2. The riser is available in several configurations, routing the SCSI signals to either external devices or into the chassis.

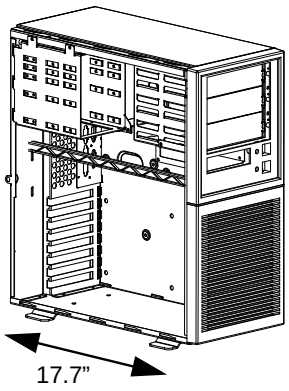


Figure 8. ALTServer angle view, showing slot locations and peripheral bays

POWER SUPPLY

The ALTServer integrates a 230 watt switchable power supply for all onboard resources, add-in cards, and peripherals. The Astec Corp. model SA230-3415 supports operating settings at 100-120 VAC (5 Amps AC) or 200-240 VAC (3 Amps AC). The input voltage is selected using a switch on the back of the system.

AC POWER INPUT SPECIFICATIONS

Input frequency 50/60 Hz	
AC Voltage	*Current*
90-135	5.0 A
	4.0 A

Table 4. Power Supply Input Specifications.

DC OUTPUT SPECIFICATIONS

DC Voltage	*Max. Current Load*	*Minimum Current Load*
+5V	30.0A	2.0A
-5V	0.5A	0A
+12V	8.0A	.25A
-12V	1.0A	0A

Table 5. Power Supply DC Output Specifications.

POWER CONSUMPTION

The following tables list the current and power consumed by system resources in a configuration which includes two Pentium processors and 8 SIMMs (two active and six standby). This information is preliminary and is provided as a guide for calculating approximate total system power usage with additional resources added.

CURRENT

DC Voltage	*Typical Current**	*Max. Continuous Current*
+5V	8.85 amps	15.75
-5V	Not required	Not required
+12V	38 milliamps	80 milliamps
-12V	18 milliamps	23 milliamps

Table 6. ALTServer current consumption (preliminary)

WATTS

Resource	*Max Power*	*Typical Power*
Two 90 MHz processors with 32 MB SIMMs, no add-in cards and no peripherals	80 Watts	45 Watts

Table 7. ALTServer wattage consumption (preliminary)

FLOPPY DRIVE

The ALTServer integrates a 3½" Teac Floppy drive Model FD-235HF into the external 3½" bay. This is the same proven floppy disk drive that has been used on many previous Intel systems.

SPEAKER

The standard system ships with an external speaker installed. The user may enable/disable the device using the System Configuration Utility or program the speaker via port 61H. The speaker provides error beep code information during POST if the system cannot use the video interface.

CHASSIS COLOR

The chassis color is beige. The bottom and back of the chassis are not painted.

Appendix A – User-Installable Upgrades

PROCESSORS

Single-processor ALTServer platforms can be upgraded by using a processor with a faster clock speed. The baseboard is designed to operate with 75 MHz, 90 MHz, 100 MHz or 120 MHz Pentium processors.

Dual-processor configurations must always have Pentium processors with the same clock installed in the two Zero Insertion Force (ZIF) sockets. Users also must observe the table below in matching the voltage regulation characteristics of the processors:

Primary	*Intel Part #*	*Secondary*
STD	**TBD**	**VRE or VR**
VRE	**TBD**	**VRE**
VR	**TBD**	**VR**

When upgrading processors, it is also important to ensure the CPU Speed and voltage jumpers are set properly. See the appendix for details.

SYSTEM MEMORY

Eight 72-pin sockets on the baseboard will accept up to 256 MB of system memory using 70 ns fast page SIMMs of the following sizes: 256K x 36 (1 MB), 512K x 36 (2 MB), 1M x 36 (4 MB), 2M x 36 (8 MB), 4M x 36 (16 MB), and 8M x 36 (32 MB) SIMMs. The minimum memory size is 2 MB and the maximum memory size, using eight 32 MB SIMMs, is 256 MB. Non-parity memory can be used by disabling parity checking with the SCU.

The eight SIMM sockets are arranged as four banks (Bank 0, 1, 2, and 3) with each bank consisting of two sockets. Both SIMMs in a bank must be of the same memory size and type, although separate banks may have different sizes and types of memory installed. In some instances, for electrical reasons only, it may be essential to populate Bank 0 first.

Because of the constant changes in the memory market, Intel engineering continually analyzes SIMMs by comparing information in the SIMM vendor's data book with the required timings on the ALTServer baseboard. Memory also is tested by either Intel or by respected OEM customers. A list of compatible/qualified SIMMs and those known to be incompatible is maintained on the Intel FaxBack* service (1-800-628-2283).

SECONDARY (L2) CACHE MEMORY

The ALTServer provides an upgradeable second level (L2) cache using Integrated Device Technology (IDT) or Corsair cache modules. Five cache upgrade options are available, as shown in the table below:

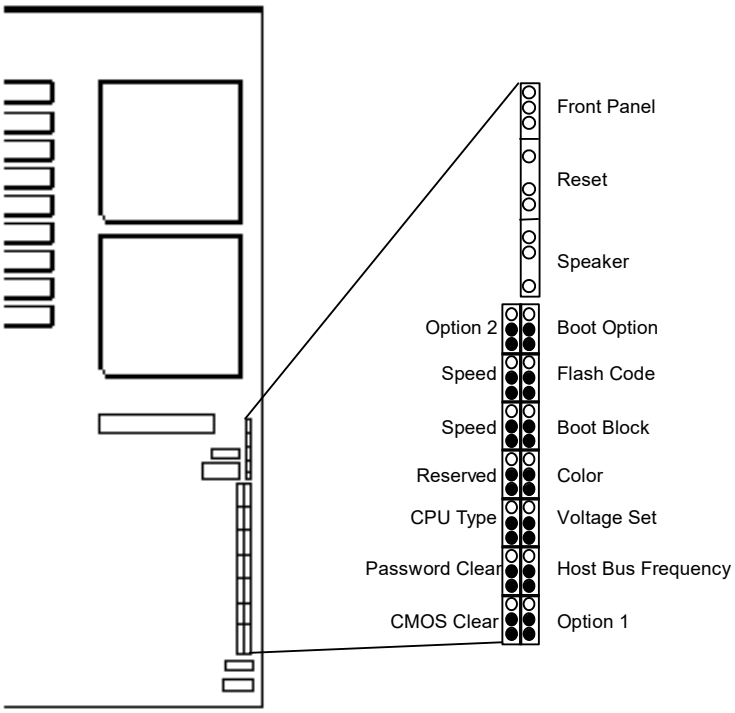
Cache SRAM Type	*Total Cache Size*	*Module*
None	0KB	None installed
Asynchronous	256KB	IDT7MP6189-15(ns)
Asynchronous	512KB	Corsair
Burst Synchronous	256KB	IDT7MP6181-9(ns)
Burst Synchronous	512KB	IDT7MP6182-9(ns)

GRAPHICS DRAM

Video DRAM memory can be upgraded using one 256K x 16, 60 ns, DIP component. While some DRAM parts rated at 70 ns will function in ALTServer platforms, Intel does not warrant the use of these 70 ns parts, or assume any liability concerning the use of these parts.

DRAM Size	*Vendor*	*DRAM Part #*
256K x 16	TBD	TBD

Appendix B – Jumpers



Purpose	*Location*	*Selection*	*Description*
CMOS Clear	J1B	*1-2, Protect 2-3, Clear	When set to 'Clear' the NVRAM settings will be set to their default values.
Option 1&2	J1A&J7B	*1-2, Option High 2-3, Option Low	Reserved for future feature enhancement options.
Host Bus Frequency	J2A	*1-2, Bus:Core=2:3 2-3,.Bus:Core=1:2	When set to 'Bus:Core=2:3", CPU sockets contain P54C Pentium Processors. If P54CS Processors are installed, this jumper must be set to 'Bus:Core=1:2'.
Password Clear	J2B	*1-2, Protect 2-3, Clear	When set to 'Clear' the password stored in CMOS will be cleared
Voltage Set	J3A	*1-2, VR 2-3, VRE	When set to 'VR', the primary socket contains a STD or VR Pentium Processor.
CPU Type	J3B	*1-2, CPU1=Primary 2-3, CPU2=Primary	When set to 'CPU1', the primary CPU is installed in ZIF socket U7H1
Color	J4A	*1-2, Color 2-3, Monochrome	When set to 'Color', the primary video display supports color graphics.
Reserved	J4B	*1-2, Disable & Ground 2-3, Enable Kick Start	Reserved for future feature enhancement options.
Boot Block	J5A	*1-2, Protect 2-3, Erase/Program	When set to 1-2, the FLASH BIOS region that contains the actual system booting code is protected and cannot be updated.
Speed	J5B J6B	*1-2, 60MHz 2-3, 66MHz (1-2), 50MHz *1-2, 60MHz 2-3, 66MHz (2-3), 50MHz	When set to 1-2, either the only CPU or both CPUs are 60/90 Mhz Pentium Processors. These jumpers select the speed of both CPUs and must always be adjusted as a set (J5B and J6B) and not individually.
Flash Code	J6A	*1-2, Erase/Program 2-3, Protected	When set to 2-3, the Flash BIOS is protected and cannot be updated. This setting also protects the BIOS setup and EISA configuration information and prevents the user from changing any system settings. Default jumper (1-2) allows the user to enter and modify selections in the System Config. Utility.
Boot Option	J7A	*1-2, Normal Boot 2-3, Recovery	When set to 'Normal Boot' the system will run from the normal section of the Flash BIOS. Move only when the Flash BIOS becomes corrupted and the

			system needs to boot from protected recovery BIOS section.

Appendix C – Connectors

I/O RISER BOARD

The following table shows the pinout of the I/O riser board connector on the motherboard, indicating corresponding I/O connector pins. This connector is similar to a standard 144-pin SIMM connector.

Pin	*I/O Connector Pin*	*Pin*	*I/O Connector Pin*	*Pin*	*I/O Connector Pin*	*Pin*	*I/O Connector Pin*
1	Mouse 4	37	SCSI 48	73	SCSI 68	109	SCSI 39
2	Mouse 1	38	SCSI 47	74	SCSI 67	110	SCSI 38
3	Mouse 5	39	SCSI 46	75	SCSI 66	111	SCSI 37
4	Keyboard 4	40	SCSI 45	76	SCSI 65	112	SCSI 36
5	Keyboard 1	41	Video 15	77	SCSI 64	113	SCSI 35
6	Keyboard 5	42	Ground	78	Ground	114	Ground
7	Serial Port A 4	43	Video 14	79	Ground	115	Ground
8	Serial Port A 3	44	Video 13	80	Ground	116	Ground
9	Serial Port A 2	45	Ground	81	Ground	117	Ground
10	Serial Port A 1	46	Video 12	82	Ground	118	Ground
11	Serial Port A 6	47	Video 11	83	Ground	119	Ground
12	Serial Port A 7	48	Video 1	84	Ground	120	Ground
13	Serial Port A 8	49	Video 2	85	Ground	121	Ground
14	Serial Port A 9	50	Video 3	86	Ground	122	Ground
15	Serial Port B 4	51	Ground	87	Ground	123	Ground
16	Serial Port B 3	52	Video 4	88	Ground	124	Ground
17	Serial Port B 2	53	Parallel Port 13	89	Ground	125	Ground
18	Serial Port B 1	54	Parallel Port 12	90	Ground	126	Ground
19	Serial Port B 6	55	Parallel Port 11	91	Ground	127	Ground
20	Serial Port B 7	56	Ground	92	Ground	128	Ground
21	Serial Port B 8	57	Parallel Port 10	93	Ground	129	Ground
22	Serial Port B 9	58	Ground	94	Ground	130	Ground
23	SCSI 17	59	Parallel Port 9	95	Ground	131	Ground
24	SCSI 18	60	Parallel Port 8	96	Ground	132	Ground
25	SCSI 19	61	Parallel Port 7	97	Ground	133	Ground
26	SCSI 63	62	Parallel Port 6	98	Ground	134	Ground
27	SCSI 62	63	Parallel Port 5	99	Ground	135	Ground
28	SCSI 61	64	Parallel Port 17	100	Ground	136	Ground
29	SCSI 60	65	Parallel Port 4	101	Ground	137	Ground
30	SCSI 59	66	Parallel Port 16	102	Ground	138	Ground
31	SCSI 58	67	Parallel Port 3	103	Ground	139	Ground
32	SCSI 57	68	Parallel Port 15	104	SCSI 44	140	Ground
33	SCSI 55	69	Parallel Port 2	105	SCSI 43	141	Ground
34	SCSI 53	70	Parallel Port 14	106	SCSI 42	142	Ground
35	SCSI 52	71	Ground	107	SCSI 41	143	Ground
36	SCSI 51	72	Parallel Port 1	108	SCSI 40	144	Ground

PS/2 STYLE MOUSE/KEYBOARD

The keyboard and mouse connectors are mounted on the I/O riser board. The mouse connector is normally stacked over the keyboard connector. I/O riser connector pin numbers are shown in parentheses.

Pin	*Keyboard Signal*	*Description*
1 (5)	KEYDAT	Keyboard Data
2	(NC)	Not connected
3	GND	Ground
4 (4)	FUSED_VCC	Supply voltage (via fuse, shared by mouse connector)
5 (6)	KEYCLK	Keyboard Clock
6	(NC)	Not connected

The mouse connector is PS/2 compatible, with pinout shown below:

1 (2)	MSEDAT	Mouse Data
2	(NC)	Not connected
3	GND	Ground
4 (1)	FUSED_VCC	Supply voltage
5 (3)	MSECLK	Mouse Clock
6	(NC)	Not connected

SERIAL PORTS

Two 9-pin connectors are provided on the I/O riser board for Serial ports A and B. By default, port A is the top connector. Each port can be set to one of four different COMx ports (refer to the I/O address map), and can be enabled separately. When enabled, each port can be programmed to generate edge or level sensitive interrupts. When disabled, serial port interrupts are available to add-in cards. I/O riser connector pins for ports A and B respectively, are shown in parentheses.

Pin	*Name*	*Description*
1 (7, 18)	DCD	Data Carrier Detected
2 (8, 17)	RXD	Receive Data
3 (9, 16)	TXD	Transmit Data
4 (10, 15)	DTR	Data Terminal Ready
5	GND	Ground
6 (11, 19)	DSR	Data Set Ready
7 (12, 20)	RTS	Return to Send
8 (13, 21)	CTS	Clear to Send
9 (14, 22)	RIA	Ring Indication Active

PARALLEL PORT

The AIP provides one PS/2-compatible, 25-pin bi-directional parallel port. BIOS programming of the AIP configuration registers enable the port, and determine the port address and interrupt. When disabled, the interrupt is available to add-in cards. The parallel port connector appears on the I/O riser board (pins shown in parentheses):

Pin	*Name*	*Pin*	*Name*
1 (72)	STROBE#	14 (70)	AUFDXT#
2 (69)	D0	15 (68)	ERROR#
3 (67)	D1	16 (66)	INIT#
4 (65)	D2	17 (64)	SLCTIN#
5 (63)	D3	18	GND
6 (62)	D4	19	GND
7 (61)	D5	20	GND
8 (60)	D6	21	GND
9 (59)	D7	22	GND
10 (57)	ACK#	23	GND
11 (55)	BUSY	24	GND
12 (54)	PE	25	GND
13 (53)	SLCT		

GRAPHICS MONITOR PORT

Pin	*Signal*	*Pin*	*Signal*
1 (48)	RED	9	GND
2 (49)	GREEN	10	GND
3 (50)	BLUE	11 (47)	Pull-up
4 (52)	Pull-up	12 (46)	Pull-up
5	GND	13 (44)	HSYNC
6	GND	14 (43)	VSYNC
7	GND	15 (41)	Pull-up
8	GND		

FRONT PANEL AND LCD DISPLAY

The INCA component drives a front panel interface and LCD display. Additional required circuitry consists primarily of two ICs and one 34-pin connector. The electrical interface on the ALTServer is compatible with the Sharp P/N LM16X21A (Intel P/N 201508-001) LCD Display. For complete information, refer to the data sheet for the Sharp component. The connector is for a 34-pin ribbon cable that connects to a distribution board for LEDs, key lock assembly and LCD display, with pinout shown below:

Pin	*Signal*	*Function*
1	SPKDAT	Speaker DATA
2	+5V	
3	+5V STANDBY	
4	PS-ON	Power Supply on status
5	FP-RESET#	Front Panel Reset
6	0V	
7	N/C	
8	0V	
9	HD1 LED VCC	Internal Controller Drive LED
10	HD1 LED RTN	Internal Controller Drive LED RETURN
11	HD2 LED RTN	ADD-IN Controller Drive LED RETURN
12	HD2 LED VCC	ADD-IN Controller Drive LED
13	KEYBD KEYLOCK#	Front Panel Keylock Switch
14	0V	
15	SECURE MODE	Secure Mode Status from Main Board
16	CHASSIS SWT	Chassis Door Switch
17	KEY	
18	+5V	
19	I2C-SDA	I2C Serial Data
20	CHASSIS SWT RET	Chassis Door Switch Return
21	LCD-SD	LCD Serial Data
22	KS#	Kick Start RTC
23	LCD-SCLK	LCD Serial Clock
24	I2C-SCL	I2C Clock
25	LCD-PCLK	LCD Parallel Clock
26	0V	
27	EN	Reserved
28	0V	
29	RW	LCD READ/WRITE
30	N/C	
31	RS	Reserved
32	PWR#	Shut Down Power
33	LCD-VDD	LCD Voltage
34	0V	

PRIMARY POWER

The ALTServer uses a 12-pin standard AT power supply connector with the following pinout:

Pin	*Signal*	*Pin*	*Signal*
1	PWRGOOD	7	GND
2	+5V	8	GND
3	+12V	9	-5V
4	-12V	10	+5V
5	GND	11	+5V
6	GND	12	+5V

12V FAN POWER

There are two fan connectors, both appropriately located for the placement of a fan. The connectors are 3-pin, single in-line, .025 in. square pin with the following pinout:

Pin	*Signal*
1	Fan Rotation Sense
2	+12V
3	GND

IDE INTERFACE

The 40 pin IDE connector is located on the baseboard. The IDE interface does not support the Enhanced IDE (E-IDE) specification so the maximum number of disk drives that may be connected is two.

Pin	Function	Pin	Function
1	IDERST*	21	IDEDRQ
2	GND	22	GND
3	ID7	23	IDEIOW*
4	ID8	24	GND
5	ID6	25	IDEIOR*
6	ID9	26	GND
7	ID5	27	CHRDY
8	ID10	28	SPSYNC
9	ID4	29	IDEDAK*
10	ID11	30	GND
11	ID3	31	IDEIRQ14
12	ID12	32	IDEIO16*
13	ID2	33	IDESA1
14	ID13	34	PDIAG*
15	ID1	35	IDESA0
16	ID14	36	IDESA2
17	ID0	37	IDECS0*
18	ID15	38	IDECS1*
19	GND	39	IDEHDACT*/DRVPRES*
20	Keyed	40	GND

PCI CONNECTORS

Following is a summary of PCI signal pins, including the signal mnemonic, electrical type, full name, and brief description. The electrical types are as follows:

Type	*Description*
in	Input is a standard input-only signal.
out	Totem Pole Output is a standard active driver.
t/s	Tri-State is a bi-directional, tri-state input/output pin.
s/t/s	Sustained Tri-State is an active low tri-state signal owned and driven by one and only one agent at a time, subject to specific timing restrictions.
o/d	Open Drain allows multiple devices to share signals as a wired-OR.

Signal(s)	*Type*	*Name and Description*
AD[31::00]	t/s	Address and Data are multiplexed; during the first clock of a transaction (address phase) they contain a 32-bit physical address; during subsequent clocks, data. As address bits, AD0 and AD1 have no significance; instead, they are encoded to indicate the burst type.
C/BE[3::0]#	t/s	Bus Command and Byte Enable are multiplexed; during the address phase of a transaction, they define the bus command; during the data phase they determine which byte lanes carry valid data.
DEVSEL#	s/t/s	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, it indicates whether any device on the bus has been selected.
FRAME#	s/t/s	Cycle Frame is driven by the current master to indicate the beginning and duration of an access.
GNT#	in	Grant indicates to the agent that the arbiter has granted access to the bus. This is a point to point signal. Every master has its own GNT#.
IDSEL	in	Initialization Device Select is used as a chip select instead of the upper 24 address lines during configuration read and write transactions.
IRDY#	s/t/s	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. During a write, IRDY# indicates that valid data is present. During a read, it indicates the master is prepared to accept data.
INT[A-D]#	o/d	Interrupts are defined as “level sensitive” and asserted low using open drain output drivers. The assertion and deassertion of INT[A-D]# lines is asynchronous to CLK.
LOCK#	s/t/s	Lock indicates an atomic operation that may require multiple transactions to complete.
PAR	t/s	Indicates even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents.
PERR#	s/t/s	Parity Error reports a data parity error on all commands except Special Cycle.
PRSNT1# PRSNT2#	in	Present Lines indicate the presence of a PCI add-in board in the connector, and the power requirements of the add-in board.
REQ#	out	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ#.
RST#	in	Reset forces the PCI sequencer of each device to a known state.
SBO#	in/out	Snoop Backoff indicates whether the current memory access may proceed or is required to be retried.
SDONE	in/out	Snoop Done indicates the status of the snoop for the current cache access.
SERR#	o/d	System Error reports address parity errors, data parity errors on Special Cycle commands, or any other system error where the result will be catastrophic.
STOP#	s/t/s	Stop indicates the current target is requesting the Master to stop the current transaction.
TCK	in	Test Clock clocks state information and data into and out of the device during boundary scan. All of the test related pins conform to the Test Access Port (TAP) and Boundary Scan Architecture defined by IEEE Standard 1149.1
TDI	in	Test Input shifts data and instructions into the TAP in a serial manner.
TDO	out	Test Output shifts data out of the device. If an add-in card does not implement a TAP, TDI and TDO should be tied together.
TMS	in	Test Mode Select controls the state of the TAP controller.
TRDY#	s/t/s	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. During a read TRDY# indicates that valid data is present. During a write it indicates the target is prepared to accept data.
TRST#	in	Test Reset is used to force the TAP controller into a test logic reset state.

EISA BUS SIGNALS

Following is a summary of EISA signal pins, including the signal mnemonic, name, and brief description. A “bus master” can be either the PCEB, or EISA expansion board with master capability.

Signal(s)	*Name and Description*
AENx	Address Enable for slot x (x = 1 to 6). When asserted, an I/O slave in the slot responds to addresses and I/O commands
BALE	Bus Address Latch Enable. When asserted, indicates a valid address on LA[31::24]# and LA[23::2].
BCLK	Bus Clock. Synchronizes events on the EISA bus (at 8.33 MHz nominal).
BE[3::0]#	Byte Enables identify specific bytes in a Dword. Combinations determine which byte lane carries valid data.
CHRDY	Channel Ready. Driven low (never high) by a memory or I/O slave to lengthen the current bus cycle by an integral number of BCLK ticks.
CMD#	Provides timing control within a cycle.
D[15::8]	Third-highest-order 8-bits of 32-bit data bus (byte lane 1) on EISA connector.
D[23::16]	Second-highest-order 8-bits of 32-bit data bus (byte lane 2) on EISA connector.
D[31::24]	High-order 8-bits of 32-bit data bus (byte lane 3) on EISA connector.
D[7::0]	Low-order 8-bits of 32-bit data bus (byte lane 0) on EISA connector.
DAK[7::0]#	DMA Acknowledge lines.
DRQ[7::0]	DMA Request lines.
EX16#	Asserted by slaves to indicate support of 16-bit transfers only.
EX32#	Asserted by slaves to indicate support of 32-bit transfers.
EXRDY	Negated by slaves to request wait states (wait state = 1 BCLK tick).
IO16#	16-bit I/O Capable. Indicates that this is a 16-bit I/O slave.
IOCHK#	Signals a serious error.
IORC#	I/O Read Command. Asserted by the bus master to indicate that the I/O slave may drive data (qualified by AENx).
IOWC#	I/O Write Command. Asserted by the bus master to indicate valid data for an I/O slave (qualified by AENx).
IRQ[15::14], IRQ[12::9], IRQ[7::3]	Interrupt request lines.
LA[23::2]	Portion of the Latchable Address bus seen by all devices (16- and 32-bit).
LA[31::24]#	High-byte of the Latchable Address bus, wired to 32-bit portion of connector only. The latchable address is pipelined from one bus cycle to the next.
LOCK#	Guarantees exclusive access to memory or I/O cycles for the bus master asserting this signal.
M/IO#	Memory or I/O. Indicates the current cycle type that the bus master is using.
M16#	16-bit Memory Capable. Only ISA memory slaves generate this signal.
MAKx	Master Bus Acknowledge. Asserted by system board to grant bus access to requesting EISA master (x = slot number).
MASTER16#	16-bit EISA master indicator.
MRDC#	Master Memory Read Command. When asserted by bus master, indicates the addressed memory slave may drive data.
MREQx#	Master Bus Request. Asserted by EISA masters until sys. board responds with MAKx# (x = slot) to obtain access to bus.
MSBURST#	Master Burst. Indicates to an EISA slave that the bus master is capable of burst cycles.
MWTC#	Master Memory Write Command. When asserted by bus master, indicates the addressed memory slave may latch data.
NOWS#	No Wait State. An ISA slave asserts NOWS# to indicate that no more clock cycles are required to complete this transaction. An EISA asserts NOWS# to generate compressed cycles (1.5 BCLKs/cycle).
OSC	14.31818 MHz clock for timer loops.
REFRESH#	When asserted, indicates that a memory refresh cycle is in progress.
RESDRV	When asserted, causes a hard reset of ISA and EISA expansion boards.
SA[19::0]	Low-order 20-bits of the 32-bit address, valid throughout the entire bus command cycle.
SBHE#	System Bus High Enable. When asserted, indicates the 16-bit expansion board should drive data on high half of D[15::0]
SLBURST#	Slave Burst. Asserted by slaves that support burst cycles.
SMRDC#	System Memory Read Command. . When asserted by the system board, indicates that the addressed memory slave may drive data. Only asserted during ISA read accesses from 00000000H through 000FFFFFH.
SMWTC#	System Memory Write Command. When asserted by the system board, indicates that the addressed memory slave may latch data. Only asserted during ISA write accesses to 00000000H through 000FFFFFH.
START#	Provides timing control for the bus master at the start of a cycle.
TC	Terminal Count. As an output, indicates that the DMA word count rolls over from 0 to FFFFFFH. As an input, indicates that the DMA slave wants to terminate the transfer.

W/R#	When high, indicates a write cycle; when low a read.

Appendix D – System Configuration Utility

The System Configuration Utility (SCU) and system CFG/OVL files will be compressed and stored in the system BIOS ROM. Up to 256 KB of ROM is available for storage of the CU and CFG/OVL files. Any additional files will be maintained on floppy disk in DOS format. The CU will be decompressed into RAM and executed during POST if the user elects to re configure the system. This will be activated by the user when the F1 key is typed in response to the BIOS prompt.

The CU modifies the ISA CMOS RAM and EISA non-volatile RAM, under direction of the user. The actual hardware configuration is accomplished by the BIOS Power-On-Self-Test routines and the ISA Plug-N-Play Auto Configuration Manager.

The CU always updates a checksum for both areas, so that any potential data corruption will be detectable by the BIOS, before the actual hardware configuration takes place. If the data has been corrupted, the BIOS will request that the user configure the system, before the system is booted.

SCU-CONFIGURABLE FEATURES (Default values are in **bold type**)

Configuration Feature	*Selection Options*	*Notes*
System ID String	None	Configured by the User or System Integrator, using the ROM-based or disk-based configuration utility.
Display Processor Type(s) and Max. Speed and Failed Status	N/A	Display only
Power-On Speed	**Fast** / Slow	BIOS programs the SLOWH timer before boot.
Cache control	Disabled / **Enabled**	BIOS will enable cache before booting OS.
Display BIOS version string	N/A	Display only
Display CFG and OVL versions	N/A	Display only
Video Subsystem		
Video	N/A	Auto configured, see text.
Memory Subsystem		
Base Memory	512 / **640** KB	
Total Memory		Display only.
Automatic Memory Resizing	**Enable** / Disable	
Skip Memory Test	Enable/ **Disable**	
Memory 15M-16M	**Enable**/Disable	
	Floppy Subsystem	
Floppy Autodetect	**Enable** / Disable	
Floppy Drive Type	*Auto / 360 / 1.2 / **1.44**	
IDE Subsystem		
Onboard IDE Controller	**Auto** / Disable	
Number of Hard Disks supported.	**Not user selectable, always 4**	
IDE Auto configuration	**Auto** / Custom	
SCSI Subsystem		
SCSI Controller	**Enable** / Disable	
SCSI BIOS Shadow	**None**	Must be shadowed, **not user selectable.**
SCSI Channel Selection	**Internal** / External	
SCSI Boot Selection	**SCSI-A** / SCSI-B	
KB/Mouse Subsystem		
NumLock State at Boot	On / **Off**	
Typematic Speed	Slow / Medium / **Fast**	
Mouse	Auto detected	**Using AMI Keyboard Controller**
Serial Subsystem		
Serial Port Address	220h, 228h, 238h, 2E8h, **2F8h**, 338h, 3E8h, **3F8h**	Serial-A = COM1(3F8), Serial-B = COM2 (2F8)
Serial Port IRQ	**3** or **4**	Serial-A=IRQ 4, Serial-B=IRQ 3
Select Serial Port Redirection	**Disable**/ port 1/ port 2	2 ports
Serial Port Baud Rate	19.2Kb/ 9600b/ 2400b	

Serial Port Terminal Type	VT100 / IBM-PC ANSI	

SCU-CONFIGURABLE FEATURES (Continued / Default values are in **bold type**)

Parallel Subsystem		
Parallel Port Address	**378h**, 278h, 3BCh	1 port
Parallel Port IRQ	5 or **7**	1 port
Parallel Port Mode	**ISA-compatible**, PS/2, EPP/ECP	
Security Subsystem		
Administrative Password	Set/**Not Set**	
User Password	Set/**Not Set**	
Keyboard Pushbutton Lock	N/A	Enable security only if either user or administration password is enabled.
Keyboard Lockout Timer	Timeout, 1-127 (**10 min),** Disabled	
Network Server Mode	Enable / **Disable**	
Video Blanking	Enable / **Disable**	
Reset Button and Power Switch Locking	**Enable** / Disable	
Floppy Boot	**A: then C:**, C: then A:, C: only, A: only	
Floppy Writes	**Enable** / Disable	
Secure Mode Hot-Key	Ctrl-Alt-*key* or **None**	Ctrl-Alt-*Key* enters secure mode immediately.
Boot Without Keyboard	N/A	No error message will be displayed.
CMOS Lock Switch	N/A	Not supported in HW. See 'Admin Password'
LCD Display		
LCD	**Enable** / Disable	
LCD Display String After Boot	(user defined string or default)	**Default** is "**N x PID Speed System Ready** " where **N** = number of processors, **PID** is processor ID string, and **Speed** is the processor in MHz.
Management Subsystem		
+5 V Upper Warning Level	0.02 - 5.4 V in 0.02 V steps	**5.26V** default
+5 V Lower Warning Level	0.02 - 5.4 V in 0.02 V steps	**4.76V** default
+5 V Upper Critical Level	0.02 - 5.4 V in 0.02 V steps	**5.4V** default
+5 V Lower Critical Level	0.02 - 5.4 V in 0.02 V steps	**4.6V** default
+12 V Upper Warning Level	0.1 - 14.9 V in 0.1 V steps	**12.6 V** default
+12 V Lower Warning Level	0.1 - 14.9 V in 0.1 V steps	**11.4 V** default
+12 V Upper Critical Level	0.1 - 14.9 V in 0.1 V steps	**12.96 V** default
+12 V Lower Critical Level	0.1 - 14.9 V in 0.1 V steps	**11.04 V** default
+3.3 V Upper Warning Level	0.02 - 3.74 V in 0.02 V steps	**3.62 V** default
+3.3 V Lower Warning Level	0.02 - 3.74 V in 0.02 V steps	**3.14 V** default
+3.3 V Upper Critical Level	0.02 - 3.74 V in 0.02 V steps	**3.72 V** default
+3.3 V Lower Critical Level	0.02 - 3.74 V in 0.02 V steps	**2.96 V** default
-12 V Upper Warning Level	-16.7 to -5.9V in .1V steps	**-11.4 V** default
-12 V Lower Warning Level	-16.7 to -5.9V in .1V steps	**-12.6 V** default
-12 V Upper Critical Level	-16.7 to -5.9V in .1V steps	**-11.0 V** default
-12 V Lower Critical Level	-16.7 to -5.9V in .1V steps	**-13.0 V** default
Temp. Probe #1 Upper Warning Level	0 °C to 200 °C in 2 °C steps	TBD
Temp. Probe #1 Lower Warning Level	0 °C to 200 °C in 2 °C steps	0
Temp. Probe #1 Upper Critical Level	0 °C to 200 °C in 2 °C steps	TBD
Temp. Probe #1 Lower Critical Level	0 °C to 200 °C in 2 °C steps	0
Temp. Probe #2 Upper Warning Level	0 °C to 200 °C in 2 °C steps	TBD
Temp. Probe #2 Lower Warning Level	0 °C to 200 °C in 2 °C steps	0
Temp. Probe #2 Upper Critical Level	0 °C to 200 °C in 2 °C steps	TBD
Temp. Probe #2 Lower Critical Level	0 °C to 200 °C in 2 °C steps	0
Event Logging	**Enable** / Disable	Controls onboard event logging.

Appendix E – AMIBIOS Messages and Beep Codes

ERROR MESSAGES

BEEP CODES

The BIOS indicates failures with beep codes prior to the initialisation of the video adapter. The beep code is a series of individual beeps, each equal in length. The following table describes the error conditions associated with each beep code:

Beep Count	*Error Condition*
1	Refresh failure
2	Parity can't be reset
3	First 64KBmemory failure
4	Timer not operational
5	Processor failure
6	8042 gate a20 is off (v_mode)
7	Exception interrupt error
8	Display memory r/w error
9	ROM checksum error
10	Shutdown reg. r/w error

POST CODES AND COUNTDOWN CODES

The BIOS indicates the current stage of the Power-On Self Test (POST) after the video adapter has been successfully initialized. A two-digit hex code is sent to I/O location 80h. This code can be shown on an LED display if a Port 80h card is installed. The current countdown code will also be displayed on the LCD panel, once it is initialized.

CODES DISPLAYED DURING RECOVERY BOOT PROCESS

The following table contains the Port 80 codes and the POST countdown codes displayed during the recovery boot process. This process is enabled by moving the Flash jumper from the position marked *Boot* to the opposite position, and cold-booting the system. During this process the floppy disk in drive A is booted and a BIOS image is automatically installed.

CP	*YY*	*Reason*
02h		Disable internal cache
08h		Disable DMA controller #1, #2, disable interrupt cntlr #1, #2, reset video display.
13h		Init all chipset registers (Enable LCD display here)
*15h	900	Initialise system timer
*1Bh	800	Real mode base 64k test
*20h	700	16k base ram test
*23h	650	SDetup interrupt vectors
*40h	600	Test memory in virtual mode.
*65h	500	Initialise 8237 dma cntlr
*67h	400	8259 interrupt cntlr test
*80h	300	Unmask diskette, kb and timer interrupts
*88h	200	Floppy unit initialisation
*A0h	100	Cache enable
*00h	000	Boot OS.

CP= AMIBIOS check point (Port 80) code; YY= ALTServer BIOS countdown code

CODES DISPLAYED DURING NORMAL BOOT PROCESS

CP	*XX*	*Reason*
D0h		Returned from ResetInit
D1h		PowerOnInit
D2h		Return from PowerOnInit
D3h		SoftResetEntryPoint:
D4h		Test to see if we are in Protected mode (entered from POST.BIN not
D5h		Checksum only the LOADER.BIN
D6h		Loader.bin checksum good. (Enable LCD in InitBeforeKBCInit)
*D7h	900	Issue BAT command to KBD controller.
D8h		After waitForEmptyBuffer
D9h		After Empty8042InputBufferX
DAh		After Retrieve8042OutputBufferX
DBh	820	Keyboard Init Passed
DDh		After initAfterKBCInitEnd
DFh		2nd Empty8042InputBufferX
*E0h	780	Initialize Master/Slave PICs
E1h		Before ChipsetInitEnd (before chip set initialization ends)
E2h		After ChipsetInitEnd (after chip set initialization ends)
*E3h	760	Initialize timer channel 0 for system timer.
E4h		Before beginning memory test need to clear any pending parity errors.
E6h	740	Test RAM from 0-640KB
E7h		GetMinPartitionSizeX(get minimum partition size)
E8h		RAM failure, call RemapMemoryPartitionX(memory failure)
E9h		RAM test complete, passed.
EBh	730	Set up stack at 30:100
EBh		BIOS just shadowed
ECh		Make F000h DRAM R/W Enabled
EDh		Dispatch POST
*23h	700	Setup interrupt vectors
24h		Just after call to SetPostEnvironment(after a call to setup the POST environment)
0Dh		CustomCheckManufacturingMode and CheckDefaultJumper
0Eh	690	Check validity of CMOS
0Fh		Force CMOS defaults
10h		CMOS init complete
25h		After Initialize CMOS pointers in EBDA
*F0h	600	EISA slot initialization
F1h		Enable extended NMI sources
F2h		Test extended NMI sources
28h		Set monochrome mode
29h		Set color display
2Ah		Clear parity status if any
2Bh		Call ChipsetBeforeVideoInit
2Ch	580	Video option ROM search
2Dh		Call CustomAfterVideoInit (calls custom code aftyer video has initialized)
2Eh	570	After video init
2Fh	560	After mono display setup
30h		Before check for vertical retrace
31h		Test for color display memory
32h		Check for vertical retrace
34h		Video card detected
35h	520	Initialize Console Redirection
36h		InitializeMessagingServices and ClearScreen
37h	500	CustomDisplaySignon
F3h		EISA ErrorDisplay
80h	370	KB/mouse port check
81h		Keyboard error determination.
82h		Enable Keyboard Interrupts and initialize keyboard circular buffer
83h		Check if keyboard is locked
F5h	330	Initialize mouse
39h		CustomUpdateScreenPointers,CustomDisplaySetupMessage,CustomDisplayKeyboardSignon,CustomDisplayMouseSignon
3Bh		Jumps to 'StartMemoryTesting' in next module.
43h	290	call GetMinPartitionSizeX
4Fh		call DisableEnhancedPost
52h		call ChipsetAdjustMemorySize
*61h	250	DMA register tests
62h		DMA test OK
64h		DMA controller latch test
65h		Initialize 8237 DMA controller
66h		clear DMA write request reg and mask set/ reset reg
*67h	220	8259 Interrupt cntlr test
F4h		Enable extended NMI sources
8Ch	140	Chipset@Devinit and ConfigurePeripheralController
8Fh	130	Floppy Initialization
91h	120	HD initialization
92h		Set printer, rs-232 time out
96h		Before Option ROM scan
97h	080	Option ROM scan C800h-E000h
98h		After Option Rom scan
9Ah		Soft reset (1234) --> (1200)
9Dh	070	Timer data area initialization
A0h		Printer setup
A1h		RS_232 setup
A2h		After KB circular buffer set up
ABh		Before NPX test and init
*ACh	060	NPX test and init
ADh		Update coProcessor info in cmos and recalculate checksum
AEh		Set typematic rate
*AFh	050	KBD read ID command
B0h		Wait for READ ID response
A3h		Display POST errors
A6h		Before Setup
*A7h	030	Call Setup

B1h		Enable Cache for boot
B3h		Setup display mode set
B4H		Jmp preos.asm (jump to program outside)
BBh	020	Start of PreOS
00h	000	Execute BOOT

Appendix F – BIOS Upgrades & Recovery

The ALTServer incorporates the AMIBIOS in a Flash memory component. Flash BIOS allows easy upgrades without the need to replace an EPROM. The upgrade utility fits on a floppy diskette and provides the capability to save, verify, and update the system BIOS. The upgrade utility can be run from a hard drive or a network drive, but no memory managers can be installed during upgrades. The latest upgrade utility and BIOS code are available to qualified customers on the Intel bulletin board. Once the utility is obtained, UNZIP the archive and copy the files to a bootable MS-DOS 5.0, or 6 diskette. Reboot the system with the upgrade diskette in the bootable floppy drive.

In the unlikely event that a Flash upgrade is interrupted catastrophically, it is possible the BIOS may be left in an unusable state. Recovering from this condition requires the following steps (be sure a power supply and speaker have been attached to the board, and a floppy drive is connected as drive A:)

- 1. Change Boot Option jumper (J7A) to the recovery mode position (2-3)
- 2. Install the bootable upgrade diskette into drive A: and reboot the system
- 3. Because of the small code in the non-erasable boot block area, no video is available to direct the procedure. It can be monitored using the speaker and the drive LED. When the system beeps and the drive LED is lit, the system is copying recovery code into the Flash device. When the LED goes off, recovery is complete.
- 4. Turn the system off.
- 5. Change the Boot Option jumper back to the default position (1-2)
- 6. Leave the upgrade floppy in drive A:, turn the system on, and continue with the original upgrade.

Appendix G – Memory Map

Address Range (in Hex)[Block Range]	*Block Size*	*Resource*	*Notes*
0000_0000 - 0003_FFFF	256 KB	System memory	
0004_0000 - 0007_FFFF	256 KB	System memory	
0008_0000 - 0009_FFFF [512 KB - 640 KB]	(4) 32 KB blocks	System memory or ISA memory	1. Configurable. 2. DRAM is lost if ISA Memory.
000A_0000 - 000B_FFFF [640 KB - 768 KB]	(4) 32 KB blocks	System memory or ISA memory	1. ISA Video Data RAM 2. Supports SMM attribute.
000C_0000 - 000E_FFFF [768 KB - 960 KB]	(12) 16 KB blocks	System memory or ISA memory	1. Configurable. 2. Can be shadowed/cached. 3. DRAM is lost if ISA Memory.
000F_0000 - 000F_FFFF [960 KB - 1024 KB]	64 KB	ISA memory	1. System BIOS (Fixed). 2. Can be shadowed / cached. 3. DRAM is lost if not Shadowed.
0010_0000 - 00EF_FFFF [1 MB - 15 MB]	14 MB	System memory or unused	1. Depends on installed DRAM.
00F0_0000 - 00FF_FFFF [15 MB - 16 MB]	1 MB	System memory or EISA/ISA memory	1. Depends on installed DRAM. 2. Can be configured for AT EPROM space*. 3. If AT EPROM enabled, DRAM is lost. 4. Supports SMM attribute
0100_0000 - 3FFF_FFFF [16 MB - 1 GB]	1008 MB	System memory or Unused	1. Depends on installed DRAM
4000_0000 - BFFF_FFFF [2 GB - 3 GB]	1024 MB	EISA memory or Xpress I/O slave memory	
C000_0000 - C1FF_FFFF [3 GB - (3G + 32 MB)]	32 MB	Memory mapped math coprocessor (Weitek)	
C200_0000 - FEBF_FFFF [(3GB + 32 MB) - (3GB + 976 MB)]	944 MB	EISA memory	
FEC0_0000 - FEC0_0FFF	4 KB	I/O APIC #1	Default for ESC
FEC0_1000 - FEC0_1FFF	4 KB	I/O APIC #2	Default for INCA
FEC0_2000 - FEC0_2FFF	4 KB	I/O APIC #3	
FEC0_3000 - FEC0_3FFF	4 KB	I/O APIC #4	

FEC0_4000 - FFDF_FFFF	32752 KB	EISA memory	
FFE0_0000 - FFFF_FFFF [(3GB + 1008 MB) - (3 G + 1024 MB)]	32 MB	EISA (BIOS/ECU)	

*The top 128 KB of this area is used for EPROM. The remaining 896 KB is available for AT add-in cards.

Appendix H – I/O Map

Hex Address(es)	*Resource*	*Notes*
0000 - 001F	DMA Controller 1	ESC
0020 - 0021	Interrupt Controller 1	ESC
0022 - 0023	ESC Configuration Space Access Ports	
0024 - 0025	AIP Configuration Space Access Ports	
0026 - 0027		
0040 - 005F	Programmable Timer	ESC
0060 - 0064	Keyboard Controller	Keyboard chip select from ESC
0061	NMI Status & Control Register	ESC
0070	NMI Mask (bit 7) & RTC Address (bits 6:0)	Write Only.
0071	Real Time Clock (RTC)	RTC chip select from ESC
0080 - 0081	PCEB BIOS Timer	
0080 - 008F	DMA Low Page Register	ESC
0092	System Control Port A (PC-AT control Port)	INCA Register
0094	Video Display Controller	Cirrus 5430
00A0 - 00BF	Interrupt Controller 2	ESC; 82374EB
00C0 - 00DF	DMA Controller 2	ESC;82374EB
00F0	Clear NPX error	Resets IRQ13
00F8 - 00FF	x87 Numeric CoProcessor	
0102	Video Display Controller	
0170 - 0177	Secondary Fixed Disk Controller (IDE)	
01F0 - 01F7	Primary Fixed Disk Controller (IDE)	
0200 - 0207	Game I/O Port	
0220 - 022F	Serial Port A	
0238 - 023F	Serial Port A	
0278 - 027F	Parallel Port 3	
02E8 - 02EF	Serial Port B	
02F8 - 02FF	Serial Port B	
0338 - 033F	Serial Port B	
0370 - 0375	Secondary Floppy	
0376	Secondary IDE	
0377	Secondary IDE/Floppy	
0378 - 037F	Parallel Port 2	
03B4 - 03BA	Monochrome Display Port	
03BC - 03BF	Parallel Port 1	
03C0 - 03CF	Video Display Controller	
03D4 - 03DA	Color Graphics Controller	
03E8 - 03EF	Serial Port A	
03F0 - 03F5	Floppy Disk Controller	
03F6 - 03F7	Primary IDE - Secondary. Floppy	
03F8 - 03FF	Serial Port A (Primary)	
0400 - 043F	DMA Controller 1, Extended Mode Registers.	ESC
0461	Extended NMI / Reset Control	ESC
0462	Software NMI	ESC
0464	Last EISA Bus master granted	
0480 - 048F	DMA High Page Register.	ESC
04C0 - 04CF	DMA Controller 2, High Base Register.	
04D0 - 04D1	Interrupt Controllers 1 and 2 Control Register.	
04D4 - 04D7	DMA Controller 2, Extended Mode Register.	

04D8 - 04DF	Reserved	
04E0 - 04FF	DMA Channel Stop Registers	
0678-067A	Parallel Port (ECP)	
0778-077A	Parallel Port (ECP)	
07BC-07BE	Parallel Port (ECP)	
0800 - 08FF	NVRAM	
0C80 - 0C83	EISA System Identifier Registers	ESC

I/O MAP (CONTINUED)

Hex Address(es)	*Resource*	*Notes*
0C84	Board Revision Register	
0C85 - 0C86	BIOS Function Control	
0CF8	PCI CONFIG_ADDRESS Register	PCMC
0CF9	PCMC Turbo and Reset control	
0CFC	PCI CONFIG_DATA Register	PCMC
n000 - n0FF	EISA Slot n I/O Space	n = 1 to 15.
x100 - x3FF	ISA I/O slot alias address	alias of 100H - 3FFH.
n400 - n4FF	EISA Slot n I/O Space	n = 1 to 15.
x500 - x7FF	ISA I/O slot alias address	alias of 100H - 3FFH.
n800 - n8FF	EISA Slot n I/O Space	n = 1 to 15.
x900 - xBFF	ISA I/O slot alias address	alias of 100H - 3FFH.
nC00 - nCFF	EISA Slot n I/O Space	n = 1 to 15.
xD00 - xFFF	ISA I/O slot alias address	alias of 100H - 3FFH.
46E8	Video Display Controller	
xx00 - xx1F*	SCSI registers	AIC-7870

*SCSI I/O base address is set using configuration registers.

Appendix I – Interrupts & DMA Channels

Source	*PCI or ISA Interrupt*	*Device Input*
PCI Conn. A	INTA#	INCA PCI 0
PCI Conn. B	INTA#	INCA PCI 1
PCI Conn. C	INTA#	INCA PCI 2
PCI Conns. A,B,C	INTB#	INCA PCI 5
PCI Conns. A,B,C	INTC#	INCA PCI 6
PCI Conns. A,B,C	INTD#	INCA PCI 7
Timer	IRQ00	ESC IRQ0
Keyboard	IRQ01	ESC IRQ1
Serial Port B	IRQ03 for COM2 (typ.)	INCA PCI 11
Serial Port A	IRQ04 for COM1 (typ.)	INCA PCI 10
SCSI IRQ		INCA SCSI 0
Parallel Port	IRQ05	INCA SCSI 1
Floppy	IRQ06	INCA XXINT 0
Parallel Port	IRQ07	INCA XXINT 1
Video	IRQ09	INCA PCI 8
	IRQ10	ESC IRQ10
	IRQ11	ESC IRQ11
Mouse	IRQ12	ESC IRQ12
Math error	IRQ13	ESC IRQ13
IDE	IRQ14	INCA PCI 9
	IRQ15	ESC IRQ15

Appendix J – Graphics Resolutions and Frequencies

The Cirrus 5430 video controller provides all standard IBM VGA modes. With 512 KB of video memory, the standard ALTServer goes beyond standard VGA support. The following tables show all supported video modes using the standard 512 KB of video memory, as well as with a user-installable upgrade to 1 MB of video memory. The following tables show the standard and extended modes that the chip supports, including the number of colors and palette size (e.g., 16 colors out of 256K colors), resolution, pixel frequency, and scan frequencies. All modes are supported with 512KB of video memory unless otherwise specified.

Mode(s)[Hex]	*Colors (number /palette size)*	*Resolution*	*Pixel Freq. (MHz)*	*Horiz. Freq. (KHz)*	*Vert. Freq. (Hz)*
0, 1	16/256K	360 X 400	14	31.5	70
2, 3	16/256K	720 X 400	28	31.5	70
4, 5	4/256K	320 X 200	12.5	31.5	70
6	2/256K	640 X 200	25	31.5	70
7	Mono	720 X 400	28	31.5	70
D	16/256K	320 X 200	12.5	31.5	70
E	16/256K	640 X 200	25	31.5	70
F	Mono	640 X 350	25	31.5	70
10	16/256K	640 X 350	25	31.5	70
11	2/256K	640 X 480	25	31.5	60
12	16/256K	640 X 480	25	31.5	60
12+	16/256K	640 X 480	31.5	37.5	75
13	256/256K	320 X 200	12.5	31.5	70
14, 55	16/256K	1056 X 400	41.5	31.5	70
54	16/256K	1056 X 350	41.5	31.5	70
58, 6A	16/256K	800 X 600	40	37.8	60
58, 6A	16/256K	800 X 600	49.5	46.9	75
5C	256/256K	800 X 600	36	35.2	56
5C	256/256K	800 X 600	40	37.9	60
5C	256/256K	800 X 600	49.5	46.9	75
5D	16/256K (interlaced)	1024 X 768	44.9	35.5	87
5D	16/256K	1024 X 768	65	48.3	60
5D	16/256K	1024 X 768	75	56	70
5D	16/256K	1024 X 768	78.7	60	75
5F	256/256K	640 X 480	25	31.5	60
5F	256/256K	640 X 480	31.5	37.5	75
60*	256/256K (interlaced)	1024 X 768	44.9	35.5	87
60*	256/256K	1024 X 768	65	48.3	60
60*	256/256K	1024 X 768	75	56	70
60*	256/256K	1024 X 768	78.7	60	75
64*	64K	640 X 480	25	31.5	60
64*	64K	640 X 480	31.5	37.5	75
65*	64K	800 X 600	36	35.2	56
65*	64K	800 X 600	40	37.8	60
65*	64K	800 X 600	49.5	46.9	75
66*	32K Direct/256 Mixed	640 X 480	25	31.5	60
66*	32K Direct/256 Mixed	640 X 480	31.5	37.5	75
67*	32K Direct/256 Mixed	800 X 600	40	37.8	60
67*	32K Direct/256 Mixed	800 X 600	49.5	46.9	75
6C*	16/256K (interlaced)	1280 X 1024	75	48	87

* Requires 1MB video memory option

Appendix K – Environmental & Reliability Standards

The topics in this section specify the normal operating conditions for the ALTServer. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those shown in the following table may cause permanent damage (provided for stress testing only).

Operating Temperature	0°C to +55°C
Storage Temperature	-55°C to +150°C
Voltage on any signal with respect to VSS	-0.3 to VCC +0.3 V
Supply Voltage with Respect to VSS	-0.3 to +5.5 V

ENVIRONMENTAL

The ALTServer is intended for use in a Class B environment (residential). It meets the Intel Board Environmental Specification 112000 Rev. G. The following table summarizes environmental limits for the ALTServer:

Parameter	*Condition*	*Specification*
Temperature	Non-Operating	-40^{O}C to +70^{O}C
	Operating	+0^{O}C to +50^{O}C
Airflow	300 LFM	40^{O}C
	400LFM	45^{O}C
	500LFM	50^{O}C
Humidity	Non-Operating	92% Relative Humidity max. @ 36^{O}C
	Operating	80% Relative Humidity max. @ 36°C
Altitude	Non-Operating	50,000 feet (15,240 meters)
	Operating	10,000 feet (3048 meters)
ESD	1.0kV	No Errors
	2.5kV	No Errors
	5.0kV	5% Soft Errors, 0% Hard Errors, No physical damage
	7.5kV	10% Soft Errors, 0% Hard Errors, No physical damage
	10.0kV	25% Soft Errors, 5% Hard Errors, No physical damage
	12.5kV	50% Soft, 10% Hard, No physical damage
	15.0kV	100% Soft, 25% Hard, No physical damage
	25.0kV	100% Soft, 100% Hard, No physical damage
Shock	Non-Operating	30.0G, 11ms, 1/2 sine

ELECTRICAL

ALTServer DC specifications are summarized here, for motherboard signaling environment, power connectors, and 5V power budget. Refer to *PCI Local Bus Specification Rev. 2.0*, and *EISA Bus Specification* for PCI and EISA/ISA DC and AC electrical specifications. Refer also to the documentation for ASIC devices used on the ALTServer. The following tables show the required DC specifications for 5V and 3.3V Altair bus signaling environments.

Symbol	*Parameter*	*Condition*	*Min*	*Max*	*Units*
V_{cc}	Supply Voltage		4.75	5.25	V
TA	Operating Temp.	Still Air	0	55	°C
V_{ih}	Input High Voltage		2.2	V_{cc} +1.2	V
V_{il}	Input Low Voltage		-1.2	0.8	V
I_{ih}	Input High Current	V_{in} = 2.7		1.0	mA
I_{il}	Input Low Current	V_{in} = 0.5		-1.6	mA
V_{oh}	Output High Voltage	I_{oh}, max V_{cc}, min	2.4		V
V_{ol}	Output Low Voltage	I_{ol},max V_{cc}, min		0.55	V

ALTServer 5 Volt DC Specification

Symbol	Parameter	Condition	Min	Max	Units
Vcc3	Supply Voltage		3.0	3.6	V
Vih	Input High Voltage		0.475 x Vcc3	Vcc +0.5	V
Vil	Input Low Voltage		-0.5	0.325 x Vcc3	V
Iih	Input High Leakage Current	Vin = 2.7		±10	µA
Iil	Input Low Leakage Current	Vin = 0.5		±10	µA
Voh	Output High Voltage	Iout = -0.5 mA	0.9 x Vcc3		V
Vol	Output Low Voltage	Iout = -1.5 mA		0.1 x Vcc3	V

ALTServer 3.3 Volt DC Specification

RELIABILITY DATA

The Mean-Time-Between-Failures (MTBF) data is calculated from predicted data @ 55C.

MTBF	Temperature
73,189 Hours.	55°C

Appendix L – Customer Support

The ALTServer is backed by Intel's industry-leading support groups in the OEM Products and Services Division (OPSD), including IntelTechDirect, which includes these major services:

INTEL APPLICATIONS SUPPORT

A direct link to highly qualified and well trained technical personnel.

- Toll-free access to Intel support engineers for problem resolution
- Responses within 24 hours Monday-Friday
- Expert assistance geared to the special needs of OEMs and VARs

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A full service bulletin board with product information, demo software and more.

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  - Americas 916-356-3600
  - Europe 44-793-496340
- Modem speeds up to 14.4k baud with standard software
- FLASH BIOS upgrade files
- Modem set at no parity, 8 data bits, 1 stop bit.
- Master BBS file list and FaxBack catalog available at 800-897-2536.

WINDOWS HELP FILES

- Monthly Product updates available to qualified users on the bulletin board
- Official notification of engineering changes and technical data
- Easy information retrieval using Windows Help file format
- Intel platform system, board, and BIOS revision histories
- Hardware and software compatibility notes
- Documentation updates, spare parts and order information

FAXBACK

- Product descriptions and technical data sent to any fax machine from a touch-tone phone
- Information on End-of-Life products
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  - U.S. Toll Free 800-628-2283 (Americas: 916-356-3105)
  - Europe 44-793-496646