# Advanced/RH Motherboard Specification Update

Release Date: October 1997

Order Number: 281808-015

The Advanced/RH motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call in North America 1-800-879-4683, Europe 44-0-1793-431-155, France 44-0-1793-421-777,

Germany 44-0-1793-421-333, other Countries 708-296-9333

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# REVISION HISTORY

| Date of Revision | Version | Description |
|---|---|---|
| April 1996 | -001 | This document is the first Specification Update for the Intel Advanced/RH motherboard. |
| May 1996 | -002 | Added Erratum 6. |
| June 1996 | -003 | Added Errata 7-10 and Changed Status of Errata 3-4. |
| August 1996 | -004 | Added Documentation Changes section. |
| September 1996 | -005 | Added Erratum 11 and Documentation Changes 1-22. |
| October 1996 | -006 | Added Documentation Changes 23-24, Updated Errata 1 and 6. |
| November 1996 | -007 | Added Erratum 12, Updated Errata 1 and 9. Removed Documentation Changes 1-24, which were incorporated into revision -004 of the specification. |
| December 1996 | -008 | Added Errata 13-16. |
| January 1997 | -009 | Added Errata 17-18 and PBA/BIOS Table. |
| February 1997 | -010 | Updated the Status of Errata 12, 14, 15, 16 and 18. |
| March 1997 | -011 | Added AA Revision to Motherboard Identification table. Revised format of PBA/BIOS revision table. Updated Errata 1, 2, 5, 6 and 9. Added Errata 19-21, Specification Clarifications 1-2 and Documentation Changes 1-11. |
| April 1997 | -012 | Removed Specification Clarification 1 and Documentation Changes 1-11, which were incorporated into revision -006 of the specification. Renumbered Specification Clarification 2 to 1. Added Erratum 22. |
| June 1997 | -013 | Added Specification Change 1, Specification Clarifications 2-3 and Documentation Changes 1-2. Updated Erratum 20 and Specification Clarification 1. |
| July 1997 | -014 | Added Erratum 23, Specification Clarification 4 and Documentation Changes 3-6. |
| October 1997 | -015 | Added Erratum 24 and Documentation Change 7. |

# PREFACE

This document is an update to the specifications contained in the *Advanced/RH Motherboard Technical Product Specification* (Order Number 281809). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Pentium® Processor Specification Update* (Order Number 242480) for specification updates concerning the Pentium processor. Items contained in the *Pentium Processor Specification Update* that either do not apply to the Advanced/RH motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *82430HX PCIset Specification Update* (Order Number 297652) for specification updates concerning the 82430HX PCIset. Items contained in the *82430HX PCIset Specification Update* that either do not apply to the Advanced/RH motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *82371SB PIIX3 Specification Update* (Order Number 297658) for specification updates concerning the 82371SB PIIX3. Items contained in the *82371SB PIIX3 Specification Update* that either do not apply to the Advanced/RH motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

## *Nomenclature*

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

**Errata** are design defects or errors. Characterized errata may cause the Advanced/RH motherboard's behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision level are present on all motherboards.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

# Specification Update for Advanced/RH Motherboards

# GENERAL INFORMATION

**Basic Advanced/RH Motherboard Identification Information**

| AA Revision | PBA Revision | 82430HX PCIset Stepping | BIOS Revision | Notes |
|---|---|---|---|---|
| 650350-302 | 648621-302 | A1 | 1.00.03.CV2 | 1, 2, 3, 4, 11 |
| 650350-303 | 648621-303 | A1 | 1.00.05.CV2 | 1, 2, 3, 4, 11 |
| 650350-304 | 648621-304 | A1 | 1.00.05.CV2 | 1, 5, 6, 7, 11 |
| 650350-305 | 648621-305 | A1 | 1.00.05.CV2 | 1, 5, 6, 7, 11 |
| 650350-306 | 648621-306 | A1 | 1.00.05.CV2 | 1, 5, 6, 7, 11 |
| 650350-307 | 648621-307 | A1 | 1.00.09.CV2 | 1, 5, 6, 7, 11 |
| 650350-308 | 648621-308 | A3 | 1.00.09.CV2 | 1, 8, 9, 10, 11 |
| 650350-328 | 648621-328 | A3 | 1.00.10.CV2 | 1, 8, 9, 10, 11 |
| 650350-329 | 648621-329 | A3 | 1.00.10.CV2 | 1, 8, 9, 10, 11 |
| 650350-330 | 648621-330 | A3 | 1.00.10.CV2 | 1, 8, 9, 10, 11 |
| 650350-331 | 648621-331 | A3 | 1.00.13.CV2 | 1, 8, 9, 10, 11 |
| 655121-300 | 655118-300 | A1 | 1.00.02.CV2 | 1, 2, 3, 4, 11 |
| 655121-301 | 655118-301 | A1 | 1.00.03.CV2 | 1, 2, 3, 4, 11 |
| 655121-302 | 655118-302 | A1 | 1.00.05.CV2 | 1, 2, 3, 4, 11 |
| 655121-303 | 655118-303 | A1 | 1.00.05.CV2 | 1, 2, 3, 4, 11 |
| 655121-304 | 655118-304 | A1 | 1.00.05.CV2 | 1, 5, 6, 7, 11 |
| 655121-305 | 655118-305 | A1 | 1.00.05.CV2 | 1, 5, 6, 7, 11 |
| 655121-306 | 655118-306 | A1 | 1.00.09.CV2 | 1, 5, 6, 7, 11 |
| 655121-307 | 655118-307 | A3 | 1.00.09.CV2 | 1, 8, 9, 10, 11 |
| 655121-327 | 655118-327 | A3 | 1.00.10.CV2 | 1, 8, 9, 10, 11 |
| 655257-300 | 655232-300 | A1 | 1.00.02.CV2 | 1, 2, 3, 4, 11 |
| 655257-301 | 655232-301 | A1 | 1.00.03.CV2 | 1, 2, 3, 4, 11 |
| 655257-302 | 655232-302 | A1 | 1.00.05.CV2 | 1, 2, 3, 4, 11 |
| 655257-303 | 655232-303 | A1 | 1.00.05.CV2 | 1, 2, 3, 4, 11 |
| 655257-304 | 655232-304 | A1 | 1.00.05.CV2 | 1, 5, 6, 7, 11 |
| 655257-305 | 655232-305 | A1 | 1.00.05.CV2 | 1, 5, 6, 7, 11 |
| 655257-306 | 655232-306 | A3 | 1.00.09.CV2 | 1, 8, 9, 10, 11 |
| 655257-325 | 655232-325 | A3 | 1.00.09.CV2 | 1, 8, 9, 10, 11 |
| 655257-326 | 655232-326 | A3 | 1.00.10.CV2 | 1, 8, 9, 10, 11 |
| 655257-327 | 655232-327 | A3 | 1.00.10.CV2 | 1, 8, 9, 10, 11 |
| 655257-328 | 655232-328 | A3 | 1.00.10.CV2 | 1, 8, 9, 10, 11 |

| AA Revision | PBA Revision | 82430HX PCIset Stepping | BIOS Revision | Notes |
|---|---|---|---|---|
| 655257-329 | 655232-329 | A3 | 1.00.13.CV2 | 1, 8, 9, 10, 11 |
| 670917-306 | 664638-306 | A3 | 1.00.11.CV2 | 1, 8, 9, 10, 12 |
| 670917-307 | 664638-307 | A3 | 1.00.12.CV2 | 1, 8, 9, 10, 12 |
| 670917-308 | 664638-308 | A3 | 1.00.12.CV2 | 1, 8, 9, 10, 12 |
| 670917-309 | 664638-309 | A3 | 1.00.12.CV2 | 1, 8, 9, 10, 12 |
| 670917-310 | 664638-310 | A3 | 1.00.13.CV2 | 1, 8, 9, 10, 12 |

NOTES:

1. The PBA number is found on a small label on the component side of the board.
2. The 82430HX PCIset kit used on this PBA revision consists of two components as follows:

| Device | Stepping | S-Spec Numbers |
|---|---|---|
| 82439HX | A1 | SU087 |
| 82371SB | A1 | SU052 |

3. The following errata contained in the *82430HX PCIset Specification Update* (Order Number 297652) either do not apply to the Advanced/RH motherboard or have been worked around in this PBA and/or BIOS revision: 2-3. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82430HX PCIset Specification Update*.
4. The following errata contained in the *82371SB PIIX3 Specification Update* (Order Number 297658) either do not apply to the Advanced/RH motherboard or have been worked around in this PBA and/or BIOS revision: 2-12. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82371SB PIIX3 Specification Update*.
5. The 82430HX PCIset kit used on this PBA revision consists of two components as follows:

| Device | Stepping | S-Spec Numbers |
|---|---|---|
| 82439HX | A1 | SU087 |
| 82371SB | B0 | SU093 |

6. The following errata contained in the *82430HX PCIset Specification Update* (Order Number 297652) either do not apply to the Advanced/RH motherboard or have been worked around in this PBA and/or BIOS revision: 2-3. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82430HX PCIset Specification Update*.
7. The following errata contained in the *82371SB PIIX3 Specification Update* (Order Number 297658) either do not apply to the Advanced/RH motherboard or have been worked around in this PBA and/or BIOS revision: 1-7. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82371SB PIIX3 Specification Update*.
8. The 82430HX PCIset kit used on this PBA revision consists of two components as follows:

| Device | Stepping | S-Spec Numbers |
|---|---|---|
| 82439HX | A3 | SU115 |
| 82371SB | B0 | SU093 |

9. The following errata contained in the *82430HX PCIset Specification Update* (Order Number 297652) either do not apply to the Advanced/RH motherboard or have been worked around in this PBA and/or BIOS revision: 1-3. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82430HX PCIset Specification Update*.

10. The following errata contained in the *82371SB PIIX3 Specification Update* (Order Number 297658) either do not apply to the Advanced/RH motherboard or have been worked around in this PBA and/or BIOS revision: 1-7. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82371SB PIIX3 Specification Update*.
11. The following errata contained in Part I of the *Pentium® Processor Specification Update* (Order Number 242480) either do not apply to the Advanced/RH motherboard or have been worked around in this PBA and/or BIOS revision: 5, 7, 9-11, 13-14, 16-17, 29, 31, 34, 36-37, 39, 40, 46, 48-50, 58, 60-64, 66-67, 69, 71-80, all DP errata, all AP errata, all TCP errata. All other errata in Part I may apply to this revision level of the motherboard, depending on the stepping of the processor or the specific software that is being executed. Also, some of these errata apply only to motherboards being used in an application development environment. For specific details of any erratum please refer to the *Pentium Processor Specification Update*.
12. The following errata contained in Part I of the *Pentium Processor Specification Update* (Order Number 242480) either do not apply to the Advanced/RH motherboard or have been worked around in this PBA and/or BIOS revision: 5, 7, 9-11, 13-14, 16-17, 29, 31, 34, 36-37, 39, 40, 46, 48-50, 58, 60-64, 66-67, 69, 71, all DP errata, all AP errata, all TCP errata. All other errata in Part I may apply to this revision level of the motherboard, depending on the stepping of the processor or the specific software that is being executed. Also, some of these errata apply only to motherboards being used in an application development environment. For specific details of any erratum please refer to the *Pentium Processor Specification Update.*

## *Summary Table of Changes*

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Advanced/RH motherboard. Intel intends to fix some of the errata in a future revision of the motherboard, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

**CODES USED IN SUMMARY TABLE**

| | |
|---|---|
| Doc: | Document change or update that will be implemented. |
| Fix: | This erratum is intended to be fixed in a future revision of the motherboard or BIOS. |
| Fixed: | This erratum has been previously fixed. |
| NoFix: | There are no plans to fix this erratum. |
| Shaded: | This erratum is either new or modified from the previous version of the document. |

| NO. | PLANS | SPECIFICATION CHANGES |
|---|---|---|
| 1 | Doc | Support for 233 MHz Pentium® processors with MMX™ technology |
| **NO.** | **PLANS** | **ERRATA** |
| 1 | Fixed | The A3 stepping of the ATI264-VT video controller SGRAM configuration is limited to 2 Mbytes of video memory |
| 2 | NoFix | The A3 stepping of the ATI264-VT video controller is limited to 63 MHz MCLOCK |
| 3 | NoFix | MIDI and wave playback disrupted by system suspend |
| 4 | NoFix | Sound recorder volume controls are locked |
| 5 | Fixed | ECC non-detection of single/double bit errors on partial memory writes |
| 6 | Fixed | Onboard Creative Labs Vibra* 16S audio does not release resources when disabled |
| 7 | Fixed | BIOS SETUP does not recognize February 29, 2000 as a valid date |
| 8 | Fixed | System BIOS does not recognize certain dates as valid |
| 9 | Fixed | PCI Delayed Transactions are not supported |
| 10 | Fixed | System BIOS may detect memory in unpopulated SIMM* rows |
| 11 | Fixed | Secondary IDE hard drives may not be recognized during startup |
| 12 | Fixed | BIOS does not support no-emulation mode for CD-ROM boot |
| 13 | Fixed | Memory errors or system lockups with ECC enabled |
| 14 | Fixed | Flash Memory Update Utility (FMUP) may cause BIOS verification error |
| 15 | Fixed | Random characters may be displayed during POST |
| 16 | Fixed | CMOS checksum may be lost if power is cycled during boot |
| 17 | Fixed | Resource conflict with onboard ATI* video |
| 18 | Fixed | I/O ports not available with manual peripheral configuration |

| NO. | PLANS | ERRATA |
|---|---|---|
| 19 | Fixed | No video displayed using dual video configuration |
| 20 | NoFix | Slave on secondary IDE channel is not disabled |
| 21 | Fix | System BIOS does not recognize bootable USB devices |
| 22 | NoFix | Cannot meet FCC Class B requirements using unshielded USB cable |
| 23 | NoFix | Windows* 95 SVGA Drivers Not Supported |
| 24 | Fix | Floppy drive always reported by system BIOS |
| **NO.** | **PLANS** | **SPECIFICATION CLARIFICATIONS** |
| 1 | Doc | Support for Pentium® Processors with MMX™ Technology |
| 2 | Doc | Advanced Power Management (APM) will not function as expected with Universal Serial Bus (USB) enabled |
| 3 | Doc | PCI 2.1 Specification optional features |
| 4 | Doc | Administrator and user passwords |
| **NO.** | **PLANS** | **DOCUMENTATION CHANGES** |
| 1 | Doc | Revision of Section 1.12, “Reliability” |
| 2 | Doc | Revision of Section 5.1, “Specifications” |
| 3 | Doc | Revision of Section 1.11.3, “Clear CMOS (J4L1-A)” |
| 4 | Doc | Revision of Section 1.14.1, “Power Supply Considerations” |
| 5 | Doc | Revision of Section 1.6.1, “82439HX Xcelerated Controller (TXC)” |
| 6 | Doc | Revision of Section 3.4.15.8, “Critical Events in Log” |
| 7 | Doc | Addition of onboard video IRQ section |

The errata described in this specification update apply to combinations of PBA revision and BIOS revision as shown in the table below. Descriptions of the individual errata referred to by number in the table below are found in the ERRATA section of this document.

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 648621-302 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2 | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 648621-303 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 648621-304 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 648621-304 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 648621-305 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 648621-306 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 648621-307 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2 | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2 | 2-5, 17, 20-23 |
| | 1.00.11.CV2 | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 648621-308 | 1.00.02.CV2‡ | 1-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2 | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2 | 2-5, 17, 20-23 |
| | 1.00.11.CV2 | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 648621-328 | 1.00.02.CV2‡ | 1-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2 | 2-5, 17, 20-23 |
| | 1.00.11.CV2 | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 648621-329 | 1.00.02.CV2‡ | 1-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2 | 2-5, 17, 20-23 |
| | 1.00.11.CV2 | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 648621-330 | 1.00.02.CV2‡ | 1-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2 | 2-5, 17, 20-23 |
| | 1.00.11.CV2 | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 648621-331 | 1.00.02.CV2‡ | 1-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2‡ | 2-5, 17, 20-23 |
| | 1.00.11.CV2‡ | 2-5, 17, 20-23 |
| | 1.00.12.CV2‡ | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 655118-300 | 1.00.02.CV2 | 1-23 |
| | 1.00.03.CV2 | 1-5, 7-23 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-23 |
| | 1.00.07.CV2 | 1-5, 9, 12-23 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-23 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-23 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-23 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 23, 24 |

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 655118-301 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2 | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 23, 24 |
| 655118-302 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 23, 24 |
| 655118-303 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 23, 24 |

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 655118-304 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 23, 24 |
| 655118-305 | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 23, 24 |
| 655118-306 | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2‡ | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2‡ | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 23, 24 |

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 655118-307 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2 | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2 | 2-5, 17, 20-23 |
| | 1.00.11.CV2 | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 23, 24 |
| 655118-327 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2 | 2-5, 17, 20-23 |
| | 1.00.11.CV2 | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 23, 24 |
| 655232-300 | 1.00.02.CV2 | 1-22 |
| | 1.00.03.CV2 | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 655232-301 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2 | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 655232-302 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 655232-303 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 655232-304 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 655232-305 | 1.00.02.CV2‡ | 1-22 |
| | 1.00.03.CV2‡ | 1-5, 7-22 |
| | 1.00.05.CV2 | 1-5, 9, 11, 12-22 |
| | 1.00.07.CV2 | 1-5, 9, 12-22 |
| | 1.00.09.CV2 | 1-5, 9, 12, 14-22 |
| | 1.00.10.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.11.CV2 | 1-5, 9, 17, 19-22 |
| | 1.00.12.CV2 | 1-5, 9, 17, 19-20, 22 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 655232-306 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2 | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2 | 2-5, 17, 20-23 |
| | 1.00.11.CV2 | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 655232-325 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2 | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2 | 2-5, 17, 20-23 |
| | 1.00.11.CV2 | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 655232-326 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2 | 2-5, 17, 20-23 |
| | 1.00.11.CV2 | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 655232-327 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2 | 2-5, 17, 20-23 |
| | 1.00.11.CV2 | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 655232-328 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2 | 2-5, 17, 20-23 |
| | 1.00.11.CV2 | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 655232-329 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2 | 2-5, 17, 20-23 |
| | 1.00.11.CV2‡ | 2-5, 17, 20-23 |
| | 1.00.12.CV2‡ | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 1-5, 9, 17, 19-20, 22, 24 |
| 664638-306 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2‡ | 2-5, 17, 20-23 |
| | 1.00.11.CV2 | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 2-5, 17, 20, 23, 24 |

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 664638-307 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2‡ | 2-5, 17, 20-23 |
| | 1.00.11.CV2‡ | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 2-5, 17, 20, 23, 24 |
| 664638-308 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2‡ | 2-5, 17, 20-23 |
| | 1.00.11.CV2‡ | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 2-5, 17, 20, 23, 24 |
| 664638-309 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2‡ | 2-5, 17, 20-23 |
| | 1.00.11.CV2‡ | 2-5, 17, 20-23 |
| | 1.00.12.CV2 | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 2-5, 17, 20, 23, 24 |

| PBA Revision | BIOS Revision | Errata That Apply |
|---|---|---|
| 664638-310 | 1.00.02.CV2‡ | 2-18, 20-23 |
| | 1.00.03.CV2‡ | 2-5, 7-18, 20-23 |
| | 1.00.05.CV2‡ | 2-5, 9, 11, 12-18, 20-23 |
| | 1.00.07.CV2‡ | 2-5, 9, 12-18, 20-23 |
| | 1.00.09.CV2‡ | 2-5, 12, 14-18, 20-23 |
| | 1.00.10.CV2‡ | 2-5, 17, 20-23 |
| | 1.00.11.CV2‡ | 2-5, 17, 20-23 |
| | 1.00.12.CV2‡ | 2-5, 17, 20, 23 |
| | 1.00.13.CV2 | 2-5, 17, 20, 23, 24 |

NOTE:

‡ This combination of BIOS revision and PBA revision has not undergone regression testing. Use of a PBA with down-revision BIOS is an untested combination and is undertaken at the user's risk.

# SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the *Advanced/RH Motherboard Technical Product Specification* (Order Number 281809). All Specification Changes will be incorporated into a future version of that specification.

## *1. Support for 233 MHz Pentium® processors with MMX™ technology*

Support for 233 MHz Pentium® processors with MMX™ technology is available in PBA revision 664638-306 and higher. Below are the jumper settings:

| Processor Freq. (MHz) | Jumpers J4L1-C | Jumpers J4L1-D | Host Bus Freq. (MHz) | PCI Bus Freq. (MHz) | ISA Bus Freq. (MHz) | Bus/Processor Freq. Ratio |
|---|---|---|---|---|---|---|
| 100/233 | 1-2 and 5-6 | 1-2 and 4-5 | 66 | 33 | 8.33 | 1.5 |

NOTE:

There are no additional jumpering requirements for Pentium processors with MMX technology.

The 100 MHz Pentium processor and the 233 MHz Pentium processor with MMX technology have identical jumper settings. The motherboard automatically detects which processor type is installed.

# ERRATA

## 1. The A3 Stepping of the ATI264-VT Video Controller SGRAM Configuration is Limited to 2 MB of Video Memory

**PROBLEM:** The A3 stepping of the ATI264-VT video controller SGRAM configuration only supports a maximum of 2 MB of video memory.

**IMPLICATION:** The upgrade module for expansion up to 4MB (available through ATI Technologies) is not supported on PBAs using the A3 stepping of the video controller. Users of these PBA's will be limited to a maximum of 2 MB of video memory.

**WORKAROUND:** None.

**STATUS:** This erratum was fixed in PBA revision 648621-307, 655118-307, 655232-306 and with the A4 stepping of the ATI264-VT video controller.

## 2. The A3 Stepping of the ATI264-VT Video Controller is Limited to 63 MHz MCLOCK

**PROBLEM:** Planned operation at 70 MHz is not available in the A3 stepping of the controller.

**IMPLICATION:** Operation at 63 MHz results in lower performance compared with planned operation at 70 MHz.

**WORKAROUND:** None.

**STATUS:** This erratum will not be fixed. In PBA revision 648621-307, 655118-307 and 655232-306 with the A4 stepping of the ATI264-VT video controller, the MCLOCK was increased to 67 MHz.

## 3. MIDI and Wave Playback Disrupted By System Suspend

**PROBLEM:** If the system is put into Advanced Power Management (APM) suspend mode while a MIDI or wave file is being played and then the system is brought out of the power-down state the audio does not resume correctly.

**IMPLICATION:** If the user wants to resume audio playback after an APM suspension the system may have to be rebooted.

**WORKAROUND:** Reboot as indicated above.

**STATUS:** This erratum will not be fixed.

## 4. Sound Recorder Volume Controls are Locked

**PROBLEM:** The user cannot use the Microsoft Sound Recorder controls to change volume while recording.

**IMPLICATION:** Recording volume cannot be directly controlled by the user.

**WORKAROUND:** Record with the playback volume turned up fully.

**STATUS:** This erratum will not be fixed.

## 5. ECC Non-detection of Single/Double Bit Errors on Partial Memory Writes

**PROBLEM:** When the 82439HX TXC performs a partial write to main memory (data less than a 64-bit quadword) in ECC mode, single bit errors are corrected but not logged. Double bit errors are not detected or logged.

**IMPLICATION:** Normally, the controller is able to buffer writes and group them into quadwords. In all these cases where 64 bits are written to memory at a time, both single and double bit errors will be signaled to the operating system. Single bit errors will be corrected using the information contained in the checkbits that are stored with the data in memory. Double bit errors cannot be corrected by the memory controller, but the operating system can warn the user that the error has occurred.

If the controller must perform a partial write, a read-merge-write cycle will occur so that the proper checkbits can be regenerated across the entire 64 bits to be written into DRAM. If erroneous data is read during this cycle, the following will occur:

For single bit errors, the error will be corrected based on the memory checkbits. The corrected data will be written back to memory, but the error will not be flagged to the system, so the user will not receive information from the error log that could be useful in isolating a failing memory module.

For double-bit errors, no error will be detected or signaled to the operating system. The erroneous data will be rewritten to memory and a set of regenerated checkbits will be rewritten at the same time, marking the erroneous data as correct.

**WORKAROUND:** None identified at this time. However, for ECC systems that require only single bit error protection, the A1 stepping of the 430HX PCIset does provide this level of reliability.

**STATUS:** This erratum was fixed in PBA revision 648621-308, 655118-307 and 655232-306 when used with BIOS revision 1.00.10.CV2.

## 6. Onboard Creative Vibra* 16S Audio Does Not Release Resources When Disabled

**PROBLEM:** There is a conflict with assignment of the I/O address between the FM synthesizer in the onboard Creative Labs Vibra* 16S audio controller and the FM synthesizer of a user-supplied add-in sound card.

**IMPLICATION:** An add-in card cannot be used to provide FM synthesis under any operating system.

**WORKAROUND:** Use the on-board Creative Labs Vibra16S FM synthesizer.

**STATUS:** This erratum was fixed in BIOS revision 1.00.03.CV2 for the Windows* 95 operating system and in PBA revision 648621-307 and 655232-306 for all other operating systems.

## 7. BIOS SETUP Does Not Recognize February 29, 2000 As a Valid Date

**PROBLEM:** The BIOS Setup program will not allow the system date to be set to Feb 29, 2000.

**IMPLICATION:** Any program that uses the system time and date stamps to determine when to perform some activity will not perform that scheduled activity. Date and time stamps for files created on these dates will be incorrect.

**WORKAROUND:** If the system BIOS has not been upgraded, the system date will have to be reset to the correct date on March 1, 2000.

**STATUS:** This erratum was fixed in BIOS revision 1.00.05.CV2.

## 8. System BIOS Does not Recognize Certain Dates As Valid

**PROBLEM:** If the motherboard is powered on or reset with the system date set to October 20-31 or December 20-31, the system BIOS will report “CMOS Time and Date Not Set” and the system date will be reset to Jan 01, 1990 during Power On Self Test (POST). If the user resets the system to the correct date and reboots, the system BIOS reports the same error message and again resets the date to Jan 01, 1990.

**IMPLICATION:** Any program that uses the system time and date stamps to determine when to perform some activity will not perform that scheduled activity. Date and time stamps for files created on these dates will be incorrect.

**WORKAROUND:** None identified at this time.

**STATUS:** This erratum was fixed in BIOS revision 1.00.05.CV2.

## 9. PCI Delayed Transactions Are Not Supported

**PROBLEM:** An erratum to the A1 stepping of the 82371SB PCI ISA IDE Xcelerator (PIIX3) requires that the option for Delayed Transactions be turned off by the BIOS.

**IMPLICATION:** System level performance and compatibility are not affected by turning off delayed transactions. The system will be PCI 2.1 compatible and will support all PCI 2.1 compliant cards.

**WORKAROUND:** None identified at this time.

**STATUS:** This erratum was fixed in PBA revision 648621-308, 655118-307 and 655232-306 when used with BIOS revision 1.00.09.CV2.

## 10. System BIOS May Detect Memory In Unpopulated SIMM* Rows

**PROBLEM:** During Power-On Self Test (POST), the system BIOS may improperly determine that memory is present in an unpopulated SIMM* bank. Subsequently, the BIOS memory sizing algorithm may fail to reflect the correct total memory configuration.

**IMPLICATION:** If memory is falsely detected in the first SIMM bank (Bank 0), a POST error (code E8h) will be generated and the system will not boot. If memory is falsely detected in the middle SIMM bank (Bank 1) where the outside SIMM banks (Banks 0 and 2) are actually populated, then only the memory in the first SIMM bank will be detected during the BIOS memory sizing phase. No sizing problems have been observed in cases where memory is falsely detected in a higher numbered SIMM bank and the lowest numbered bank is populated.

**WORKAROUND:** Install SIMMs in consecutive banks beginning with Bank 0.

**STATUS:** This erratum was fixed in BIOS revision 1.00.05.CV2.

## 11. Secondary IDE Hard Drives May Not Be Recognized During Startup

**PROBLEM:** An IDE hard drive connected to the secondary IDE channel will not be recognized on a cold boot if an IDE device is not connected to the primary IDE channel.

**IMPLICATION:** After a cold boot with that system configuration, the IDE hard drive on the secondary IDE channel is not available

**WORKAROUND:** Switch the cables on the motherboard so the IDE hard drive is connected to the primary IDE channel.

**STATUS:** This erratum was fixed in BIOS Release 1.00.07.CV2.

## 12. BIOS Does Not Support No-Emulation Mode for CD-ROM Boot

**PROBLEM:** The system BIOS does not support booting from an "El Torito" bootable CD-ROM using the no-emulation mode format.

**IMPLICATION:** Booting from a CD-ROM using no emulation mode is not supported. For example, Microsoft Windows* NT* version 4.0 uses no-emulation mode for its boot CD-ROM.

**WORKAROUND:** Boot the computer from a floppy or hard disk, then install or run the program from the CD-ROM.

**STATUS:** This erratum was fixed in BIOS revision 1.00.10.CV2.

## 13. Memory Errors or System Lockups with ECC Enabled

**PROBLEM:** ECC memory timing parameters implemented in the BIOS violate 82430HX PCIset design guidelines.

**IMPLICATION:** The system may experience memory errors or system lockups when using ECC SIMM*s with ECC enabled in the BIOS Setup program.

**WORKAROUND:** If using ECC SIMMs, disable ECC Memory Error Detection in the BIOS Setup Program.

**STATUS:** This erratum was fixed in BIOS revision 1.00.09.CV2.

## 14. Flash Memory Update Utility (FMUP) May Cause BIOS Verification Error

**PROBLEM:** The Flash Memory Update Utility (FMUP) will report an error when trying to compare motherboard BIOS 1.00.09.CV2 with the BIOS file on the diskette if the CLEAR CMOS jumper is set. Using the "Verify flash memory area with a file" option in FMUP after performing a BIOS upgrade, will also do a compare with the event log. Since the Clear CMOS jumper causes an event to be logged, it will not match the original file.

**IMPLICATION:** The FMUP "Verify flash memory area with a file" option will result in a flash verification error even though the flash BIOS was successfully updated.

**WORKAROUND:** If the CLEAR CMOS jumper is set, do not use the "Verify flash memory area with a file" option. If the "Verify flash memory area with a file" option is going to be used, do not set the CLEAR CMOS jumper.

**STATUS:** This erratum was fixed in BIOS revision 1.00.10.CV2.

## 15. Random Characters May Be Displayed During POST

**PROBLEM:** The Desktop Management Interface (DMI) fields located in flash memory that contain product name and serial number information are not programmed correctly.

**IMPLICATION:** Random characters may be displayed for the product name and serial number during POST.

**WORKAROUND:** None.

**STATUS:** This erratum was fixed in BIOS revision 1.00.10.CV2.

## 16. CMOS Checksum May Be Lost If Power Is Cycled During Boot

**PROBLEM:** If the computer power is turned off during a short portion of the boot process, the CMOS checksum byte is not updated. The next time the computer is turned on, the message "CMOS Checksum Invalid" will be displayed.

**IMPLICATION:** When the message is displayed, the correct checksum has already been recalculated and stored. No user action is required to recover from the error. If the additional message:

> Date and Time Not Set
> Press <F1> for Setup, <Esc> to Boot

is displayed, the user must reset the current date and time using the BIOS Setup program.

**WORKAROUND:** None.

**STATUS:** This erratum was fixed in BIOS revision 1.00.10.CV2.

## 17. Resource Conflict with Onboard ATI* Video

**PROBLEM:** The system may fail to initialize a 3COM 3C595 bus mastering network card when configured as a Windows* NT* 3.51 server or workstation. Windows NT reports that there is a conflict with the resources of the 3COM 3C595 network card and the onboard ATI* video.

**IMPLICATION:** The resource conflict will not allow the server to logon to the domain controller. Attaching to the network as a workstation may be intermittent.

**WORKAROUND:** None.

**STATUS:** This erratum was fixed with revision 3.0 of the ATI Mach64* drivers for Windows NT 3.51 available at http:\\www.intel.com.

## 18. I/O Ports Not Available with Manual Peripheral Configuration

**PROBLEM:** Setting the Peripheral Configuration to Manual Mode in the BIOS Setup Program will cause the serial ports and the parallel port to become unavailable. The BIOS Setup Program will display the resource information for the ports and show them to be enabled.

**IMPLICATION:** The serial and parallel ports will not function. This problem is only seen in BIOS release 1.00.09.CV2.

**WORKAROUND:** Set the Peripheral Configuration to Auto in the BIOS Setup Program.

**STATUS:** This erratum was fixed in BIOS revision 1.00.10.CV2.

## 19. No Video Displayed Using Dual Video Configuration

**PROBLEM:** A limitation with the current video BIOS is that an add-in video card with VGA* disabled cannot be supported because the onboard video is set to sparse I/O mode.

**IMPLICATION:** A dual display configuration that requires an add-in video card to drive the second monitor in non VGA* mode cannot be used. This only occurs on motherboards that have the A3 stepping of the ATI264-VT video controller.

**WORKAROUND:** None.

**STATUS:** This erratum was fixed in the A4 stepping of the ATI264-VT video controller on PBA revision 648621-307, 655118-307 and 655232-306.

## *20. Slave on Secondary IDE Channel is not Disabled*

**PROBLEM:** If the IDE Device Configuration option in BIOS Setup is set to disable the secondary IDE slave device, it will not be disabled in the following configuration:

- ATAPI device attached as master to the secondary IDE connector.
- ATAPI device attached as slave to the secondary IDE connector.

**IMPLICATION:** In the above configuration, any ATAPI device attached as a secondary slave will remain enabled even if the BIOS setting for the secondary slave is set to disabled.

**WORKAROUND:** None.

**STATUS:** This erratum will not be fixed.

## *21. System BIOS Does Not Recognize Bootable USB Devices*

**PROBLEM:** The system BIOS does not recognize a USB keyboard or mouse during a system boot. A USB keyboard or mouse is not recognized until an operating system that supports USB is loaded.

**IMPLICATION:** 1. The user is not able to use a USB keyboard to enter the BIOS Setup or to respond to error messages that are displayed before an operating system with USB support is loaded.
2. The user is not able to use a USB keyboard or mouse with any operating system that does not have USB support.

**WORKAROUND:** Use a standard PS/2* style keyboard and mouse in any configuration where input is required before an operating system with USB support is loaded.

**STATUS:** This erratum will be fixed in a future BIOS revision.

## *22. Cannot Meet FCC Class B Requirements using Unshielded USB Cable*

**PROBLEM:** The motherboard will generate excessive electromagnetic radiation on unshielded USB cables, even if no device or a low speed (sub-channel) USB device is attached to the cable.

**IMPLICATION:** Systems based on this motherboard will not meet FCC Part 15 Class B requirements when unshielded USB cable is used. Although this condition is a violation of the USB v1.0 specification, it is not believed to have any effect on normal USB device operation.

**WORKAROUND:** Use USB devices with shielded cable that meet the requirements for high speed (fully-rated) USB devices.

**STATUS:** This erratum will not be fixed.

## 23. Windows* 95 SVGA Drivers Not Supported

**PROBLEM:** The A4 stepping of the onboard ATI* 264VT video controller will not support the use of the SVGA drivers available with Windows* 95 at 800 x 600 resolution.

**IMPLICATION:** When Windows 95 starts, the following error will be displayed:

"There is a problem with your display settings. The adapter type is incorrect, or the current settings do not work with your hardware"

Windows 95 will then display the Display Settings screen. This does not occur with the A3 stepping of the ATI 264 VT video controller.

**WORKAROUND:** Use the ATI 264VT drivers available at http://www.intel.com for all display settings.

**STATUS:** This erratum will not be fixed. This erratum only affects PBA 648621-307, 655118-307, 655232-306, 664638-306 and higher.

## 24. Floppy Drive Always Reported by System BIOS

**PROBLEM:** The system BIOS loads the default CMOS settings and does not check for the existence of a floppy drive. Whether a floppy drive is present or not, the BIOS will report that a floppy drive is connected to the system during POST and within BIOS Setup.

**IMPLICATION:** User will not be notified of floppy drive errors during POST as expected. The user will be unaware of a problem until the floppy drive is accessed.

**WORKAROUND:** None.

**STATUS:** This erratum only affects BIOS revision 1.00.013.CV2 and will be fixed in a future BIOS revision.

# SPECIFICATION CLARIFICATIONS

The Specification Clarifications listed in this section apply to the *Advanced/RH Motherboard Technical Product Specification* (Order Number 281809). All Specification Clarifications will be incorporated into a future version of that specification.

## *1. Support for Pentium® Processors with MMX™ Technology*

Support for Pentium® processors with MMX™ technology is available in PBA revision 664638-306 and higher.

## *2. Advanced Power Management (APM) Will Not Function as Expected with Universal Serial Bus (USB) Enabled*

The following will be added to Section 1.6.3, Universal Serial Bus and Section 3.1.8, Advanced Power Management:

Advanced Power Management will not function as expected when a USB keyboard or mouse is used. USB activity is not monitored by the APM event counter, therefore, activity from a USB keyboard or mouse will not keep the system awake or bring a system out of APM sleep mode. If a USB keyboard or mouse is being used, APM should be disabled.

## *3. PCI 2.1 Specification Optional Features*

The following will be added to Section 1.10.2, Memory/Expansion Connectors:

The following optional features in the PCI 2.1 Specification are not implemented on the Advanced/RH motherboard:

- Cache Support Pins **SBO#** and **SDONE** (Section 2.2.7)
- **PRSNTx#** (Section 2.2.8)
- **CLKRUN#** (Section 2.2.8)
- 64 Bit Bus Extension Pins (Section 2.2.9)
- 66 MHz support (Section 2.2.8)
- JTAG/Boundary scan (Section 2.2.10)

## *4. Administrator and User Passwords*

The following will be added to Section 3.5.1, Administrative and User Access Modes:

If an administrator password has been set, but no user password has been set, a user can create a password by entering BIOS Setup at boot by pressing the <F1> key and pressing enter at the administrator password prompt. Once in BIOS Setup, a user will be able to create a new user password.

Once defined, a user password can be cleared by either defining a new user password in Setup, or by moving the Password Clear jumper (J4L1-A) on the motherboard. See Section 1.11.12, Password Clear Jumper for more information on how to use this jumper.

# DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *Advanced/RH Motherboard Technical Product Specification* (Order Number 281809). All Documentation Changes will be incorporated into a future version of the appropriate Advanced/RH motherboard documentation.

## *1. Revision of Section 1.12, Reliability*

This section will be replaced in its entirety as follows:

The Mean-Time-Between-Failures (MTBF) data is calculated from predicted data @ 55 °C.

Motherboard MTBF: 72391 hours calculated

## *2. Revision of Section 5.1, Specifications*

The following note will be added to the table entry for PCI compliance:

NOTE: Certain optional PCI features have not been implemented on this motherboard, see section 1.14 for more information.

## *3. Revision of Section 1.11.3, Clear CMOS (J4L1-A)*

This section will be replaced in its entirety as follows:

Allows CMOS settings to be reset to default values by moving the jumper from pins 4-5 to pins 5-6 and turning the system on. When the system reports that “NVRAM cleared by jumper”, the system can be turned off, and the jumper should be returned to the 4-5 position to restore normal operation. Default is for this jumper to be on pins 4-5.

Caution: This procedure should only be done if, after a BIOS update, the system does not boot to a point where BIOS Setup can be entered or if, after CMOS default settings have been restored from within the Setup program, the system does not boot to the operating system.

## *4. Revision of Section 1.14.1, Power Supply Considerations*

The following will be added to the list of requirements that a power supply must meet

- A pull-up resistor of ~5 K Ohms connecting PS_ON# to +5 V Standby

## *5. Revision of Section 1.6.1, 82439HX Xcelerated Controller (TXC)*

The fourth bullet in this section will be replaced in its entirety as follows:

- Fully synchronous PCI bus interface
    - — 25/30/33 MHz
    - — PCI to DRAM data transfers up to or greater than 100 MB/sec
    - — Up to 4 PCI masters in addition to the PIIX3

## 6. Revision of Section 3.4.15.8, Critical Events in Log

This section will be replaced in its entirety as follows:

The bottom of the Event Log screen includes several information fields that display information about the date and time of the last event of a specific type, as well as a count of how many events of that type are logged.

Table 45 lists the event types that are available.

**Table 45. Event Log Types**

| Event Type | Detail | |
|---|---|---|
| Single Bit ECC Events | Number of errors logged | None *(initial value)* |
| Multiple Bit ECC Events | Number of errors logged | None *(initial value)* |
| POST Errors | Number of errors logged during POST | None *(initial value)* |

## 7. Addition of Onboard Video IRQ Section

The following section will be added after Section 3.4.12.3:

**ONBOARD VIDEO IRQ**

Enables or disables the allocation of an interrupt to the onboard video controller. The options are:

- Disabled
- Enabled (**default**)