intel®

Advanced/EV Motherboard Specification Update

The Advanced/EV motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
August 1996	-001	This document is the first Specification Update for the Intel Advanced/EV motherboard.
September 1996	-002	Modified Errata 3-4, Added Documentation Change 1.
October 1996	-003	Added Specification Change 1, Erratum 6.
December 1996	-004	Added Erratum 7.
April 1997	-005	Added Errata 8-9 and PBA/BIOS Table.
August 1997	-006	Added Erratum 10, Specification Change 2 and Documentation Changes 2-3.

intel®

PREFACE

This document is an update to the specifications contained in the *Advanced/EV Motherboard Technical Product Specification* (Order Number 281835). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Pentium® Processor Specification Update* (Order Number 242480) for specification updates concerning the Pentium processor. Items contained in the *Pentium Processor Specification Update* that either do not apply to the Advanced/EV motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *82430FX PCIset Specification Update* (Order Number 297733) for specification updates concerning the 82430FX PCIset. Items contained in the *82430FX PCIset Specification Update* that either do not apply to the Advanced/EV motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the Advanced/EV motherboard's behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision level are present on all motherboards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

**Specification Update for
Advanced/EV Motherboards**

GENERAL INFORMATION

Basic Advanced/EV Motherboard Identification Information

AA Revision	PBA Revision	82430FX PCIset Stepping	BIOS Revision	Notes
	636348-401	A1	1.00.02.CB0	1, 2, 5
	636348-402	A1	1.00.02.CB0	1, 2, 5
	636348-501	A1	1.00.02.CB0	1, 2, 5
	636348-502	A1	1.00.02.CB0	1, 2, 5
	636348-503	A1	1.00.02.CB0	1, 2, 5
636682-001 639454-001	636348-504	A1	1.00.03.CB0	1, 2, 5
	636635-501	A2	1.00.02.CB0	1, 3, 5
	636635-502	A2	1.00.02.CB0	1, 3, 5
	636635-503	A2	1.00.03.CB0	1, 3, 5
	636635-804	A2	1.00.03.CB0	1, 3, 5
	636635-824	A1	1.00.03.CB0	1, 4, 5
	636635-825	A1	1.00.04.CB0	1, 4, 5
636601-001 647695-001	636635-845	A2	1.00.04.CB0	1, 3, 5
	638859-500	A1	1.00.02.CB0	1, 2, 5
	638859-501	A1	1.00.02.CB0	1, 2, 5
	638859-502	A1	1.00.02.CB0	1, 2, 5
	638859-503	A1	1.00.02.CB0	1, 2, 5
639060-001	638859-504	A1	1.00.03.CB0	1, 2, 5
	641508-700	A2	1.00.02.CB0	1, 3, 5
	641508-701	A2	1.00.02.CB0	1, 3, 5
	641508-702	A2	1.00.03.CB0	1, 3, 5
	641508-800	A2	1.00.02.CB0	1, 3, 5
	641508-801	A2	1.00.02.CB0	1, 3, 5
	641508-802	A2	1.00.03.CB0	1, 3, 5
	641508-822	A1	1.00.03.CB0	1, 4, 5
	641508-823	A1	1.00.04.CB0	1, 4, 5
639831-001 639831-002	641508-843	A2	1.00.04.CB0	1, 3, 5
	641961-800	A2	1.00.02.CB0	1, 3, 5
	641961-801	A2	1.00.03.CB0	1, 3, 5

intel

AA Revision	PBA Revision	82430FX PCIset Stepping	BIOS Revision	Notes
	641961-821	A1	1.00.03.CB0	1, 4, 5
644385-001	641961-822	A1	1.00.04.CB0	1, 4, 5
	641961-842	A2	1.00.04.CB0	1, 3, 5
	646254-800	A2	1.00.03.CB0	1, 3, 5
	646254-820	A1	1.00.03.CB0	1, 4, 5
	646254-821	A1	1.00.04.CB0	1, 4, 5
646258-001	646254-841	A2	1.00.04.CB0	1, 3, 5

NOTES:
1. The PBA number is found on a small label on the component side of the board.
2. The 82430FX PCIset kit used on this PBA revision consists of three different components as follows:

Device	Stepping	S-Spec Numbers
82437FX	A1	SZ968
82438FX	A1	SZ969
82371FB	A1	SZ997

3. The 82430FX PCIset kit used on this PBA revision consists of three different components as follows:

Device	Stepping	S-Spec Numbers
82437FX	A2	SZ999
82438FX	A1	SZ969
82371FB	A1	SZ997

4. The 82430FX PCIset kit used on this PBA revision consists of three different components as follows:

Device	Stepping	S-Spec Numbers
82437FX	A1	SZ966
82438FX	A1	SZ965
82371FB	A1	SZ964

5. The following errata contained in Part I of the *Pentium® Processor Specification Update* (Order Number 242480) either do not apply to the Advanced/EV motherboard or have been worked around in this PBA and/or BIOS revision: 5, 7, 9-11, 13-14, 16-17, 29, 31, 34, 36-37, 39, 40, 46, 48-50, 58, 60-64, 66-67, 69, 71-79, all DP errata, all AP errata, all TCP errata. All other errata in Part I may apply to this revision level of the motherboard, depending on the stepping of the processor or the specific software that is being executed. Also, some of these errata apply only to motherboards being used in an application development environment. For specific details of any erratum please refer to the *Pentium Processor Specification Update.*

4

intel.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Advanced/EV motherboard. Intel intends to fix some of the errata in a future revision of the motherboard, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the motherboard or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	SPECIFICATION CHANGES
1	Doc	The BIOS does not support a bootable CD-ROM

NO.	PLANS	ERRATA
1	NoFix	Locked PCI cycles for the A-1 stepping of the 82437FX TSC component do not terminate properly
2	NoFix	Onboard Creative Labs Vibra16* audio controller produces noise with games
3	Fixed	Onboard Creative Labs Vibra16 audio controller fails to initialize low DMA channel
4	Fixed	Using the options "Use ICU" and PnPOS="Windows95 TM" causes error
5	NoFix	Non-English keyboard support in DOS disables turbo/deturbo
6	NoFix	Onboard Creative Labs Vibra16S* audio does not release resources when disabled
7	NoFix	CMOS checksum may be lost if power is cycled during boot
8	NoFix	BIOS does not support no-emulation mode for CD-ROM boot
9	NoFix	Slave on secondary IDE channel is not disabled
10	Fixed	BIOS SETUP does not recognize February 29, 2000 as a valid date

NO.	PLANS	SPECIFICATION CLARIFICATIONS
1	Doc	Mono recording uses left channel only
2	Doc	Administrator and user passwords

NO.	PLANS	DOCUMENTATION CHANGES
1	Doc	Revision of 166 MHz jumper settings in Appendix B
2	Doc	Revision of "Clear CMOS - Switch 4" section
3	Doc	Revision of "Peripheral Component Interconnect (PCI) PCIset" section

The errata described in this specification update apply to combinations of PBA revision and BIOS revision as shown in the table below. Descriptions of the individual errata referred to by number in the table below are found in the ERRATA section of this document.

PBA Revision	BIOS Revision	Errata That Apply
636348-401	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1,2 5-9
636348-402	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1,2 5-9
636348-501	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1,2 5-9
636348-502	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1,2 5-9
636348-503	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1,2 5-9
636348-504	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1,2 5-9

PBA Revision	BIOS Revision	Errata That Apply
636635-501	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9
636635-502	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9
636635-503	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9
636635-804	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9
636635-824	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9
636635-825	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9
636635-845	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9

PBA Revision	BIOS Revision	Errata That Apply
638859-500	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9
638859-501	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9
638859-502	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9
638859-503	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9
638859-504	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9
641508-800	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9
641508-801	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9

PBA Revision	BIOS Revision	Errata That Apply
641508-802	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9
641508-800	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9
641508-801	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9
641508-802	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9
641508-822	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9
641508-823	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9
641508-843	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9

PBA Revision	BIOS Revision	Errata That Apply
641961-800	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9
641961-801	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9
641961-821	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9
641961-822	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9
641961-842	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9
646254-800	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9
646254-820	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9

PBA Revision	BIOS Revision	Errata That Apply
646254-821	1.00.02.CB0	1-10
	1.00.03.CB0	1-2, 5-10
	1.00.04.CB0	1-2, 5-10
	1.00.05.CB0	1-2, 5-9
	1.00.06.CB0	1-2, 5-9
646254-841	1.00.02.CB0	2-10
	1.00.03.CB0	2, 5-10
	1.00.04.CB0	2, 5-10
	1.00.05.CB0	2, 5-9
	1.00.06.CB0	2, 5-9

NOTE:

‡   This combination of BIOS revision and PBA revision has not undergone regression testing. Use of a PBA with down-revision BIOS is an untested combination and is undertaken at the user's risk.

intel®

SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the Advanced/EV *Motherboard Technical Product Specification* (Order Number 281835). All Specification Changes will be incorporated into a future version of that specification.

1. *The BIOS Does Not Support a Bootable CD-ROM*

The option to allow the system to boot from a CD-ROM drive will be removed from the description of the BIOS Setup Program.

intel®

ERRATA

1.   Locked PCI Cycles for the A-1 Stepping of the 82437FX TSC Component Do Not Terminate Properly

PROBLEM: With the A-1 stepping of the 82437FX system controller (TSC) component, locked PCI cycles do not terminate properly if the target device signals Retry after the LOCK# signal has been asserted. If another PCI bus master device accesses memory under these conditions, the memory access will never be completed and the system will lock up. This lockup has only been seen with certain VGA* video cards when the video driver uses the XCHG instruction.

IMPLICATION: The system video may lock at certain times with Microsoft Windows* 95 if the default VGA driver is used.

WORKAROUND: Use the alternate Windows 95 VGA driver (named VGA.DRV) found in the \drivers\display\vga directory on the Windows 95 CD-ROM. Copy this into the windows\system directory on the hard drive.

STATUS: This erratum was present in the PBA revisions referenced in notes 2 and 4 in the general information section.

2.   Onboard Creative Labs Vibra16* Audio Controller Produces Noise with Games

PROBLEM: The onboard Creative Labs Vibra16* audio controller produces noise in several games. The noise is either an audio pop or static noise.

IMPLICATION: The games will run correctly but the user may find the noise distracting.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

3.   Onboard Creative Labs Vibra16 Audio Controller Fails to Initialize Low DMA Channel

PROBLEM: The Onboard Creative Labs Vibra16 audio controller fails to initialize a low DMA channel during the setup for Microsoft Windows 95. The following error message is displayed: "INVALID BLASTER = /D:???."

IMPLICATION: The system will not play WAV files.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.03.CB0.

4.   Using the Setup Options "UseICU" and PnPOS="Windows95 TM" Together Causes Boot Failure

PROBLEM: Booting Microsoft Windows 95 with the following combination of options selected from the Plug and Play Configuration section of the Advanced menu:

Configuration Mode: Use ICU

13

Boot with PnP OS: Windows95 TM

causes the error message, "Primary Boot Device Not Found, Press F1 for Setup, Esc to Boot."

IMPLICATION: Microsoft Windows* 95 cannot boot with these options.

WORKAROUND: Choose a different combination of options from this menu. However, other combinations may not initialize plug and play devices correctly. Users should upgrade to a BIOS revision in which this erratum is fixed.

STATUS: This erratum was fixed in the BIOS revision 1.00.03.CB0.

5. Non-English Keyboard Support in DOS Disables Turbo/Deturbo

PROBLEM: When using non-English keyboard support in DOS, the control keys CTRL-ALT+ and CTRL-ALT- no longer set the Turbo or Deturbo options.

IMPLICATION: The Turbo and Deturbo options cannot be set with non-English support enabled in DOS.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

6. Onboard Creative Vibra16S* Audio Does Not Release Resources When Disabled

PROBLEM: There is a conflict with assignment of the I/O address between the FM synthesizer in the onboard Creative Labs Vibra16S* audio controller and the FM synthesizer of a user-supplied add-in sound card.

IMPLICATION: An add-in card cannot be used to provide FM synthesis under any operating system.

WORKAROUND: Use the on-board Creative Labs Vibra16S FM synthesizer.

STATUS: This erratum will not be fixed.

7. CMOS Checksum May Be Lost If Power Is Cycled During Boot

PROBLEM: If the computer power is turned off during a short portion of the boot process, the CMOS checksum byte is not updated. The next time the computer is turned on, the message "CMOS Checksum Invalid" will be displayed.

IMPLICATION: When the message is displayed, the correct checksum has already been recalculated and stored. No user action is required to recover from the error. If the additional message:

> Date and Time Not Set
> Press <F1> for Setup, <Esc> to Boot

is displayed, the user must reset the current date and time using the BIOS Setup program.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

8.   BIOS Does Not Support No-Emulation Mode for CD-ROM Boot

PROBLEM: The system BIOS does not support booting from an "El Torito" bootable CD-ROM using the no-emulation mode format.

IMPLICATION: Booting from a CD-ROM using no emulation mode is not supported. For example, Microsoft Windows* NT* version 4.0 uses no-emulation mode for its boot CD-ROM.

WORKAROUND: Boot the computer from a floppy or hard disk, then install or run the program from the CD-ROM.

STATUS: This erratum will not be fixed.

9.   Slave on Secondary IDE Channel is not Disabled

PROBLEM: If the IDE Device Configuration option in BIOS Setup is set to disable the secondary IDE slave device, it will not be disabled in the following configuration:

- ATAPI device attached as master to the secondary IDE connector.

- ATAPI device attached as slave to the secondary IDE connector.

IMPLICATION: In the above configuration, any ATAPI device attached as a secondary slave will remain enabled even if the BIOS setting for the secondary slave is set to disabled.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

10.   BIOS SETUP Does Not Recognize February 29, 2000 As a Valid Date

PROBLEM: The BIOS Setup program will not allow the system date to be set to Feb 29, 2000.

IMPLICATION: Any program that uses the system time and date stamps to determine when to perform some activity will not perform that scheduled activity. Date and time stamps for files created on these dates will be incorrect.

WORKAROUND: If the system BIOS has not been upgraded, the system date will have to be reset to the correct date on March 1, 2000.

STATUS: This erratum was fixed in BIOS revision 1.00.05.CB0.

intel®

SPECIFICATION CLARIFICATIONS

The Specification Clarifications listed in this section apply to the *Advanced/EV Technical Product Specification* (Order Number 281835). All Specification Clarifications will be incorporated into a future version of that specification.

1.   *Mono Recording Uses Left Channel Only*

The following will be added after paragraph three of the subsection *audio subsystem*:

When the audio is set to record in mono mode, only the left channel of a stereo sound source will be recorded.

2.   *Administrator and User Passwords*

The following will be added to Administrative and User Access Modes:

If an administrator password has been set, but no user password has been set, a user can create a password by entering BIOS Setup at boot by pressing the <F1> key and pressing enter at the administrator password prompt. Once in BIOS Setup, a user will be able to create a new user password.

Once defined, a user password can be cleared by either defining a new user password in Setup, or by moving the Password Clear switch (3) on the motherboard. See Password Clear - Switch 3 for more information on how to use this switch.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *Advanced/EV Motherboard Technical Product Specification* (Order Number 281835). All Documentation Changes will be incorporated into a future version of the appropriate Advanced/EV motherboard documentation.

1.   Revision of 166 MHz Jumper Settings in Appendix B

Table B-1 External CPU Clock Speed Switch Settings, will be replaced in its entirety to revise the jumper settings for 166 MHz Pentium® processors:

External Bus Speed	Bus Clock Multiplier	Processor Speed (MHz)	Switch 6	Switch 7	Switch 8	J1N1
50	1.5	75	off	on	off	4/5
60	1.5	90	off	off	off	4/5
66	1.5	100	off	on	on	4/5
60	2	120	on	off	off	4/5
66	2	133	on	on	on	4/5
60	5/2	150	on	off	off	5/6
66	5/2	166	on	on	on	5/6
66	3	200	off	on	on	5/6

Table B-1 External CPU Clock Speed Switch Settings

2.   Revision of Clear CMOS - Switch 4 Section

This section will be replaced in its entirety as follows:

Allows CMOS settings to be reset to default values by moving the switch from OFF to ON and turning the system on. When the system reports that "NVRAM cleared by switch", the system can be turned off, and the switch should be returned to the OFF position to restore normal operation. Default is for this switch to be in the off position.

Caution: This procedure should only be done if, after a BIOS update, the system does not boot to a point where BIOS Setup can be entered or if, after CMOS default settings have been restored from within the Setup program, the system does not boot to the operating system.

3.   Revision of Peripheral Component Interconnect (PCI) PCIset Section

The fourth bullet in the first column in this section will be replaced in its entirety as follows:

•   Fully synchronous PCI bus interface

⎯   25/30/33 MHz

⎯   PCI to DRAM data transfers up to or greater than 100 MB/sec

— PCI to DRAM posting of 12 Dwords

— 5 Dword buffers for CPU to PCI write posting

— 4 Dword buffers for PCI to Memory bus master cycles

— Support for up to 5 PCI masters