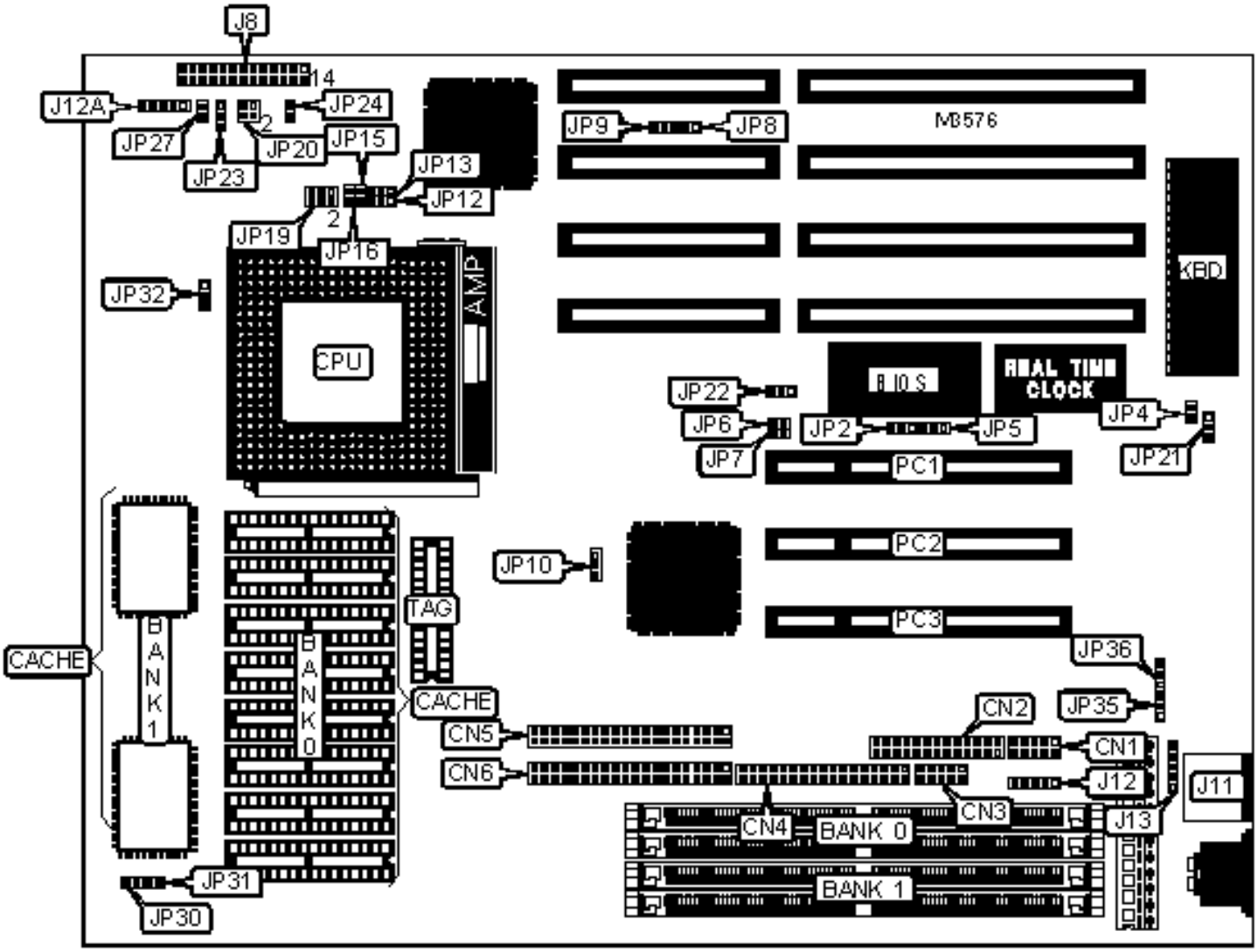
PIONEX TECHNOLOGIES, INC.

MB-8500TAC-A (VER. 5)

Configuration



CONNECTIONS

Purpose	Location	Purpose	Location
Serial port 1	CN1	Green PC connector	J8 pins 17 & 18
Parallel port	CN2	IDE interface LED	J8 pins 20 & 21
Serial port 2	CN3	VCC ground connector	J8 pins 25 & 26
Floppy drive interface	CN4	PS/2 mouse port	J11
IDE interface 2	CN5	IR connector	J12
IDE interface 1	CN6	IR connector	J12A
Speaker	J8 pins 1 - 4	PS/2 mouse interface	J13
Power LED & keylock	J8 pins 5 - 9	Chassis fan power	JP19
Turbo LED	J8 pins 10 & 11	32-bit PCI slots	PC1 - PC3
Reset switch	J8 pins 12 & 13		

USER CONFIGURABLE SETTINGS

	Function	Label	Position
»	Factory configured - do not alter	JP2	Unidentified
»	CMOS memory normal operation	JP4	Open
	CMOS memory clear	JP4	Closed
	Flash BIOS voltage select 12v	JP5	Pins 2 & 3 closed
	Flash BIOS voltage select 5v	JP5	Pins 1 & 2 closed
	BIOS type select EPROM	JP5	Open
	Secondary IDE IRQ select IRQ15	JP8	Pins 1 & 2 closed
	Secondary IDE IRQ select IRQ through PCI	JP8	Pins 2 & 3 closed
	Primary IDE IRQ14 enabled	JP9	Closed
	Primary IDE IRQ14 disabled	JP9	Open
»	Factory configured - do not alter	JP12	Unidentified

»	Factory configured - do not alter	JP13	Unidentified
»	Factory configured - do not alter	JP22	Pins 2 & 3 closed
»	Factory configured - do not alter	JP30	Pins 1 & 2 closed
»	Factory configured - do not alter	JP32	Unidentified

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
8MB	(2) 1M x 36	None
16MB	(2) 2M x 36	None
16MB	(2) 1M x 36	(2) 1M x 36
24MB	(2) 1M x 36	(2) 2M x 36
32MB	(2) 4M x 36	None
32MB	(2) 2M x 36	(2) 2M x 36
40MB	(2) 1M x 36	(2) 4M x 36
48MB	(2) 2M x 36	(2) 4M x 36
64MB	(2) 8M x 36	None
64MB	(2) 4M x 36	(2) 4M x 36

DRAM CONFIGURATION (CON'T)		
Size	Bank 0	Bank 1
72MB	(2) 1M x 36	(2) 8M x 36
80MB	(2) 2M x 36	(2) 8M x 36
96MB	(2) 4M x 36	(2) 8M x 36
128MB	(2) 8M x 36	(2) 8M x 36
Note: Board accepts EDO memory.		

CACHE CONFIGURATION

Size	Bank 0	Bank 1	TAG
256KB (A)	None	(2) 32K x 32	None
256KB (B)	(8) 32K x 8	None	(1) 8K x 8
512KB (A)	(8) 64K x 8	None	(1) 16K/32K x 8
512KB (B)	(8) 64K x 8	None	(1) 16K x 8

Note: Board will either have asynchronous or synchronous cache installed.

CACHE JUMPER CONFIGURATION

Size	JP10
None	Open
256KB (B) (STD/Aster TAG)	Open
512KB (A) (STD TAG)	Pins 1 & 2 closed
512KB (B) (Aster TAG)	Pins 2 & 3 closed

CPU SPEED SELECTION (CYRIX)

CPU speed	Clock speed	Multiplier	JP6	JP7	JP15	JP16	JP21
120MHz	50MHz	2x	Open	Open	Open	Closed	1 & 2
133MHz	55MHz	2x	Open	Closed	Open	Closed	1 & 2
150MHz	60MHz	2x	Closed	Closed	Open	Closed	2 & 3
166MHz	66MHz	2x	Closed	Open	Open	Closed	2 & 3

Note: Pins designated should be in the closed position.

CPU SPEED SELECTION (AMD)

CPU speed	Clock speed	Multiplier	JP6	JP7	JP15	JP16	JP21
75MHz	66MHz	1x	Closed	Open	Open	Closed	2 & 3

75MHz	50MHz	1.5x	Open	Open	Open	Open	1 & 2
90MHz	55MHz	1.5x	Open	Closed	Open	Open	2 & 3
90MHz	60MHz	1.5x	Closed	Closed	Open	Open	2 & 3
100MHz	66MHz	1.5x	Closed	Open	Open	Open	2 & 3
Note: Pins designated should be in the closed position.							

CPU SPEED SELECTION (INTEL)

CPU speed	Clock speed	Multiplier	JP6	JP7	JP15	JP16	JP21
75MHz	50MHz	1.5x	Open	Open	Open	Open	1 & 2
90MHz	60MHz	1.5x	Closed	Closed	Open	Open	2 & 3
100MHz	66MHz	1.5x	Closed	Open	Open	Open	2 & 3
120MHz	60MHz	2x	Closed	Closed	Open	Closed	2 & 3
133MHz	66MHz	2x	Closed	Open	Open	Closed	2 & 3
150MHz	60MHz	2.5x	Closed	Closed	Closed	Closed	2 & 3
166MHz	66MHz	2.5x	Closed	Open	Closed	Closed	2 & 3
180MHz	60MHz	3x	Closed	Closed	Closed	Open	2 & 3
200MHz	66MHz	3x	Closed	Open	Closed	Open	2 & 3
Note: Pins designated should be in the closed position.							

CPU TYPE SELECTION

Type	JP20	JP23	JP24
CX M1	Pins 1 & 2, 3 & 4 closed	Pins 1 & 2 closed	Open
AM K5	Pins 1 & 2, 3 & 4 closed	Pins 1 & 2 closed	Open
P54C/CQS/CT	Pins 1 & 2, 3 & 4 closed	Pins 1 & 2 closed	Open
P55C/CT	Open	Pins 2 & 3 closed	Closed

CPU VOLTAGE SELECTION	
Voltage	JP27
3.4v	Closed
3.5v	Open

SERIAL PORT 2 SELECTION		
Setting	JP35	JP36
Used as COM2	Pins 1 & 2 closed	Pins 1 & 2 closed
Used as IR connector	Pins 2 & 3 closed	Pins 2 & 3 closed