ACER, INC.

V60N
Configuration


## CONNECTIONS

| Purpose | Location | Purpose | Location |
| :---: | :---: | :---: | :---: |
| Software shutdown connector | CN1 | Reset switch | CN11 |
| Serial port 1 | CN2 | PS/2 mouse port | CN12 |
| IDE interface 1 | CN3 | Chassis fan power | JP2 |
| IDE interface 2 | CN4 | Software power key | JP6 |
| Serial port 2 | CN5 | Turbo LED | JP7 |
| Parallel port | CN6 | Power LED \& | JP8 |
| Floppy drive interface | CN7 | Green PC connector | JP11/pins 1 \& 3 |
| USB connector | CN8 | Reset switch | JP11/pins 2 \& 4 |
| IR connector | CN9 | 32 -bit PCI slots | PC1-PC4 |
| IDE interface LED | CN10 | RAID slot | SL1 |

USER CONFIGURABLE SETTINGS

|  | Function | Label | Position |
| :---: | :---: | :---: | :---: |
| " | Password disabled | JP1 | Pins 2 \& 3 closed |
|  | Password enabled | JP1 | Pins 1 \& 2 closed |
| " | Factory configured - do not alter | JP3 | Unidentified |
| " | BIOS type select 128KB | JP4 | Pins 1 \& 2 closed |
|  | BIOS type select 256KB | JP4 | Pins 2 \& 3 closed |
|  | Software select shutdown mode | JP14 | Pins 1 \& 2 closed |
|  | Software select normal mode | JP14 | Pins 2 \& 3 closed |
|  | Flash BIOS voltage select 12 v | JP15 | Pins 1 \& 2 closed |
|  | Flash BIOS voltage select 5 v | JP15 | Pins 2 \& 3 closed |


| Size | Bank 0 | Bank 1 | Bank 2 |
| :---: | :---: | :---: | :---: |
| 8Мв | (1) $1 \mathrm{M} \times 64$ | None | None |
| 16MB | (1) $2 \mathrm{M} \times 64$ | None | None |
| 16MB | (1) $1 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ | None |
| 24 MB | (1) $2 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ | None |
| 24 MB | (1) $1 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ |
| з2мв | (1) $4 \mathrm{M} \times 64$ | None | None |
| з2мв | (1) $2 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ |
| з2мв | (1) $2 \mathrm{M} \times 64$ | (1) $2 \mathrm{M} \times 64$ | None |
| 40MB | (1) $4 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ | None |

SIMM CONFIGURATION (CON'T)

| Size | Bank 0 | Bank 1 | Bank 2 |
| :---: | :---: | :---: | :---: |
| 40MB | (1) $2 \mathrm{M} \times 64$ | (1) $2 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ |
| 48MB | (1) $4 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ |
| 48MB | (1) $4 \mathrm{M} \times 64$ | (1) $2 \mathrm{M} \times 64$ | None |
| 48MB | (1) $2 \mathrm{M} \times 64$ | (1) $2 \mathrm{M} \times 64$ | (1) $2 \mathrm{M} \times 64$ |
| 56MB | (1) $4 \mathrm{M} \times 64$ | (1) $2 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ |
| 64MB | (1) $8 \mathrm{M} \times 64$ | None | None |
| 64MB | (1) $4 \mathrm{M} \times 64$ | (1) $2 \mathrm{M} \times 64$ | (1) $2 \mathrm{M} \times 64$ |
| 64MB | (1) $4 \mathrm{M} \times 64$ | (1) $4 \mathrm{M} \times 64$ | None |
| 72MB | (1) $8 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ | None |
| 72MB | (1) $4 \mathrm{M} \times 64$ | (1) $4 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ |
| 80MB | (1) $8 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ | (1) $1 \mathrm{M} \times 64$ |
| 80MB | (1) $8 \mathrm{M} \times 64$ | (1) $2 \mathrm{M} \times 64$ | None |
| 80MB | (1) $4 \mathrm{M} \times 64$ | (1) $4 \mathrm{M} \times 64$ | (1) $2 \mathrm{M} \times 64$ |

## CPU SPEED SELECTION

| CPU speed | Clock speed | Multiplier | JP5/1 | JP5/2 | JP5/3 | JP5/4 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 150 MHz | ${ }^{60 \mathrm{MHz}}$ | ${ }^{2.5 x}$ | on | off | off | off |
| 166 MHz | ${ }^{66 \mathrm{MHz}}$ | ${ }^{2.5 x}$ | off | on | off | off |
| 180 MHz | ${ }^{60 \mathrm{MHz}}$ | ${ }^{3 x}$ | on | off | off | off |
| 200 MHz | ${ }^{66 \mathrm{MHz}}$ | ${ }^{3 x}$ | off | on | off | off |

CPU SPEED SELECTION (CON'T)

| CPU speed | Clock speed | Multiplier | JP5/5 | JP5/6 | JP5/7 | JP5/8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 150МНz | 60MHz | 2.5x | on | Off | on | on |
| 166MHz | ${ }^{66 \mathrm{MHz}}$ | 2.5x | On | Off | On | on |
| 180MHz | 60MH2 | 3 x | on | on | Off | on |
| 200 MHz | ${ }^{66 \mathrm{MHz}}$ | 3 x | On | On | Off | on |

## CPU VOLTAGE SELECTION

| Voltage | JP9 | JP10 | JP12 | JP13 |
| :---: | :---: | :---: | :---: | :---: |
| 2.5 v | Pins 2 \& 3 closed | Pins 1 \& 2 closed | Pins 1 \& 2 closed | Pins 1 \& 2 closed |
| 2.6 v | Pins 1 \& 2 closed | Pins 2 \& 3 closed | Pins 1 \& 2 closed | Pins 1 \& 2 closed |
| $2.7 v$ | Pins 2 \& 3 closed | Pins 1 \& 2 closed | Pins 2 \& 3 closed | Pins 2 \& 3 closed |
| 2.8 v | Pins 1 \& 2 closed | Pins 2 \& 3 closed | Pins 2 \& 3 closed | Pins 1 \& 2 closed |
| 2.9v | Pins 1 \& 2 closed | Pins 2 \& 3 closed | Pins 1 \& 2 closed | Pins 2 \& 3 closed |
| 3.0 v | Pins 1 \& 2 closed | Pins 2 \& 3 closed | Pins 2 \& 3 closed | Pins 2 \& 3 closed |
| 3.1 v | Pins 2 \& 3 closed | Pins 2 \& 3 closed | Pins 1 \& 2 closed | Pins 1 \& 2 closed |
| $3.2 v$ | Pins 1 \& 2 closed | Pins 1 \& 2 closed | Pins 2 \& 3 closed | Pins 2 \& 3 closed |
| 3.3 v | Pins 2 \& 3 closed | Pins 2 \& 3 closed | Pins 2 \& 3 closed | Pins 1 \& 2 closed |


| 3.4 v | Pins 2 \& 3 closed | Pins 2 \& 3 closed | Pins $1 \& 2$ closed |
| :---: | :---: | :---: | :---: |
| 3.5 v | Pins $2 \& 3$ closed | Pins $2 \& 3$ closed | Pins $2 \& 3$ closed $2 ~ 3$ closed |

