# AR-B9637
# INDUSTRIAL GRADE
# CPU BOARD
# User’ s Guide

Edition: 1.2
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# 0.PREFACE

## 0.1 COPYRIGHT NOTICE AND DISCLAIMER

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## 0.2 WELCOME TO THE AR-B9637 CPU BOARD

This guide introduces the Acrosser AR-B9637 CPU board.

The following information describes this card’s functions, features, and how to start, set up and operate your AR-B9637. General system information can also be found here.

## 0.3 BEFORE YOU USE THIS GUIDE

If you have not already installed this AR-B9637, refer to the Chapter 3, “Setting Up The System” in this guide. Check the packing list, make sure the accessories are complete.

The AR-B9637 diskette provides the newest information about the card**. Please refer to the files of the enclosed utility diskette**. It contains the modification, hardware & software information, and it has updates to product functions that may not be mentioned here.

## 0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires servicing, contact the dealer from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original packaging for this purpose.

You can assure efficient servicing of your product by following these guidelines:

1. Include your name, address, daytime telephone and facsimile numbers and E-mail.
2. A description of the system configuration and/or software at the time is malfunction,
3. And a brief description of the symptoms.

## 0.5 TECHNICAL SUPPORT AND USER COMMENTS

User’s comments are always welcome as they assist us in improving the usefulness of our products and the understanding of our publications. They form a very important part of the input used for product enhancement and revision.

We may use and distribute any of the information you supply in any way we believe appropriate without incurring any obligation. You may, of course, continue to use the information you supply.

If you have suggestions for improving particular sections or if you find any errors, please indicate the manual title and book number.

Please send your comments to Acrosser Technology Co., Ltd. or your local sales representative.

Internet electronic mail to: **webmaster@acrosser.com**

Check our FAQ sheet for quick fixes to known technical problems.

## 0.6 ORGANIZATION

This manual covers the following topics (see the Table of Contents for a detailed listing):

- Chapter 1, “Overview”, provides an overview of the system features and packing list.
- Chapter 2, “System Controller” describes the major structure.
- Chapter 3, “Setting Up the System”, describes how to adjust the jumper, and the connector’s settings.
- Chapter 4, “Installation”, describes setup procedures including information on the utility diskette.
- Chapter 5, “BIOS Console”, provides the BIOS options settings.

## 0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.

Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always best to safeguard against accidents that may result in expensive repairs. The following measures should be sufficient to protect your equipment from static discharge:

- Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
- When unpacking and handling the board or other system components, place all materials on an anti-static surface.
- Be careful not to touch the components on the board, especially the “golden finger” connectors on the bottom of the board.

# 1. OVERVIEW

This is a AR-B9637 Pentium Grade Firewall CPU Board with Ethernet, DOM.
This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Specification
- Packing List
- Features

## 1.1 SPECIFICATION

- CPU : NS GEODE GX1/GXLV
- Chipset:Cyrix CS5530A
- RAM Memory:Onboard 32MB SDRAM
- Flash Disk:Supports one socket for DiskOnModule
- Ethernet:3 x 10M/100M-Base2 with RJ-45 connector (PCI BUS)
- BIOS:AMI or AWARD flash BIOS
- RTC:BQ3287MT Chips
- Speaker:Supports external speaker
- LED Indicator:Power, HD and LAN LEDs
- Jumper:3 x 2 Jumper select base clock and CPU clock multiplier
- Power Connector:One 3-pin connector
- Power Req.:5V, 2.5A
- PC Board:6 layers,EMI considered
- Dimensions:178 mm x 102 mm

## 1.2 PACKING LIST

Some accessories are included with the system. Before you begin installing your AR-B9637 board, take a moment to make sure that the following items have been included inside the AR-B9637 package.

- The quick setup manual
- 1 AR-B9637 all-in-one single CPU board
- AR-B9461 I/O Board (extension card)
- Software utility diskettes.

## 1.3 FEATURES

The system provides a number of special features that enhance its reliability, ensure its long-term availability, and improve its expansion capabilities, as well as its hardware structure.

- CPU NS GEODE GX1/GXLV
- Cyrix CS5530A Chipset
- Onboard 32MB SDRAM
- Supports DOM Flash Disk
- 3 x 10/100M-Base2 Ethernet
- AMI or AWARD flash BIOS
- Power Req.: 5V, 2.5A
- Dimensions: 178 mm x 102 mm

# 2. SYSTEM CONTROLLER

This chapter describes the main structure of the AR-B9637 CPU board. The following topics are covered:

- Microprocessors
- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Serial Port
- Parallel Port

## 2.1 MICROPROCESSOR

The AR-B9637 uses the NS GEODE GX1/GXLV CPU (or other GXM CPUs), it is an advanced 32-bit x86 compatible processor offering high performance, fully accelerated 2D graphics, a 64-synchronous DRAM controller and a PCI bus controller, all on a single chip. This latest generation of the MediaGX processor enables a new class of premium performance notebook/desktop, and IPC computer designs.

The MediaGX MMX enhanced processor companion chips provide advanced video and audio functions and permit direct interface to memory. This high-performance 64-bit processor is x86 instruction set compatible and supports MMX technology.

This processor is the latest member of the NS MediaGX family, offering high performance, fully accelerated 2D graphics, synchronous memory interface and a PCI bus controller, all on a single chip. As described in separate manuals, the CS5520 and the CS5530 I/O Companion chips fully enable the features of the MediaGX processor with MMX support. These features include full VGA and VESA video, 16-bit stereo sound, IDE interface, ISA interface, SMM power management, and AT compatibility logic. In addition, the newer CS5530 provides an Ultra DMA/33 interface, MPEG2 assist, and is AC97 Version 2.0 audio compliant.

In addition to the advanced CPU features, the MediaGX processor integrates a host of functions which are typically implemented with external components. A full-function graphics accelerator provides pixel processing and rendering functions.

The NS MediaGX MMX-Enhanced Processor represents a new generation of x86-compatible 64-bit microprocessors with sixth-generation features. The decoupled load/store unit (within the memory management unit) allows multiple instructions in a single clock cycle. Other features include single-cycle execution, single-cycle instruction decode, 16KB write-back cache, and clock rates up to 266MHz. These features are possible by the use of advanced-process technologies and superpipelining.

## 2.2 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented on the AR-B9637 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high-speed information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The Following is the system information for the DMA channels:

| Slave with four 8-bit chnls | Master with three 16-bit chnls |
|---|---|
| **DMA Controller 1** | **DMA Controller 2** |
| Channel 0: Spare | Channel 4(0): Cascade for controller 1 |
| Channel 1: IBM SDLC | Channel 5(1): Spare |
| Channel 2: Diskette adapter | Channel 6(2): Spare |
| Channel 3: Spare | Channel 7(3): Spare |

**DMA Channel Controller**

## 2.3 KEYBOARD CONTROLLER

The 8042 processor is programmed to support the keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

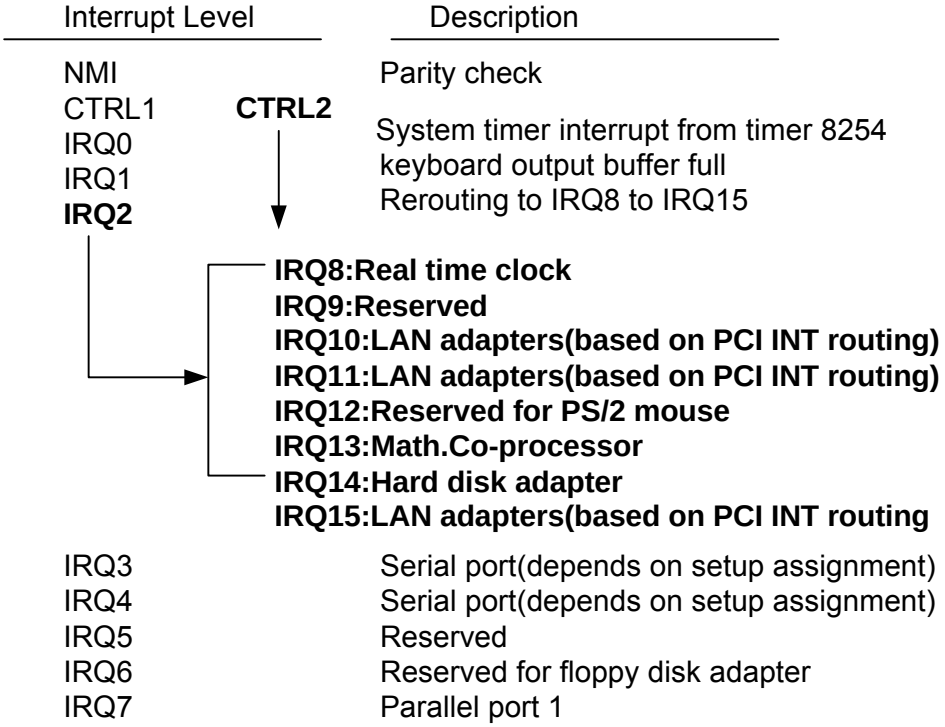
Data can be written to the keyboard by writing data to the output buffer of the keyboard controller.

Each byte of data is sent to the keyboard controller in a series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to keyboard controller until acknowledgment is received for the previous byte sent. The “output buffer full” interruption may be used for both send and receive routines.

## 2.4 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the AR-B9637 board. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute. These two controllers are cascaded with the second controller representing IRQ8 to IRQ15, which is rerouted through IRQ2 on the first controller.

The following is the system information of interrupt levels:




**Interrupt Controller**

### 2.4.1 I/O Port Address Map

| Hex Range | Device |
|---|---|
| 000-01F | DMA controller 1 |
| 020-021 | Interrupt controller 1 |
| 022-023 | Cyrix CS5530A |
| 040-04F | Timer 1 |

| Hex Range | Device |
|---|---|
| 050-05F | Timer 2 |
| 060-06F | 8042 keyboard/controller |
| 070-071 | Real-time clock (RTC), non-maskable interrupt (NMI) |
| 080-09F | DMA page registers |
| 0A0-0A1 | Interrupt controller 2 |
| 0C0-0DF | DMA controller 2 |
| 0F0 | Clear Math Co-processor |
| 0F1 | Reset Math Co-processor |
| 0F8-0FF | Math Co-processor |
| 170-178 | Reserved for Fixed disk 1 |
| 1F0-1F8 | Fixed disk 0 |
| 201 | Reserved for Game port |
| 208-20A | EMS register 0 |
| 218-21A | EMS register 1 |
| 278-27F | Parallel printer port (depends on setup assignment) |
| 2E8-2EF | Serial port (depends on setup assignment) |
| 2F8-2FF | Serial port (depends on setup assignment) |
| 300-31F | Prototype card/streaming type adapter |
| 320-33F | Reserved |
| 378-37F | Parallel printer port (depends on setup assignment) |
| 380-38F | SDLC, bisynchronous |
| 3A0-3AF | Bisynchronous |
| 3B0-3BF | Monochrome display and printer port 3 (LPT 3) |
| 3C0-3CF | EGA/VGA adapter |
| 3D0-3DF | Color/graphics monitor adapter |
| 3E8-3EF | Serial port 3 (depends on setup assignment) |
| 3F0-3F7 | Reserved for diskette controller |
| 3F8-3FF | Serial port (depends on setup assignment) |

**I/O Port Address Map**

## 2.4.2 Real-Time Clock and Non-Volatile RAM

The AR-B9637 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long periods of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed as follows:

| Address | Description |
|---|---|
| 00 | Seconds |
| 01 | Second alarm |
| 02 | Minutes |
| 03 | Minute alarm |
| 04 | Hours |
| 05 | Hour alarm |
| 06 | Day of week |
| 07 | Date of month |
| 08 | Month |
| 09 | Year |
| 0A | Status register A |
| 0B | Status register B |
| 0C | Status register C |
| 0D | Status register D |
| 0E | Diagnostic status byte |
| 0F | Shutdown status byte |
| 10 | Diskette drive type byte, drive A and B |
| 11 | Fixed disk type byte, drive C |
| 12 | Fixed disk type byte, drive D |
| 13 | Reserved |
| 14 | Equipment byte |
| 15 | Low base memory byte |
| 16 | High base memory byte |
| 17 | Low expansion memory byte |
| 18 | High expansion memory byte |
| 19-2D | Reserved |
| 2E-2F | 2-byte CMOS checksum |
| 30 | Low actual expansion memory byte |
| 31 | High actual expansion memory byte |
| 32 | Date century byte |
| 33 | Information flags (set during power on) |
| 34-7F | Reserved for system BIOS |

**Real-Time Clock & Non-Volatile RAM**

## 2.4.3 Timer

The AR-B9637 provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.
Application programs can load different counts into this timer to generate various sound frequencies.

## 2.5 SERIAL PORT

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, 1.5 (in a five-bit format only) or two stop bits(in a 6,7, or 8-bit format). The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time

required to handle the communications link.

The following table is a summary of each ACE accessible register

| DLAB | Port Address | Register |
|---|---|---|
| 0 | base + 0 | Receiver buffer (read) |
| | | Transmitter holding register (write) |
| 0 | base + 1 | Interrupt enable |
| X | base + 2 | Interrupt identification (read only) |
| X | base + 3 | Line control |
| X | base + 4 | MODEM control |
| X | base + 5 | Line status |
| X | base + 6 | MODEM status |
| X | base + 7 | Scratched register |
| 1 | base + 0 | Divisor latch (least significant byte) |
| 1 | base + 1 | Divisor latch (most significant byte) |

**ACE Accessible Registers**

**(1) Receiver Buffer Register (RBR)**

Bit 0-7: Received data byte (Read Only)

**(2) Transmitter Holding Register (THR)**

Bit 0-7: Transmitter holding data byte (Write Only)

**(3) Interrupt Enable Register (IER)**

Bit 0: Enable Received Data Available Interrupt (ERBFI)
Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)
Bit 2: Enable Receiver Line Status Interrupt (ELSI)
Bit 3: Enable MODEM Status Interrupt (EDSSI)
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

**(4) Interrupt Identification Register (IIR)**

Bit 0: “0” if Interrupt Pending
Bit 1: Interrupt ID Bit 0
Bit 2: Interrupt ID Bit 1
Bit 3: Must be 0
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

**(5) Line Control Register (LCR)**

Bit 0: Word Length Select Bit 0 (WLS0)
Bit 1: Word Length Select Bit 1 (WLS1)

| WLS1 | WLS0 | Word Length |
|---|---|---|
| 0 | 0 | 5 Bits |
| 0 | 1 | 6 Bits |
| 1 | 0 | 7 Bits |
| 1 | 1 | 8 Bits |

Bit 2: Number of Stop Bit (STB)
Bit 3: Parity Enable (PEN)
Bit 4: Even Parity Select (EPS)
Bit 5: Stick Parity
Bit 6: Set Break
Bit 7: Divisor Latch Access Bit (DLAB)

**(6) MODEM Control Register (MCR)**

Bit 0: Data Terminal Ready (DTR)
Bit 1: Request to Send (RTS)
Bit 2: Out 1 (OUT 1)
Bit 3: Out 2 (OUT 2)
Bit 4: Loop
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

**(7) Line Status Register (LSR)**

Bit 0: Data Ready (DR)
Bit 1: Overrun Error (OR)
Bit 2: Parity Error (PE)
Bit 3: Framing Error (FE)
Bit 4: Break Interrupt (BI)
Bit 5: Transmitter Holding Register Empty (THRE)
Bit 6: Transmitter Shift Register Empty (TSRE)
Bit 7: Must be 0

**(8) MODEM Status Register (MSR)**

Bit 0: Delta Clear to Send (DCTS)
Bit 1: Delta Data Set Ready (DDSR)
Bit 2: Training Edge Ring Indicator (TERI)
Bit 3: Delta Receive Line Signal Detect (DSLSD)
Bit 4: Clear to Send (CTS)
Bit 5: Data Set Ready (DSR)
Bit 6: Ring Indicator (RI)
Bit 7: Received Line Signal Detect (RSLD)

**(9) Divisor Latch (LS, MS)**

| | LS | MS |
|---|---|---|
| Bit 0: | Bit 0 | Bit 8 |
| Bit 1: | Bit 1 | Bit 9 |
| Bit 2: | Bit 2 | Bit 10 |
| Bit 3: | Bit 3 | Bit 11 |
| Bit 4: | Bit 4 | Bit 12 |
| Bit 5: | Bit 5 | Bit 13 |
| Bit 6: | Bit 6 | Bit 14 |
| Bit 7: | Bit 7 | Bit 15 |

| Desired Baud Rate | Divisor Used to Generate 16x Clock |
|---|---|
| 300 | 384 |
| 600 | 192 |
| 1200 | 96 |
| 1800 | 64 |
| 2400 | 48 |
| 3600 | 32 |
| 4800 | 24 |
| 9600 | 12 |
| 14400 | 8 |
| 19200 | 6 |
| 28800 | 4 |
| 38400 | 3 |
| 57600 | 2 |
| 115200 | 1 |

**Serial Port Divisor Latch**

## 2.6 PARALLEL PORT

### (1) Register Address

| Port Address | Read/Write | Register |
|---|---|---|
| base + 0 | Write | Output data |
| base + 0 | Read | Input data |
| base + 1 | Read | Printer status buffer |
| base + 2 | Write | Printer control latch |

**Registers’ Address**

### (2) Printer Interface Logic

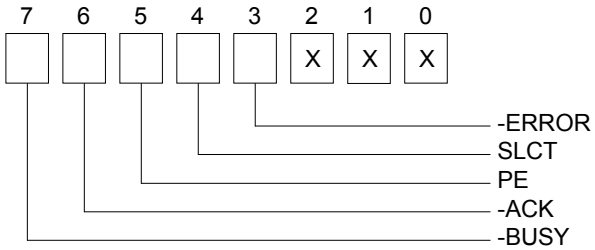
The parallel port of the W83977F-A is for attaching various devices that accept eight bits of parallel data at standard TTL level.

### (3) Data Swapper

The system microprocessor can read the contents of the printer’s Data Latch through the Data Swapper by reading the Data Swapper address.

### (4) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described as follows:




**Printer Status Buffer**

**NOTE:** X presents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer’s ACK signal. A0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

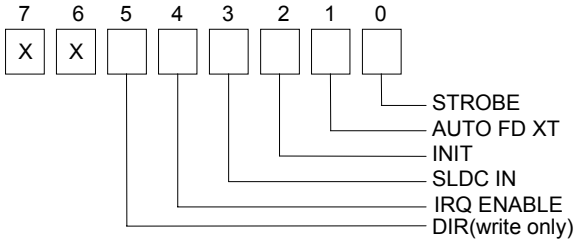
Bit 5: A1 means the printer has detected the end of the paper.

Bit 4: A1 means the printer is selected.

Bit 3: A0 means the printer has encountered an error condition.

### (5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:




**Bit’s Definition**

**NOTE:** X presents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write only.

Bit 4: A1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A1 in this bit position selects the printer.

Bit 2: A0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A1 causes the printer to line-feed after a line is printed.

Bit 0: A0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

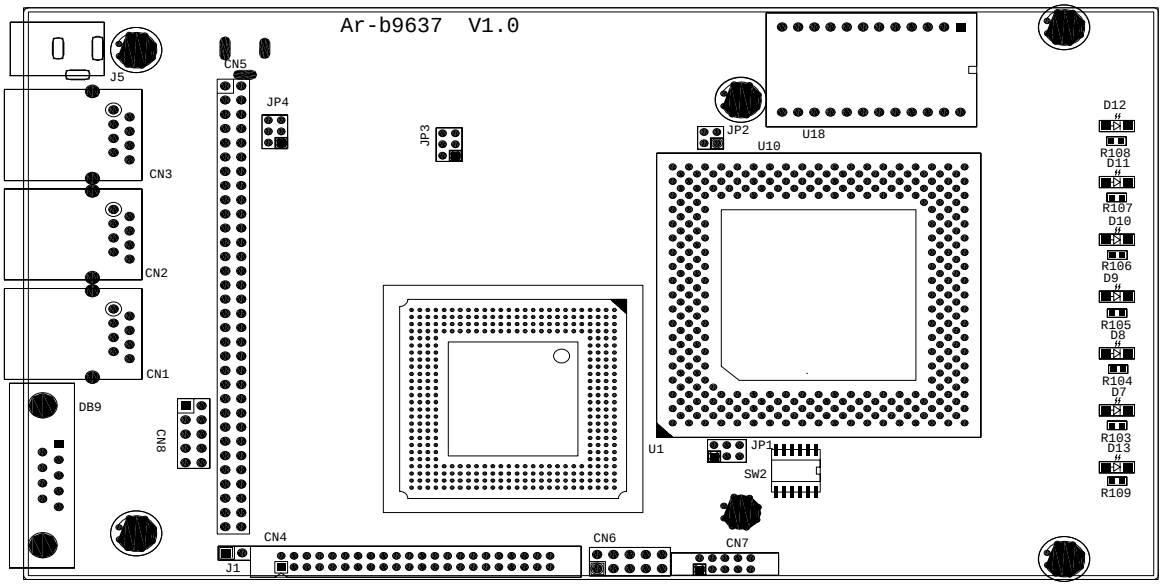
# 3. SETTING UP THE SYSTEM

This section describes pin assignments for the system’s external connectors and the jumper settings.

- Overview
- System Setting

## 3.1 OVERVIEW

AR-B9637 Pentium Grade Firewall CPU Board with Ehternet , DOM. This section provides the hardware’s jumper settings, the connectors’ locations, and the pin assignments. The #1 pin assignments have all been designed on the right side of the board with a “block” indication on the diagram.



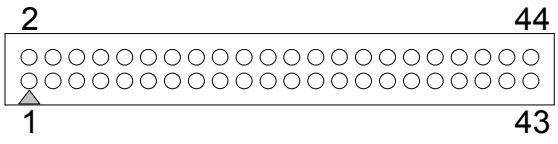

## 3.2 SYSTEM SETTING

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

**CAUTION:** Do not touch any electronic components unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage electronic components.

### 3.2.1 Hard Disk (IDE) Connector (CN4)

A 44-pin header type connector (CN4) is provided to interface with up to two embedded hard disk drives (IDE AT bus). This interface, through a 44-pin cable, allows the user to connect up to two drives in a “daisy chain” fashion. To enable or disable the hard disk controller, please use the BIOS Setup program, which is explained further in chapter 5. The following table illustrates the pin assignments of the hard disk drive’s 44-pin connector.

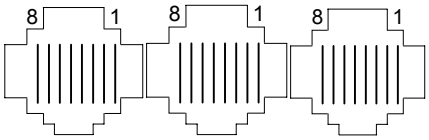


| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | -RESET | 2 | GROUND |
| 3 | DATA 7 | 4 | DATA 8 |
| 5 | DATA 6 | 6 | DATA 9 |
| 7 | DATA 5 | 8 | DATA 10 |
| 9 | DATA 4 | 10 | DATA 11 |
| 11 | DATA 3 | 12 | DATA 12 |
| 13 | DATA 2 | 14 | DATA 13 |
| 15 | DATA 1 | 16 | DATA 14 |
| 17 | DATA 0 | 18 | DATA 15 |
| 19 | GROUND | 20 | NOT USED |
| 21 | IDEDREQ | 22 | GROUND |
| 23 | -IOW A | 24 | GROUND |
| 25 | -IOR A | 26 | GROUND |
| 27 | IDEIORDYA | 28 | GROUND |
| 29 | -DACKA | 30 | GROUND |
| 31 | AINT | 32 | GROUND |
| 33 | SA 1 | 34 | Not Used |
| 35 | SA 0 | 36 | SA 2 |
| 37 | CS 0 | 38 | CS 1 |
| 39 | HD LED A | 40 | GROUND |
| 41 | VCC | 42 | VCC |
| 43 | GROUND | 44 | Not Used |

**Hard Disk (IDE) Connector**

## 3.2.2 Network Setting (CN1, CN2, CN3)

The CN1, CN2 & CN3 RJ-45 header are the standard network headers. The following table is the pin assignment.

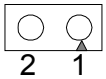



| PIN (CN12) | FUNCTION |
|---|---|
| 1 | TPTX+ |
| 2 | TPTX - |
| 3 | TPRX+ |
| 4 | Not Used |
| 5 | Not Used |
| 6 | TPRX - |
| 7 | Not Used |
| 8 | Not Used |

**RJ-45 Pin Assignment**

## 3.2.3 Reset Header (J1)

The J1 is used to connect to an external reset switch. Shorting these two pins will reset the system.



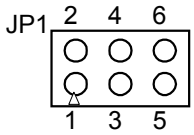

1 Reset+
2 Reset-

## 3.2.4 Power Connector (J5)

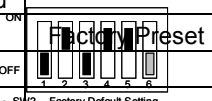
The J5 is an power connector.


## 3.2.5 CPU Select

### (1) CPU Clock Multiplier Select (JP1)



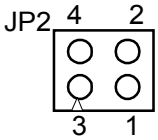

| 1-2 | 3-4 | 5-6 | Multiplier | Note |
|---|---|---|---|---|
| CLOSE | CLOSE | CLOSE | 4X | |
| CLOSE | CLOSE | OPEN | 10X | |
| CLOSE | OPEN | CLOSE | 9X | |
| CLOSE | OPEN | OPEN | 5X | |
| OPEN | CLOSE | CLOSE | Reserved | |
| OPEN | CLOSE | OPEN | 6X | |
| OPEN | OPEN | CLOSE | 7X | |
| OPEN | OPEN | OPEN | Reserved | |



Factory Preset

**JP1: CPU Clock Multiplier**

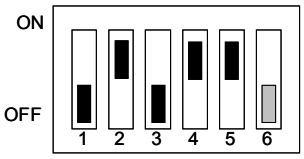
### (2) CPU Base Clock Select (JP2)




| 1-2 | 3-4 | Base Clock | PCI Clock |
|---|---|---|---|
| ON | ON | 50MHz | 25MHz |
| OFF | ON | 66.6MHz | 33.3MHz |
| ON | OFF | 60MHz | 30MHz |

**JP2: CPU Base Clock**

### (3) CPU Logic Core Voltage Select (SW2)

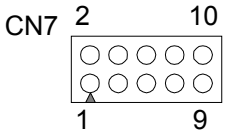


SW2 -- Factory Default Setting

| 1 | 2 | 3 | 4 | 5 | 6 | Voltage |
|---|---|---|---|---|---|---|
| OFF | ON | ON | OFF | ON | OFF | 1.6V |
| OFF | ON | OFF | ON | ON | OFF | 1.8V |
| OFF | ON | ON | ON | ON | OFF | 2.0V |
| OFF | ON | OFF | OFF | OFF | OFF | 2.2V |
| ON | OFF | ON | OFF | OFF | OFF | 2.5V |
| ON | OFF | OFF | ON | OFF | OFF | 2.9V |

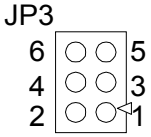
**SW2: CPU Logic Core Voltage Select**

### 3.2.6 CRT Connector (CN7)




| | |
|---|---|
| 1. Red | 6. AGND |
| 2. AGND | 7. V.S |
| 3. Green | 8. DDCD |
| 4. GND | 9. H.S |
| 5. Blue | 10.DDCK |

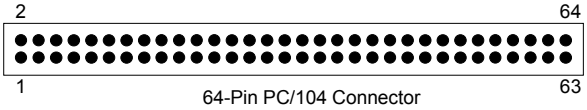
### 3.2.9 Ethernet LAN Jumper (JP3)

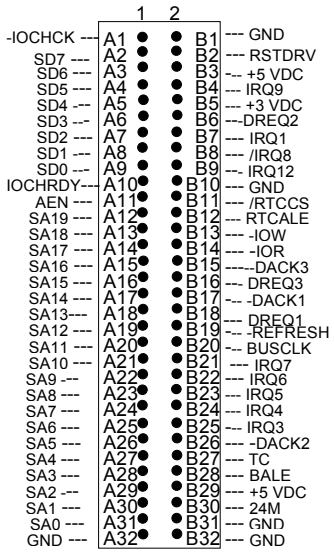



| | | |
|---|---|---|
| 1-2 | Close (Ethernet-1ON) | Open (Ethernet-1 OFF) |
| 3-4 | Close (Ethernet-2ON) | Open (Ethernet-2 OFF) |
| 5-6 | Close (Ethernet-3ON) | Open (Ethernet-3 OFF) |

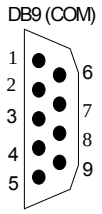
**JP3: Ethernet LAN Jumper Setting**

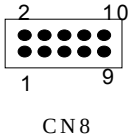
### 3.2.10 PC104 Connector (CN5)




### 3.2.11 COMB (DB9)




CN8

**Note: One general COM port function has been represented by the DB9 connector, however, the function only works when AR-B9461A has also been occupied with CN8.**

# 4. INSTALLATION

This chapter describes the installation procedure. The following topics are covered:

- Overview
- Utility Diskettes

## 4.1 OVERVIEW

This chapter provides information for you to set up a working system based on the AR-B9637 CPU board. Please carefully read the details of the CPU board's hardware descriptions before installation. Pay special attention to the jumper settings, switch settings and cable connections.

Follow steps listed below for proper installation:

**Step 1:** Read the CPU board's hardware description in this manual.

**Step 2 :** Set jumpers.

**Step 3 :** Make sure that the power supply connected to your AR-B9637 CPU board is turned off.

**Step 4 :** Connect all necessary cables. Make sure that the HDC; serial and parallel cables are connected to pin 1 of the related connector (not upside down).

**Step 5:** Connect the hard disk flat cables from the CPU board to the drives. Connect a power source to drive.

**Step 6:** Plug the keyboard into the keyboard connector.

**Step 7:** Turn on the power.

**Step 8:** Configure your system with the BIOS Setup program (section 5) then re-boot your system.

**Step 9:** If the CPU board does not work, turn off the power and read the hardware description carefully again.

**Step 10:** If the CPU board still does not perform properly, return the board to your dealer for immediate service.

## 4.2 UTILITY DISKETTE

The AR-B9637 provides three utility diskettes.

### 4.2.1 Driver Installation

The AR-B9637 provides LAN function drivers for the WIN95, WIN98, WIN2000, WINCE, LINUX, and NT. The driver can auto-setup in the specified mode. The user must first decompress the compressed file.

**The 1st step: Decompress the zip files included in the diskettes to your hard disk.**

**The 2nd step: Execute the corresponding files to setup the system.**

The files list and descriptions are as follow:

| Disk 1 | |
|---|---|
| Files | README.TXT 391 09-22-00 11:17 README.TXT<br>GEODEW~1 <DIR> 09-22-00 10:53 Geode win9x<br>WINCED~1 <DIR> 09-22-00 10:53 WinCE driver |
| Descriptions | 1. GEODE win9x<br>Includes auto-execution program that will setup/install Geode Media drivers in Windows 9X environment.<br>2. WinCE driver<br>Includes the GxM drivers needed in Win CE environment. |
| **Disk 2** | |
| Files | NT4~1 0DR <DIR> 09-22-00 10:53 NT4.0 driver<br>LINUXD~1 <DIR> 09-22-00 10:53 Linux driver<br>WIN200~1 <DIR> 09-22-00 10:53 Win2000 driver<br>README.TXT 1,611 04-23-99 11:48 README.TXT |
| Descriptions | 1. NT4.0 driver<br>Includes the GxM drivers needed in NT4.0 environment.<br>2. Linux driver<br>Includes the GxM drivers needed in Linux environment.<br>3. Win2000 driver<br>Includes the GxM drivers needed in Win2000 environment. |
| **Disk 3** | |
| Files | 8139SW.EXE |
| Description | An auto extract file that includes:<br>1. Device drivers of RTL8139A for various operating systems<br>2. LAN Configuration EEPROM programmer<br>3. Diagnostic and modification program for RTL8139 |

# 5. BIOS CONSOLE

This chapter describes the AR-B9637 BIOS menu displays and explains how to perform common tasks needed to get up and running, and presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- BIOS Features Setup
- Chipset Features Set
- PNP/PCI Configuration
- Load Default Setting
- Integrated Peripherals
- Password Setting
- IDE HDD Auto Detection
- BIOS Exit

## 5.1 BIOS SETUP OVERVIEW

Once you enter Award BIOS CMOS Setup Utility by holding the "Delete" button during boot-up, the Main Menu will appear on the screen. The Main Menu allows you to select from various setup functions and two exit choices. Use arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.

ROM PCI/ISA BIOS (2A434AVH)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

| | |
|---|---|
| STANDARD CMOS SETUP | INTEGRATED PERIPHERALS |
| BIOS FEATURES SETUP | SUPERVISOR PASSWORD |
| CHIPSET FEATURES SETUP | USER PASSWORD |
| PNP/PCI CONFIGURATION | IDE HDD AUTO DETECTION |
| LOAD BIOS DEFAULTS | SAVE & EXIT SETUP |
| LOAD SETUP DEFAULTS | EXIT WITHOUT SAVING |
| Esc: Quit | ↑↓→←: Select Item |
| F10: Save & Exit Setup | (Shift) F2: Change Color |
| Time, Date, Hard Disk Type… | |

**BIOS Setup Main Menu**

**CAUTION:** 1. AR-B9637 BIOS the factory-default setting is used to the <LOAD BIOS DEFAULTS> Acrosser recommends using the BIOS default setting, unless you are very familiar with the setting function, or you can contact the technical support engineer.
2. If the BIOS settings are lost, the CMOS will detect the <LOAD SETUP DEFAULTS> to boot the operation system, this option will reduce the performance of the system. Acrosser recommends choosing the <LOAD BIOS DEFAULTS> in the main menu. This option gives best-case values that should optimize system performance.
3. The BIOS settings are described in detail in this section.

## 5.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

ROM PCI/ISA BIOS (2A434AVH)
STANDARD CMOS SETUP
AWARD SOFTWARE, INC.

Date (mm:dd:yyyy): Tue, Mar 16, 2000
Time (hh:mm:ss): 16:39:30

| | <type> | | CYLS. | HEADS | PRECOMP | LANDZONE | SECTORS | MODE |
|---|---|---|---|---|---|---|---|---|
| Drive C : | 0 | ( 0Mb) | 0 | 0 | 0 | 0 | 0 | AUTO |
| Drive D: | 0 | ( 0Mb) | 0 | 0 | 0 | 0 | 0 | AUTO |

Drive A: None
Drive B: None

Video: EGA/VGA

Halt On: All, But Keyboard

Base Memory: 640K
Extended Memory: 29184K
Other Memory: 384K

Total Memory: 30208K

Esc: Quit ↑↓→←: Select Item PU/PD/+/-: Modify
F1: Help (Shift) F2: Change Color

**Standard CMOS Setup**

### Date & Time Setup

Highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

### Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master>, <Pri Slave>, <Sec Master> and <Sec Slave> so the user can install up to two hard disks. For the master and slave jumpers, please refer to the hard disk’s installation descriptions and the hard disk jumper settings in section three of this manual.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during boot-up. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives, which do not support this feature, then you must configure the hard disk drive in the standard method by choosing the HDD type, which should be noted directly on the HDD.

### Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

### Video

This option selects the type of adapter used for the primary system monitor that must match your video display card and monitor. Although secondary monitors are supported, you do not have to select the type in Setup.

You have two ways to boot up the system:

1. When VGA as primary and monochrome as secondary, the selection of the video type is “ VGA Mode”.

2 When monochrome as primary and VGA as secondary, the selection of the video type is “Monochrome Mode”.

.

| | |
|---|---|
| EGA/VGA | Enhanced Graphics Adapter/Video Graphics Array. For EGA, VGA, SEGA, or PGA monitor adapters |
| CGA 40 | Color Graphics Adapter, power up in 40 column mode |
| CGA 80 | Color Graphics Adapter, power up in 80 column mode |
| MONO | Monochrome adapter, includes high resolution monochrome adapters |

**Halt On**

This option determines whether the computer will stop if an error is detected during power up.

| | |
|---|---|
| No errors | The system boot will not be stopped for any error that may be detected. |
| All errors | Whenever the BIOS detects a non-fatal error the system will be stopped and you will be prompted. |
| All, But Keyboard | The system boot will not stop for a keyboard error, it will stop for all other errors. |
| All, But Diskette | The system boot will not stop for a disk error, it will stop for all other errors. |
| All, But Disk/Key | The system boot will not stop for a keyboard or disk error, it will stop for all other errors. |

## 5.3 BIOS FEATURES SETUP

The <BIOS FEATURES SETUP> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings for optimal performance.

It is suggested that you leave the settings on the factory default unless you are well versed in BIOS features.

ROM PCI/ISA BIOS (2A434AVH)
BIOS FEATURES SETUP
AWARD SOFTWARE, INC.

| | | | |
|---|---|---|---|
| CPU Internal Cache | : Enabled | Video BIOS Shadow | : Enabled |
| Quick Power On Self Test | : Enabled | | |
| Boot Sequence | : C, CDROM,A | | |
| | | Cyrix 6x86/MII CPUID | : Enabled |
| Boot Up NumLock Status | : On | | |
| Boot Up System Speed | : High | | |
| Gate A20 Option | : Fast | | |
| Memory Parity Check | : Disabled | | |
| Typematic Rate Setting | : Enabled | | |
| Typematic Rate (Chars/Sec) | : 30 | | |
| Typematic Delay (Msec) | : 250 | | |
| Security Option | : Setup | Esc: Quit | ↑↓→←: Select Item |
| PCI/VGA Palette Snoop | : Disabled | F1: Help | PU/PD/+/-: Modify |
| | | F5: Old Values | (Shift) F2: Change Color |
| | | F6: Load BIOS Defaults | |
| | | F7: Load Setup Defaults | |

**BIOS Features Setup**

**CPU Internal Cache/External Cache**

The two functions speed up memory access. However, it depends on CPU/chipset design. If your CPU is without Internal cache then this item <CPU Internal Cache> will not be show. The AR-B 9625's GXM Cyrix CPU has an internal cache and will automatically be set to <enabled>.

**Quick Power On Self Test**

This option speeds up Power On Self Test (POST) after you power on the computer. If it is set to Enable, BIOS will shorten or skip some items’ checks during POST.

**Boot Sequence**

The option determines which drive computer searches first for the disk operating system.

**Boot Up NumLock Status**

This item is used to activate the NumLock function upon system boot. If the setting is on, after a boot, the NumLock light is lit, and the user can use the number keys.

**Boot Up System Speed**

This item is used to choose the boot-up speed of system. The choices provided are <LOW> and <HIGH>.

**Gate A20 Option**

This item is chosen as <Normal>, the A20 signal is controlled by a keyboard controller or chipset hardware. The selection is “Fast” means the A20 signal is controlled by Port 92 or a chipset specific method.

**Memory Parity Check**

An approach that generates and checks parity on each memory transfer and provides an interrupt if an error is found. This item is to <Disabled> or <Enabled> this function.

**Typematic Rate Setting**

To enable typematic rate and typematic delay programming. If you disable the typematic rate and typematic delay programming, the system BIOS will use the default value of these 2 items and the default is controlled by the keyboard.

**Typematic Rate (Chars/Sec)**

Typematic Rate sets the rate at which characters on the screen repeat when a key is pressed and held down. The settings are 6, 8, 10, 12, 15, 20, 24, or 30 characters per second.

**Typematic Delay (Msec)**

The number selected indicates the time period between two identical characters appearing on screen.

**Security Option**

The option allows the user to limit access to the System and Setup, or just to Setup.

| | |
|---|---|
| System | The system will not boot and access to Setup will de denied if the correct password is not entered at the prompt. |
| Setup | The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt. |

**Note:** To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

**PCI/VGA Palette Snoop**

This option must be set to Enabled if any ISA adapter card installed in the computer requires VGA palette snooping.

**Video BIOS Shadow**

ROM Shadow copies Video BIOS code from slower ROM to faster RAM. Video BIOS can then execute from RAM. This makes your system faster.

**Cyrix 6x86/MII CPUID**

The option is to determine whether or not to use the function of controlling or accessing the Cyrix 6x86/MII CPUID.

## 5.4 CHIPSET FEATURES SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen. This selection is automatic.

ROM PCI/ISA BIOS (2A434AVF)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

| | | |
|---|---|---|
| SDRAM CAS latency Time | : 3 T | |
| SDRAM Clock Ratio Div By | : 4 | |
| 16-bit I/O Recovery (CLK) | : 5 | |
| 8-bit I/O Recovery (CLK) | : 5 | |
| | | Esc: Quit ↑↓→←: Select Item |
| | | F1: Help PU/PD/+/-: Modify |
| | | F5: Old Values (Shift) F2: Color |
| | | F6: Load BIOS Defaults |
| | | F7: Load Setup Defaults |

**Chipset Features Setup**

### SDRAM CAS latency Time

This item is to setup the SDRAM CAS# signal latency time, the smaller value you set it, the higher efficiency you will get.

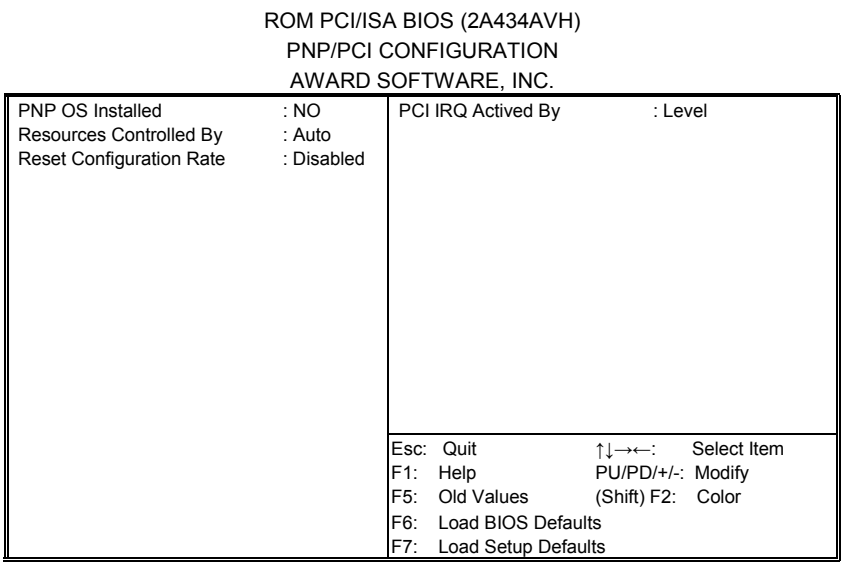
### SDRAM Clock Ratio Div By

This item is to determine the SDRAM Clock Ratio.

### 16-Bit I/O Cycle Recovery Time
### 8-Bit I/O Cycle Recovery Time

These options specify the length of the delay (in BUSCLK) inserted between consecutive 8-bit/16-bit I/O operations.

## 5.5 PNP/PCI CONFIGURATION




**PNP/PCI CONFIGURATION**

**PNP OS Installed**

This item is to choose whether or not installing the PNP(Plug & Play) operation system.

**Resources Controlled By**

The available choices are <Auto>&<Manual>. To choose <Auto>the resources will be under the control of system automatically. If <Manual> chosen , the following items will be listed.

**<IRQ (3,4,5,7,9,10,11,12,14,15)>** Setting these items one by one will clear up the conflict between NON-PNP ISA extension cards and PNP system.

**<DMA(0,1,3,5,6,7)>** These items are used for the PNP ISA(PCI) cards or NON-PNP old ISA cards which use DMA channel to enable them work normally.

**Reset Configuration Data**

This item is used to <enable> the function of Reset Configuration Data or not.

**PCI IRQ Actived By**

This item is to determine the active mode.

## 5.6 LOAD DEFAULT SETTING

This section permits the user to select a group of settings for all BIOS Setup options. Not only can you use these items to quickly set system configuration parameters, you can choose a group of settings that have a better chance of working when the system is having configuration related problems.

### 5.6.1 Load BIOS Defaults

User can load the optimal default settings for the BIOS. The <LOAD BIOS DEFAULTS> uses best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

```
Load high performance settings (Y/N)?
```

### 5.6.2 Load Setup Defaults

User can load the <LOAD SETUP DEFAULTS> Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.
The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

```
Load failsafe settings (Y/N)?
```

## 5.7 INTEGRATED PERIPHERALS

This section is designed to configure the peripheral features.

ROM PCI/ISA BIOS (2A434AVH)
INTEGRATED PERIPHERALS
AWARD SOFTWARE, INC.

| | | | |
|---|---|---|---|
| IDE HDD Block Mode | : Enabled | | |
| Primary IDE Channel | : Enabled | | |
| Master Drive PIO Mode | : Auto | | |
| Slave Drive PIO Mode | : Auto | | |
| IDE Primary Master UDMA | : Disabled | | |
| IDE Primary Slave UDMA | : Disabled | | |
| KBC input clock | : 8 MHz | | |
| | | : | |
| Onboard Serial Port 1 | : 3F8/IRQ4 | Multiple Monitor Support | : No Onboard |
| Onboard Serial Port 2 | : 2F8/IRQ3 | | |
| Onboard IR Controller | : Disabled | Video Memory Size | : 2.5M |
| | | Esc: Quit | ↑↓→←: Select Item |
| | | F1: Help | PU/PD/+/-: Modify |
| | | F5: Old Values | (Shift) F2: Color |
| Onboard Parallel Port | 378/IRQ7 | F6: Load BIOS Defaults | |
| Parallel Port Mode | SPP | F7: Load Setup Defaults | |

**Integrated Peripherals**

### IDE HDD Block Mode

This option allows your hard disk controller to use the fast block mode to transfer data to and from your hard disk drive (HDD).

| | |
|---|---|
| Enabled | IDE controller uses block mode. |
| Disabled | IDE controller uses standard mode. |

### IDE PIO

IDE hard drive controllers can support up to two separate hard drives. These drives have a master/slave relationship, which is determined by the cabling configuration used to attach them to the controller. Your system supports one IDE controller – a primary and a secondary – so you have the ability to install up to four separate hard disks.

PIO means Programmed Input/Output. Rather than have the BIOS issue a series of commands to effect a transfer to or from the disk drive, PIO allows the BIOS to tell the controller what it wants and then let the controller and the CPU perform the complete task by themselves. This is simpler and more efficient (and faster). Your system supports five modes, numbered from 0 to 4, which primarily differ in timing. When Auto is selected, the BIOS will select the best available mode.

### KBC input clock

This item it to chose the input clock of Keyboard Controller

### OnBoard Serial Port 1 & 2

This options are used to select the port address of the on-board serial port A. The options are 3F8H, 2F8H, 3E8H, 2E8H, Auto and Disable. Port 1 is COM A, Port 2 is Com D and so on. Port four can be set to be IrDA (Choose Auto) if the IrDA device has been connected.

### OnBoard Parallel Port

This option is used to select the port address of the on-board parallel port. The options are 378H, 278H, 3BCH, and Disabled.

### Parallel Port Mode

This option specifies the parallel port Mode. The settings are Printer or Extended (Bi-direction).

**Multiple Monitor Support**

This is to determine the highest priority that the monitor supports. <PCI First> is the default setting. The other two choices are <No Onboard> and <M/B First>.

## 5.8 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed.

### 5.8.1 Setting Password

Select the appropriate password icon from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after BIOS is completed. The next time the system boots, the prompt for the password function is present and is enabled.

```
Enter new supervisor password:
```

### 5.8.2 Password Checking

The password check option is enabled in Advanced Setup by choosing either **Always** (the password prompt appears every time the system is powered on) or **Setup** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. User can enter a password by typing with the keyboard. Enter a 1-6 character password. The password does not appear on the screen when typed. Make sure you write it down.

## 5.9 IDE HDD AUTO DETECTION

This option detects the parameters of an IDE hard disk drive, and automatically enters them into the Standard CMOS Setup screen.

## 5.10 BIOS EXIT

This section is used to exit the BIOS main menu in two types of situation. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

### 5.10.1 Save & Exit Setup

This item set in the <Standard CMOS Setup>, <BIOS Features Setup>, <Chipset Features Setup>, <Power Management Setup>, <Integrated Peripherals> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you in saving data to CMOS and Exit the Setup.

```
Save current settings and exit (Y/N) ?
```

### 5.10.2 Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to Abandon all Data and Exit Setup.

```
Quit without saving (Y/N) ?
```

### Windows Installation Notice:

1. While AR-B9637/9461 does not have floppy disk function, the proper way to setup the Windows system is to copy all the drivers needed to your hard disk or CD-ROM and to execute them from the related devices.
2. Please refer to BIOS setup section in this manual for booting from CD-ROM
3. If you find any difficulty in the operating systems installation, please contact our technical support for futher assistance.