

AR-B9629
Half Size All-In-One
386SX CPU BOARD
User's Guide

Edition: 1.11
Book Number: AR-B9629-05.0613

Table of Contents

| | | |
|-----------|---|------------|
| 0. | PREFACE | 0-3 |
| 0.1 | COPYRIGHT NOTICE AND DISCLAIMER | 0-3 |
| 0.2 | WELCOME TO THE AR-B9629 CPU BOARD | 0-3 |
| 0.3 | BEFORE YOU USE THIS GUIDE | 0-3 |
| 0.4 | RETURNING YOUR BOARD FOR SERVICE | 0-3 |
| 0.5 | TECHNICAL SUPPORT AND USER COMMENTS | 0-3 |
| 0.6 | ORGANIZATION | 0-4 |
| 0.7 | STATIC ELECTRICITY PRECAUTIONS | 0-4 |
| 1. | OVERVIEW | 1-1 |
| 1.1 | INTRODUCTION | 1-1 |
| 1.2 | PACKING LIST | 1-1 |
| 1.3 | FEATURES | 1-1 |
| 2. | SYSTEM CONTROLLER | 2-1 |
| 2.1 | MICROPROCESSOR | 2-1 |
| 2.2 | DMA CONTROLLER | 2-1 |
| 2.3 | KEYBOARD CONTROLLER | 2-2 |
| 2.4 | INTERRUPT CONTROLLER | 2-2 |
| 2.4.1 | I/O Port Address Map | 2-3 |
| 2.4.2 | Real-Time Clock and Non-Volatile RAM | 2-4 |
| 2.4.3 | Timer | 2-4 |
| 2.5 | SERIAL PORT | 2-5 |
| 2.6 | PARALLEL PORT | 2-7 |
| 3. | SETTING UP THE SYSTEM | 3-1 |
| 3.1 | OVERVIEW | 3-1 |
| 3.2 | SYSTEM SETTINGS | 3-2 |
| 3.2.1 | Clock Jumper (JP1) | 3-2 |
| 3.2.2 | Reset (J1) | 3-2 |
| 3.2.3 | PS2 KB4 Mouse (J4) | 3-2 |
| 3.2.4 | ISA Bus Connector (CN1) | 3-3 |
| 3.2.5 | External Buzzer (J2) | 3-4 |
| 3.2.6 | Power Connector (J3) | 3-5 |
| 3.2.7 | I/O Connector for KB/MS, serial port, parallel port (CN3) | 3-5 |
| 4. | BIOS CONSOLE | 4-6 |
| 4.1 | BIOS SETUP OVERVIEW | 4-6 |
| 4.2 | STANDARD CMOS SETUP | 4-7 |
| 4.3 | ADVANCED CMOS SETUP | 4-8 |
| 4.4 | ADVANCED CHIPSET SETUP | 4-10 |
| 4.5 | PERIPHERAL SETUP | 4-11 |
| 4.6 | AUTO-DETECT HARD DISKS | 4-12 |
| 4.7 | PASSWORD SETTING | 4-12 |
| 4.7.1 | Setting Password | 4-12 |
| 4.7.2 | Password Checking | 4-12 |
| 4.8 | LOAD DEFAULT SETTING | 4-12 |
| 4.8.1 | Auto Configuration with Optimal Setting | 4-12 |
| 4.8.2 | Auto Configuration with Fail Safe Setting | 4-12 |
| 4.9 | BIOS EXIT | 4-13 |
| 4.9.1 | Save Settings and Exit | 4-13 |
| 4.9.2 | Exit Without Saving | 4-13 |
| 4.10 | BIOS UPDATE | 4-14 |
| 5. | SPECIFICATIONS | 5-1 |
| 6. | PLACEMENT & DIMENSIONS | 6-1 |
| 6.1 | PLACEMENT | 6-1 |
| 6.2 | DIMENSIONS | 6-2 |

0.PREFACE

0.1 COPYRIGHT NOTICE AND DISCLAIMER

This document is copyrighted, 2002, by Acrosser Technology Co., Ltd. All rights are reserved. No part of this manual may be reproduced, copied, transcribed, stored in a retrieval system, or translated into any language or computer language in any form or by any means, such as electronic, mechanical, magnetic, optical, chemical, manual or other means without the prior written permission or original manufacturer.

Acrosser Technology assumes no responsibility or warranty with respect to the content in this manual and specifically disclaims any implied warranty of merchantability or fitness for any particular purpose. Furthermore, Acrosser Technology reserves the right to make improvements to the products described in this manual at any times without notice. Such revisions will be posted on the Internet (WWW.ACROSSER.COM) as soon as possible.

Possession, use, or copy of the software described in this publication is authorized only pursuant to valid written license from Acrosser or an authorized sub licensor.

ACKNOWLEDGEMENTS

Acrosser, AMI, IBM PC/AT, ALI, Windows 3.1, MS-DOS...are registered trademarks.

All other trademarks and registered trademarks are the property of their respective owners.

0.2 WELCOME TO THE AR-B9629 CPU BOARD

This guide introduces the Acrosser AR-B9629 CPU Board.

Use information provided in this manual describes this card's functions and features. It also helps you start, set up and operate your AR-B9629. General system information can also be found in this publication.

0.3 BEFORE YOU USE THIS GUIDE

Please refer to the Chapter 3, "Setting System," in this guide, if you have not already installed this AR-B9629. Check the packing list before you install and make sure the accessories are completely included.

AR-B9629 CD provides the newest information regarding the CPU card. **Please refer to the README.DOC file of the enclosed utility CD.** It contains the modification and hardware & software information, and adding the description or modification of product function after manual printed.

0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires any services, contact the distributor or sales representative from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original shipping container for this purpose.

You can help assure efficient servicing for your product by following these guidelines:

1. Include your name, address, daytime telephone, facsimile number and E-mail.
2. A description of the system configuration and/or software at the time of malfunction.
3. A brief description of the problem occurred.

0.5 TECHNICAL SUPPORT AND USER COMMENTS

User's comments are always welcome as they assist us in improving the quality of our products and the understanding of our publications. They create a very important part of the input used for product enhancement and revision.

We may use and distribute any of the information you provide in any way we appropriate without incurring any obligation. You may, of course, continue to use the information you provide.

If you have any suggestions for improving particular sections or if you find any errors, please send your comments to Acrosser Technology Co., Ltd. or your local sales representative and indicate the manual title and book number.

Internet electronic mail to: webmaster@acrosser.com

0.6 ORGANIZATION

This information for users covers the following topics (see the Table of Contents for a detailed listing):

- Chapter 1, "Overview", provides an overview of the system features and packing list.
- Chapter 2, "System Controller" describes the major structure.
- Chapter 3, "Setting Up the System", describes how to adjust the jumper, and the connectors setting.
- Chapter 4, "BIOS Console", providing the BIOS options setting.
- Chapter 5, Specifications
- Chapter 6, Placement & Dimensions

0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.

Static electricity is a constant danger to the computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. Therefore, It is an important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always the best to safeguard against accidents, which may result in expensive repairs. The following measures should generally be sufficient to protect your equipment from static discharge:

- Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
- When unpacking and handling the board or other system components, place all materials on an antic static surface.
- Be careful not to touch the components on the board, especially the "golden finger" connectors on the bottom of every board.

1. OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

1.1 INTRODUCTION

The AR-B9629 is a new generation half-size, 386SX board. This card offers much greater performance than the older cards such as support for onboard 2MB DRAM.

The unit also comes with a programmable watchdog timer and other typical interfaces. The 386 CPU board is excellent for embedded systems, MMI's, workstations, medical applications or POS/POI systems.

1.2 PACKING LIST

The accessories are included with the system. Before you begin installing your AR-B9629 board, take a moment to make sure that the following items have been included inside the AR-B9629 package.

- The quick setup manual
- 1 AR-B9629 all-in-one single CPU board
- 1 AR-B9449 ISA card (Reserved)
- 1 Parallel port interface cable (Reserved)
- 1 PS/2 mouse & keyboard cables (Reserved)

1.3 FEATURES

The system provides a number of special features that enhance its reliability, ensure its availability, and improve its expansion capabilities, as well as its hardware structure.

- ALI 80386SX-33/40 MHz CPU
- PC/AT compatible keyboard & Mouse
- Programmable watchdog timer
- Flash BIOS
- Signal 5V power requirement
- Multi-layer PCB for noise reduction
- Dimensions: 82.6mmX57.2mm

2. SYSTEM CONTROLLER

This chapter describes the major structure of the AR-B9629 CPU board. The following topics are covered:

- Microprocessor
- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Serial Port (AR-B9449)
- Parallel Port (AR-B9449)

2.1 MICROPROCESSOR

The AR-B9629 uses the ALI M6117 CPU; it is designed to perform systems like Intel's 386SX system with deep green features.

The 386SX core is the same as M1386SX of Acer Labs. Inc. and 100% object code compatible with the Intel 386SX microprocessor. System manufacturers can provide 386 CPU based systems optimized for both cost and size. Instruction pipelining and high bus bandwidth ensure short average instruction execution time and high system production. Furthermore, it can keep the state internally from charge leakage while external clock to the core is stopped without storing the data in registers. The power consumption here is almost zero until the clock stops. The internal structure of this core is 32-bit data and address bus with very low supply current. Real mode as well as Protected mode are available and can run MS-DOS /MS-Windows.

2.2 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented in the AR-B9629 board. Each controller is a four-channel DMA device that will generate the memory addresses and will control signals necessary to transfer information directly between a peripheral device and memory. This allows high speeding information transference with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transferring to 8-bit peripherals (DMA1) and three channels for transferring to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The following is the system information of DMA channels:

| DMA Controller 1 | DMA Controller 2 |
|-----------------------------|-------------------------------------|
| Channel 0: Spare | Channel 4: Cascade for controller 1 |
| Channel 1: IBM SDLC | Channel 5: Spare |
| Channel 2: Diskette adapter | Channel 6: Spare |
| Channel 3: Spare | Channel 7: Spare |

Table 2-1 DMA Channel Controller

2.3 KEYBOARD CONTROLLER

The 8042 processor is programmed to support the keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

Data can be written to the keyboard by writing data to the output buffer of the keyboard controller.

Each byte of data is sent to the keyboard controller in series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to keyboard controller until acknowledgment is received for the previous byte sent. The "output buffer full" interruption may be used for both send-and-receive routines.

2.4 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the AR-B9629 board. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute.

The following is the system information of interrupts levels:

| <u>Interrupt Level</u> | <u>Description</u> |
|------------------------|--|
| NMI | Parity check |
| CTRL1 | CTRL2 |
| IRQ 0 | System timer interrupt from timer 8254 |
| IRQ 1 | Keyboard output buffer full |
| IRQ 2 | Rerouting to IRQ 8 & IRQ 14 |
| | — IRQ 8: Real time clock |
| | — IRQ 12: PS/2 mouse |
| | — IRQ 13: Math. coprocessor |
| | — IRQ 14: Hard disk adapter (AR-B9449) |
| IRQ 4 | Serial port 1 (AR-B9449) |
| IRQ 6 | Floppy disk adapter (AR-B9449) |
| IRQ 7 | Parallel port 1 (AR-B9449) |

Figure 2-1 Interrupt Controller

2.4.1 I/O Port Address Map

| Hex Range | Device |
|-----------|---|
| 000-01F | DMA controller 1 |
| 020-021 | Interrupt controller 1 |
| 022-023 | ALI M6117 chipset address |
| 040-04F | Timer 1 |
| 050-05F | Timer 2 |
| 060-06F | 8042 keyboard/controller |
| 070-071 | Real-time clock (RTC), non-maskable interrupt (NMI) |
| 080-09F | DMA page registers |
| 0A0-0A1 | Interrupt controller 2 |
| 0C0-0DF | DMA controller 2 |
| 0F0 | Clear Math Co-processor |
| 0F1 | Reset Math Co-processor |
| 0F8-0FF | Math Co-processor |
| 170-178 | Fixed disk 1 |
| 1F0-1F8 | Fixed disk 0 |
| 208-20A | EMS register 0 |
| 218-21A | EMS register 1 |
| 300-31F | Prototype card/streaming type adapter |
| 378-37F | Parallel printer port 1 (LPT 1) |
| 380-38F | SDLC, bisynchronous |
| 3A0-3AF | Bisynchronous |
| 3B0-3BF | Monochrome display and printer port 3 (LPT 3) |
| 3D0-3DF | Color/graphics monitor adapter |
| 3F0-3F7 | Diskette controller |
| 3F8-3FF | Serial port 1 (COM 1) |

Table 2-2 I/O Port Address Map

2.4.2 Real-Time Clock and Non-Volatile RAM

The AR-B9629 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long periods of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed below:

| Address | Description |
|---------|---|
| 00 | Seconds |
| 01 | Second alarm |
| 02 | Minutes |
| 03 | Minute alarm |
| 04 | Hours |
| 05 | Hour alarm |
| 06 | Day of week |
| 07 | Date of month |
| 08 | Month |
| 09 | Year |
| 0A | Status register A |
| 0B | Status register B |
| 0C | Status register C |
| 0D | Status register D |
| 0E | Diagnostic status byte |
| 0F | Shutdown status byte |
| 10 | Diskette drive type byte, drive A and B |
| 11 | Fixed disk type byte, drive C |
| 12 | Fixed disk type byte, drive D |
| 13 | Reserved |
| 14 | Equipment byte |
| 15 | Low base memory byte |
| 16 | High base memory byte |
| 17 | Low expansion memory byte |
| 18 | High expansion memory byte |
| 19-2D | Reserved |
| 2E-2F | 2-byte CMOS checksum |
| 30 | Low actual expansion memory byte |
| 31 | High actual expansion memory byte |
| 32 | Date century byte |
| 33 | Information flags (set during power on) |
| 34-7F | Reserved for system BIOS |

Table 2-3 Real-Time Clock & Non-Volatile RAM

2.4.3 Timer

The AR-B9629 provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.
Application programs can load different counts into this timer to generate various sound frequencies.

2.5 SERIAL PORT

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are not only used to convert parallel data to a serial format on the transmit side but also used to convert serial data to parallel on the receiver side. In order of transmission and reception, the serial format is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are not only included to use this 16x clock to drive the receiver logic but also included in the ACE as a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The following table is a summary of each ACE accessible register

| DLAB | Port Address | Register |
|------|--------------|--|
| 0 | base + 0 | Receiver buffer (read) |
| | | Transmitter holding register (write) |
| 0 | base + 1 | Interrupt enable |
| X | base + 2 | Interrupt identification (read only) |
| X | base + 3 | Line control |
| X | base + 4 | MODEM control |
| X | base + 5 | Line status |
| X | base + 6 | MODEM status |
| X | base + 7 | Scratched register |
| 1 | base + 0 | Divisor latch (least significant byte) |
| 1 | base + 1 | Divisor latch (most significant byte) |

Table 2-4 ACE Accessible Registers

(1) Receiver Buffer Register (RBR)

Bit 0-7: Received data byte (Read Only)

(2) Transmitter Holding Register (THR)

Bit 0-7: Transmitter holding data byte (Write Only)

(3) Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)

Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)

Bit 2: Enable Receiver Line Status Interrupt (ELSI)

Bit 3: Enable MODEM Status Interrupt (EDSSI)

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

(4) Interrupt Identification Register (IIR)

Bit 0: "0" if Interrupt Pending

Bit 1: Interrupt ID Bit 0

Bit 2: Interrupt ID Bit 1

Bit 3: Must be 0

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

(5) Line Control Register (LCR)

Bit 0: Word Length Select Bit 0 (WLS0)

Bit 1: Word Length Select Bit 1 (WLS1)

| <u>WLS1</u> | <u>WLS0</u> | <u>Word Length</u> |
|-------------|-------------|--------------------|
| 0 | 0 | 5 Bits |
| 0 | 1 | 6 Bits |
| 1 | 0 | 7 Bits |
| 1 | 1 | 8 Bits |

Bit 2: Number of Stop Bit (STB)

Bit 3: Parity Enable (PEN)

Bit 4: Even Parity Select (EPS)

Bit 5: Stick Parity

Bit 6: Set Break

Bit 7: Divisor Latch Access Bit (DLAB)

(6) MODEM Control Register (MCR)

Bit 0: Data Terminal Ready (DTR)

Bit 1: Request to Send (RTS)

Bit 2: Out 1 (OUT 1)

Bit 3: Out 2 (OUT 2)

Bit 4: Loop

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

(7) Line Status Register (LSR)

Bit 0: Data Ready (DR)

Bit 1: Overrun Error (OR)

Bit 2: Parity Error (PE)

Bit 3: Framing Error (FE)

Bit 4: Break Interrupt (BI)

Bit 5: Transmitter Holding Register Empty (THRE)

Bit 6: Transmitter Shift Register Empty (TSRE)

Bit 7: Must be 0

(8) MODEM Status Register (MSR)

Bit 0: Delta Clear to Send (DCTS)

Bit 1: Delta Data Set Ready (DDSR)

Bit 2: Training Edge Ring Indicator (TERI)

Bit 3: Delta Receive Line Signal Detect (DSLSD)

Bit 4: Clear to Send (CTS)

Bit 5: Data Set Ready (DSR)

Bit 6: Ring Indicator (RI)

Bit 7: Received Line Signal Detect (RSLD)

(9) Divisor Latch (LS, MS)

| | LS | MS |
|--------|-----------|-----------|
| Bit 0: | Bit 0 | Bit 8 |
| Bit 1: | Bit 1 | Bit 9 |
| Bit 2: | Bit 2 | Bit 10 |
| Bit 3: | Bit 3 | Bit 11 |
| Bit 4: | Bit 4 | Bit 12 |
| Bit 5: | Bit 5 | Bit 13 |
| Bit 6: | Bit 6 | Bit 14 |
| Bit 7: | Bit 7 | Bit 15 |

| Desired Baud Rate | Divisor Used to Generate 16x Clock |
|--------------------------|---|
| 300 | 384 |
| 600 | 192 |
| 1200 | 96 |
| 1800 | 64 |
| 2400 | 48 |
| 3600 | 32 |
| 4800 | 24 |
| 9600 | 12 |
| 14400 | 8 |
| 19200 | 6 |
| 28800 | 4 |
| 38400 | 3 |
| 57600 | 2 |
| 115200 | 1 |

Table 2-5 Serial Port Divisor Latch

2.6 PARALLEL PORT**(1) Register Address**

| Port Address | Read/Write | Register |
|---------------------|-------------------|-----------------------|
| base + 0 | Write | Output data |
| base + 0 | Read | Input data |
| base + 1 | Read | Printer status buffer |
| base + 2 | Write | Printer control latch |

Table 2-6 Registers' Address

(2) Printer Interface Logic

The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

(3) Data Swapper

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address.

(4) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described below:

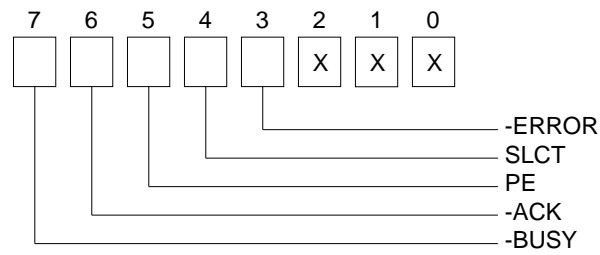


Figure 2-2 Printer Status Buffer

NOTE: X represents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

Bit 5: A 1 means the printer has detected the end of the paper.

Bit 4: A 1 means the printer is selected.

Bit 3: A 0 means the printer has encountered an error condition.

(5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

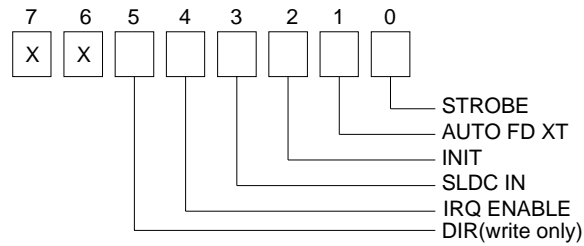


Figure 2-3 Bit's Definition

NOTE: X represents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is writing only.

Bit 4: A 1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A 1 in this bit position selects the printer.

Bit 2: A 0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

3. SETTING UP THE SYSTEM

This section describes the pin assignments for system's external connectors and the jumper settings.

- Overview
- System Setting

3.1 OVERVIEW

The AR-B9629 is an all-in-one, half-size, 386SX CPU board. This section provides hardware jumper settings, the connectors' locations, and the pin assignment.

CAUTION: The CPU board doesn't support the SIMM-type DRAM.

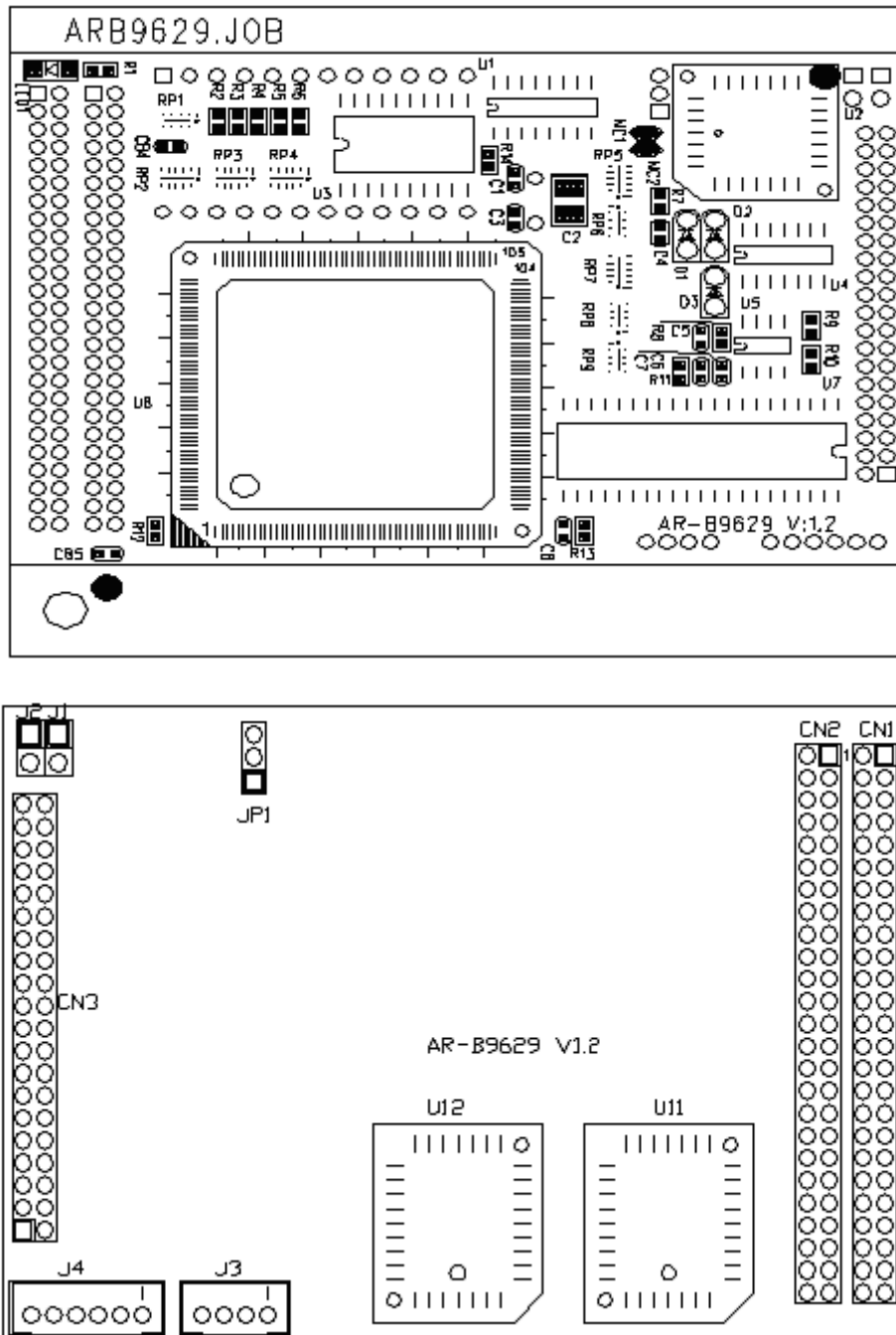


Figure 3-1 External System Location

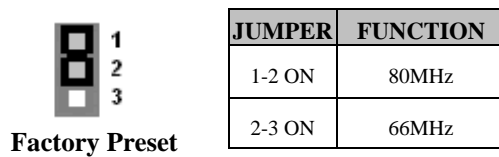
3.2 SYSTEM SETTINGS

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor [shorting plug] that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the AR-B9629 jumper pins, and the factory-default settings.

CAUTION: Do not touch any electronic component unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage the electronic components.

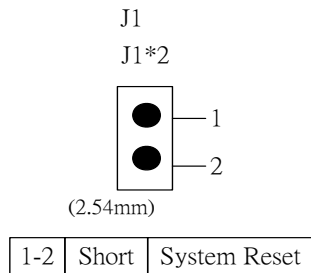
3.2.1 Clock Jumper (JP1)



JP1: Clock Jumper

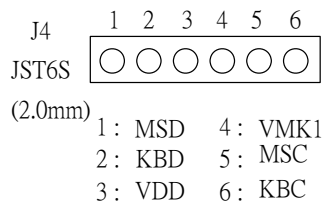
3.2.2 Reset (J1)

Reserved



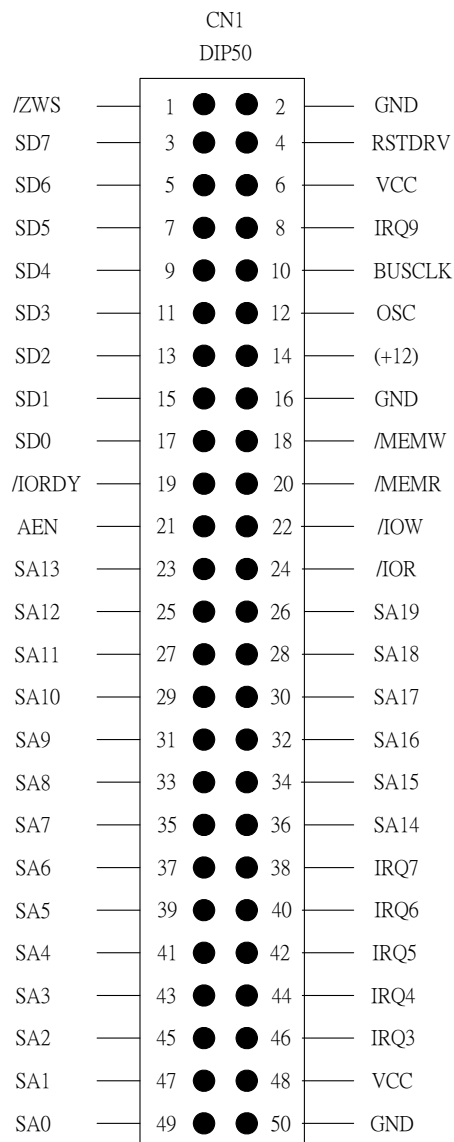
J1: Reset

3.2.3 PS2 KB4 Mouse (J4)

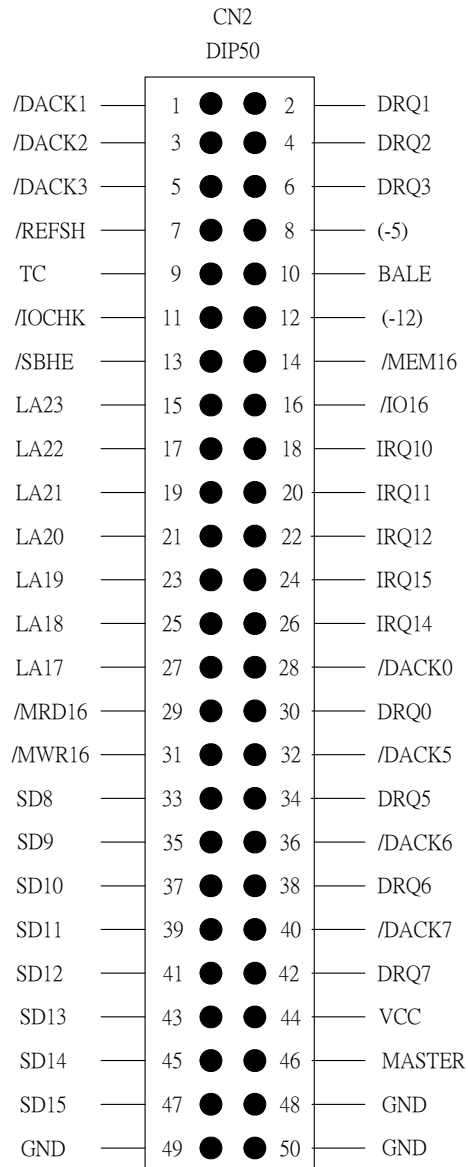


J4: PS2 KB4 Mouse

3.2.4 ISA Bus Connector (CN1)



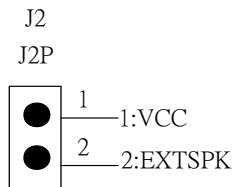
CN1: ISA Bus Connector



CN2: ISA Bus Connector

3.2.5 External Buzzer (J2)

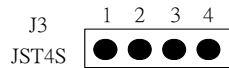
Reserved



J2: External Buzzer

3.2.6 Power Connector (J3)

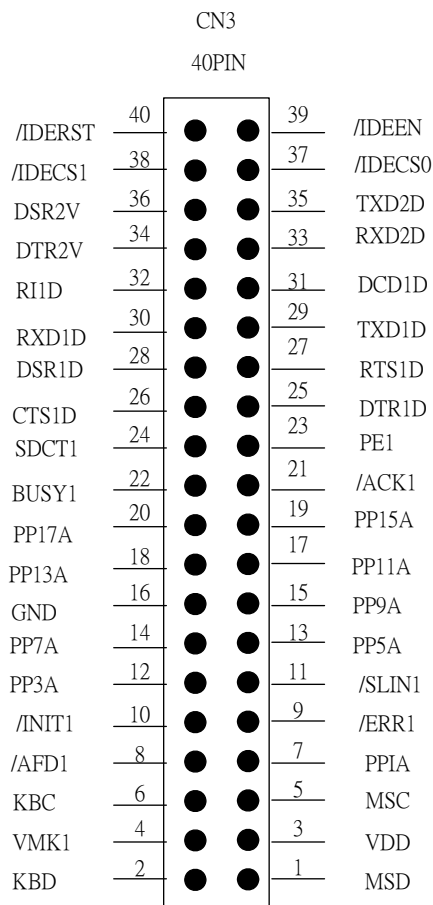
Reserved



1 : VDD
2 : GND
3 : GND
4 : VDD

J3: Power Connector

3.2.7 I/O Connector for KB/MS, serial port, parallel port (CN3)



CN3: I/O Connector

4. BIOS CONSOLE

This chapter describes the AR-B9629 BIOS menu displays and explains how to perform common tasks needed to get up and running, and presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Peripheral Setup
- Auto-Detect Hard Disks
- Password Setting
- Load Default Setting
- BIOS Exit

4.1 BIOS SETUP OVERVIEW

BIOS is a program used to initialize and set up the I/O system of the computer, which includes the ISA bus and connected devices such as the video display, diskette drive, and the keyboard.

The BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS Default Values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

After the computer turned on, the BIOS will perform a diagnostics of the system and will display the size of the memory that is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

The BIOS Setup main menu includes some options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to assure the option and configure the functions.

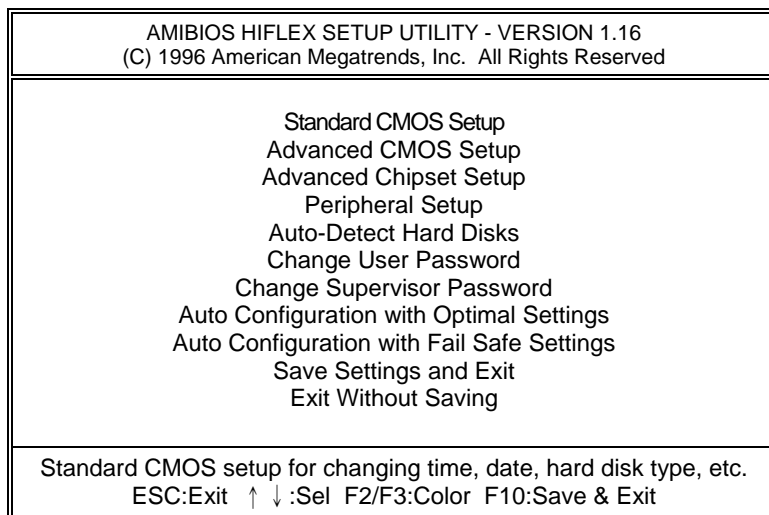


Figure 4-1 BIOS: Setup Main Menu

- CAUTION:**
1. AR-B9629 BIOS the factory-default setting is used to the <Auto Configuration with Optimal Settings> Acrosser recommends using the BIOS default setting, unless you are very familiar with the setting function, or you can contact the technical support engineer.
 2. If the BIOS loss setting, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operation system, this option will reduce the performance of the system. Acrosser recommends choosing the <Auto Configuration with Optimal Setting> in the main menu. The option is best-case values that should optimize system performance.
 3. The BIOS settings are described in detail in this section.

4.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

| AMIBIOS SETUP - STANDARD CMOS SETUP | |
|--|-------------------|
| (C) 1996 American Megatrends, Inc. All Rights Reserved | |
| Date (mm/dd/yyyy): Sun Dec 06, 1998 | 640KB |
| Time (hh/mm/ss): 13:39:30 | 1MB |
| Floppy Drive A: 1.44 MB 3.5 | |
| Floppy Drive B: Not Installed | |
| | LBA Blk 32Bit PIO |
| Type Size Cyln Head Wpcom Sec Mode Mode Mode Mode | |
| Pri Master : Auto | Auto |
| Pri Slave : Auto | Auto |
| Boot Sector Virus Protection Disabled | |
| Month: Jan - Dec | ESC:Exit ↑ ↓ :Sel |
| Day: 01 - 31 | PgUp/PgDn:Modify |
| Year: 1901 - 2099 | F2/F3:Color |

Figure 4-2 BIOS: Standard CMOS Setup

Date & Time Setup

Highlight the <Date> field and then press the [Page Up] / [Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] / [Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master>, <Pri Slave>, <Sec Master> and <Sec Slave> so the user can install up to two hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during bootup. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives, which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

Boot Sector Virus Protection

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is <Disabled>. This setting is recommended because it conflicts with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

4.3 ADVANCED CMOS SETUP

The <Advanced CMOS SETUP> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings.

| AMBIOS SETUP – ADVANCED CMOS SETUP (C) 1998 American Megatrends, Inc. All Rights Reserved | | |
|--|----------|---------------------------------|
| 1st Boot Device | IDE-0 | Available Options : Disabled |
| 2nd Boot Device | Floppy | |
| 3rd Boot Device | IDE-1 | IDE-0 |
| 4th Boot Device | Disabled | IDE-1 |
| Try Other Boot Devices | Yes | IDE-2 |
| Quick Boot | Disabled | IDE-3 |
| BootUp Num-Lock | On | Floppy |
| Floppy Drive Swap | Disabled | ARMD-FDD |
| Floppy Drive Seek | Disabled | ARMD-HDD |
| Floppy Access Control | Normal | CDROM |
| HDD Access Control | Normal | SCSI |
| PS/2 Mouse Support | Disabled | NETWORK |
| Typematic Rate | Slow | |
| System Keyboard | Absent | |
| Primary Display | Absent | |
| Password Check | Setup | |
| Wait For 'F1' If Error | Enabled | |
| Hit 'DEL' Message Display | Enabled | |
| C000, 32k Shadow | Disabled | |
| C800, 32k Shadow | Disabled | |
| D000, 32k Shadow | Disabled | ESC:Exit ↑ ↓ :Sel |
| D800, 32k Shadow | Disabled | PgUp/PgDn:Modify |
| E000, 32k Shadow | Disabled | F2/F3:Color |
| E800, 32k Shadow | Disabled | |
| INTERNAL-FLASH-DISK | E8000H | |

Figure 4-3 BIOS: Advanced CMOS Setup

1st Boot Device

2nd Boot Device

3rd Boot Device

4th Boot Device

These options determine where the system looks first for an operating system. The default setting is to check first the hard disk and then the floppy drive, and last the CDROM.

BootUp Num-Lock

This item is used to activate the Num Lock function upon system boot. If the setting is on, after a boot, the Num Lock light is lit, and user can use the number key.

Floppy Drive Swap

The option reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of **Disabled** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When the function's setting is <**Enabled**>, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Floppy Drive Seek

If the <Floppy Drive Seek> item is setting **Enabled**, the BIOS will seek the floppy <A> drive one time upon bootup.

PS/2 Mouse Support

The setting of **Enabled** allows the system to detect a PS/2 mouse on bootup. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. **Disabled** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

System Keyboard

This function specifies that a keyboard will be attached to the computer.

Primary Display

The option is used to set the type of video display card installed in the system.

Password Check

This option enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If **Always** is chosen, a user password prompt appears every time the computer is turned on. If **Setup** is chosen, the password prompt appears if the BIOS executed.

Wait for 'F1' If Error

AMIBIOS POST error messages are followed by:

Press <F1> to continue

If this option is set to **Disabled**, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Hit 'DEL' Message Display

Set this option to **Disabled** to prevent the message as follows:

Hit 'DEL' if you want to run setup

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Shadow

These options control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

| SETTING | DESCRIPTION |
|----------|--|
| Disabled | The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory. |
| Enabled | The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution. |
| Cached | The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory. |

Table 4-1 Shadow Setting

4.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.

| AMIBIOS SETUP - ADVANCED CHIPSET SETUP (C) 1995 American Megatrends, Inc. All Rights Reserved | | |
|--|------------|--|
| AT Bus Clock | 14.318 / 2 | Available Options : 14.318/2 PLCK2/3 PLCK2/4 PLCK2/5 PLCK2/6 PLCK2/8 PLCK2/10 PLCK2/12 ESC:Exit ↑ ↓ :Sel PgUp/PgDn:Modify F2/F3:Color |
| Slow Refresh | 15 us | |
| RAS Precharge time | 3.5T | |
| RAS Active Time Insert Wait | Disable | |
| CAS Precharge Time Insert Wait | Disable | |
| Memory Write Insert Wait | Disable | |
| ISA I/O High Speed | Disable | |
| ISA Memory High Speed | Disable | |
| I/O Recovery | Enable | |
| I/O Recovery Period | 1.25 us | |
| 16Bit ISA Insert Wait | Disable | |
| Watchdog Timer Output Control | Disable | |
| WatchDog Timeout Issue Signal | Reset | |

Figure 4-4 BIOS: Advanced Chipset Setup

AT Bus Clock

This option sets the polling clock speed of ISA Bus (PC/104).

-
- NOTE:** 1. PCLK means the CPU inputs clock.
2. Acrosser recommends user setting at the range of 8MHz to 10MHz.

Slow Refresh

This option sets the DRAM refresh cycle time.

RAS Precharge Time

The DRAM RAS precharge time.

Time Insert Wait

The DRAM time insert wait: RAS Active and CAS Precharge function setting.

ISA High Speed

The Speed field shows the speed at which the processor runs internally.

I/O Recovery

If I/O Recovery Feature options are enabled, the BIOS insert a delay time between two I/O commands. The delay time is defined in I/O Recovery Period option.

4.5 PERIPHERAL SETUP

This section is used to configure peripheral features.

| AMIBIOS SETUP - PERIPHERAL SETUP (C) 1998 American Megatrends, Inc. All Rights Reserved | | |
|--|---------|---|
| Hard disk Delay | Disable | Available Options : 3 Sec 5 Sec 10 Sec 15 Sec ESC:Exit ↑ ↓ :Sel PgUp/PgDn:Modify F2/F3:Color |
| OnBoard Primary IDE | Primary | |
| OnBoard FDC | Auto | |
| OnBoard Serial Port1 | 3F8h | |
| OnBoard Serial Port1 IRQ | 4 | |
| OnBoard Serial Port2 | 2F8h | |
| OnBoard Serial Port2 IRQ | 3 | |
| OnBoard Parallel Port | 378 | |
| Parallel Port Mode | Normal | |
| EPP Version | N/A | |
| Parallel Port IRQ | 7 | |
| Parallel Port DMA Channel | N/A | |

Figure 4-5 BIOS: Peripheral Setup

Hard Disk Delay

If this option is set to **Disabled** and the system BIOS executes too fast, the result is the BIOS can't find the hard disk drive.

OnBoard IDE

This option specifies the onboard IDE controller channels that will be used.

OnBoard FDC

This option enables the floppy drive controller on the AR-B9629.

OnBoard Serial Port

This option enables the serial port on the AR-B9629.

OnBoard Parallel Port

This option enables the parallel port on the AR-B9629.

Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes that adhere to the IEEE P1284 specifications.

Parallel Port DMA Channel

This option is only available if the setting for the parallel Port Mode option is ECP.

4.6 AUTO-DETECT HARD DISKS

This option detects the parameters of an IDE hard disk drive, and automatically enters them into the Standard CMOS Setup screen.

4.7 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. User can set either a Supervisor password or a User password.

4.7.1 Setting Password

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after BIOS completes. The next time the system boots, you are prompted for the password function is present and is enabled.

Enter new supervisor password:

4.7.2 Password Checking

The password check option is enabled in Advanced Setup by choosing either **Always** (the password prompt appears every time the system is powered on) or **Setup** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. User can enter a password by typing on the keyboard. As user select Supervisor or User. The BIOS prompts for a password, user must set the Supervisor password before user can set the User password. Enter 1-6 character as password. The password does not appear on the screen when typed. Make sure you write it down.

4.8 LOAD DEFAULT SETTING

In this section permit user to select a group of setting for all BIOS Setup options. You not only can use these items to quickly set system configuration parameters, but also can choose a group of settings that have a better chance of working when the system is having configuration related problems.

4.8.1 Auto Configuration with Optimal Setting

User can load the optimal default settings for the BIOS. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

Load high performance settings (Y/N) ?

4.8.2 Auto Configuration with Fail Safe Setting

User can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.

The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

Load failsafe settings (Y/N) ?

4.9 BIOS EXIT

This section is used to exit the BIOS main menu in two types situation. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

4.9.1 *Save Settings and Exit*

This item set in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you to save data to CMOS and Exit the Setup.

Save current settings and exit (Y/N) ?

4.9.2 *Exit Without Saving*

When you select this option, the following message will appear at the center of the screen to help to Abandon all Data and Exit Setup.

Quit without saving (Y/N) ?

4.10 BIOS UPDATE

The BIOS program instructions are contained within computer chips called FLASH ROMs that are located on your system board. The chips can be electronically reprogrammed, allowing you to upgrade your BIOS firmware without removing and installing chips.

The AR-B9629 provides FLASH BIOS update function for you to easily upgrade newer BIOS version. Please follow the operating steps for updating new BIOS:

Step 1: Turn on your system and don't detect the CONFIG.SYS and AUTOEXEC.BAT files. Keep your system in the real mode.

Step 2: Insert the FLASH BIOS diskette into the floppy disk drive.

Step 3: In the MS-DOS mode, you can type the AMIFLASH program.

```
A:\>AMIFLASH
```

Step 4: The screen will show the message as follow:

Enter the BIOS File name from which Flash EPROM will be programmed. The File name must and with a <ENTER> or press <ESC> to exit.

Step 5: And then please enter the file name to the box of <Enter File Name>. And the box of <Message> will show the notice as follow. In the bottom of this window always show the gray statement.

Flash EPROM Programming is going to start. System will not be usable until Programming of Flash EPROM is successfully complete. In case of any error, existing Flash EPROM must be replaced by new program Flash EPROM.

Step 6: As the gray statement, press the <Y> key to updating the new BIOS. And then the <Message> box will show the <Programming Flash EPROM>, and the gray statement shows <Please Wait>.

Step 7: The BIOS update is successful, the message will show <Flash Update Completed - Pass>.

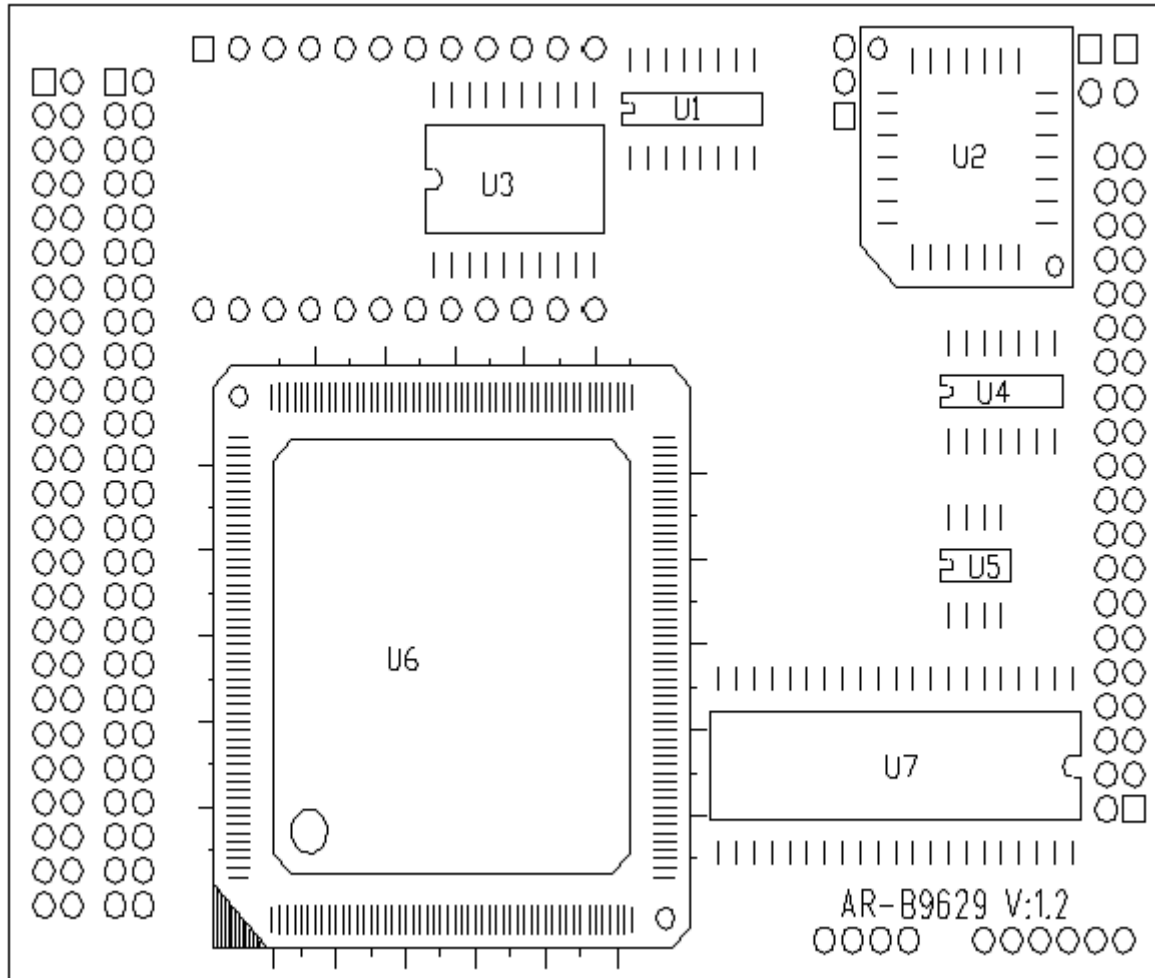
-
- NOTE:**
1. After turn on the computer and the system didn't detect the boot procedure, please press the [F5] key immediately. The system will pass the CONFIG.SYS and AUTOEXEC.BAT files.
 2. The BIOS Flash disk is not the standard accessory. Now the onboard BIOS is the newest BIOS, if user needs adding some functions in the future please contact technical supporting engineers, they will provide the newest BIOS for updating.
 3. The file of AMIFLASH.EXE had to use the attached diskette's file, if not user had to use the Version 6.31.

5. SPECIFICATIONS

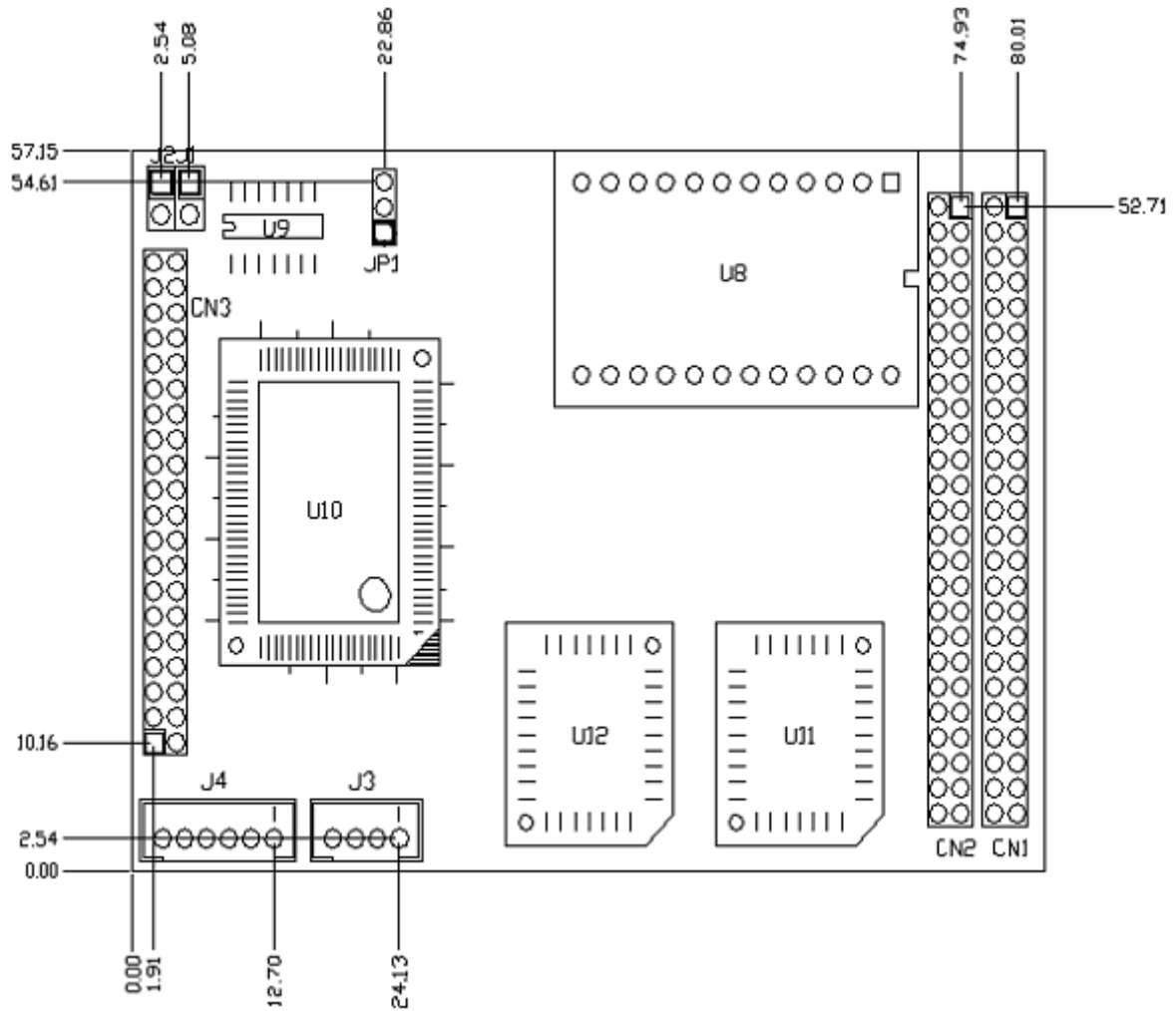
| | |
|---------------------------|--|
| Model No. | AR-B9629 |
| Description | 386 Grade CPU Board with EPROM socket, ISA Bus |
| Version/ Date | V0.1, 10/24/02 |
| CPU & Chipset: | ALI 386SX-33 CPU; ALI M6117C, 25/33/40 MHz (default: 40) |
| System Memory: | 2M Byte EDO ROM on-Board |
| Memory: | 512K EPROM socket (one SSD socket for 27C040) |
| Power Connector: | JST 4S Connector |
| I/O: | 2 Serial Ports (TTL Level), 1 Printer Port, 1 IDE Port, Keyboard and Mouse Port, ISA Interface Connector |
| Extension BUS: | Two 50 pins 2.0 mm connectors for ISA bus extension |
| LED Indicator: | On Board power LED |
| Power Requirement: | +5V-1.0A maximum (based on 33 MHz clock frequency) |
| CE-Design In | Add EMI components to keyboard and PS/2 mouse |
| PC Board: | 4 layers |
| Dimensions: | 82.6 mmX57.2mm |
| Operating Temp. | 0~60°C |
| Storage Temp. | -20~80°C |
| Operating Humidity | 0~90% relative humidity none-condensing |
| Order Information: | AR-B9449 is a collocation tool for writing program on AR-B9629 |

6. PLACEMENT & DIMENSIONS

6.1 PLACEMENT



6.2 DIMENSIONS



Unit: mil (1 inch = 25.4 mm = 1000 mil)

Note:

If the content in Setting is inconsistent with CD-ROM, please refer to the Setting as priority.