AR-B9622
Half Size All-In-One
386SX CPU BOARD
User's Guide

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0.PREFACE

0.1 COPYRIGHT NOTICE AND DISCLAIMER

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0.2 WELCOME TO THE AR-B9622 CPU BOARD

This guide introduces the Acrosser AR-B9622 CPU board.

Use the information describes this card's functions, features, and how to start, set up and operate your AR-B9622. You can also find general system information here.

0.3 BEFORE YOU USE THIS GUIDE

If you have not already installed this AR-B9622, refer to the Chapter 3, "Setting Up the System" in this guide. Check the packing list, make sure the accessories are in the package.

AR-B9622 diskette provides the latest information about the card**. Please refer to the README.DOC file of the enclosed utility diskette**. It contains the modification and hardware & software information, and adding the description or modification of product function after manual published.

0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires servicing, contact the dealer from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original shipping container for this purpose.

You can help assure efficient servicing of your product by following these guidelines:

1. Include your name, address, telephone and facsimile number where you may be reached during the day.
2. A description of the system configuration and/or software at the time of malfunction.
3. A brief description of the symptoms.

0.5 TECHNICAL SUPPORT AND USER COMMENTS

User's**錯誤! 尚未定義書籤。** comments are always welcome as they assist us in improving the usefulness of our products and the understanding of our publications. They form a very important part of the input used for product enhancement and revision.

We may use and distribute any of the information you supply in any way we believe appropriate without incurring any obligation. You may, of course, continue to use the information you supply.

If you have suggestions for improving particular sections or if you find any errors, please indicate the manual title and book number.

Please send your comments to Acrosser Technology Co., Ltd. or your local sales representative.

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0.6 ORGANIZATION

This information for users covers the following topics (see the Table of Contents for a detailed listing):

- Chapter 1, "Overview", provides an overview of the system features and packing list.
- Chapter 2, "System Controller" describes the major structure.
- Chapter 3, "Setting Up the System", describes how to adjust the jumper, and the connectors setting.
- Chapter 4, "CRT/LCD Flat Panel Display", describes the configuration and installation procedure using LCD display.
- Chapter 5, "Installation", describes setup procedures including information on the utility diskette.
- Chapter 6, "BIOS Console", providing the BIOS options setting.
- Chapter 7, Specifications
- Chapter 8, Placement & Dimensions
- Chapter 9, Programming RS-485 & Index

0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.

Static electricity is a constant danger to the computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always the best to safeguard against accidents which may result in expensive repairs. The following measures should generally be sufficient to protect your equipment from static discharge:

- Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
- When unpacking and handling the board or other system components, place all materials on an antic static surface.
- Be careful not to touch the components on the board, especially the "golden finger" connectors on the bottom of every board.

1. OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

1.1 INTRODUCTION

The AR-B9622 is a new generation half-size, 386SX board. This card offers much greater performance than the older cards such as support for onboard 4MB DRAM and one RS-232C/485 and three RS-232C ports and one socket for the DiskOnChip from 2MB up to 72MB.

The unit also comes with a programmable watch dog timer and other typical interfaces. The 386 CPU board is excellent for embedded systems, MMI's, work stations, medical applications or POS/POI systems. As well, an RS-232C/485 port provides the remote control. RS-485 interface is only offered recently on 386 cards.

Especially the AR-B9622's on-board VGA, offers the most exciting possibilities yet to the industry. The on-board VGA/LCD controller brings about a whole new dimension of industrial computing. No longer do you have to worry about adding an extra card to your system. The VGA/LCD unit comes with 1MB V-RAM on board and uses the C&T 65545 Chipset, to support a wide range of LCD Panels.

1.2 PACKING LIST

The accessories are included with the system. Before you begin installing your AR-B9622 board, take a moment to make sure that the following items have been included inside the AR-B9622 package.

- The quick setup manual
- 1 AR-B9622 all-in-one single CPU board
- 1 Hard disk drive interface cable
- 1 VGA 10-pin cable
- 2 Parallel port interface cables
- 1 Keyboard adapter
- 1 PS/2 mouse adapter
- 4 phone-jack to DB-9 adapters
- 2 Software utility diskettes

1.3 FEATURES

The system provides a number of special features that enhance its reliability, ensure its availability, and improve its expansion capabilities, as well as its hardware structure.

- 80386SX-33/40 MHz CPU
- PC/104 extension bus
- On-board CRT and LCD panel display
- Supports IDE hard disk drives
- Supports floppy disk drives
- Supports 2 bi-directional parallel port
- PC/AT compatible keyboard
- Up to 72MB for one DiskOnChip
- Programmable watchdog timer
- Flash BIOS
- Signal 5V power requirement
- Multi-layer PCB for noise reduction
- Dimensions : 145mmX142mm

2. SYSTEM CONTROLLER

This chapter describes the major structure of the AR-B9622 CPU board. The following topics are covered:

- Microprocessor
- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Serial Port
- Parallel Port

2.1 MICROPROCESSOR

The AR-B9622 uses the ALI M6117 CPU; it is designed to perform systems like Intel's 386SX system with deep green features.

The 386SX core is the same as M1386SX of Acer Labs. Inc. and 100% object code compatible with the Intel 386SX microprocessor. System manufacturers can provide 386 CPU based systems optimized for both cost and size. Instruction pipelining and high bus bandwidth ensure short average instruction execution time and high system throughput. Furthermore, it can keep the state internally from charge leakage while external clock to the core is stopped without storing the data in registers. The power consumption here is almost zero until the clock stops. The internal structure of this core is 32-bit data and address bus with very low supply current. Real mode as well as Protected mode are available and can run MS-DOS /MS-Windows.

2.2 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented in the AR-B9622 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speeding information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Table 2-1 DMA Channel Controller

2.3 KEYBOARD CONTROLLER

The 8042 processor is programmed to support the keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

Data can be written to the keyboard by writing data to the output buffer of the keyboard controller.

Each byte of data is sent to the keyboard controller in series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to keyboard controller until acknowledgment is received for the previous byte sent. The "output buffer full" interruption may be used for both send-and-receive routines.

2.4 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the AR-B9622 board. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute.

The following is the system information of interrupt levels:

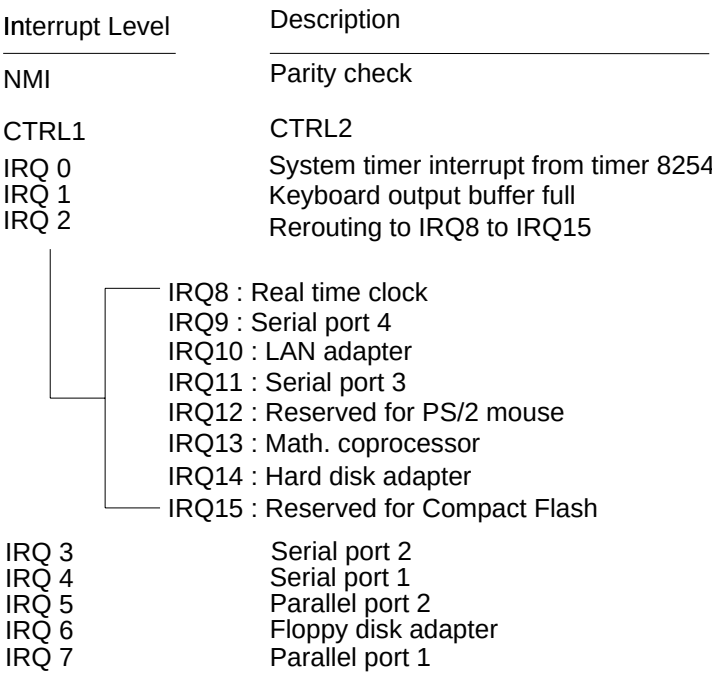


Figure 2-1 Interrupt Controller

2.4.1 I/O Port Address Map

Hex Range	Device
000-01F	DMA controller 1
020-021	Interrupt controller 1
022-023	ALI M6117 chipset address
040-04F	Timer 1
050-05F	Timer 2
060-06F	8042 keyboard/controller
070-071	Real-time clock (RTC), non-maskable interrupt (NMI)
080-09F	DMA page registers
0A0-0A1	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0	Clear Math Co-processor
0F1	Reset Math Co-processor
0F8-0FF	Math Co-processor
170-178	Fixed disk 1
1F0-1F8	Fixed disk 0
201	Game port
208-20A	EMS register 0
218-21A	EMS register 1
278-27F	Parallel printer port 2 (LPT 2)
2E8-2EF	Serial port 4 (COM 4)
2F8-2FF	Serial port 2 (COM 2)
300-31F	Prototype card/streaming type adapter
320-33F	LAN adapter
378-37F	Parallel printer port 1 (LPT 1)
380-38F	SDLC, bisynchronous
3A0-3AF	Bisynchronous
3B0-3BF	Monochrome display and printer port 3 (LPT 3)
3C0-3CF	EGA/VGA adapter
3D0-3DF	Color/graphics monitor adapter
3E8-3EF	Serial port 3 (COM 3)
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1 (COM 1)

Table 2-2 I/O Port Address Map

2.4.2 Real-Time Clock and Non-Volatile RAM

The AR-B9622 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long periods of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed below:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

Table 2-3 Real-Time Clock & Non-Volatile RAM

2.4.3 Timer

The AR-B9622 provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.
Application programs can load different counts into this timer to generate various sound frequencies.

2.5 SERIAL PORT

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The following table is a summary of each ACE accessible register

DLAB	Port Address	Register
0	base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	base + 1	Interrupt enable
X	base + 2	Interrupt identification (read only)
X	base + 3	Line control
X	base + 4	MODEM control
X	base + 5	Line status
X	base + 6	MODEM status
X	base + 7	Scratched register
1	base + 0	Divisor latch (least significant byte)
1	base + 1	Divisor latch (most significant byte)

Table 2-4 ACE Accessible Registers

(1) Receiver Buffer Register (RBR)

Bit 0-7: Received data byte (Read Only)

(2) Transmitter Holding Register (THR)

Bit 0-7: Transmitter holding data byte (Write Only)

(3) Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)
Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)
Bit 2: Enable Receiver Line Status Interrupt (ELSI)
Bit 3: Enable MODEM Status Interrupt (EDSSI)
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(4) Interrupt Identification Register (IIR)

Bit 0: "0" if Interrupt Pending
Bit 1: Interrupt ID Bit 0
Bit 2: Interrupt ID Bit 1
Bit 3: Must be 0
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(5) Line Control Register (LCR)

Bit 0: Word Length Select Bit 0 (WLS0)
Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)
Bit 3: Parity Enable (PEN)
Bit 4: Even Parity Select (EPS)
Bit 5: Stick Parity
Bit 6: Set Break
Bit 7: Divisor Latch Access Bit (DLAB)

(6) MODEM Control Register (MCR)

Bit 0: Data Terminal Ready (DTR)
Bit 1: Request to Send (RTS)
Bit 2: Out 1 (OUT 1)
Bit 3: Out 2 (OUT 2)
Bit 4: Loop
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(7) Line Status Register (LSR)

Bit 0: Data Ready (DR)
Bit 1: Overrun Error (OR)
Bit 2: Parity Error (PE)
Bit 3: Framing Error (FE)
Bit 4: Break Interrupt (BI)
Bit 5: Transmitter Holding Register Empty (THRE)
Bit 6: Transmitter Shift Register Empty (TSRE)
Bit 7: Must be 0

(8) MODEM Status Register (MSR)

Bit 0: Delta Clear to Send (DCTS)
Bit 1: Delta Data Set Ready (DDSR)
Bit 2: Training Edge Ring Indicator (TERI)
Bit 3: Delta Receive Line Signal Detect (DSLSD)
Bit 4: Clear to Send (CTS)
Bit 5: Data Set Ready (DSR)
Bit 6: Ring Indicator (RI)
Bit 7: Received Line Signal Detect (RSLD)

(9) Divisor Latch (LS, MS)

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Table 2-5 Serial Port Divisor Latch

2.6 PARALLEL PORT

(1) Register Address

Port Address	Read/Write	Register
base + 0	Write	Output data
base + 0	Read	Input data
base + 1	Read	Printer status buffer
base + 2	Write	Printer control latch

Table 2-6 Registers' Address

(2) Printer Interface Logic

The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

(3) Data Swapper

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address.

(4) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described below:

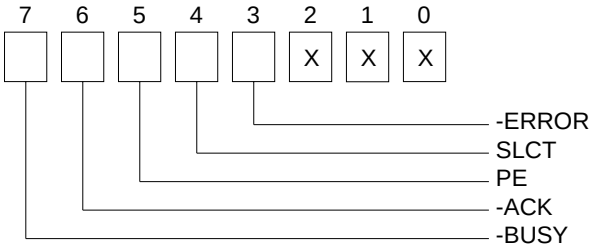


Figure 2-2 Printer Status Buffer

NOTE: X represents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and can not accept data.

Bit 6: This bit represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

Bit 5: A 1 means the printer has detected the end of the paper.

Bit 4: A 1 means the printer is selected.

Bit 3: A 0 means the printer has encountered an error condition.

(5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

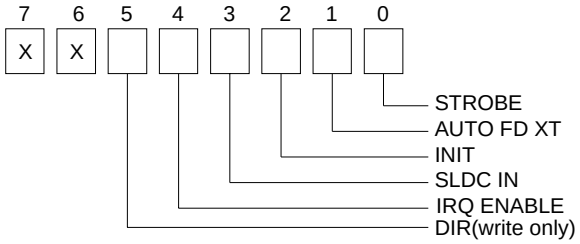


Figure 2-3 Bit's Definition

NOTE: X represents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write only.

Bit 4: A 1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A 1 in this bit position selects the printer.

Bit 2: A 0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

3. SETTING UP THE SYSTEM

This section describes the pin assignments for system's external connectors and the jumper settings.

- Overview
- System Setting

3.1 OVERVIEW

The AR-B9622 is an all-in-one, half-size, 386SX CPU board. This section provides hardware jumper settings, the connectors' locations, and the pin assignment.

CAUTION: The CPU board doesn't support the SIMM-type DRAM.

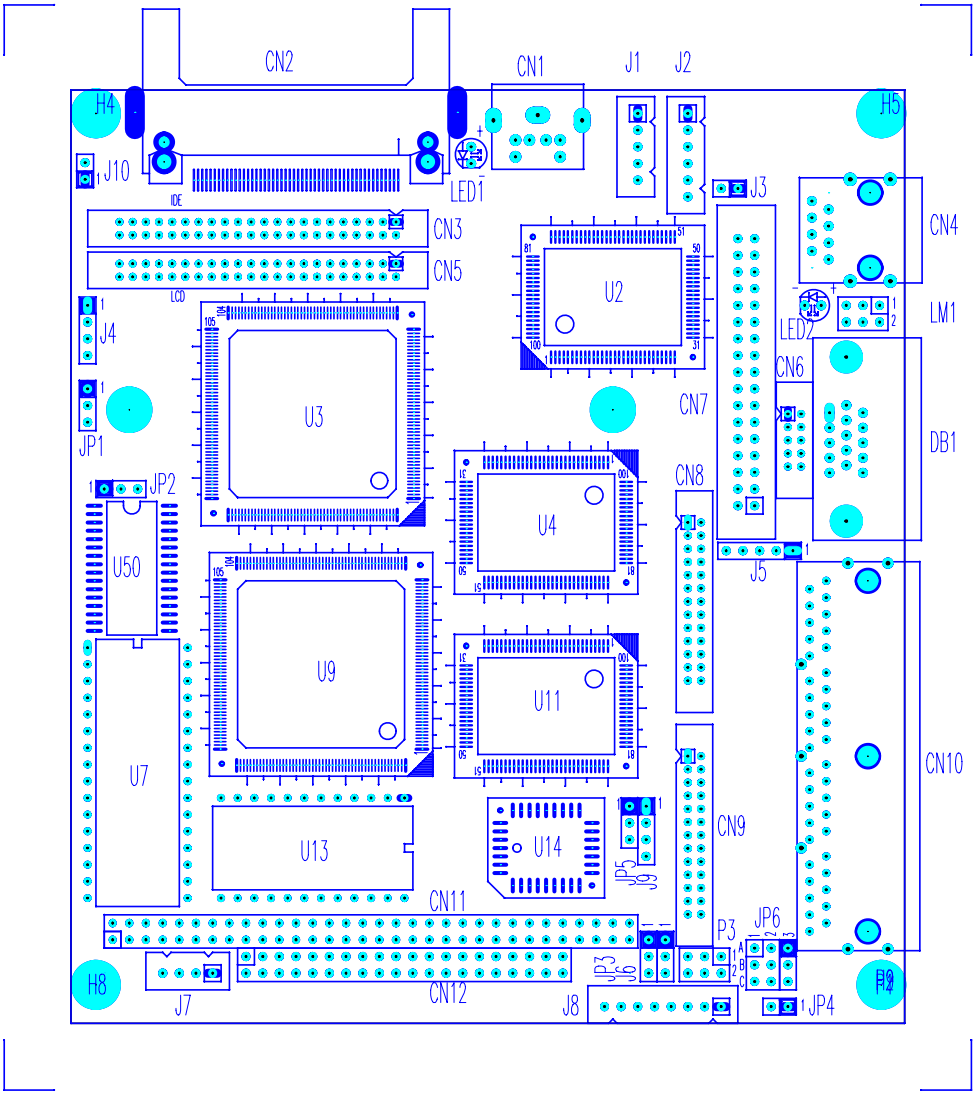


Figure 3-1 External System Location

3.2 SYSTEM SETTINGS

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor [shorting plug] that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the AR-B9622 jumper pins, and the factory-default settings.

CAUTION: Do not touch any electronic component unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage the electronic components.

3.2.1 Keyboard Connector

(1) 6-Pin Mini DIN Keyboard Connector (CN1)

CN1 is a Mini-DIN 6-pin connector. This keyboard connector is the PS/2 type keyboard connector. This connector is also used for a standard IBM-compatible keyboard that uses the keyboard adapter cable.

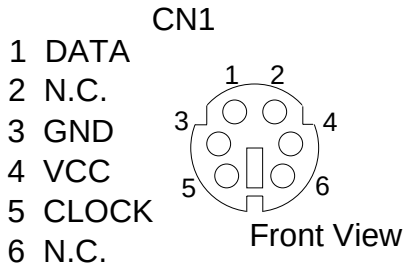


Figure 3-2 CN1: 6-Pin Mini Din Keyboard Connector

(2) AUX. Keyboard Connector (J1)

A PC/AT compatible keyboard can be used by connecting the provided adapter cable between J1 and the keyboard. The pin assignments of J1 connector are as follows:

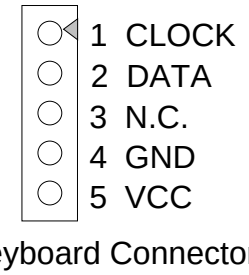
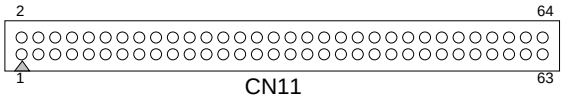


Figure 3-3 J1: AUX. Keyboard Connector

3.2.2 PC/104 Connector

(1) 64 Pin PC/104 Connector Bus A & B (CN11)

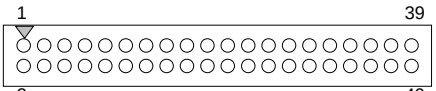


CN11

	1	2	
-IOCHCK ---	A1	B1	--- GND
SD7 ---	A2	B2	--- RSTDRV
SD6 ---	A3	B3	--- +5 VDC
SD5 ---	A4	B4	--- IRQ9
SD4 ---	A5	B5	--- -5 VDC
SD3 ---	A6	B6	--- DRQ2
SD2 ---	A7	B7	--- -12 VDC
SD1 ---	A8	B8	--- -ZWS
SD0 ---	A9	B9	--- +12 VDC
IOCHRDY---	A10	B10	--- GND
AEN ---	A11	B11	--- -SMEMW
SA19 ---	A12	B12	--- -SMEMR
SA18 ---	A13	B13	--- -IOW
SA17 ---	A14	B14	--- -IOR
SA16 ---	A15	B15	--- -DACK3
SA15 ---	A16	B16	--- DRQ3
SA14 ---	A17	B17	--- -DACK1
SA13 ---	A18	B18	--- DRQ1
SA12 ---	A19	B19	--- -REFRESH
SA11 ---	A20	B20	--- BUSCLK
SA10 ---	A21	B21	--- IRQ7
SA9 ---	A22	B22	--- IRQ6
SA8 ---	A23	B23	--- IRQ5
SA7 ---	A24	B24	--- IRQ4
SA6 ---	A25	B25	--- IRQ3
SA5 ---	A26	B26	--- -DACK2
SA4 ---	A27	B27	--- TC
SA3 ---	A28	B28	--- BALE
SA2 ---	A29	B29	--- +5 VDC
SA1 ---	A30	B30	--- OSC
SA0 ---	A31	B31	--- GND
GND ---	A32	B32	--- GND

Figure 3-4 CN11: 64-Pin PC/104 Connector Bus A & B

(2) 40 Pin PC/104 Connector Bus C & D (CN12)



CN12

	1	2	
GND ---	C1	D1	--- GND
-BHE ---	C2	D2	--- -MEM16
LA23 ---	C3	D3	--- -IOCS16
LA22 ---	C4	D4	--- IRQ10
LA21 ---	C5	D5	--- IRQ11
LA20 ---	C6	D6	--- IRQ12
LA19 ---	C7	D7	--- IDEIRQA
LA18 ---	C8	D8	--- IDEIRQB
LA17 ---	C9	D9	--- -DACK0
-MRD16 ---	C10	D10	--- DRQ0
-MWR16 ---	C11	D11	--- -DACK5
SD8 ---	C12	D12	--- DRQ5
SD9 ---	C13	D13	--- -DACK6
SD10 ---	C14	D14	--- DRQ6
SD11 ---	C15	D15	--- -DACK7
SD12 ---	C16	D16	--- DRQ7
SD13 ---	C17	D17	--- +5 VDC
SD14 ---	C18	D18	--- -MASTER
SD15 ---	C19	D19	--- GND
Not Used ---	C20	D20	--- GND

Figure 3-5 CN12: 40-Pin PC/104 Connector Bus C & D

(3) PC/104 ISA Signal Description

Name	Description
BUSCLK [Output]	The BUSCLK signal of the I/O channel is asynchronous to the CPU clock.
RSTDRV [Output]	This signal goes high during power-up, low line-voltage or hardware reset
SA0 - SA19 [Input / Output]	The System Address lines run from bit 0 to 19. They are latched onto the falling edge of "BALE"
LA17 - LA23 [Input/Output]	The Unlatched Address line run from bit 17 to 23
SD0 - SD15 [Input/Output]	System Data bit 0 to 15
BALE [Output]	The Buffered Address Latch Enable is used to latch SA0 – SA19 onto the falling edge. This signal is forced high during DMA cycles
-IOCHCK [Input]	The I/O Channel Check is an active low signal which indicates that a parity error exist on the I/O board
IOCHRDY [Input, Open collector]	This signal lengthens the I/O, or memory read/write cycle, and should be held low with a valid address
IRQ 3-7, 9-12, 14, 15 [Input]	The Interrupt Request signal indicates I/O service request attention. They are prioritized in the following sequence : (Highest) IRQ 9, 10, 11, 12, 13, 15, 3, 4, 5, 6, 7 (Lowest)
-IOR [Input/Output]	The I/O Read signal is an active low signal which instructs the I/O device to drive its data onto the data bus
-IOW [Input/Output]	The I/O write signal is an active low signal which instructs the I/O device to read data from the data bus
-SMEMR [Output]	The System Memory Read is low while any of the low 1mega bytes of memory are being used
-MEMR [Input/Output]	The Memory Read signal is low while any memory location is being read
-SMEMW [Output]	The System Memory Write is low while any of the low 1mega bytes of memory is being written
-MEMW [Input/Output]	The Memory Write signal is low while any memory location is being written
DRQ 0-3, 5-7 [Input]	DMA Request channels 0 to 3 are for 8-bit data transfers. DMA Request channels 5 to 7 are for 16-bit data transfers. DMA request should be held high until the corresponding DMA has been completed. DMA request priority is in the following sequence:(Highest) DRQ 0, 1, 2, 3, 5, 6, 7 (Lowest)
-DACK 0-3, 5-7 [Output]	The DMA Acknowledges 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3 and 5 to 7
AEN [output]	The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the CPU is driving the address bus
-REFRESH [Input/Output]	This signal is used to indicate a memory refresh cycle and can be driven by the microprocessor on the I/O channel
TC [Output]	Terminal Count provides a pulse when the terminal count for any DMA channel is reached
SBHE [Input/Output]	The System Bus High Enable indicates the high byte SD8 - SD15 on the data bus

Name	Description
-MASTER [Input]	The MASTER is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh
-MEMCS16 [Input, Open collector]	The Memory Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data memory operation
-IOCS16 [Input, Open collector]	The I/O Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data I/O operation
OSC [Output]	The Oscillator is a 14.31818 MHz signal
-ZWS [Input, Open collector]	The Zero Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting additional wait cycle

Table 3-1 PC/104 ISA Pin Assignment

3.2.3 Hard Disk (IDE) Connector (CN3)

A 44-pin header type connector (CN3) is provided to interface with up to two embedded hard disk drives (IDE AT bus). This interface, through a 44-pin cable, allows the user to connect up to two drives in a "daisy chain" fashion. To enable or disable the hard disk controller, please use BIOS Setup program to select. The following table illustrates the pin assignments of the hard disk drive's 40-pin connector.

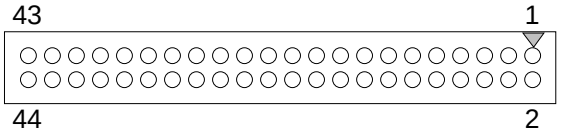


Figure 3-6 CN3: Hard Disk (IDE) Connector

Pin	Signal	Pin	Signal
1	-RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	NOT USED
21	Not Used	22	GROUND
23	-IOW A	24	GROUND
25	-IOR A	26	GROUND
27	-CHRDY A	28	DALE
29	Not Used	30	GROUND
31	-IRQ 14	32	-IO16
33	SA 1	34	NOT USED
35	SA 0	36	SA 2
37	CS 0	38	CS 1
39	HD LED A	40	GROUND
41	VCC	42	VCC
43	GROUND	44	Not Used

Table 3-2 CN3: Hard Disk (IDE) Connector

3.2.4 PS/2 Mouse Connector (J2)

To use the PS/2 mouse, an adapter cable has to be connected to the J2 (6-pin header type) connector. This adapter cable is mounted on a bracket and is included in your AR-B9622 package. The connector for the PS/2 mouse is a Mini-DIN 6-pin connector. The pin assignments for the PS/2 port connector are as follows:

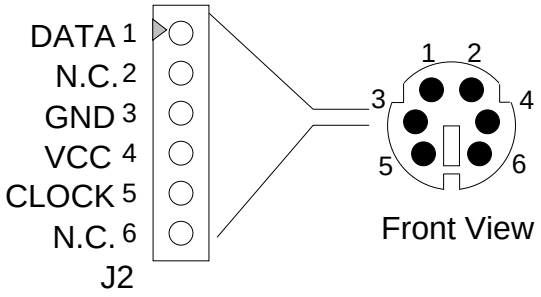


Figure 3-7 J2: PS/2 Mouse Connector

3.2.5 FDD Port Connector (CN7)

The AR-B9622 provides a 34-pin header type connector for supporting up to two floppy disk drives.

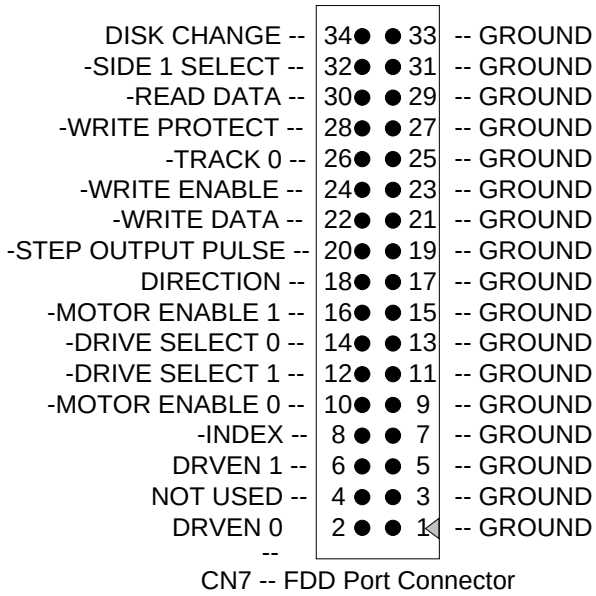


Figure 3-8 CN7: FDD Port Connector

3.2.6 Reset Header (J3)

J3 is used to connect to an external reset switch. Shorting these two pins will reset the system.

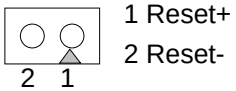


Figure 3-9 J3: Reset Header

3.2.7 Parallel Port Connector (CN8 & CN9)

To use the parallel port, an adapter cable has connected to the CN8 or CN9 (26-pin header type) connector. This adapter cable is mounted on a bracket and is included in your AR-B9622 package. The connector for the parallel port is a 25 pin D-type female connector.

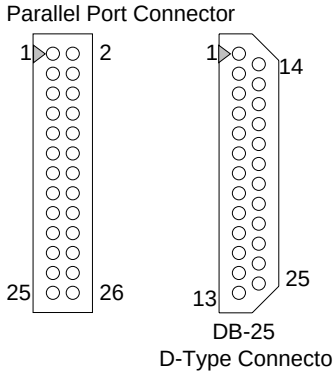


Figure 3-10 CN8 & CN9: Parallel Port Connector

CN8&CN9	DB-25	Signal	CN8&CN9	DB-25	Signal
1	1	-Strobe	2	14	-Auto Form Feed
3	2	Data 0	4	15	-Error
5	3	Data 1	6	16	-Initialize
7	4	Data 2	8	17	-Printer Select In
9	5	Data 3	10	18	Ground
11	6	Data 4	12	19	Ground
13	7	Data 5	14	20	Ground
15	8	Data 6	16	21	Ground
17	9	Data 7	18	22	Ground
19	10	-Acknowledge	20	23	Ground
21	11	Busy	22	24	Ground
23	12	Paper	24	25	Ground
25	13	Printer Select	26	--	No Used

Table 3-3 Parallel Port Pin Assignment

3.2.8 Power Connector (J7 & J8)

J7 is a 4-pin power connector and J8 is one 8-pin power connector. Using the J8, you can connect the power supply to the on board power connector for stand alone applications directly.

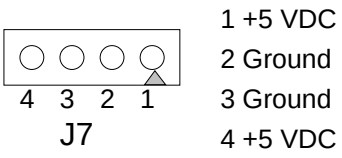


Figure 3-11 J7: 4-Pin Power Connector

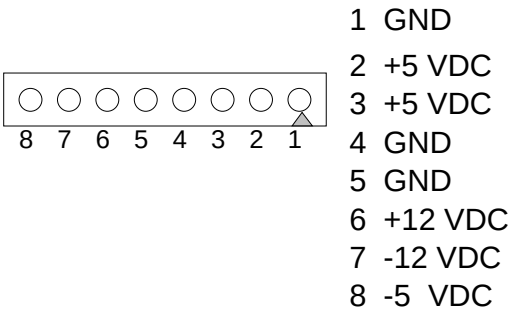


Figure 3-12 J8: 8-Pin Power Connector

3.2.9 Serial Port

(1) Full RS-232 Signal / Power Select for COM-A (P3)

P3 select the full RS-232 signal or power select for CN10--COM A, if user chooses the power supported then the COM A's RTS will be instead of the +12VDC signal; and the CN10--COM A's CTS will be instead of the +5VDC signal.

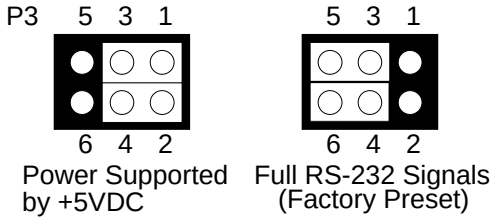


Figure 3-13 P3: Full RS-232 Signal / Power Select for COM-A

(2) RS-232/RS-485 Select for COM-D (JP6)

JP6 selects the on-board RS-232/RS-485 for CN10 – COM D.

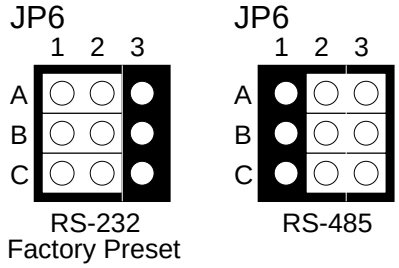


Figure 3-14 JP6: RS-232/RS-485 Select for COM-D

(3) RS-485 Terminator Select (JP4)

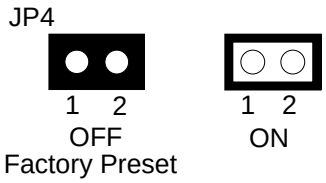


Figure 3-15 JP4: RS-485 Terminator Select

(4) RS-232 and Digital I/O Signal Output Select for COM D (JP3)

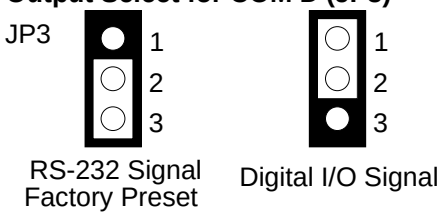


Figure 3-16 JP3: RS-232 and Digital I/O Signal Output Select for COM-D

(5) Digital I/O Signal Output Header for COM D (J6)

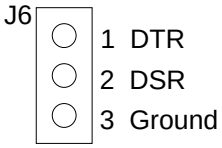


Figure 3-17 J6: Digital I/O Signal Output Header for COM D

(6) RS-232C Connector (CN10)

There are four serial ports with EIA RS-232C interface on the AR-B9622. COM A, COM B and COM C use three on-board serial port Phone-Jack 10-pin female connector (CN10) which is located at the right top side of the card. To configure these four serial ports, use the BIOS Setup program to do well, and COM D can be adjust the jumpers on P1 & P2 for choice RS-485 or RS-232C.

The pin assignments of the CN10 for serial port A, B, C & D are as follows:

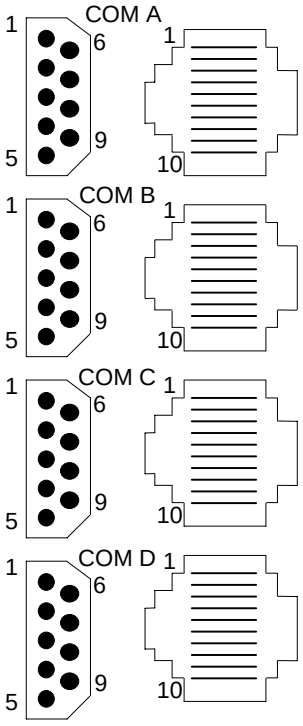


Figure 3-18 CN10: RS-232C Connector

CN10-A	DB-9	Signal	CN10-A	DB-9	Signal
1	1	-DCD	2	8	-CTS / +5V
3	7	-RTS / +5V	4	6	-DSR
5	2	RXD	6	3	TXD
7	4	-DTR	8	5	GND
9	5	GND	10	9	-RI

Table 3-4 Serial Port RS-232 COM A Pin Assignment

CN10-B	CN10-C	DB-9	Signal	CN10-B	CN10-C	DB-9	Signal
1	1	1	-DCD	2	2	8	-CTS
3	3	7	-RTS	4	4	6	-DSR
5	5	2	RXD	6	6	3	TXD
7	7	4	-DTR	8	8	5	GND
9	9	5	GND	10	10	9	-RI

Table 3-5 Serial Port RS-232 COM B & C Pin Assignment

CN10-D	DB-9	Signal	CN10-D	DB-9	Signal
1	1	-DCD	2	8	-CTS
3	7	-RTS / 485N+	4	6	-DSR
5	2	RXD	6	3	TXD
7	4	-DTR / 485N-	8	5	GND
9	5	GND	10	9	-RI

Table 3-6 Serial Port RS-232/RS-485 COM D Pin Assignment

(7) COM-C RI Signal Output Select (JP5)

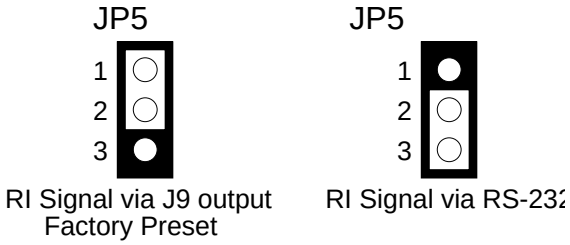


Figure 3-19 JP5: COM-C RI Signal Output Select

(8) TTL Header (J9)

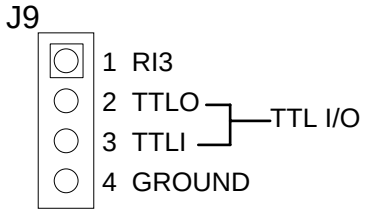


Figure 3-20 J9: TTL Header

3.2.10 Compact Flash Connector (CN2)

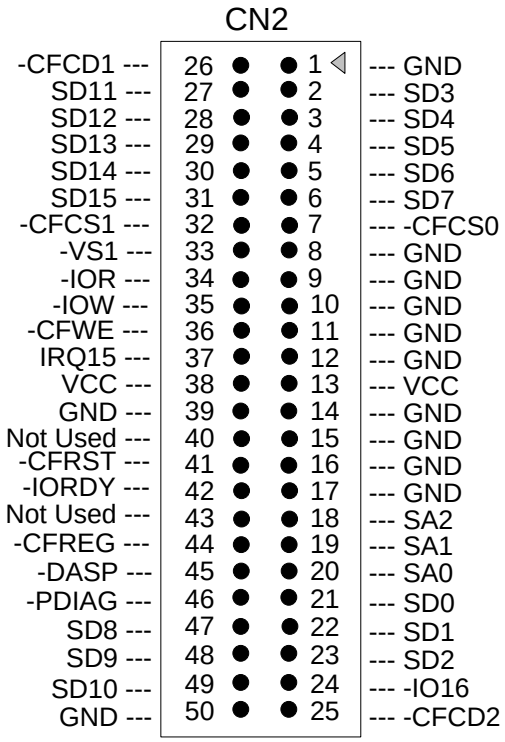


Figure 3-21 CN2: Compact Flash Connector

3.2.11 RJ-45 Connector (CN4)

The CN4 connects RJ-45 header, it's the standard network header. The following table is CN4 pin assignment.

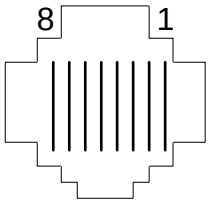


Figure 3-22 CN4: RJ-45 Connector

PIN (CN4)	FUNCTION
1	TPTX+
2	TPTX -
3	TPRX+
4	Not Used
5	Not Used
6	TPRX -
7	Not Used
8	Not Used

Table 3-7 RJ-45 Pin Assignment

3.2.12 CPU Base Clock Select (JP2)

The CPU base clock (Input clock) is twice of its operation clock.

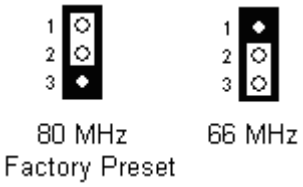


Figure 3-23 JP2: CPU Base Clock Select

3.2.13 D.O.C. Installation (U7)

Step 1: Insert programmed DiskOnChip into sockets U7 setting as DOC.

Step 2: Line up and insert the AR-B9622 card into any free space of your computer.

Step 3: Use the D.O.C. in no HDD equipment, and after installed D.O.C. we can easily boot the system from D.O.C..

4. CRT/LCD FLAT PANEL DISPLAY

This section describes the configuration and installation procedure when using the LCD and CRT displays.

- LCD Flat Panel Displays
- Supported LCD Panels
- CRT & LCD Displays

4.1 LCD FLAT PANEL DISPLAYS

Using the Flash Memory Writer utility to download the new BIOS file into the ROM chip to configure the BIOS default settings for different types of LCD panels. And then, set your system properly and configure the AR-B9622 VGA module for the right type of LCD panel you are using.

The samples of LCD models listed on the table are just some of the LCD panel models available in the market that the Chips & Technologies used by AR-B9622 VGA module can support. If you are using a different LCD panel other than those listed, choose from the panel description column which type of LCD panel you are using.

The following shows the block diagram of using AR-B9622 for LCD display.

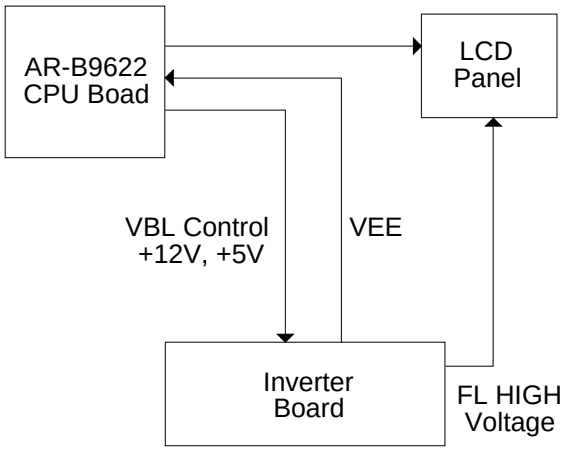


Figure 4-1 LCD Panel Block Diagram

The block diagram shows that AR-B9622 still needs components to be used for LCD panel. The inverter board provides the control for the brightness and the contrast of the LCD panels while the inverter is the one that supplies the high voltage to drive the LCD panel. Each item will be explained further in the section.

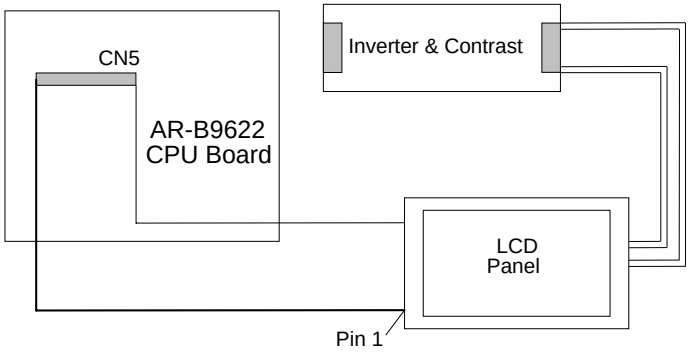


Figure 4-2 LCD Panel Cable Installation Diagram

NOTE: Be careful with the pin orientation when installing the connectors and the cables. A wrong connection can easily destroy your LCD panel. The pin 1 of the cable connectors is indicated with a sticker and the pin1 of the ribbon cable is usually with different color.

http:\\www.acrosser.com

4.2 CRT & LCD DISPLAY

The AR-B9622 supports CRT color monitor, STN, Dual-Scan, TFT, monochrome and color panels. It can be connected to create a compact video solution for the industrial environment. 1MB of V-RAM on-boarded allows a maximum CRT resolution of 800X600 with 256 colors and a LCD resolution of 640X480 with 64K colors. For different VGA display modes, your monitor must possess certain characteristics to display the mode you want.

4.2.1 CRT Connector (CN6 & DB1)

CN6 is a 10-pin connector that attaches to the CRT monitor via a D-sub 15-pin adapter cable. The pin assignments for the CN6 & DB1 connectors are as follows:

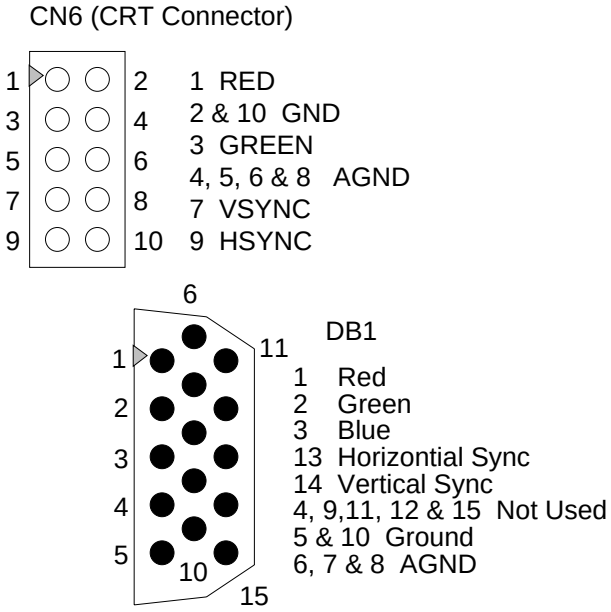


Figure 4-3 DB1 & CN6: CRT Connector

4.2.2 LCD Setting

(1) DE/E Signal from M or LP Select (JP1)

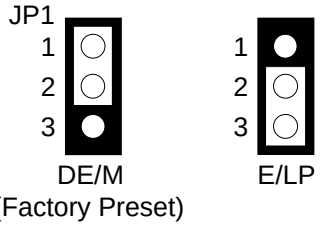


Figure 4-4 JP1: DE/E Signal from M or LP Select

(2) LCD Panel Display Connector (CN5)

Attach a display panel connector to this 44-pin connector with pin assignments shown below:

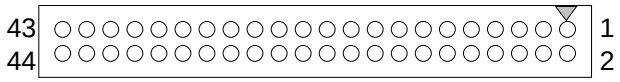


Figure 4-5 CN5: LCD Display Connector

Pin	Signal	Pin	Signal
1	GND	2	SHFCLK
3	GND	4	LP
5	FLM	6	GND
7	P0(B0)	8	P1(B1)
9	P2(B2)	10	P3(B3)
11	P4(B4)	12	P5(B5)
13	GND	14	P6(B6)
15	P7(B7)	16	P8(G0)
17	P9(G1)	18	P10(G2)
19	P11(G3)	20	GND
21	P12(G4)	22	P13(G5)
23	P14(G6)	24	P15(G7)
25	P16(R0)	26	P17(R1)
27	GND	28	P18(R2)
29	P19(R3)	30	P20(R4)
31	P21(R5)	32	P22(R6)
33	P23(R7)	34	GND
35	VCC	36	VCC
37	+12V	38	+12V
39	GND	40	GND
41	DE	42	ENABLK
43	GND	44	Not Used

Table 4-8 LCD Display Assignment

5. INSTALLATION

This chapter describes the procedure of the installation. The following topics are covered:

- Overview
- Utility Diskette
- Watchdog Timer

5.1 OVERVIEW

This chapter provides information for you to set up a working system based on the AR-B9622 CPU board. Carefully read the details of the CPU board's hardware descriptions before installation, especially the jumper settings, switch settings and cable connections.

Follow the steps listed below for proper installation:

Step 1 : Read the CPU board's hardware description in this manual.

Step 2 : Set jumpers.

Step 3 : Make sure that the power supply connected to your passive CPU board is turned off.

Step 4 : Connect all necessary cables. Make sure that the FDC, HDC, serial and parallel cables are connected to pin 1 of the related connector.

Step 5 : Connect the hard disk/floppy disk flat cables from the CPU board to the drives. Connect a power source to each drive.

Step 6 : Plug the keyboard into the keyboard connector.

Step 7 : Turn on the power.

Step 8: Configure your system with the BIOS Setup program then re-boot your system.

Step 9: If the CPU board does not work, turn off the power and read the hardware description carefully again.

Step 10: If the CPU board still does not perform properly, return the board to your dealer for immediate service.

5.2 UTILITY DISKETTE

AR-B9622 provides two VGA driver diskettes, supporting WIN31 & DOS applications. If your operating system is the other operating system, please contact Acrosser that will provide the technical supporting for the VGA resolution.

There are two diskettes: disk 1 is for WIN31 & MS-DOS VGA resolution, disk 2 is for the network utility and manual. Every diskette is attached with the README.* file. Please refer to the file of README for any troubleshooting before installing the driver.

5.2.1 VGA Driver

WIN 3.1 Driver

For the WIN31 operating system, user must in the DOS mode decompress the compress file. And then follow the steps:

Step 1: In the DOS mode, execute the SETUP.EXE file.
`A:\>SETUP`

Step 2: The screen shows the chip type. Press any key to enter the main menu.

Step 3: There are some items for choice to setup. Please choose the <Windows Version 3.1> item notice the function key defined. Press [ENTER] selected the <All Resolutions>, when this line appears [*] symbol, which means this item is selected. Pressing [End] starts to install.

Step 4: The screen will show the dialog box, demanding the user to type the WIN31's path. The default is C:\WINDOWS.

Step 5: As the setup is completed, the system will generate the message as follows.

Installation is done!

Change to your Windows directory and type SETUP to run the Windows Setup program. Choose one of the new drivers marked by an *. Please refer to the User's Guide to complete the installation.

Step 6: Press the [Esc] key to return to the main menu, and re-press the [Esc] key to return to the DOS mode.

Step 7: In the WIN31, you can find the <Chips CPL> icon located in the {CONTROL PANEL} group.

Step 8: Adjust the <Refresh Rate>, <Cursor Animation>, <Font size>, <Resolution>, and <Big Cursor>.

5.2.2 BIOS FLASH Utility

In the <UTILITY> directory, there is the AMIFLASH.COM file.

1. Use the AMIFLASH.COM program to update the BIOS setting.

2. And then refer to the section "BIOS Console", as the steps to modify BIOS.

3. Now the CPU board's BIOS is the newest, user can use this program to modify BIOS function in the future, when the BIOS adds some functions.

5.2.3 Network Utility

1. Use the PKUNZIP.EXE program to decompress the file in the DOS mode.
   For Example

```
C:\>MD NET
C:\>CD NET
C:\NET>COPY A:\PKUNZIP.EXE C:\NET
C:\NET>COPY A:\UM9008.ZIP C:\NET
C:\NET>PKUNZIP -D UM9008.ZIP
```

2. And then enter the operating system as the installation processes. Please refer to the decompressed file. There is the README file in every sub-directory, and has detailed description for installing the drivers.

5.3 WATCHDOG TIMER

This section describes how to use the Watchdog Timer, disabled, enabled, and trigger.

The AR-B9622 is equipped with a programmable time-out period watchdog timer. User can use the program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger it every time before it times out. If your program fails to trigger or disable this timer before it times out because of system hang-up, it will generate a reset signal to reset the system. The time-out period can be programmed to be 30.5 μ seconds to 512 seconds.

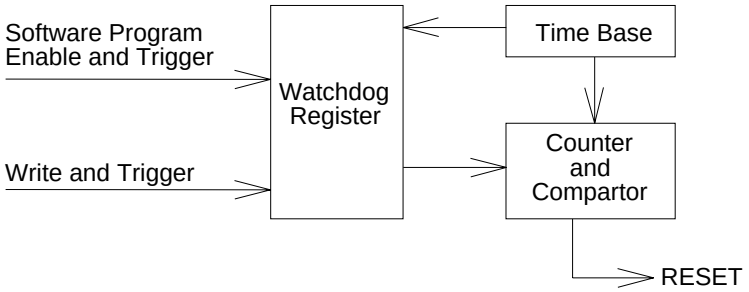


Figure 5-1 Watchdog Block Diagram

5.3.1 Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect crashes or hang-ups. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times-out. After you trigger the watchdog timer, it will be set to zero and start to count again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system or trigger the IRQ15 signal to tell your program that the watchdog is times out.

Watchdog timer -INDEX 39H, 3AH, 3BH

3Bh		3Ah		39h	
D7	0	D7	0	D7	0

Counter [MSB …LSB]

For example

INDEX	3Bh	3Ah	39h	
	00h	00h	01h	30.5 μ sec
	--	--	02h	61 μ sec
	00h	01h	00h	7.8 m sec
	00h	02h	00h	15.6 m sec
	01h	00h	00h	2 sec
	02h	00h	00h	4 sec
	FFh	FFh	FFh	512 sec

If you want to generate IRQ15 signal to warn your program when watchdog times out, the following table listed the relation of timer factors between time-out period. And if you use the IRQ15 signal to warn your program when watchdog timer out, please enter the BIOS Setup the <Peripheral Setup> menu, the <OnBoard PCI IDE> and <IDE Prefetch> these two items must set to ***Primary***.

NOTE: 1. If you program the watchdog to generate IRQ15 signal when it times out, you should initial IRQ15 interrupt vector and enable the second interrupt controller (8259 PIC) in order to enable CPU to process this interrupt. An interrupt service routine is required too.

2. Before you initial the interrupt vector of IRQ15 and enable the PIC, please enable the watchdog timer previously, otherwise the watchdog timer will generate an interrupt at the time watchdog timer is enabled.

5.3.2 Watchdog Enabled/Disabled - INDEX 37H

Bit 7 Reserved. Please do not set this bit.
In old version M6117C data sheet, this bit is counter read mode.

Bit 6 0 disable watchdog timer
1 enable watchdog timer

Bit 5-0 Other function.
Please do not modify these bits.

5.3.3 Select Watchdog Report Signal - INDEX 38H

Bit 7-4 watchdog timer time out report signal select
0000 no output signal
0001 IRQ3 selected
0010 IRQ4 selected
0011 IRQ5 selected
0100 IRQ6 selected
0101 IRQ7 selected
0110 IRQ9 selected
0111 IRQ10 selected
1000 IRQ11 selected
1001 IRQ12 selected
1010 IRQ14 selected
1011 IRQ15 selected
1100 NMI selected
1101 system reset selected
1110 no output signal
1111 no output signal

Bit 3-0 Other function.
Please do not modify these bits.

5.3.4 Timeout Status & Reset Watchdog - INDEX 3CH

Bit 7 0 timer timeout not happened
1 timer timeout happened
Read only.

Bit 5 Write this bit "1" to reset timer
The value on this bit has no meaning.

Bit 6 Other function.
Bit 4-0 Please do not modify these bits.

5.3.5 Programming Watchdog - Basic Operation

If we would like to access M6117C configuration register, we need to unlock register at first and lock it after finishing operation.

(1) Unlock Configuration Register

```
mov   al, 013h
out   22h, al
nop
nop
mov   al, 0c5h
out   23h, al
nop
nop
```

(2) Lock Configuration Register

```
mov     al, 013h
out     22h, al
nop
nop
mov     al, 000h
out     23h, al
nop
nop
```

(3) Read the Value at Configuration Register

For example, read INDEX 3Ch:
Unlock configuration register

```
mov     al, 03ch
out     22h, al
nop
nop
in      al, 23h
nop
nop

push    ax
```

Lock configuration register

```
pop     ax          ; AL - result
```

(4) Write Data to Configuration Register

For example, write 0FFh to INDEX 3Bh:
Unlock configuration register

```
mov     al, 03bh
out     22h, al
nop
nop
mov     al, 0ffh
out     23h, al
nop
nop
```

Lock configuration register

(5) if the function of WATCHDOG is applied,please follow the following instruction to write the command at the first line of the config.sys file.
DEVICE=C:\INIT9008.SYS
In order to avoide LAN error.

6. BIOS CONSOLE

This chapter describes the AR-B9622 BIOS menu displays and explains how to perform common tasks needed to get up and running, and presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Peripheral Setup
- Auto-Detect Hard Disks
- Password Setting
- Load Default Setting
- BIOS Exit

6.1 BIOS SETUP OVERVIEW

BIOS is a program used to initialize and set up the I/O system of the computer, which includes the ISA bus and connected devices such as the video display, diskette drive, and the keyboard.

The BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS Default Values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

After the computer turned on, the BIOS will perform a diagnostics of the system and display the size of the memory that is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

The BIOS Setup main menu includes some options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to assure the option and configure the functions.

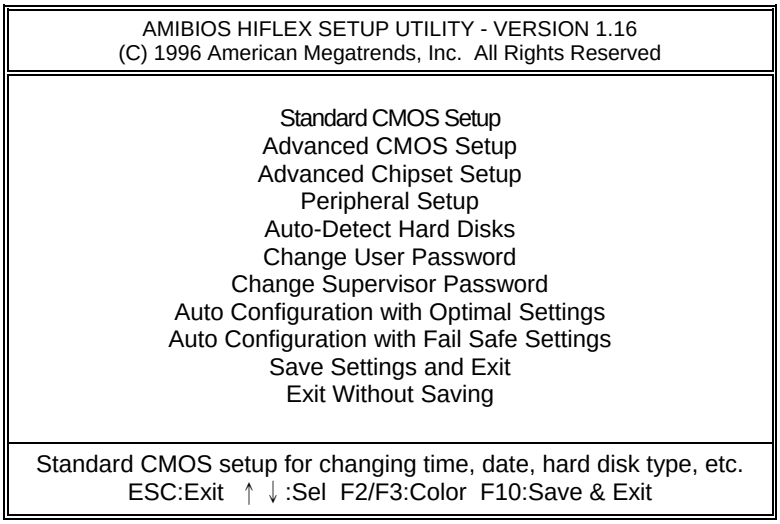


Figure 6-1 BIOS: Setup Main Menu

CAUTION: 1. AR-B9622 BIOS the factory-default setting is used to the <Auto Configuration with Optimal Settings> Acrosser recommends using the BIOS default setting, unless you are very familiar with the setting function, or you can contact the technical support engineer.

2. If the BIOS loss setting, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operation system, this option will reduce the performance of the system. Acrosser recommends choosing the <Auto Configuration with Optimal Setting> in the main menu. The option is best-case values that should optimize system performance.
3. The BIOS settings are described in detail in this section.

6.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

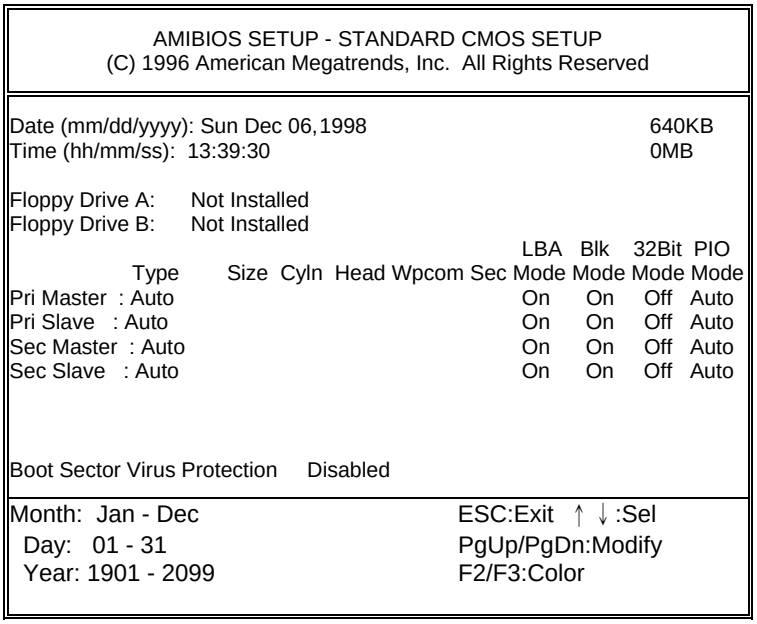


Figure 6-2 BIOS: Standard CMOS Setup

Date & Time Setup

Highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master>, <Pri Slave>, <Sec Master> and <Sec Slave> so the user can install up to two hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during bootup. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

Boot Sector Virus Protection

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is ***<Disabled>***. This setting is recommended because it conflicts with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

6.3 ADVANCED CMOS SETUP

The <Advanced CMOS SETUP> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to
remain in their default settings.

AMIBIOS SETUP – ADVANCED CMOS SETUP
(C) 1998 American Megatrends, Inc. All Rights Reserved

1st Boot Device	IDE-0	Available Options :
2nd Boot Device	Floppy	Disabled
3rd Boot Device	IDE-1	IDE-0
4th Boot Device	Disabled	IDE-1
Boot From Card BIOS	Yes	IDE-2
Try Other Boot Devices	Yes	IDE-3
BootUp Num-Lock	On	Floppy
Floppy Drive Swap	Disabled	ARMD-FDD
Floppy Drive Seek	Disabled	ARMD-HDD
Floppy Access Control	Normal	CDROM
HDD Access Control	Normal	SCSI
PS/2 Mouse Support	Disabled	NETWORK
System Keyboard	Present	
Primary Display	VGA/EGA	
Password Check	Setup	
Wait For 'F1' If Error		
Enabled		
Hit 'DEL' Message Display		
Enabled		
C000, 32k Shadow	Enabled	
C800, 32k Shadow	Disabled	ESC:Exit ↑ ↓:Sel
D000, 32k Shadow	Disabled	PgUp/PgDn:Modify
D800, 32k Shadow	Disabled	F2/F3:Color
E000, 32k Shadow	Disabled	
E800, 32k Shadow	Disabled	

Figure 6-3 BIOS: Advanced CMOS Setup

1st Boot Device
2nd Boot Device
3rd Boot Device
4th Boot Device

These options determine where the system looks first for an operating system. The default setting is to check first the hard disk and then the floppy drive, and last the CDROM.

BootUp Num-Lock

This item is used to activate the Num Lock function upon system boot. If the setting is on, after a boot, the Num Lock light is lit, and user can use the number key.

Floppy Drive Swap

The option reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When the function's setting is <***Enabled***>, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Floppy Drive Seek

If the <Floppy Drive Seek> item is setting ***Enabled***, the BIOS will seek the floppy <A> drive one time upon bootup.

PS/2 Mouse Support

The setting of ***Enabled*** allows the system to detect a PS/2 mouse on bootup. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. ***Disabled*** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

System Keyboard

This function specifies that a keyboard is attached to the computer.

Primary Display

The option is used to set the type of video display card installed in the system.

Password Check

This option enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if the BIOS executed.

Wait for 'F1' If Error

AMIBIOS POST error messages are followed by:

```
Press <F1> to continue
```

If this option is set to ***Disabled***, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Hit 'DEL' Message Display

Set this option to ***Disabled*** to prevent the message as follows:

```
Hit 'DEL' if you want to run setup
```

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Shadow

These options control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

SETTING	DESCRIPTION
Disabled	The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
Enabled	The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.
Cached	The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Table 6-1 Shadow Setting

6.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.

AMIBIOS SETUP - ADVANCED CHIPSET SETUP
(C) 1995 American Megatrends, Inc. All Rights Reserved

AT Bus Clock	14.318 / 2	Available Options :
Slow Refresh	60 us	14.318/2
RAS Precharge time	1.5T	PLCK2/3
RAS Active Time Insert Wait	Disable	PLCK2/4
CAS Precharge Time Insert Wait	Disable	PLCK2/5
Memory Write Insert Wait	Disable	PLCK2/6
Memory Miss Read Insert Wait	Disable	PLCK2/8
ISA I/O High Speed	Enable	PLCK2/10
ISA Memory High Speed	Enable	PLCK2/12
ISA Write cycle end Insert Wait	Disable	
I/O Recovery	Disable	
I/O Recovery Period	0.75 us	
On-Chip I/O Recovery	Disable	
16Bit ISA Insert Wait	Disable	
******* Watch Dog Timer *********		
WatchDog Timer	Disabled	
WDT Timeout Period Select	42 Sec	ESC:Exit ↑ ↓:Sel
WatchDog Timeout Issue Signal	Reset	PgUp/PgDn:Modify
		F2/F3:Color

Figure 6-4 BIOS: Advanced Chipset Setup

AT Bus Clock

This option sets the polling clock speed of ISA Bus (PC/104).

NOTE: 1. PCLK means the CPU inputs clock.
2. Acrosser recommends user setting at the range of 8MHz to 10MHz.

Slow Refresh

This option sets the DRAM refresh cycle time.

RAS Precharge Time

The DRAM RAS precharge time.

Time Insert Wait

The DRAM time insert wait: RAS Active and CAS Precharge function setting.

ISA High Speed

The Speed field shows the speed at which the processor runs internally.

I/O Recovery

If I/O Recovery Feature options is enabled, the BIOS inserts a delay time between two I/O commands. The delay time is defined in I/O Recovery Period option.

6.5 PERIPHERAL SETUP

This section is used to configure peripheral features.

AMIBIOS SETUP - PERIPHERAL SETUP
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Hard disk Delay	Disable	Available Options :
OnBoard IDE	Disable	3 Sec
OnBoard Primary IDE	Primary	5 Sec
OnBoard Secondary IDE	Secondary	10 Sec
OnBoard FDC	Auto	15 Sec
OnBoard Serial Port1	3F8h	
OnBoard Serial Port1 IRQ	4	
OnBoard Serial Port2	2F8h	
OnBoard Serial Port2 IRQ	3	
OnBoard Serial Port3	3E8h	
OnBoard Serial Port3 IRQ	11	
OnBoard Serial Port4	2E8h	
OnBoard Serial Port4 IRQ	9	
OnBoard Parallel Port	3BCh	
Parallel Port Mode	Normal	
EPP Version	N/A	
Parallel Port IRQ	7	
Parallel Port DMA Channel	N/A	
OnBoard Parallel Port2	278h	
Parallel Port Mode	Normal	
EPP Version	N/A	ESC:Exit ↑ ↓:Sel
Parallel Port IRQ	5	PgUp/PgDn:Modify
Parallel Port DMA Channel	N/A	F2/F3:Color

Figure 6-5 BIOS: Peripheral Setup

Hard Disk Delay

If this option is set to ***Disabled*** and the system BIOS executes too fast, the result is the BIOS can't find the hard disk drive.

OnBoard IDE

This option specifies the onboard IDE controller channels that will be used.

OnBoard FDC

This option enables the floppy drive controller on the AR-B9622.

OnBoard Serial Port

This option enables the serial port on the AR-B9622.

OnBoard Parallel Port

This option enables the parallel port on the AR-B9622.

Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes that adhere to the IEEE P1284 specifications.

Parallel Port DMA Channel

This option is only available if the setting for the parallel Port Mode option is ECP.

6.6 AUTO-DETECT HARD DISKS

This option detects the parameters of an IDE hard disk drive, and automatically enters them into the Standard CMOS Setup screen.

6.7 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. User can set either a Supervisor password or a User password.

6.7.1 Setting Password

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after BIOS completes. The next time the system boots, you are prompted for the password function is present and is enabled.

```
Enter new supervisor password:
```

6.7.2 Password Checking

The password check option is enabled in Advanced Setup by choosing either ***Always*** (the password prompt appears every time the system is powered on) or ***Setup*** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. User can enter a password by typing on the keyboard. As user select Supervisor or User. The BIOS prompts for a password, user must set the Supervisor password before user can set the User password. Enter 1-6 character as password. The password does not appear on the screen when typed. Make sure you write it down.

6.8 LOAD DEFAULT SETTING

In this section permit user to select a group of setting for all BIOS Setup options. Not only can you use these items to quickly set system configuration parameters, you can choose a group of settings that have a better chance of working when the system is having configuration related problems.

6.8.1 Auto Configuration with Optimal Setting

User can load the optimal default settings for the BIOS. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

```
Load high performance settings (Y/N) ?
```

6.8.2 Auto Configuration with Fail Safe Setting

User can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.
The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

```
Load failsafe settings (Y/N) ?
```

6.9 BIOS EXIT

This section is used to exit the BIOS main menu in two types situation. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

6.9.1 Save Settings and Exit

This item set in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you to save data to CMOS and Exit the Setup.

```
Save current settings and exit (Y/N) ?
```

6.9.2 Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to Abandon all Data and Exit Setup.

```
Quit without saving (Y/N) ?
```

6.10 BIOS UPDATE

The BIOS program instructions are contained within computer chips called FLASH ROMs that are located on your system board. The chips can be electronically reprogrammed, allowing you to upgrade your BIOS firmware without removing and installing chips.

The AR-B9622 provides FLASH BIOS update function for you to easily upgrade newer BIOS version. Please follow the operating steps for updating new BIOS:

Step 1: Turn on your system and don' t detect the CONFIG.SYS and AUTOEXEC.BAT files. Keep your system in the real mode.

Step 2: Insert the FLASH BIOS diskette into the floppy disk drive.

Step 3: In the MS-DOS mode, you can type the AMIFLASH program.

A:\>AMIFLASH

Step 4: The screen will show the message as follow:

Enter the BIOS File name from which Flash EPROM will be programmed. The File name must and with a <ENTER> or press <ESC> to exit.

Step 5: And then please enter the file name to the box of <Enter File Name>. And the box of <Message> will show the notice as follow. In the bottom of this window always show the gray statement.

Flash EPROM Programming is going to start. System will not be usable until Programming of Flash EPROM is successfully complete. In case of any error, existing Flash EPROM must be replaced by new program Flash EPROM.

Step 6: As the gray statement, press the <Y> key to updating the new BIOS.
And then the <Message> box will show the <Programming Flash EPROM>, and the gray statement shows <Please Wait>.

Step 7: The BIOS update is successful, the message will show <Flash Update Completed - Pass>.

NOTE: 1. After turn on the computer and the system didn't detect the boot procedure, please press the [F5] key immediately. The system will pass the CONFIG.SYS and AUTOEXEC.BAT files.

2. The BIOS Flash disk is not the standard accessory. Now the onboard BIOS is the newest BIOS, if user needs adding some functions in the future please contact technical supporting engineers, they will provide the newest BIOS for updating.

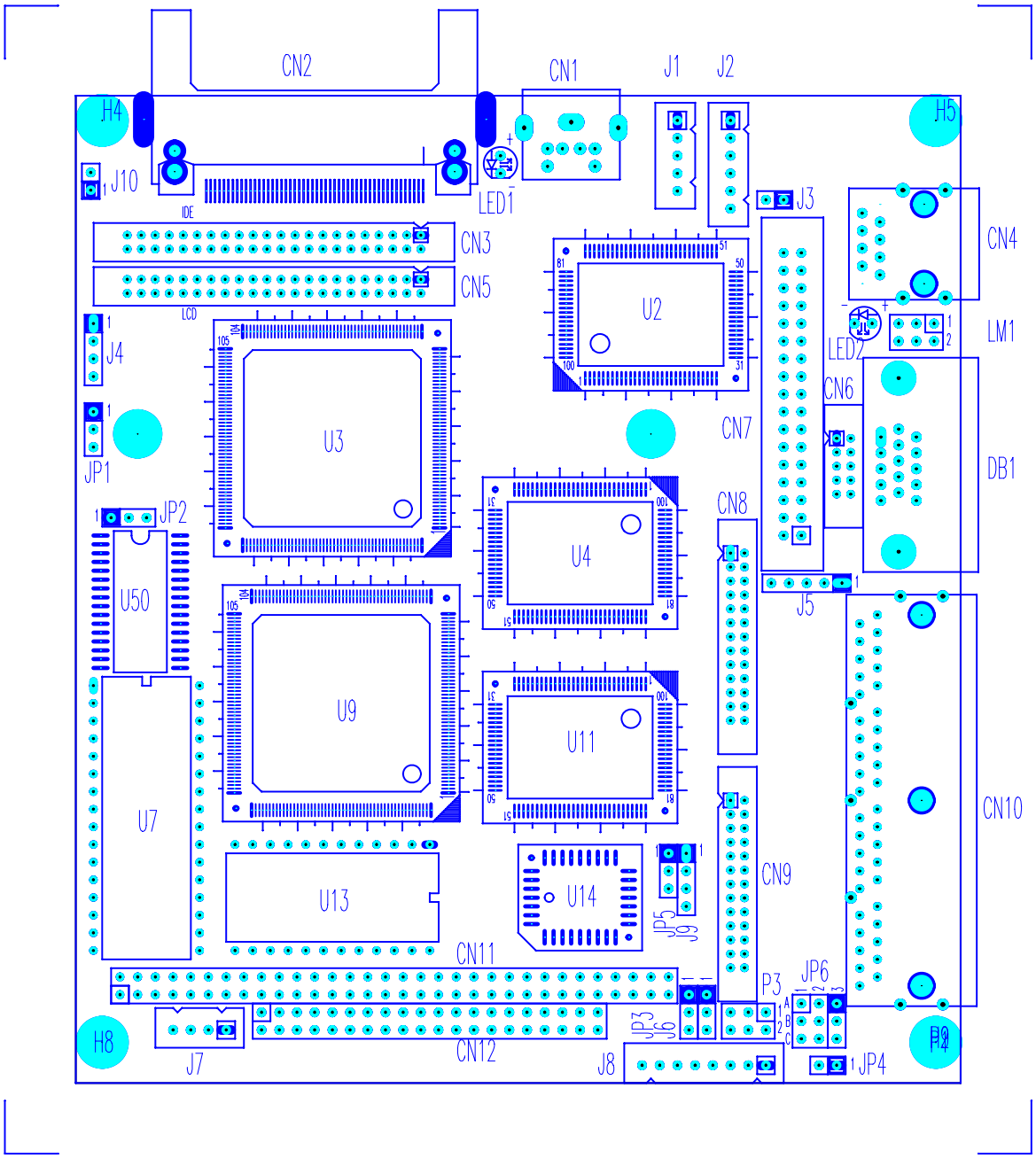
3. The file of AMIFLASH.EXE had to use the attached diskette' s file, if not user had to use the Version 6.31.

7. SPECIFICATIONS

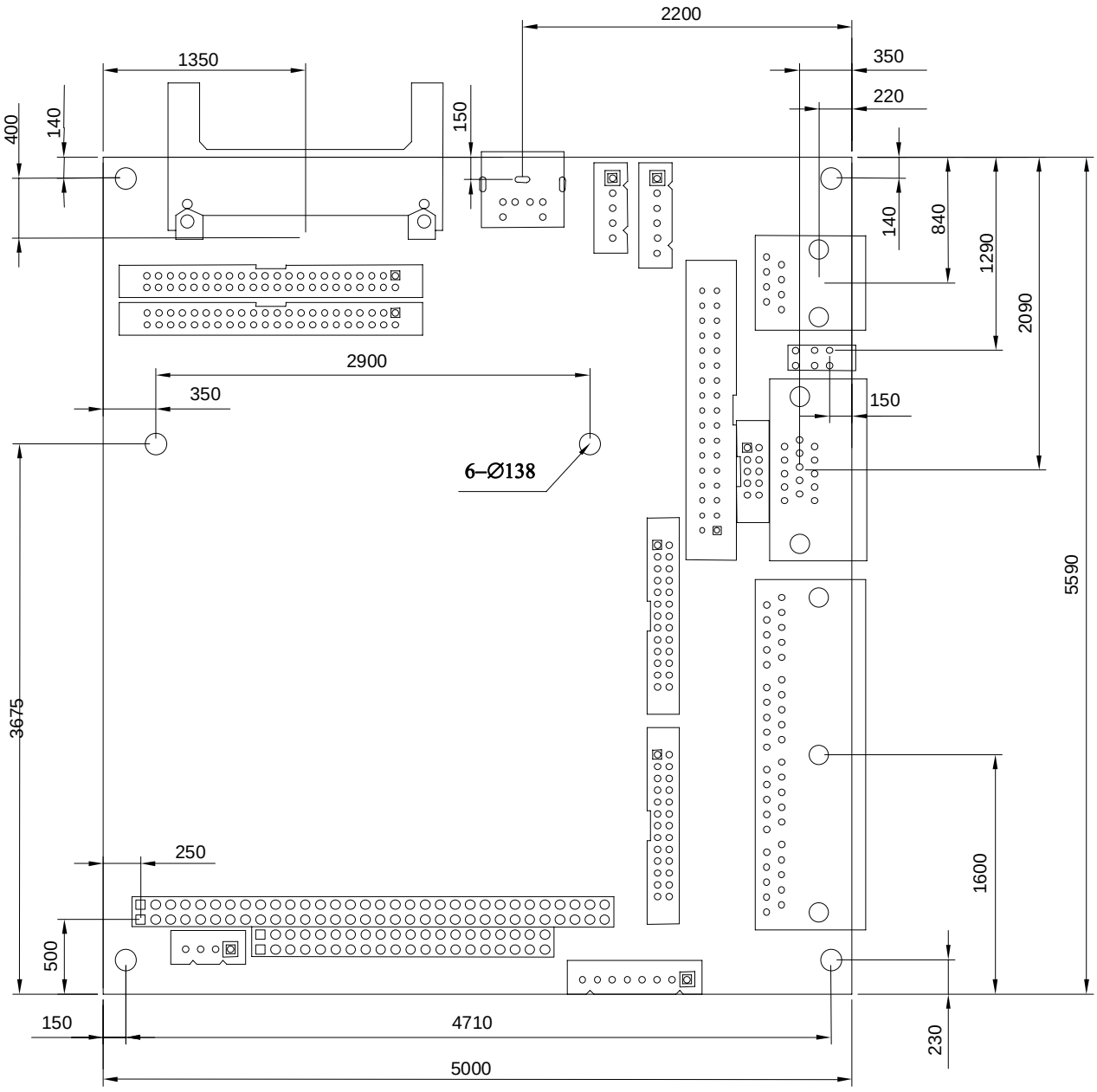
CPU & Chipset:	ALI M6117, 33/40 MHz under 5V power supply
Bus Interface:	PC/104 bus
DRAM:	4MB on-board and 4 MB with socket for expansion
CRT/LCD Display:	1 MB VRAM
HDC:	Supports two IDE type hard disk drives
FDC:	Supports two 5.25" or 3.5" floppy disk drives
Serial Port:	4 full RS-232C port with phone-jack connector
Parallel Port:	2 bi-directional centronics type parallel port
Keyboard:	PC/AT compatible keyboard with 6-pin mini-din connector
Real Time Clock:	BQ3287MT or compatible chips
BIOS:	Legal AMI Flashed system BIOS
Watchdog:	Programmable watchdog timer
Solid State Disk:	1 socket for 2MB to 72MB DiskOnChip 1 connector for 2MB to 32MB ATA Compact Flash
Ethernet:	NE2000 compatible, RJ-45 edge connector
LED Indicator:	Power LED, LAN LED, and HDD LED
Power Connector:	One 4-pin and one 8-pin (2.5mm) power connector
Power Req.:	+5V, 1.5A maximum
PC Board:	6 layers
Dimensions:	145 mmX142mm (5.71"X5.59")

8. PLACEMENT & DIMENSIONS

8.1 PLACEMENT



8.2 DIMENSIONS



Unit: mil (1 inch = 25.4 mm = 1000 mil)

9. PROGRAMMING RS-485 & INDEX

9.1 PROGRAMMING RS-485

The majority communicative operation of the RS-485 is in the same of the RS-232. When the RS-485 proceeds the transmission which needs control the TXC signal, and the installing steps are as follows:

Step 1: Enable TXC

Step 2: Send out data

Step 3: Waiting for data empty

Step 4: Disable TXC

NOTE: Please refer to the section of the "Serial Port" in the chapter "System Control" for the detail description of the COM port's register.

(1) Initialize COM port

Step 1: Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are in the same.)

Step 2: Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets "0".

NOTE: Control the AR-B9622 CPU card's DTR signal to the RS-485' s TXC communication.

(2) Send out one character (Transmit)

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

(3) Send out one block data (Transmit – the data more than two characters)

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

(4) Receive data

The RS-485's operation of receiving data is in the same of the RS-232's.

(5) Basic Language Example

a.) Initial 86C450 UART

```
10      OPEN "COM1:9600,m,8,1"AS #1 LEN=1
20      REM Reset DTR
30      OUT &H3FC, (INP(%H3FC) AND &HFA)
40      RETURN
```

b.) Send out one character to COM1

```
10      REM Enable transmitter by setting DTR ON
20      OUT &H3FC, (INP(&H3FC) OR &H01)
30      REM Send out one character
40      PRINT #1, OUTCHR$
50      REM Check transmitter holding register and shift register
60      IF ((INP(&H3FD) AND &H60) >0) THEN 60
70      REM Disable transmitter by resetting DTR
80      OUT &H3FC, (INP(&H3FC) AND &HEF)
90      RETURN
```

c.) Receive one character from COM1

```
10      REM Check COM1: receiver buffer
20      IF LOF(1)<256 THEN 70
30      REM Receiver buffer is empty
40      INPSTR$"
50      RETURN
60      REM Read one character from COM1: buffer
70      INPSTR$=INPUT$(1,#1)
80      RETURN
```

9.2 INDEX