AR-B9616

486DX/DX2/DX4

CPU Board

User’ s Guide

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0. PREFACE

0.1 COPYRIGHT NOTICE AND DISCLAIMER

ACKNOWLEDGEMENTS

0.2 WELCOME TO THE AR-B9616 CPU BOARD

This guide introduces the Acrosser AR-B9616 CPU board.
Use information provided in this manual describes this card's functions and features. It also helps you start, set up and operate your AR-B9616. General system information can also be found in this publication.

0.3 BEFORE YOU USE THIS GUIDE

Please refer to the Chapter 3, "Setting System," in this guide, if you have not already installed this AR-B9616. Check the packing list before you install and make sure the accessories are completely included.
AR-B9616 CD provides the newest information regarding the CPU card. Please refer to the README.DOC file of the enclosed utility diskette. It contains the modification and hardware & software information, and adding the description or modification of product function after manual printed.

0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires any services, contact the distributor or sales representative from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original shipping container for this purpose.
You can help assure efficient servicing for your product by following these guidelines:

1. Include your name, address, daytime telephone, facsimile number and E-mail.
2. A description of the system configuration and/or software at the time of malfunction.
3. A brief description of the problem occurred.

0.5 TECHNICAL SUPPORT AND USER COMMENTS

Users comments are always welcome as they assist us in improving the quality of our products and the readability of our publications. They create a very important part of the input used for product enhancement and revision.
We may use and distribute any of the information you provide in any way appropriate without incurring any obligation. You may, of course, continue to use the information you provide.
If you have any suggestions for improving particular sections or if you find any errors on it, please send your comments to Acrosser Technology Co., Ltd. or your local sales representative and indicate the manual title and book number.
Internet electronic mail to: Sales@acrosser.com
acrosser@tp.globalnet.com.tw

0.6 ORGANIZATION

This manual covers the following topics (see the Table of Contents for a detailed listing):

- Chapter 1, “Overview”, provides an overview of the system features and packing list.
- Chapter 2, “System Controller” describes the major structure.
- Chapter 3, “Setting System,” describes how to adjust the jumper, and the connectors setting.
- Chapter 4, “Ethernet Controller,” describes the features of the network and the method of connection.
- Chapter 5, “Installation,” describes the procedure of the installation.
- Chapter 6, “BIOS Console,” providing the BIOS options setting.
- Appendix A, Dimensions & Placement
- Appendix B, Specifications & Index

0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.

Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always best to safeguard against accidents that may result in expensive repairs. The following measures should be sufficient to protect your equipment from static discharge:

- Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
- When unpacking and handling the board or other system components, place all materials on an anti-static surface.
- Be careful not to touch the components on the board, especially the “golden finger” connectors on the bottom of the board.

1. OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

1.1 INTRODUCTION

The AR-B9616 is a industrial grade CPU card that has been designed to withstand continuous operation in harsh environments. The total on-board memory for the AR-B9616 can be configured from 1MB to 32MB by using all 72-pin type DRAM devices.

The 8 layers PCB CPU card is equipped with an IDE HDD interface, a floppy disk drive adapter, 1 parallel port, 2 serial ports, and a watchdog timer. The dimension is as compact as 100mmX160mm. Its highly condensed features make it an ideal cost/performance solution for high-end commercial and industrial applications where CPU speed and mean time between failures is critical.
A watchdog timer, which has a software programmable time-out interval, is also provided on this CPU card. It ensures that the systems will not hang-up if a program cannot execute normally.

The AR-B9616 is implemented with M1489 and M1487 chipset incorporate a memory controller, parity generation and checking, two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, an address buffer and a data buffer.

A super I/O chip (SMC37C669) is embedded in the AR-B9616 card. It combines functions of a floppy disk drive adapter, a hard disk drive (IDE) adapter, two serial (with 16C550 UART) adapters and 1 parallel adapter. Setting the BIOS setup program can do the I/O port configurations.

As an UART, the chip supports serial to parallel conversion on data characters received from a peripheral device or a MODEM, and parallel to serial conversion on data character received from the CPU. The UART includes a programmable baud rate generator; complete MODEM control capability and a processor interrupt system. As a parallel port, the SMC37C669 provides the user with a fully bi-directional parallel centronics-type printer interface.

1.2 PACKING LIST

Some accessories are included with the system. Before you begin installing your AR-B9616 CPU board, please make sure that the following items have been included inside the AR-B9616 package.

- This user's guide
- 1 AR-B9616 all-in-one single CPU board
- 1 Hard disk drive interface cable
- 1 Floppy disk drive interface cable
- 1 Parallel port interface cable
- 1 Keyboard adapter
- 1 RS-232C interface cable
- Software utility diskettes

Accessory	Description
Software utility diskette	VGA resolution drivers
Keyboard adapter	PS/2 to IBM standard type adapt cable
Parallel port interface cable	26-pin parallel port cable
Hard disk drive interface cable	44-pin HDD interface cable
Floppy disk drive interface cable	34-pin FDD interface cable

Table 1-1 Accessories

1.3 FEATURES

The system provides a number of special features that enhance its reliability, ensure its availability, and improve its expansion capabilities, as well as its hardware structure.

- Half size all-in-one Pentium grade signal board computer
- Supports up to 133MHz CPUs
- Up to 32MB DRAM system
- Supports 1MB VRAM (PCI bus, 1024X768/256 colors)
- On-board CRT and LCD panel display
- Supports IDE hard disk drives
- Supports floppy disk drives
- Supports 1 bi-directional parallel port
- Supports 2 serial ports
- PC/AT compatible keyboard
- Programmable watchdog timer
- Flash BIOS
- Built-in status LEDs indicator
- Signal 5V power requirement
- Multi-layer PCB for noise reduction
- Dimensions: 100mmX160mm

2 SYSTEM CONTROLLER

This chapter describes the major structure of the AR-B9616 CPU board. The topics are covered as follow:

- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Real-Time Clock and Non-volatile RAM
- Serial Port
- Parallel Port

2.1 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented in the AR-B9616 board. Each controller is four channels DMA device, which will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high-speed information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

Following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Table 2-1 DMA Channel Controller

2.2 KEYBOARD CONTROLLER

The 8042 processor is programmed to support the keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

Data can be written to the keyboard by writing data to the output buffer of the keyboard controller.

Each byte of data is sent to the keyboard controller in series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to keyboard controller until acknowledgment is received for the previous byte sent. The "output buffer full" interrupt may be used for both send and receive routines.

2.3 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the AR-B9616 board. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute.

Following is the system information of interrupt levels:

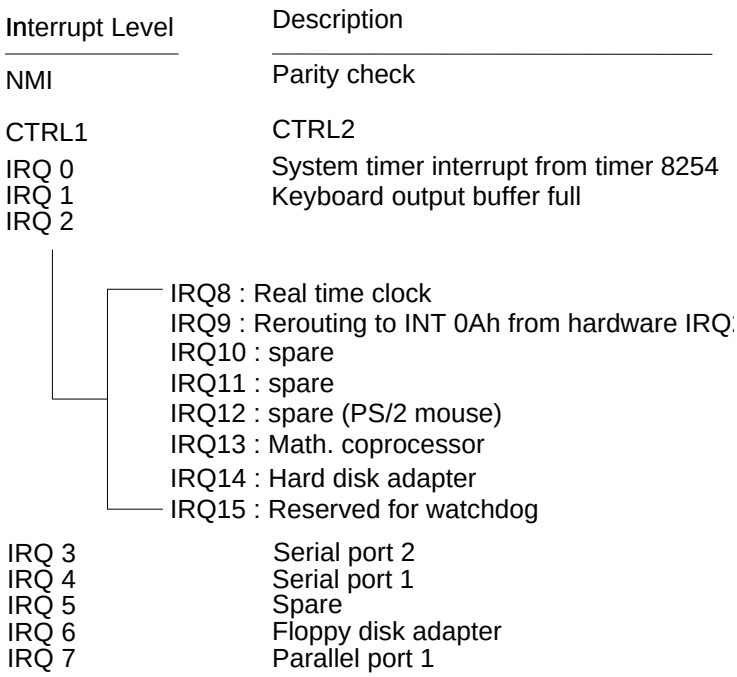

Figure 2-1 Interrupt Controller

2.3.1 Timer

The AR-B9616 provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone. Application programs can load different counts into this timer to generate various sound frequencies.

2.3.2 I/O Port Address Map

Hex Range	Device
000-01F	DMA controller 1
020-021	Interrupt controller 1
022-023	ALI M1489/M1487 Chipset Address
040-04F	Timer 1
050-05F	Timer 2
060-06F	8042 keyboard/controller
070-071	Real-time clock (RTC), non-maskable interrupt (NMI)
076-077	Watchdog
080-09F	DMA page registers
0A0-0A1	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0	Clear Math Co-processor
0F1	Reset Math Co-processor
0F8-0FF	Math Co-processor
170-178	Fixed disk 1
1F0-1F8	Fixed disk 0
201	Game port
208-20A	EMS register 0
214-215	Watchdog
218-21A	EMS register 1
278-27F	Parallel printer port 3 (LPT 2)
2E8-2EF	Serial port 4 (COM 4)
2F8-2FF	Serial port 2 (COM 2)
300-31F	Prototype card/Streaming Type Adapter
378-37F	Parallel printer port 2 (LPT 1)
380-38F	SDLC, bisynchronous
3A0-3AF	Bisynchronous
3B0-3BF	Monochrome display and printer port 1 (LPT 3)
3C0-3CF	EGA/VGA adapter
3D0-3DF	Color/Graphics monitor adapter
3E8-3EF	Serial port 3 (COM 3)
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1 (COM 1)

Table 2-2 I/O Port Address Map

2.4 REAL-TIME CLOCK AND NON-VOLATILE RAM

The AR-B9616 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long period of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed as follows:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

Table 2-3 Real-Time Clock & Non-Volatile RAM

2.5 SERIAL PORT

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are not only used to convert parallel data to a serial format on the transmit side but also used to convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are not only included the use of 16x clock to drive the receiver logic but also included in the ACE as a complete MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The following table is summary of each ACE accessible register

DLAB	Port Address	Register
0	base + 0	Receiver buffer (read)
		Transmitter Holding Register (write)
0	base + 1	Interrupt enable
X	base + 2	Interrupt identification (read only)
X	base + 3	Line control
X	base + 4	MODEM control
X	base + 5	Line status
X	base + 6	MODEM status
X	base + 7	Scratched register
1	base + 0	Divisor latch (least significant byte)
1	base + 1	Divisor latch (most significant byte)

Table 2-4 ACE Accessible Register

(1) Receiver Buffer Register (RBR)

Bit 0-7: Received data byte (Read Only)

(2) Transmitter Holding Register (THR)

Bit 0-7: Transmitter holding data byte (Write Only)

(3) Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)
Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)
Bit 2: Enable Receiver Line Status Interrupt (ELSI)
Bit 3: Enable MODEM Status Interrupt (EDSSI)
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(4) Interrupt Identification Register (IIR)

Bit 0: “0” if Interrupt Pending
Bit 1: Interrupt ID Bit 0
Bit 2: Interrupt ID Bit 1
Bit 3: Must be 0
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(5) Line Control Register (LCR)

Bit 0: Word Length Select Bit 0 (WLS0)
Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)
Bit 3: Parity Enable (PEN)
Bit 4: Even Parity Select (EPS)
Bit 5: Stick Parity
Bit 6: Set Break
Bit 7: Divisor Latch Access Bit (DLAB)

(6) MODEM Control Register (MCR)

Bit 0: Data Terminal Ready (DTR)
Bit 1: Request to Send (RTS)
Bit 2: Out 1 (OUT 1)
Bit 3: Out 2 (OUT 2)
Bit 4: Loop
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(7) Line Status Register (LSR)

Bit 0: Data Ready (DR)
Bit 1: Overrun Error (OR)
Bit 2: Parity Error (PE)
Bit 3: Framing Error (FE)
Bit 4: Break Interrupt (BI)
Bit 5: Transmitter Holding Register Empty (THRE)
Bit 6: Transmitter Shift Register Empty (TSRE)
Bit 7: Must be 0

(8) MODEM Status Register (MSR)

Bit 0: Delta Clear to Send (DCTS)
Bit 1: Delta Data Set Ready (DDSR)
Bit 2: Training Edge Ring Indicator (TERI)
Bit 3: Delta Receive Line Signal Detect (DSLSD)
Bit 4: Clear to Send (CTS)
Bit 5: Data Set Ready (DSR)
Bit 6: Ring Indicator (RI)
Bit 7: Received Line Signal Detect (RSLD)

(9) Divisor Latch (LS, MS)

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Table 2-5 Serial Port Desired Baud Rate Range

2.6 PARALLEL PORT

(1) Register Address

Port Address	Read/Write	Register
base + 0	Write	Output data
base + 0	Read	Input data
base + 1	Read	Printer status buffer
base + 2	Write	Printer control latch

Table 2-6 Register Address

(2) Printer Interface Logic

The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

(3) Data Swapper

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address.

(4) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described as follows:

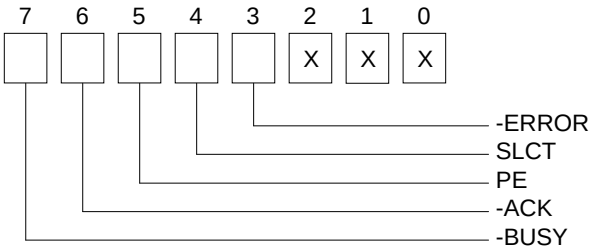

Figure 2-2 Printer Status Buffer

NOTE: X presents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer's ACK signal. A0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

Bit 5: A1 means the printer has detected the end of the paper.

Bit 4: A1 means the printer is selected.

Bit 3: A0 means the printer has encountered an error condition.

(5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

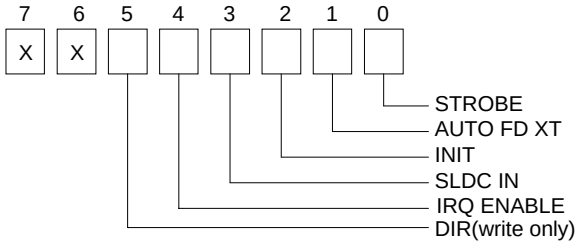

Figure 2-3 Bit Definition

NOTE: X presents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is writing only.

Bit 4: A1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A1 in this bit position selects the printer.

Bit 2: A0 starts the printer (50 microsecond pulse, minimum).

Bit 1: A1 causes the printer to line-feed after a line is printed.

Bit 0: A0.5 microsecond minimum high active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

3. SETTING SYSTEM

This chapter describes pin assignments for system's external connectors and the jumper settings.

- Overview
- System Setting

3.1 OVERVIEW

The AR-B9616 is an industrial grade CPU card that has been designed to withstand continuous operation in harsh environment. This section provides hardware's jumpers setting, the connector locations, and the pin assignment.

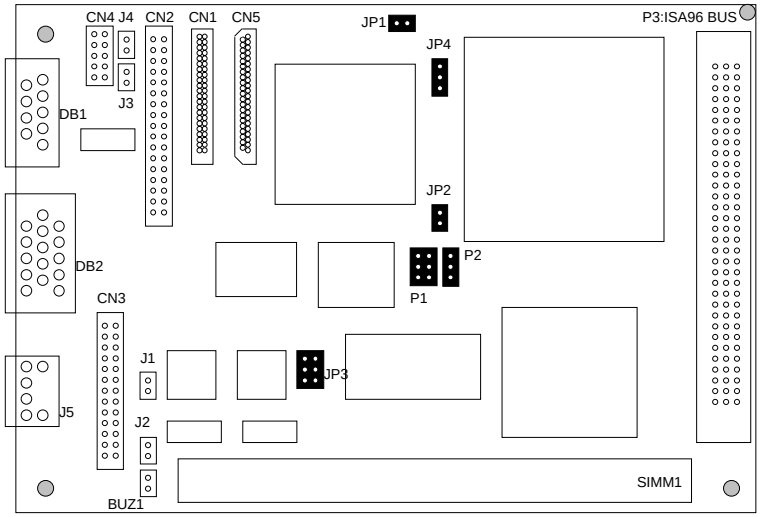

Figure 3-1 Connectors & Jumpers Location

3.2 SYSTEM SETTING

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor [shorting plug] that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the AR-B9616 jumper pins, and the factory-default setting. Note that the square pin of each jumper block is pin 1.

CAUTION: Do not touch any electronic component unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. A static discharge from your fingers can permanently damage electronic components.

3.2.1 ISA96 BUS

(1) ISA96 BUS (P3)

PIN NO.	ROW A	ROW B	ROW C
1	GND	/MASTER	/IOCHCK
2	RSTDRV	SD15	SD7
3	+5V	SD14	SD6
4	IRQ9	SD13	SD5
5	/MEMR	SD12	SD4
6	DRQ2	SD11	SD3
7	Not Used	SD10	SD2
8	/ZWS	SD9	SD1
9	Not Used	SD8	SD0
10	GND	/SBHE	/ I ORDY
11	/SMEMW	LA23	AEN
12	/SMEMR	LA22	SA19
13	/IOW	LA21	SA18
14	/IOR	LA20	SA17
15	/DACK3	LA19	SA16
16	DRQ3	LA18	SA15
17	/DACK1	LA17	SA14
18	DRQ1	/DACK7	SA13
19	/REFRESH	DRQ7	SA12
20	BUSCLK	/DACK6	SA11
21	IRQ7	DRQ6	SA10
22	IRQ6	/DACK5	SA9
23	IRQ5	DRQ5	SA8
24	IRQ4	/DACK0	SA7
25	IRQ3	DRQ0	SA6
26	/DACK2	/MEM16	SA5
27	TC	/IO16	SA4
28	BALE	IRQ15	SA3
29	+5V	IRQ14	SA2
30	OSC	IRQ12	SA1
31	/MEMW	IRQ11	SA0
32	GND	IRQ10	GND

Table 3-1 ISA96 Bus Connector Pin out

(2) I/O Channel Signal Description

Name	Description
BUSCLK [Output]	The BUSCLK signal of the I/O channel is asynchronous to the CPU clock.
RSTDRV [Output]	This signal goes high during power-up, low line-voltage or hardware reset
SA0 - SA19 [Input / Output]	The System Address lines run from bit 0 to 19. They are latched onto the falling edge of "BALE"
LA17 - LA23 [Input/Output]	The Unlatched Address line run from bit 17 to 23
SD0 - SD15 [Input/Output]	System Data bit 0 to 15
BALE [Output]	The Buffered Address Latch Enable is used to latch SA0 - SA19 onto the falling edge. This signal is forced high during DMA cycles
-IOCHCK [Input]	The I/O Channel Check is an active low signal which indicates that a parity error exist on the I/O board
IOCHRDY [Input, Open collector]	This signal lengthens the I/O, or memory read/write cycle, and should be held low with a valid address
IRQ 3-7, 9-12, 14, 15 [Input]	The Interrupt Request signal indicates I/O service request attention. They are prioritized in the following sequence : (Highest) IRQ 9, 10, 11, 12, 13, 15, 3, 4, 5, 6, 7 (Lowest)
-IOR [Input/Output]	The I/O Read signal is an active low signal which instructs the I/O device to drive its data onto the data bus
-IOW [Input/Output]	The I/O write signal is an active low signal which instructs the I/O device to read data from the data bus
-SMEMR [Output]	The System Memory Read is low while any of the low 1 mega bytes of memory are being used
-MEMR [Input/Output]	The Memory Read signal is low while any memory location is being read
-SMEMW [Output]	The System Memory Write is low while any of the low 1 mega bytes of memory is being written
-MEMW [Input/Output]	The Memory Write signal is low while any memory location is being written
DRQ 0-3, 5-7 [Input]	DMA Request channels 0 to 3 are for 8-bit data transfers. DMA Request channels 5 to 7 are for 16-bit data transfers. DMA request should be held high until the corresponding DMA has been completed. DMA request priority is in the following sequence:(Highest) DRQ 0, 1, 2, 3, 5, 6, 7 (Lowest)
-DACK 0-3, 5-7 [Output]	The DMA Acknowledges 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3 and 5 to 7
AEN [output]	The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the CPU is driving the address bus
-REFRESH [Input/Output]	This signal is used to indicate a memory refresh cycle and can be driven by the microprocessor on the I/O channel
TC [Output]	Terminal Count provides a pulse when the terminal count for any DMA channel is reached
SBHE [Input/Output]	The System Bus High Enable indicates the high byte SD8 - SD15 on the data bus
-MASTER [Input]	The MASTER is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh
-MEM16 [Input, Open collector]	The Memory Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data memory operation
-IO16 [Input, Open collector]	The I/O Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data I/O operation
OSC [Output]	The Oscillator is a 14.31818 MHz signal
-ZWS [Input, Open collector]	The Zero Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting additional wait cycle

Table 3-2 I/O Channel Signal Description

3.2.2 Hard Disk (IDE) Connector (CN1)

A 44-pin header type connector (CN1) is provided to interface with up to two embedded hard disk drives (IDE AT bus). This interface, through a 44-pin cable, allows the user to connect up to two drives in a "daisy chain" fashion. To enable or disable the hard disk controller, please use BIOS Setup program to select. The following table illustrates the pin assignments of the hard disk drive's 44-pin connector.

Pin	Signal	Pin	Signal
1	-Reset	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Not Used
21	Not Used	22	Ground
23	-IOW	24	Ground
25	-IOR	26	Ground
27	-IORDY	28	Not Used
29	Not Used	30	Ground
31	IRQ 14	32	-IO16
33	SA 1	34	Not Used
35	SA 0	36	SA 2
37	-CS 0	38	-CS 1
39	HD LED	40	Ground
41	VCC	42	VCC
43	Ground	44	Ground

Table 3-3 HDD Pin Assignment

3.2.3 FDD Port Connector (CN2)

The AR-B9616 provides a 34-pin header type connector for supporting up to two floppy disk drives. To enable or disable the floppy disk controller, please use BIOS Setup program to select.

Pin	Signal	Pin	Signal
1-33(odd)	GROUND	18	-DIRECTION
2	DRVEN 0	20	-STEP OUTPUT PULSE
4	NOT USED	22	-WRITE DATA
6	DRVEN 1	24	-WRITE ENABLE
8	-INDEX	26	-TRACK 0
10	-MOTOR ENABLE A	28	-WRITE PROTECT
12	-DRIVE SELECT B	30	-READ DATA
14	-DRIVE SELECT A	32	-SIDE 1 SELECT
16	-MOTOR ENABLE B	34	-DISK CHANGE

Table 3-4 FDD Pin Assignment

3.2.4 Parallel Port Connector (CN3)

To use the parallel port, an adapter cable has connected to the CN3 (26 pin header type) connector. This adapter cable is mounted on a bracket and is included in your AR-B9616 package. The connector for the parallel port is a 25 pin D-type female connector.

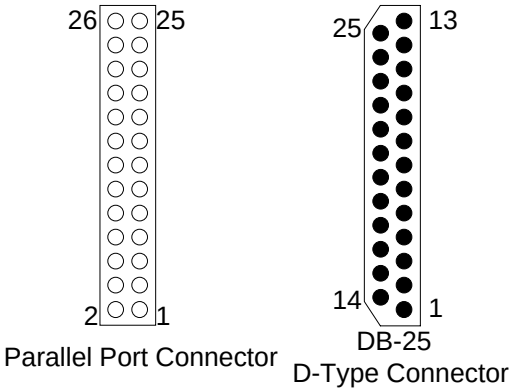

Figure 3-2 CN3: Parallel Port Connector

CN3	DB-25	Signal	CN3	DB-25	Signal
1	1	-Strobe	2	14	-Auto Form Feed
3	2	Data 0	4	15	-Error
5	3	Data 1	6	16	-Initialize
7	4	Data 2	8	17	-Printer Select In
9	5	Data 3	10	18	Ground
11	6	Data 4	12	19	Ground
13	7	Data 5	14	20	Ground
15	8	Data 6	16	21	Ground
17	9	Data 7	18	22	Ground
19	10	-Acknowledge	20	23	Ground
21	11	Busy	22	24	Ground
23	12	Paper	24	25	Ground
25	13	Printer Select	26	--	No Connect

Table 3-5 Parallel Port Pin Assignment

3.2.5 LED Header (J2, J3 & J4)

(1) Watchdog LED Header (J2)

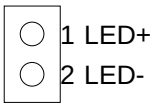

Figure 3-3 J2: Watchdog LED Header

(2) Power LED Header (J3)

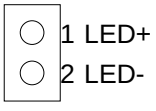

Figure 3-4 J3: Power LED Header

(3) HDD LED Header (J4)

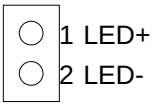

Figure 3-5 J4: HDD LED Header

3.2.6 Serial Port -- RS-232 Connector (CN4 & DB1)

There are two serial ports with EIA RS-232C interface on the AR-B9616. COM A uses one on-board D-type 9 pin male connector (DB1) and COM B uses one 10 pin header (CN4) which are located at the left side of the card.

The pin assignments of the DB1 and CN4 for serial port A & B are as follows:

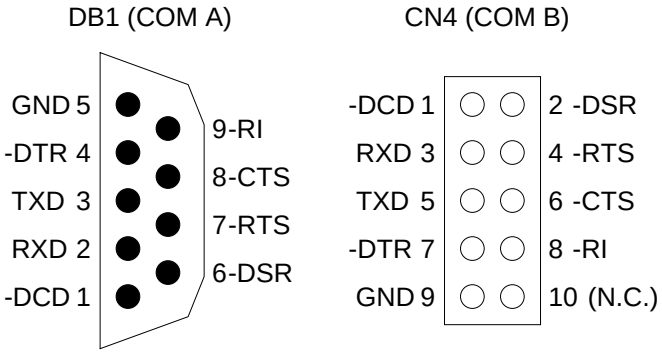

Figure 3-6 DB1 & CN4: RS-232

3.2.7 Keyboard Connector (J5)

J5 is a Mini-DIN 6-pin connector. This keyboard connector is PS/2 type keyboard connector. This connector is also for a standard IBM-compatible keyboard with the keyboard adapter cable.

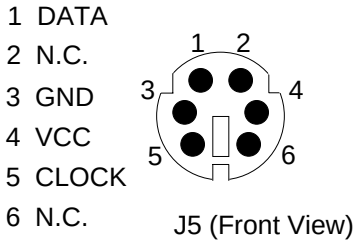

Figure 3-7 J5: Keyboard Connector

3.2.8 External Speaker Header (BUZ1)

Besides the on-board buzzer, you can use an external speaker by connecting BUZ1 header directly.

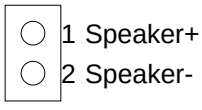

Figure 3-8 BUZ1: Speaker Header

3.2.9 Reset Header (J1)

J1 is used to connect to an external reset switch. Shorting these two pins will reset the system.

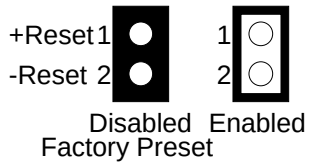

Figure 3-9 J1: Reset Header

3.2.10 CPU Setting

The AR-B9616 accepts many types of microprocessors, such as Intel/AMD/CYRIX/ST 486 DX/DX2/DX4 & 5X86. All of these CPUs include an integer processing unit, floating-point processing unit, memory-management unit, and cache. They can give two to ten-fold performance improvement in speed over the 386 processor. It depends on the clock speeds used and specific application. Like the 386 processor, the 486 processor includes both segment-based and page-based memory protection schemes. On-chip instruction pipelining reduces instruction-processing time. By performing fast, on-chip memory management and caching, the 486 processor relaxes requirements for memory response for a given level of system performance.

(1) CPU Voltage Select (P1 & P2)

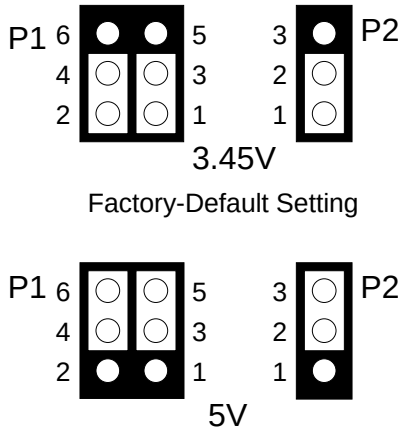

Figure 3-10 P1 & P2: CPU Voltage

(2) Write-Back/Write-Through Cache Select (JP1)

if the processor samples WB/WT high at reset, the processor is configured in write-back mode and all subsequent cache line fills sample WB/WT on the same clock edge in which it finds either RDY or the first BRDY of a burst transfer to determine if the cache line is designated as write-back mode or write-through.

Figure 3-11 JP1: Write-Back/Write-Through Cache

(3) CPU Clock Multiplier Select (JP2)

The CPU clock multipliers need to be set by JP2.

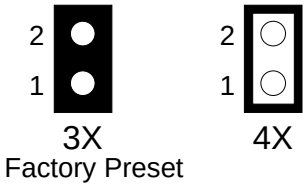

Figure 3-12 JP2: CPU Clock Multiplier

(4) CPU Base Clock Select (JP3)

This board provides different types of CPUs, the clock generator need to be set by JP3.
The CPU input clock is twice of operation clock.

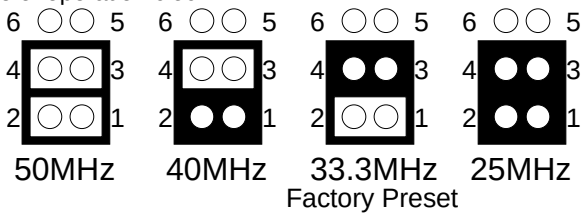

Figure 3-13 JP3: CPU Base Clock

Please refer to CPU Type in the following table for adjusting the jumper.

CPU Clock	CPU Type
25 HMz	DX-25, DX2-50, DX4-75
33 HMz	DX-33, DX2-66, DX4-100, 5X86-133
40 HMz	DX-40, DX2-80, DX4-120
50 HMz	DX-50

Table 3-6 CPU Base Clock

4. CRT/LCD DISKPLAY

This chapter describes the procedure of the installation. The following topics are covered:

- Connecting the CRT Monitor
- LCD Flat Panel Display
- Inverter Board Description
- CRT & LCD Port

4.1 CONNECTING THE CRT MONITOR

To connect a CRT monitor, an adapter cable has to be connected to the DB2 connector.

4.2 LCD FLAT PANEL DISPLAY

This section describes the configuration and installation procedure using LCD display. Skip this section if you are using CRT monitor only.

Using the Flash memory Writer utility to download the new BIOS file into the ROM chip to configure the BIOS default setting for different types of LCD panel. And then set your system properly and configure the AR-B9616 VGA module for the right type of LCD panel you are using.

The sample LCD models listed on the table are just some of the LCD panel models available in the market that the Chips & Technologies used by AR-B9616 VGA module can support. If you are using a different LCD panel other than those listed, choose from the panel description column which type of LCD panel you are using.

The following shows the block diagram of using AR-B9616 for LCD display.

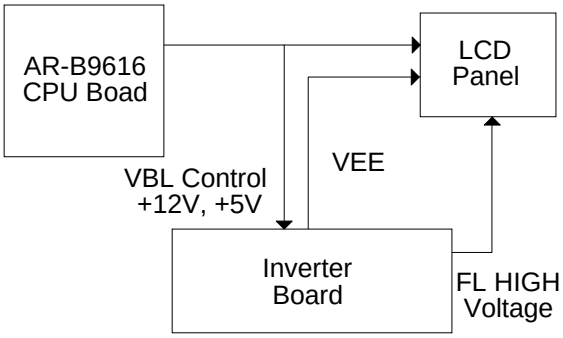

Figure 4-1 LCD Panel Block Diagram

The block diagram shows that AR-B9616 still needs components to be used for LCD panel.

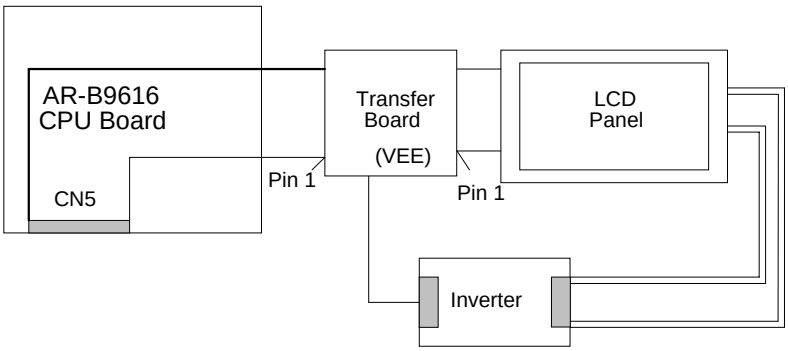

Figure 4-2 LCD Panel Cable Installation Diagram

NOTE: Be careful with the pin orientation when installing connectors and the cables. A wrong connection can easily destroy your LCD panel. The pin 1 of the cable connectors is indicated with a sticker and the pin1 of the ribbon cable is usually with different color.

4.3 CRT & LCD PORT

The AR-B9616 supports CRT color monitor, STN, Dual-Scan, TFT, monochrome and color panels. It can be connected to create a compact video solution for the industrial environment. 1MB of RAM on-boarded allows a maximum CRT resolution of 1024X768 and a LCD resolution of 640X480 with 64K colors. For different VGA display modes, your monitor must possess certain characteristics to display the mode you want

.

4.3.1 CRT Connector (DB2)

DB2 is used to connect with a VGA monitor when you are using the on-board VGA controller as display adapter. Pin assignments for the DB2 connector is as follows:

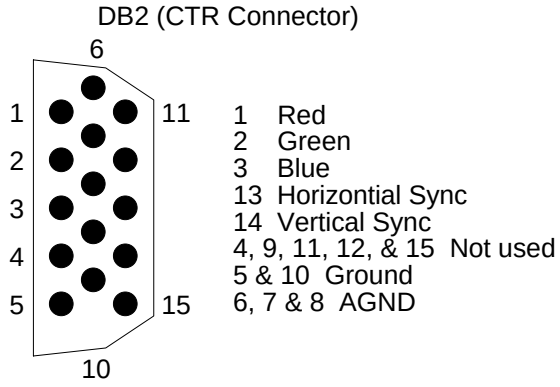

Figure 4-3 DB2: CRT Connector

4.3.2 LCD Connector

(1) DE/E Signal from M or LP Select (JP4)

AR-B9616 doesn't support VGA function, does not provide this jumper setting either.

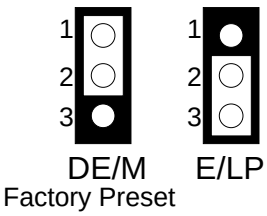

Figure 4-4 JP4: DE/E Signal from M or LP

(2) LCD Panel Display Connector (CN5)

Attach a display panel connector to this 41-pin connector with pin assignments as shown below:

Pin	Signal	Pin	Signal
1	GND	21	SHFCLK
2	FLM	22	LP
3	P0	23	GND
4	P2	24	P1
5	P4	25	P3
6	GND	26	P5
7	P7	27	P6
8	P9	28	P8
9	P11	29	P10
10	P12	30	GND
11	P14	31	P13
12	P16	32	P15
13	GND	33	P17
14	P19	34	P18
15	P21	35	P20
16	P23	36	P22
17	VCC	37	GND
18	GND	38	VCC
19	DE	39	GND
20	GND	40	DENABLK
		41	ENAVEE

Table 4-1 LCD Display Assignment

4.4 SUPPORTED LCD PANEL

At present, this VGA card can provide the total solution with inverter board for the following list of standard LCD panel. Consult your Acrosser representative for new developments, when using other models of standard LCD panels in the market.

NO.	Manufacture	Model No.	Description
1	HOSIDEN	HLM6667	MONO DSTN640X480
2	HITACHI	LMG5160XUFC	MONO DSTN640X480
3	CASIO	MD650TS00-01	MONO DSTN640X480
4	OPTREX	DMF_50260NFU-FW-8	MONO DSTN640X480
5	SANYO	LCM-5331-22NTK	DSTN640X480
6	SHARP	LM64C35P	DSTN640X480
7	HITACHI	TX26D60/TX24D55	TFT640X480-Sync
8	TOSHIBA	LTM09C015A	TFT640X480-Sync
9	SHARP	LQ10D321	TFT640X480-Sync
10	TOSHIBA	LTM09c015A	TFT640X480-LP
11	NEC	NL8060AC26-05	TFT800X600_sync
12	NEC	NL8060AC26-04	TFT800X600_sync
13	NEC	NL8060BC31-02	TFT800X600_sync
14	PLANAR	EL640.480-A	EL640X480
15	PANASONIC	S817	PLASMA640X480

Table 4-2 LCD Panel Type List

CAUTION: If you want to connect the LCD panel, must update the AR-B9616's BIOS, then you can setup the correct BIOS. Please contract with the Acrosser, Acrosser will provide the utility for this function.

5. INSTALLATION

This chapter describes the procedure of the installation. The following topics are covered:

- Overview
- Utility Diskette
- Watchdog Timer

5.1 OVERVIEW

This chapter provides information for you to set up a working system based on the AR-B9616 CPU card. Please read the details of the CPU card's hardware descriptions before installation carefully, especially jumper settings and cable connections.

Follow steps listed below for proper installation:

Step 1 : Read the CPU card's hardware description in this manual.

Step 2 : Install any DRAM SIMM onto the CPU card.

Step 3 : Set jumpers.

Step 4 : Make sure that the power supply connected to your passive back plane is turned off.

Step 5 : Plug the CPU card into a free AT-bus slot or PICMG slot on the back plane and secure it in place with a screw to the system chassis.

Step 6 : Connect all necessary cables. Make sure that the FDC, HDC, serial and parallel cables are connected to pin 1 of the related connector.

Step 7 : Connect the hard disk/floppy disk flat cables from the CPU card to the drives. Connect a power source to each drive.

Step 8 : Plug the keyboard into the keyboard connector.

Step 9 : Turn on the power.

Step 10: Configure your system with the BIOS Setup program then re-boot your system.

Step 11: If the CPU card does not work, turn off the power and read the hardware description carefully again.

Step 12: If the CPU card still does not perform properly, return the card to your dealer for immediate service.

5.2 UTILITY DISKETTE

AR-B9616 provides VGA driver, supports WIN31, WIN95, and WINNT 4.0. It attaches the README.DOC file, please refer to the file for any troubleshooting before install the driver.

5.2.1 WIN 3.1 Driver

For the WIN31 operation system, please according to the following steps for installation:

Step 1: In the <File Manager> choose the <INSTALL.EXE> file to execute for installation, and then the installation is completed. The disk drive and file path is chosen:
`A:\WIN31>INSTALL.EXE`

Step 2: User can enter the WIN31, you can find the <Chips CPL> icon located in the {CONTROL PANEL} group.

Step 3: Adjust the <Refresh Rate>, <Cursor Animation>, <Font size>, <Resolution>, and <Big Cursor>.

5.2.2 WIN 95 Driver

For the WIN95 operation system, please according to the following steps for installation:

Step 1: Enter the WIN95 operation system, please in the <Display> of <Control Panel> choose the <Change the display type> of the <Setting>, change the display connector from disk (select the <From disk install> item), and type the factory source files' path.
`A:\WIN95`

Step 2: And then you can find the <HMC86C508> item, select it and click the <OK> button.

Step 3: Finally, user can find the <DISPLAY> icon adds the <Chips> item. You can select this item, and adjust the <Screen Resolution>, <Refresh Rate>, <Font Size>…and other functions. Please refer to the messages during installation.

5.2.3 WINNT 4.0 Driver

For the WINNT4.0 operation system, please according to the following steps for installation:

Step 1: Enter the WINNT4.0 operation system. Please choose the <SETTING> item of the <DISPLAY> icon in the {CONTROL PANEL}. Please select the <From Disk Install> item, and type the factory source files' path.
`A:\NT40`

Step 2: And then you can find the <HMC86C508> item, select it and click the <OK> button.

Step 3: Finally, user can find the <DISPLAY> icon adds the <Chips> item. You can select this item, and adjust the <Screen Resolution>, <Refresh Rate>, <Font Size>…and other function. Please refer to the messages during installation.

5.2.4 BIOS & Panel Switch Utility

The disk enclosed the AMIFLASH.COM, AMIFLASH.COM's main function supports BIOS update. The AR-B9616 provides FLASH BIOS update function for you to easily upgrade newer BIOS version. Please refer to the disk's README.DOC file that contains detail update steps.

There is SW508.EXE file in the UTILITY directory for Panel Switching utility. The following steps are for installation.

Step 1: The Panel Switching Utility is used for switching different display type.

Step 2: Please type >SW508, and then Screen will show the message as follow:

1. CRT Only
2. Panel Only
3. CRT/Panel Simultaneous

Step 3: And then you can choose which one you want to.

5.3 WATCHDOG TIMER

This section describes how to use the Watchdog Timer, disabled, enabled, and trigger.

The AR-B9616 is equipped with a programmable time-out period watchdog timer. Your program can enable this watchdog timer. Once you have enabled the watchdog timer, the program should trigger it every time before it times out. If your program fails to trigger or disable this timer before it times out because of system hang-up, it will generate a reset signal to reset the system. The time-out period can be programmed to be 3 to 42 seconds.

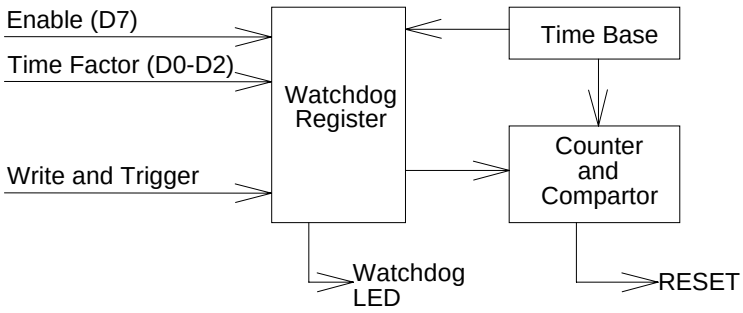

Figure 5-1 Watchdog Block Diagram

5.3.1 Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect crashes or hang-ups. Whenever the watchdog timer is enabled, the LED (LED1) will blink to indicate that the timer is counting. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times-out. After you trigger the watchdog timer, it will be set to zero and start to count again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system to tell your program that the watchdog is times out.

The factor of the watchdog timer time-out constant is approximately 6 seconds. The period for the watchdog timer time-out period is between 1 to 8 timer factors.

If you want to reset your system when watchdog times out, the following table listed the relation of timer factors between time-out periods.

Time Factor	Time-Out Period (Seconds)
80H	3
81H	6
82H	12
83H	18
84H	24
85H	30
86H	36
87H	42

Table 5-1 Time-Out Setting

5.3.2 Watchdog Timer Enabled

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog register whose address is 76H or 214H. The following is a BASICA program, which demonstrates how to enable the watchdog timer and set the time-out period at 24 seconds.

```
1000        REM Points to command register
1010              WD_REG% = 76H
1020        REM Timer factor = 84H (or 0C4H)
1030              TIMER_FACTOR% = %H84
1040        REM Output factor to watchdog register
1050              OUT WD_REG%, TIMER_FACTOR%
      .,etc.
```

5.3.3 Watchdog Timer Trigger

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in next trigger. Below is a BASICA program, which demonstrates how to trigger the watchdog timer:

```
2000        REM Points to command register
2010              WD_REG% = 76H
2020        REM Timer factor = 84H (or 0C4H)
2030              TIMER_FACTOR% = &H84
2040        REM Output factor to watchdog register
2050              OUT WD_REG%, TIMER_FACTOR%
      .,etc.
```

5.3.4 Watchdog Timer Disabled

To disable the watchdog timer, simply write a 00H to the watchdog register.

```
3000        REM Points to command register
3010              WD_REG% = BASE_PORT% + 4
3020        REM Timer factor = 0
3030              TIMER_FACTOR% = 0
3040        REM Output factor to watchdog register
3050              OUT WD_REG%, TIMER_FACTOR%
      ., etc.
```

6. BIOS CONSOLE

This chapter describes the BIOS menu displays and explains how to perform common tasks needed to get up and running. And presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Peripheral Setup
- Auto-Detect Hard Disk
- Password Setting
- Load Default Setting
- BIOS Exit

6.1 BIOS SETUP OVERVIEW

BIOS is a program used to initialize and set up the I/O system of the computer, which includes the ISA bus and connected devices such as the video display, diskette drive, and the keyboard.

These BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operation system.

The BIOS Default Values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer. After the computer is turned on, the BIOS will perform a diagnostics of the system and display the size of the memory that is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

The BIOS Setup main menu exists 11 options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to assure the option and configure the functions.

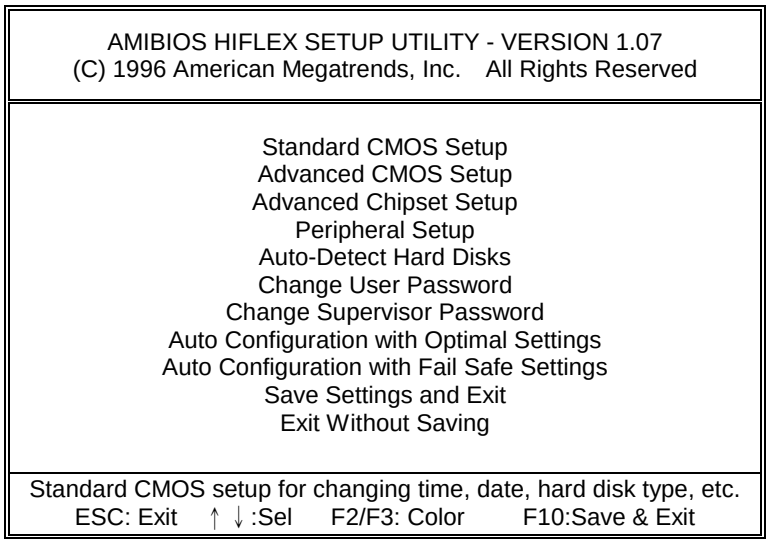

Figure 6-1 BIOS: Setup Main Menu

CAUTION: 1. AR-B9616 BIOS the factory-default setting is used to the <Auto Configuration with Optimal Settings> Acrosser recommends using the BIOS default setting, unless you are very familiar with the setting function, or you can touch the technical support engineer.

2. If the BIOS loss setting, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operation system, this option will reduce the performance of the system. Acrosser recommends choosing the <Auto Configuration with Optimal Setting> in the main menu. The option is best-case values that should optimize system performance.
3. The BIOS settings are described in detail in this section

6.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

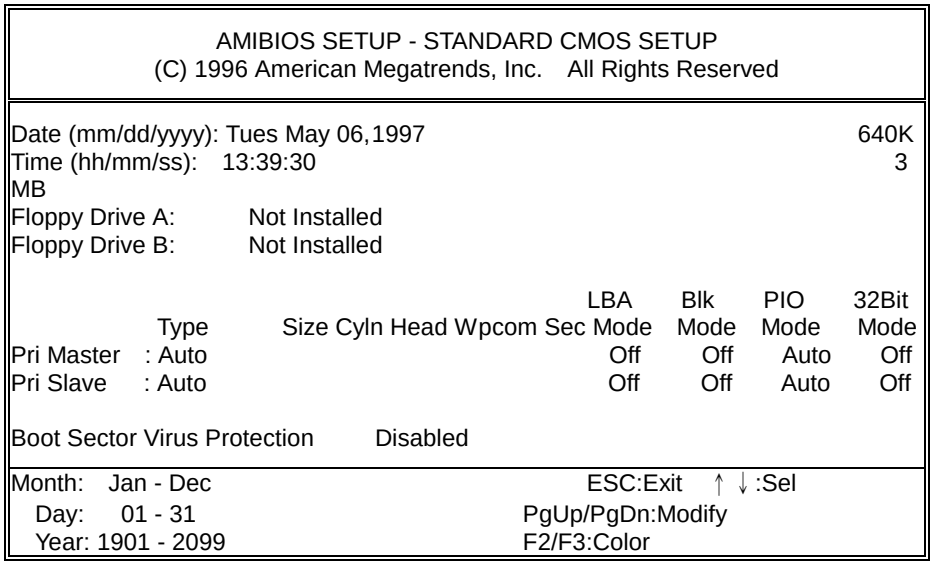

Figure 6-2 BIOS: Standard CMOS Setup

6.2.1 Time Setup

To highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

To highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

User can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

6.2.2 Floppy Setup

The <Standard CMOS Setup> option record the types of floppy disk drives installed in system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

6.2.3 Hard Disk Setup

The BIOS supported 48 types for user setting, The BIOS supported <Pri Master> and <Pri Slave> two items that user can install up to two hard disks. The master and slave jumper adjusting, please refer to the hard disk's installation description and the hard disk jumper setting.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during boot up. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives, which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option. The user type referring to the hard disk type setting, it always sets the <Cyln>, <Head> and <Sec> the three items, the BIOS will find the hard disk correct type.

6.2.4 Virus Protection

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is ***Disabled***. This setting is recommended because conflicts with new operating systems. Installation of new operating systems requires that you disable this to prevent write errors.

6.3 ADVANCED CMOS SETUP

The <Advanced CMOS Setup> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings.

AMIBIOS SETUP - ADVANCED CMOS SETUP (C) 1996 American Megatrends, Inc. All Rights Reserved		
BootUp Sequence		Available Options: C:, A:. CDROM A:, C:, CDROM CDROM, A:, C:
BootUp Num-Lock	On	
Floppy Drive Swap	Disabled	
Floppy Drive Seek	Disabled	
Typematic Rate	Fast	
System Keyboard	Present	
Primary Display	VGA/EGA	
Password Check	Setup	
Wait For 'F1' If Error	Enabled	
Hit 'DEL' Message Display	Enabled	
Internal Cache	WriteBack	
System BIOS Cacheable	Enabled	
Hard disk Delay	5 Sec	
C000, 16k Shadow	Enabled	
C400, 16k Shadow	Enabled	
C800, 16k Shadow	Disabled	
CC00, 16k Shadow	Disabled	
D000, 16k Shadow	Disabled	
D400, 16k Shadow	Disabled	
D800, 16k Shadow	Disabled	ESC:Exit ↑ ↓:Sel PgUp/PgDn:Modify F2/F3:Color
DC00, 16k Shadow	Disabled	

Figure 6-3 BIOS: Advanced CMOS Setup

6.3.1 Boot Up and Floppy

(1) Quick Boot

This category speeds up Power On Self Test (POST) after you power on the computer. If it is set to ***Enabled***, BIOS will shorten or skip some check items during POST.

(2) Boot Up Sequence

The option determines where the system looks first for an operating system. The default setting is to check first the hard disk and then the floppy drive, and last the CDROM.

(3) Boot Up Num-Lock

The item is used to active the Num Lock function upon system boot. If the setting is on, after user booted computer, the light of Num Lock is bright, and user can use the number key.

(4) Floppy Drive Swap

The option reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When enabled, the BIOS swaps floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

(5) Floppy Drive Seek

If the <Floppy Drive Seek> item is setting ***Enabled***, the BIOS will seek the floppy <A> drive one time.

6.3.2 Keyboard, VGA & Password

(1) Typematic Rate

This item specifies the speed at which a keyboard keystroke is repeated.

(2) Primary Display

The option is used to set the type of video display card installed in system.

(3) Password Check

This option enables password checking every time the computer is powered on or every time BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if BIOS is executed.

(4) System Keyboard

This function specifies that a keyboard is attached to the computer.

(5) Wait for 'F1' If Error

AMIBIOS POST error messages are followed by:

```
Press <F1> to continue
```

If this option is set to ***Disabled***, AMIBIOS does not wait for you to press the <F1> key after an error message.

(6) Hit 'DEL' Message Display

Set this option to Disabled to prevent the message as follows:

```
Hit 'DEL' if you want to run setup
```

It will prevent the message from appearing on the first BIOS screen when the computer boots.

6.3.3 System

(1) Internal Cache

This option specifies the caching algorithm used for L1 internal cache memory. The settings are:

Setting	Description
Disabled	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
WriteBack(*)	Use the write-back caching algorithm.
WriteThru	Use the write-through caching algorithm.

* presents the factory-default setting

Table 6-1 Internal Cache Setting

(2) System BIOS Cacheable

When this option is set to ***Enabled***, the contents of the F0000h system memory segment can be read from or written to L2 secondary cache memory. The contents of the F0000h memory segment are always copied from the BIOS ROM to system RAM for faster execution.

The settings are ***Enabled*** or ***Disabled***. The Optimal default setting is ***Enabled***. The Fail-Safe default setting is ***Disabled***.

(3) Shadow

These options control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

SETTING	DESCRIPTION
Disabled	The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
Enabled	The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.
Cached	The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Table 6-2 Shadow setting

6.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.

AMIBIOS SETUP - ADVANCED CHIPSET SETUP
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Auto Config Function	Enabled	Available Options :
AT Bus Clock	CLK/4	Disabled
DRAM Read Timing	Faster	Enabled
DRAM Write Timing	Faster	
Memory Parity Check	Disabled	
DRAM Hidden Refresh	Enabled	
DRAM Refresh Period Setting	60us	
Memory Hole At 15-16M		ESC:Exit ↑ ↓ :Sel
Disabled		PgUp/PgDn:Modify
ISA I/O Recovery	Disabled	F2/F3:Color
ISA I/O Recovery time	1.5us	

Figure 6-4 BIOS: Advanced Chipset Setup

(1) Memory Hole at 15-16 MB

This option specifies the range 15MB to 16MB in memory that cannot be addressed on the ISA bus.

(2) Memory Parity Check

This option enables or disables parity error checking for all system RAM. This option must be ***Disabled*** if the used DRAM SIMMs are 32-bit but not 36-bit devices.

(3) Bus Clock Selection

This option is used to select the ISA bus clock rate.

(4) I/O Recovery Time

These options specify the length of the delay (in BUSCLK) inserted between consecutive 8-bit/16-bit I/O operations.

6.5 PERIPHERAL SETUP

This section is used to configure peripheral features.

AMIBIOS SETUP - PERIPHERAL SETUP (C) 1996 American Megatrends, Inc. All Rights Reserved		
OnBoard FDC	Enabled	Available Options : Auto Disabled Enabled
OnBoard Serial Port1	3F8h	
OnBoard Serial Port1 IRQ	4	
OnBoard Serial Port2	2F8h	
OnBoard Serial Port2 IRQ	3	
OnBoard Parallel Port	378	
Parallel Port Mode	Normal	
EPP Version	N/A	
Parallel Port IRQ	7	
Parallel Port DMA Channel	N/A	
OnBoard IDE	Both	ESC:Exit ↑ ↓:Sel PgUp/PgDn:Modify F2/F3:Color

Figure 6-5 BIOS: Peripheral Setup

(1) On Board FDC

This option enables the floppy drive controller on the AR-B9616.

(2) On Board Serial Port

This option enables serial port on the AR-B9616.

(3) On Board Parallel Port

This option enables parallel port on the AR-B9616.

(4) Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications.

(5) Parallel Port DMA Channel

This option is only available if the setting for the parallel Port Mode option is ECP.

(6) On Board IDE

This option specifies the onboard IDE controller channels that will be used.

6.6 AUTO-DETECT HARD DISKS

This option detects the parameters of an IDE hard disk drive, and automatically enters them into the Standard CMOS Setup screen.

6.7 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. User can set either a Supervisor password or a User password.

6.7.1 Setting Password

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after BIOS completes. The next time the system boots, you are prompted for the password function is present and is enabled.

```
Enter new supervisor password:
```

6.7.2 Password Checking

The password check option is enabled in Advanced Setup by choosing either ***Always*** (the password prompt appears every time the system is powered on) or ***Setup*** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. User can enter a password by typing on the keyboard. As user select Supervisor or User. The BIOS prompts for a password, user must set the Supervisor password before user can set the User password. Enter a 1-6 character password. The password does not appear on the screen when typed. Make sure you write it down.

6.8 LOAD DEFAULT SETTING

In this section permit user to select a group of setting for all BIOS Setup options. Not only can you use these items to quickly set system configuration parameters, you can choose a group of setting s that have a better chance of working when the system is having configuration related problems.

6.8.1 Auto Configuration with Optimal Setting

User can load the optimal default settings for the BIOS. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

```
Load high performance setting (Y/N) ?
```

6.8.2 Auto Configuration with Fail Safe Setting

User can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.

The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

```
Load failsafe settings (Y/N) ?
```

6.9 BIOS EXIT

This section is used to exit the BIOS main menu in two types situation. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

6.9.1 Save Settings and Exit

This item set in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you to Save data to CMOS and Exit the Setup.

```
Save current settings and exit (Y/N) ?
```

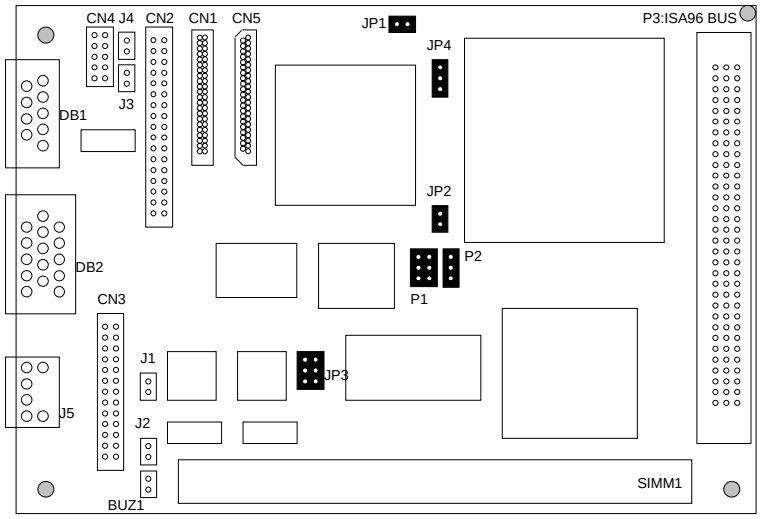
6.9.2 Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to abandon all Data and Exit Setup.

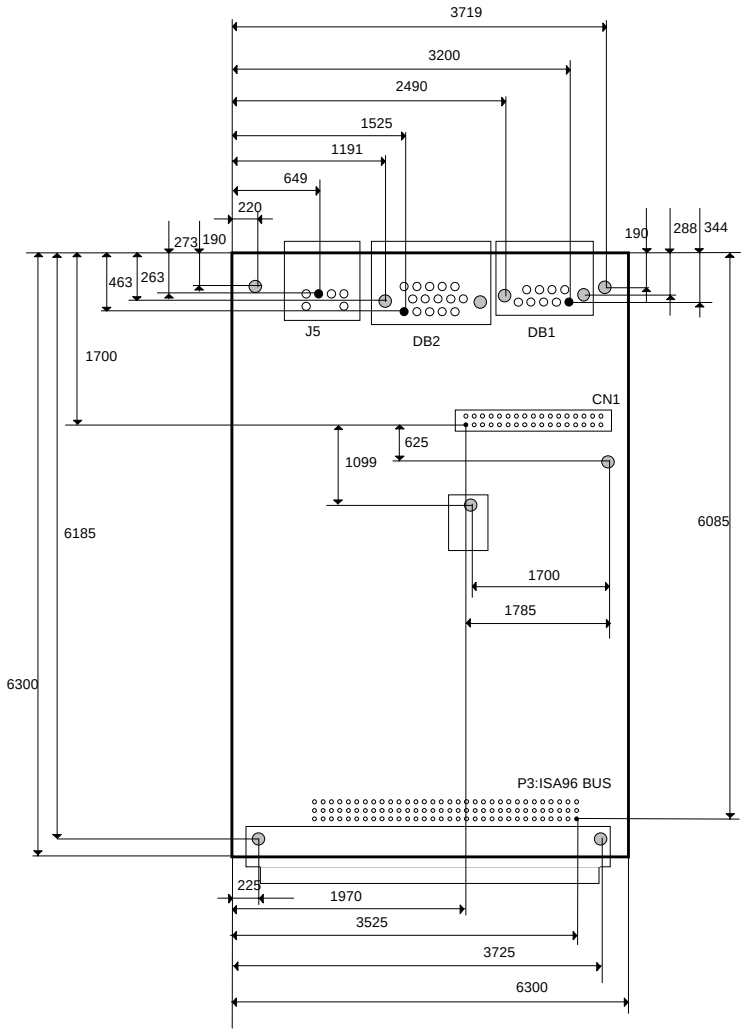
```
Quit without saving (Y/N) ?
```

A. PLACEMENT & DIMENSIONS

A.1 PLACEMENT



A.2 DIMENSIONS



Unit: mil (1 inch=25.4mm=1000 mil)

B. SPECIFICATIONS & INDEX

B.1 SPECIFICATIONS

CPU:	Supports Intel /AMD /Cyrix /IBM /ST /TI 486DX /DX2 /DX4 & 5X86, up to 133MHz CPU PGA168 socket, without CPU for standard
Chipset:	ALI M1489/M1487 chipset and C & T F65545 or compatible chips
Bus Interface:	ISA96 bus
RAM Memory:	Supports 32MB maximum (one 72-pin SIMM)
Cache Size:	0 KB
Watchdog:	Software programmable, 3 to 42 seconds time interval Watchdog LED indicator or header
VGA/LCD:	1MB VRAM (PCI bus, 1024X768/256 colors)
PCI IDE:	Supports LBA/Block mode access
FDC:	Supports 360KB/720KB/1.2MB/1.44MB FDD
Parallel:	Supports SPP/EPP/ECP mode
RS-232C:	One with DB9 connector located at front edge One with 2.54mm 10-pin connector (All support 16C550 compatible UART)
Keyboard:	PC/AT compatible with 6-pin mini-DIN connector located at front edge
BIOS:	AMI Flash BIOS (128KB, including VGA BIOS)
RTC:	BQ3287MT or compatible chips with 128bytes data RAM
Indicator:	Power LED, watchdog LED and HDD LED header
Speaker:	External speaker with 2-pin header
Bus Drive Cap.:	15 TTL level loads maximum
Power Req.:	+5V only, 2.5A maximum (base on Intel 80486DX4-100
CE Design-In:	Add EMI components to COM ports, Parallel port, CRT, and Keyboard
PC Board:	8 layers, EMI considered
Dimensions:	100mmX160mm (3.94"X6.30")

B.2 INDEX