AR-B9612

User’s Guide

Version : 2.1

1. OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

1.1 INTRODUCTION

The AR-B9612 PC/104, CPU module is a lower power consuming, high performance 386 based computer. By using the space saving features of the ALI M6117 CPU, this module is able to support up to 4MB's of DRAM and 1.5 MB's of Flash memory on board. The unit also comes with two RS-232C/RS-485 ports adding a high degree of versatility to any project. The AR-B9612 is an excellent choice for mobile systems, or as a controller for machines that are too small to accommodate traditional industrial PC's.

The AR-B9612 offers embedded applications the speed and stability of a 386SX with the size of a true PC/104 module.

1.2 PACKING LIST

The accessories are included with the system. Before you begin installing your AR-B9612 board, take a moment to make sure that the following items have been included inside the AR-B9612 package.

- This user's guide
- 1 AR-B9612 PC/104 386SX Single CPU board
- 1 Keyboard adapter cable
- 2 RS-232C interface cable
- 1 Power adapter cable

Accessory	Description
Keyboard adapter cable	1 4-pin to 6-pin mini-din PS/2 to IBM standard type adapt cable
Power adapter cable	4-pin power adapter cable
RS-232C interface cable	2 10-pin RS-232C interface cable

Table 1-1 Accessories

1.3 FEATURES

The system provides a number of special features that enhance its reliability, ensure its availability, and improve its expansion capabilities, as well as its hardware structure.

- 80386SX-33/40 MHz CPU
- PC/104 extension bus
- Up to 4MB DRAM system
- Supports 2 RS-232C/RS-485 serial port
- PC/AT compatible keyboard interface
- Supports up to 1.5MB flash disk
- Programmable watchdog timer
- Flash BIOS
- Powered-on LED indicator
- Signal 5V power requirement
- Multi-layer PCB for noise reduction
- Dimensions : 90.2mmX95.9mm

2. SYSTEM CONTROLLER

This chapter describes the major structure. The following topics are covered:

- Microprocessor
- DMA Controller
- I/O Port Address Map
- Interrupt Controller
- Serial Port
- Real-Time Clock and Non-Volatile RAM
- Timer
- Watch-Dog Timer
- FLASH Disk

2.1 MICROPROCESSOR

The AR-B9612 use the ALI M6117 CPU, it is designed to perform like Intel's 386SX system with deep green features.

The 386SX core is the same as M1386SX of Acer Labs. Inc. and 100% object code compatible with the Intel 386SX microprocessor. System manufacturers can provide 386 CPU based systems optimized for both cost and size. Instruction pipelining and high bus bandwidth ensure short average instruction execution times and high system throughput. Furthermore, it can keep the state internally from charge leakage while external clock to the core is stopped without storing the data in registers. The power consumption here is almost zero when clock stops. The internal structure of this core is 32-bit data and address bus with very low supply current. Real mode as well as protected mode are available and can run MS-DOS, MS-Windows, OS/2 and UNIX.

2.2 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented in the AR-B9612 card. Each controller is a four channel DMA device which will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speed information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

Following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Table 2-1 DMA Channel Controller

2.3 I/O PORT ADDRESS MAP

Hex Range	Device
000-01F	DMA controller 1
020-021	Interrupt controller 1
022-023	ALI M6117 chipset address
040-04F	Timer 1
050-05F	Timer 2
060-06F	8042 keyboard/controller
070-071	Real-time clock (RTC), non-maskable interrupt (NMI)
080-09F	DMA page registers
0A0-0A1	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0	Clear Math Co-processor
0F1	Reset Math Co-processor
0F8-0FF	Math Co-processor
170-178	Fixed disk 1
1F0-1F8	Fixed disk 0
201	Game port
208-20A	EMS register 0
218-21A	EMS register 1
278-27F	Parallel printer port 3 (LPT 3)
2E8-2EF	Serial port 4 (COM 4)
2F8-2FF	Serial port 2 (COM 2)
300-31F	Prototype card/Streaming Type Adapter
378-37F	Parallel printer port 2 (LPT 2)
380-38F	SDLC, bisynchronous
3A0-3AF	Bisynchronous
3B0-3BF	Monochrome display and printer port 1 (LPT 1)
3C0-3CF	EGA/VGA adapter
3D0-3DF	Color/Graphics monitor adapter
3E8-3EF	Serial port 3 (COM 3)
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1 (COM 1)

Table 2-2 I/O Port Address Map

2.4 INTERRUPT CONTROLLER

The ALI's M6 117 also provides two cascaded 8259 Programmable Interrupt Controllers (PIC). They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute.

Following is the system information of interrupt levels:

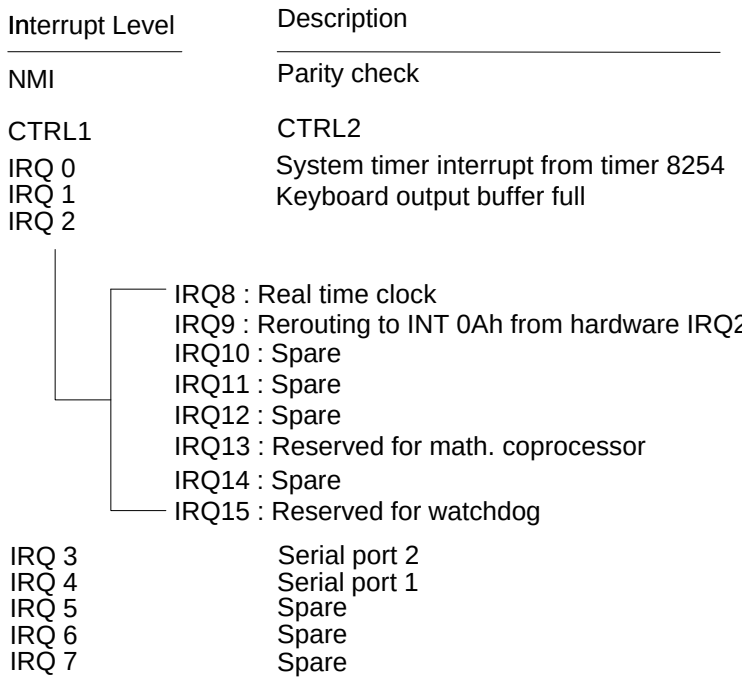

Figure 2-1 Interrupt Controller

2.5 SERIAL PORT

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE is a complete MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The follows is summary of each ACE accessible registers

DLAB	Port Address	Register
0	base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	base + 1	Interrupt enable
X	base + 2	Interrupt identification (read only)
X	base + 3	Line control
X	base + 4	MODEM control
X	base + 5	Line status
X	base + 6	MODEM status
X	base + 7	Scratched register
1	base + 0	Divisor latch (least significant byte)
1	base + 1	Divisor latch (most significant byte)

Table 2-3 ACE Accessible Register

(1) Receiver Buffer Register (RBR)

Bit 0-7: Received data byte (Read Only)

(2) Transmitter Holding Register (THR)

Bit 0-7: Transmitter holding data byte (Write Only)

(3) Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)
Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)
Bit 2: Enable Receiver Line Status Interrupt (ELSI)
Bit 3: Enable MODEM Status Interrupt (EDSSI)
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(4) Interrupt Identification Register (IIR)

Bit 0: "0" if Interrupt Pending
Bit 1: Interrupt ID Bit 0
Bit 2: Interrupt ID Bit 1
Bit 3: Must be 0
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(5) Line Control Register (LCR)

Bit 0: Word Length Select Bit 0 (WLS0)
Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)
Bit 3: Parity Enable (PEN)
Bit 4: Even Parity Select (EPS)
Bit 5: Stick Parity
Bit 6: Set Break
Bit 7: Divisor Latch Access Bit (DLAB)

(6) MODEM Control Register (MCR)

Bit 0: Data Terminal Ready (DTR)
Bit 1: Request to Send (RTS)
Bit 2: Out 1 (OUT 1)
Bit 3: Out 2 (OUT 2)
Bit 4: Loop
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(7) Line Status Register (LSR)

Bit 0: Data Ready (DR)
Bit 1: Overrun Error (OR)
Bit 2: Parity Error (PE)
Bit 3: Framing Error (FE)
Bit 4: Break Interrupt (BI)
Bit 5: Transmitter Holding Register Empty (THRE)
Bit 6: Transmitter Shift Register Empty (TSRE)
Bit 7: Must be 0

(8) MODEM Status Register (MSR)

Bit 0: Delta Clear to Send (DCTS)
Bit 1: Delta Data Set Ready (DDSR)
Bit 2: Training Edge Ring Indicator (TERI)
Bit 3: Delta Receive Line Signal Detect (DSLSD)
Bit 4: Clear to Send (CTS)
Bit 5: Data Set Ready (DSR)
Bit 6: Ring Indicator (RI)
Bit 7: Received Line Signal Detect (RSLD)

(9) Divisor Latch (LS, MS)

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock	Present Error Difference Between Desired and Actual
50	2304	---
75	1536	---
110	1047	0.026
134.5	857	0.058
150	768	---
300	384	---
600	192	---
1200	96	---
1800	64	---
2000	58	0.69
2400	48	---
3600	32	---
4800	24	---
7200	16	---
9600	12	---
14400	8	---
19200	6	---
28800	4	---
38400	3	---
57600	2	---

Table 2-4 Serial Port Divisor Latch

2.6 REAL-TIME CLOCK AND NON-VOLATILE RAM

The AR-B9612 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and registers and 50 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long period of time using an internal lithium battery.

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte

Address	Description
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

Table 2-5 Real-Time Clock & Non-Volatile RAM

2.7 TIMER

The AR-B9612 provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.
Application programs can load different counts into this timer to generate various sound frequencies.

2.8 WATCH-DOG TIMER

The watchdog timer is a circuit that may be used from your program software to detect crashes or hang-ups.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times-out. After you trigger the watchdog timer, it will be set to zero and start to count again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system.
The I/O port address of watchdog timer is located at 214Hex or 215Hex. The factor of the watchdog timer time-out constant is approximately 1.6 seconds.

2.8.1 Enabled the Watchdog Timer

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog address. The following is a BASICA program:

```
1000        REM Points to I/O port address
1010            WD_REG% = I/O_PORT
1020        REM Timer factor =80H
1030            TIMER_FACTOR% = &H80
1040        REM Output factor to watchdog
1050            OUT WD_REG%, TIMER_FACTOR%
            ,etc.
```

2.8.2 Trigger Watchdog Timer

After you enable the watchdog timer, your program must trigger the watchdog at least once every time-out period. The factor of the watchdog timer time-out constant is approximately 1.6 seconds, the trigger way just is the activity of read I/O, and not care the reading number. Below is a BASICA program which demonstrates how to trigger the watchdog timer:

```
2000        REM Points to I/O port address
2010            WD_REG% = I/O_PORT
2020        REM Input factor to watchdog
2030            WD=INP(WD_REG%)
            ,etc.
```

2.8.3 Disabled the Watchdog Timer

To disable the watchdog timer, simply write a 00H to the watchdog.

```
1000        REM Points to I/O port address
1010            WD_REG% = I/O_PORT
1020        REM Timer factor = 0
1030            TIMER_FACTOR% = 0
1040        REM Output factor to watchdog
1050            OUT WD_REG%, TIMER_FACTOR%
            ,etc.
```

2.9 FLASH DISK

The AR-B9612 provides three 32-pin JEDEC DIP sockets may be populated with up to 1.5MB FLASH. It is ideal for diskless system, high reliability and/or high speed access applications, controller for industrial or line test instruments, etc.

2.9.1 Configuration

FLASH function enables you to use 5V FLASH, allowing you to directly program the ROM disk without having to purchase any additional programming equipment to write or erase data. If small page (less or equal 512 bytes per page) 5V FLASHs are used, you can format FLASH disk and copy files onto FLASH disk just like using floppy disk. If you would like to update 1 or more files to FLASH disk, you just copy these files onto FLASH disk, you don't need to re -program the FLASH disk.

If you are not going to use the solid state disk (SSD), you can use BIOS setup program to disable the SSD BIOS. The AR-B9612 will not occupy any memory address if the SSD BIOS is disabled.

If you are going to install the EMM386.EXE driver, please use the [X] option to prevent EMM386.EXE from using the particular range of segment address as an EMS page which is used by AR-B9612. For example, write a statement in the CONFIG.SYS file as follow: (If the memory configuration of AR-B9612 is C800:0)

```
DEVICE=C:\DOS\EMM386.EXE X=C800-CBFF
```

Software Programming

You can use the DOS <FORMAT> and <COPY> command to format and copy files. Follow the following steps to format and copy files to the FLASH disk.

Step 1: Turn on your computer, when the screen shows the SSD BIOS menu, please hit the [F1] key during the system boot-up, this enables you to enter the FLASH setup program.

Step 2: Use <Page-Up>, <Page-Down>, <Right>, and <Left> arrow keys to select the correct FLASH memory type and how many memory chips are going to be used.

Step 3: Press the [F4] key to save the current settings.

Step 4: After the DOS is loaded, use the DOS [FORMAT] command to format the FLASH disk

To format the disk and copy DOS system files to the disk.

C:\>FORMAT [ROM disk letter] /S /U

To format the disk without copying DOS system files.

C:\>FORMAT [ROM disk letter] /U

Step 5: Copy your program or files to the FLASH disk by using DOS [COPY] command.

CAUTION: It is not recommended that the user format the disk and copy files to the FLASH disk very often. Since the FLASH EPROM's write cycle life time is about 10,000 or 100,000 times, writing data to the FLASH EPROM chips, especially the FLASH EPROM chips, especially the FLASH EPROM chip in the MEM1 socket.

3. SETTING SYSTEM

This section describes pin assignments for system's external connectors and the jumper settings.

- Overview
- System Setting

3.1 OVERVIEW

The AR-B9612 is one small, easy use, and single 386SX CPU board with 2 RS-232/RS-485. This section provides hardware's jumpers setting, and the connectors locations and the pin assignment.

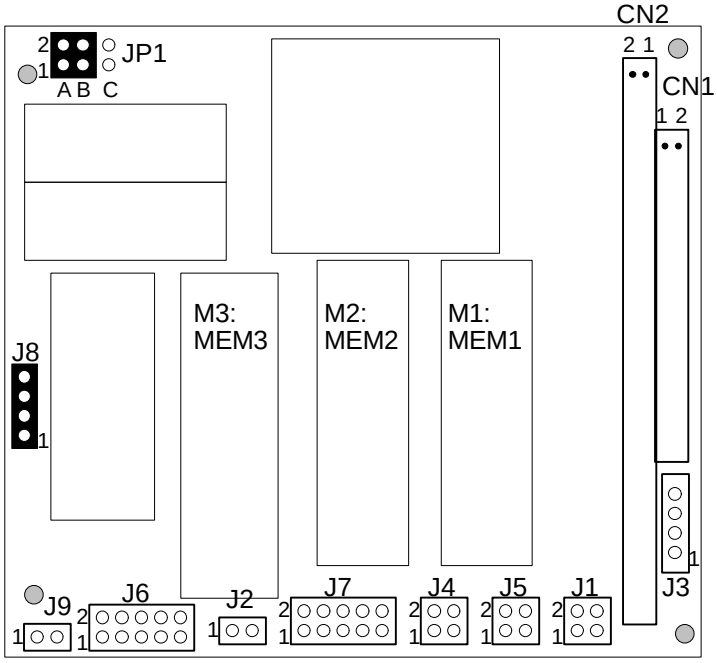

Figure 3-1 Jumpers & Connectors

3.2 SYSTEM SETTING

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor [shorting plug] that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the AR-B9612 jumper pins, and the factory-default setting. Note that the square pin of each jumper block is pin 1.

CAUTION : Do not touch any electronic component unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. A static discharge from your fingers can permanently damage electronic components.

3.2.1 PC/104 Connector

(1) 40 Pin PC/104 Connector Bus C & D (CN1)

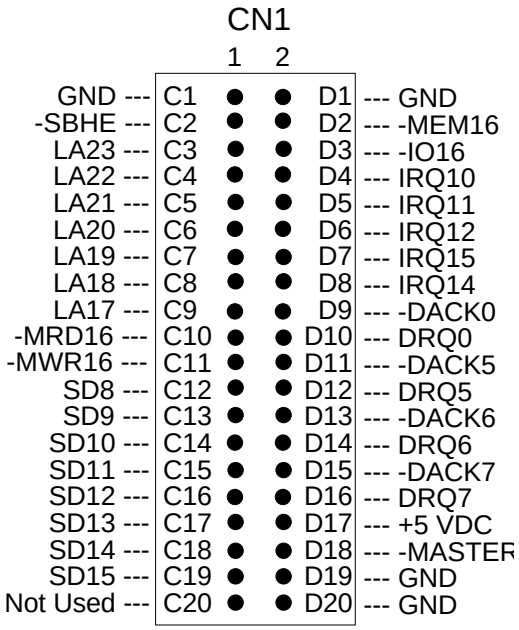

Figure 3-2 CN1:40-Pin PC/104 Connector Bus C & D

(2) 64 Pin PC/104 Connector Bus A & B (CN2)

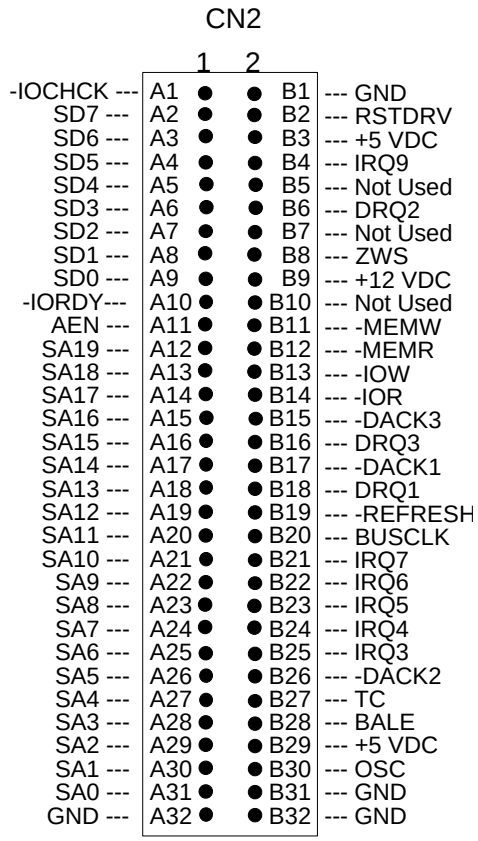

Figure 3-3 CN2:64-Pin PC/104 Connector Bus A & B

(3) I/O Channel Signal Description

Name	Description
BUSCLK [Output]	The BUSCLK signal of the I/O channel is asynchronous to the CPU clock.
RSTDRV [Output]	This signal goes high during power-up, low line-voltage or hardware reset
SA0 - SA19 [Input / Output]	The System Address lines run from bit 0 to 19. They are latched onto the falling edge of "BALE"
LA17 - LA23 [Input/Output]	The Unlatched Address line run from bit 17 to 23
SD0 - SD15 [Input/Output]	System Data bit 0 to 15
BALE [Output]	The Buffered Address Latch Enable is used to latch SA0 - SA19 onto the falling edge. This signal is forced high during DMA cycles
-IOCHCK [Input]	The I/O Channel Check is an active low signal which indicates that a parity error exist on the I/O board
IOCHRDY [Input, Open collector]	This signal lengthens the I/O, or memory read/write cycle, and should be held low with a valid address
IRQ 3-7, 9-12, 14, 15 [Input]	The Interrupt Request signal indicates I/O service request attention. They are prioritized in the following sequence : (Highest) IRQ 9, 10, 11, 12, 13, 15, 3, 4, 5, 6, 7 (Lowest)
-IOR [Input/Output]	The I/O Read signal is an active low signal which instructs the I/O device to drive its data onto the data bus
-IOW [Input/Output]	The I/O write signal is an active low signal which instructs the I/O device to read data from the data bus
-SMEMR [Output]	The System Memory Read is low while any of the low 1 mega bytes of memory are being used
-MEMR [Input/Output]	The Memory Read signal is low while any memory location is being read
-SMEMW [Output]	The System Memory Write is low while any of the low 1 mega bytes of memory is being written
-MEMW [Input/Output]	The Memory Write signal is low while any memory location is being written

Name	Description
DRQ 0-3, 5-7 [Input]	DMA Request channels 0 to 3 are for 8-bit data transfers. DMA Request channels 5 to 7 are for 16-bit data transfers. DMA request should be held high until the corresponding DMA has been completed. DMA request priority is in the following sequence:(Highest) DRQ 0, 1, 2, 3, 5, 6, 7 (Lowest)
-DACK 0-3, 5-7 [Output]	The DMA Acknowledges 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3 and 5 to 7
AEN [output]	The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the CPU is driving the address bus
-REFRESH [Input/Output]	This signal is used to indicate a memory refresh cycle and can be driven by the microprocessor on the I/O channel
TC [Output]	Terminal Count provides a pulse when the terminal count for any DMA channel is reached
SBHE [Input/Output]	The System Bus High Enable indicates the high byte SD8 - SD15 on the data bus
-MASTER [Input]	The MASTER is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh
-MEMCS16 [Input, Open collector]	The Memory Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data memory operation
-IOCS16 [Input, Open collector]	The I/O Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data I/O operation
OSC [Output]	The Oscillator is a 14.31818 MHz signal
-ZWS [Input, Open collector]	The Zero Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting additional wait cycle

Table 3-1 I/O Channel Signal Description

3.2.2 Keyboard Connector (J1)

J1 is a 6-pin mini-DIN keyboard connector. This keyboard connector is PS/2 type keyboard compatible. An PC/AT compatible keyboard can be used with the AR-B9612 card.

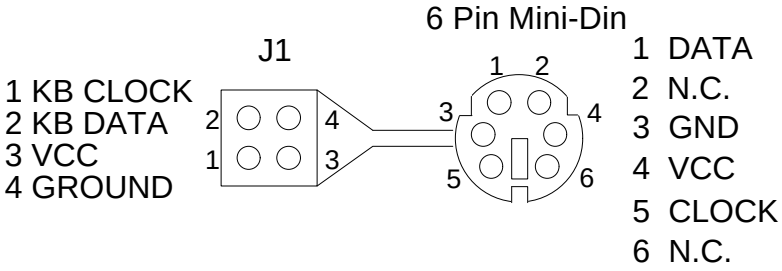

Figure 3-4 J1:Keyboard Connector

CAUTION : The keyboard adapter cable's pinouts must map to the keyboard connector's pins. Acrosser uses various color to distinguish the pinouts as follows:

Pin 1 : gray	Pin 2 : yellow
Pin 3 : red	Pin 4 : green

3.2.3 Speaker Header (J2)

The AR-B9612 provides a 2-pin header type connector for supporting up to the speaker.

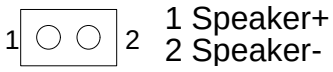

Figure 3-5 J2:Speaker Header

3.2.4 Power Connector (J3)

J3 is a 4 pin power connector, you can directly connect the power supply to the on board power connector for stand alone applications.

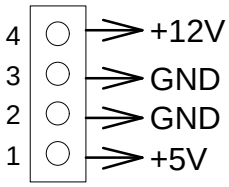

Figure 3-6 J3: Power Connector

3.2.5 Serial Port

(1) Serial Port Mode Select (J8)

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor [shorting plug] that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper even onto the pins. Be careful not to bend the pins.

The J8 is used to choose the serial port mode, include of RS-232, & RS-485.

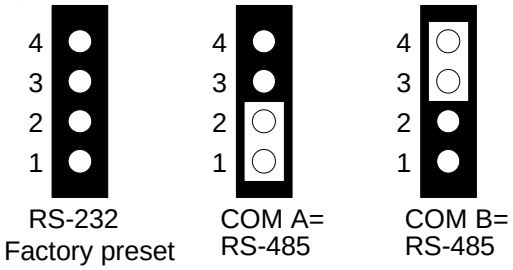

Figure 3-7 J8 : Serial Port Mode Select

(2) RS-485 Connector (J4 & J5)

J4 is used to connect the COM A port RS-485 selected, the I/O port default address is 3F8H.

J5 is used to connect the COM B port RS-485 selected, the I/O port default address is 2F8H.

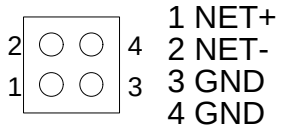

Figure 3-8 J4 & J5 : COM A & COM B RS-485

(3) RS-232C Connector (J6 & J7)

J6 is used to connect the COM A port RS-232 selected, the I/O port default address is 3F8H.

J7 is used to connect the COM B port RS-232 selected, the I/O port default address is 2F8H.

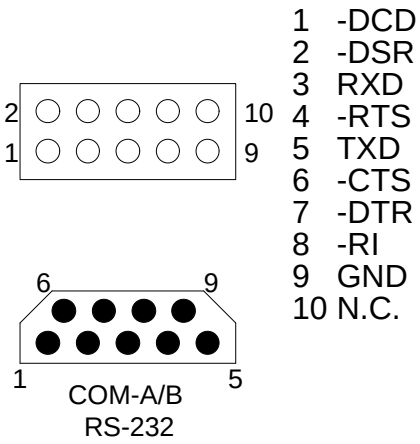

Figure 3-9 J6 & J7 : COM A & COM B RS-232

3.2.6 Reset Connector (J9)

J9 is used to connect to an external reset switch. Shorting these two pins will reset the system.

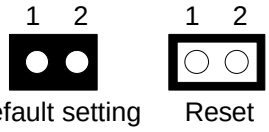

Figure 3-10 J9 : Reset Connector

3.2.7 CPU Base Clock Select (JP1)

This board provides three types of CPU clock for selecting, there is 25MHz, 33MHz, & 40MHz for choice.
The CPU input clock is twice of operation clock.

CPU Input Clock	CPU Operation Clock
50MHz	25MHz
66.6MHz	33.3MHz
80MHz	40MHz

Table 3-2 CPU Clock

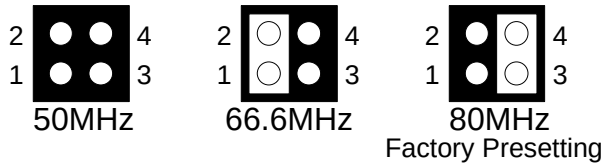

Figure 3-11 JP1 : CPU Base Clock

NOTE : The frequency of input clock is selected by JP1, it is twice of CPU clock. For example, If 33MHz CPUs used, the OSC1 clock will be 66MHz.

4. AR-B9612 BIOS CONSOLE

This chapter describes the BIOS menu displays and explains how to perform common tasks needed to get up and running. And presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Password Setting
- Load Default Setting
- BIOS Exit

4.1BIOS SETUP OVERVIEW

BIOS is a program used to initialize and set up the I/O system of the computer, which includes the ISA bus and connected devices such as the video display, diskette drive, and the keyboard.

This BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware, that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS default values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

After the computer is turned on, the BIOS will perform a diagnostics of the system and display the size of the memory that is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

The BIOS Setup main menu exists nine options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to assure the option and configure the functions.

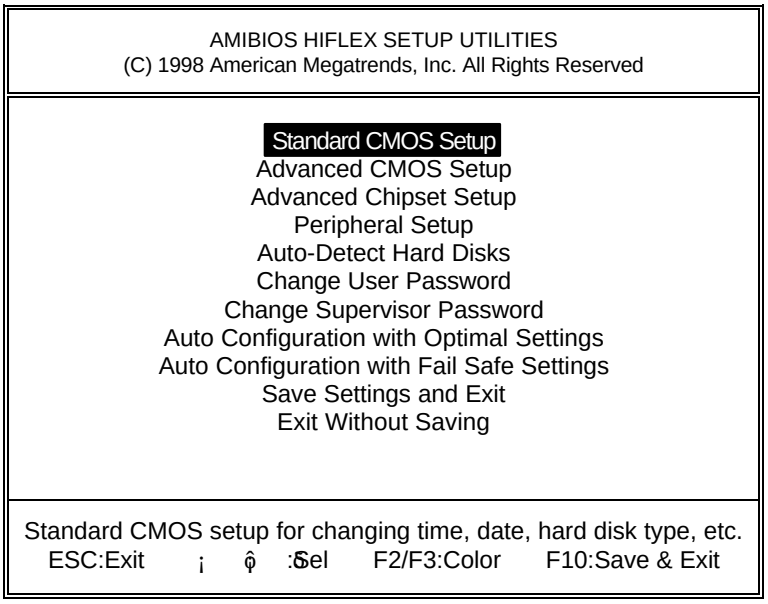

Figure 4-1 BIOS : Setup Main Menu

CAUTION: 1. AR-B9612 BIOS the factory-default setting is used to the <Auto Configuration with Optimal Settings> Acrosser recommends using the BIOS default setting, unless you are very familiar with the setting function, or you can touch the technical support engineer.

2. If the BIOS loss setting, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operation system, this option will reduce the performance of the system. Acrosser recommends choosing the <Auto Configuration with Optimal Setting> in the main menu. The option is best-case values that should optimize system performance.

3. The BIOS settings are described in detail in this section.

4.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

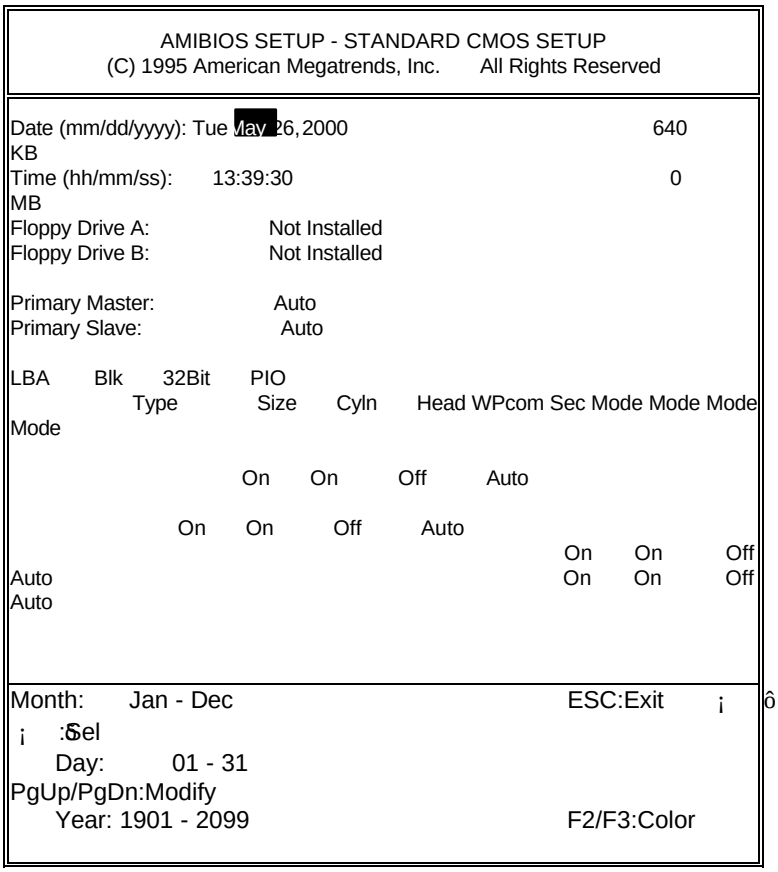

Figure 4-2 BIOS : Standard CMOS Setup

4.2.1 Time Setup

To highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

To highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

User can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

4.2.2 Floppy Setup

The <Standard CMOS Setup> option record the types of floppy disk drives installed in system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

4.2.3 Hard Disk Setup

The BIOS supported 48 types for user setting, The BIOS supported <Pri Master> and <Pri Slave> two items that user can install up to two hard disks. The master and slave jumper adjusting, please refer to the hard disk's installation description and the hard disk jumper setting.

CAUTION: AR-B9612 can not support the 32Bit Transfer, so Acrosser recommends user configure the <32Bit> field is always [Off], not setting [On].

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during bootup. This will allow you to change your hard disk drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

The user type referring to the hard disk type setting, it always sets the <Cyln>, <Head> and <Sec> the three items, the BIOS will find the hard disk size.

4.2.4 Virus Protection

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is ***Disabled***. This setting is recommended because conflicts with new operating systems. Installation of new operating systems require that you disable this to prevent write errors.

4.3 ADVANCED CMOS SETUP

The <Advanced CMOS Setup> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings.

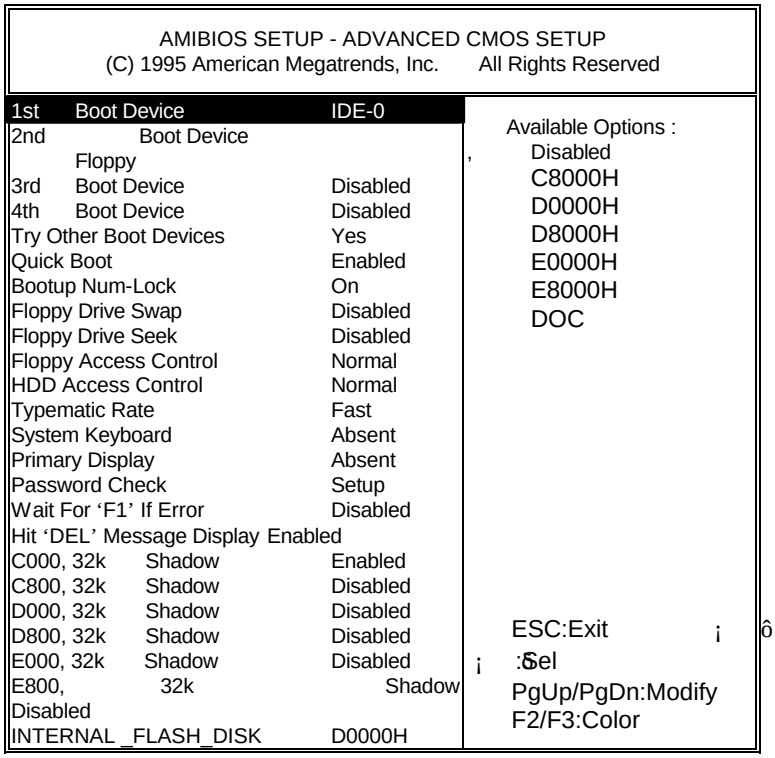

Figure 4-3 BIOS : Advanced CMOS Setup

4.3.1 BootUp and Floppy

(1) BootUp Sequence

The option determines where the system looks first for an operating system. The default setting is to check first the hard disk and then the floppy drive, and last the CDROM.

(2) BootUp Num-Lock

The item is used to active the Num Lock function upon system boot. If the setting is on, after user booted computer, the light of Num Lock is bright, and user can use the number key.

(3) Floppy Drive Swap

The option reverses the drive letter assignments of your floppy disk drives in the Swap AB setting, otherwise leave on the default setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When enabled, the BIOS swaps floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

(4) Floppy Drive Seek

If the <Floppy Drive Seek> item is setting ***Enabled***, the BIOS will seek the floppy <A> drive one time.

4.3.2 Keyboard, VGA & Password

(1) Typematic Rate

This item specifies the speed at which a keyboard keystroke is repeated.

(2) System keyboard

This function specifies that a keyboard is attached to the computer.

(3) Primary Display

The option is used to set the type of video display card installed in system.

(4) Password Check

This option enables password checking every time the computer is powered on or every time BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if BIOS is executed.

4.3.3 System

(1) Wait for 'F1' If Error

AMIBIOS POST error messages are followed by:

```
Press <F1> to continue
```

If this option is set to ***Disabled***, AMIBIOS does not wait for you to press the <F1> key after an error message.

(2) Hit 'DEL' Message Display

Set this options to ***Disabled*** to prevent the message as follows:

```
Hit 'DEL' if you want to run Setup
```

It will prevent the message from appearing on the first BIOS screen when the computer boots.

4.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.

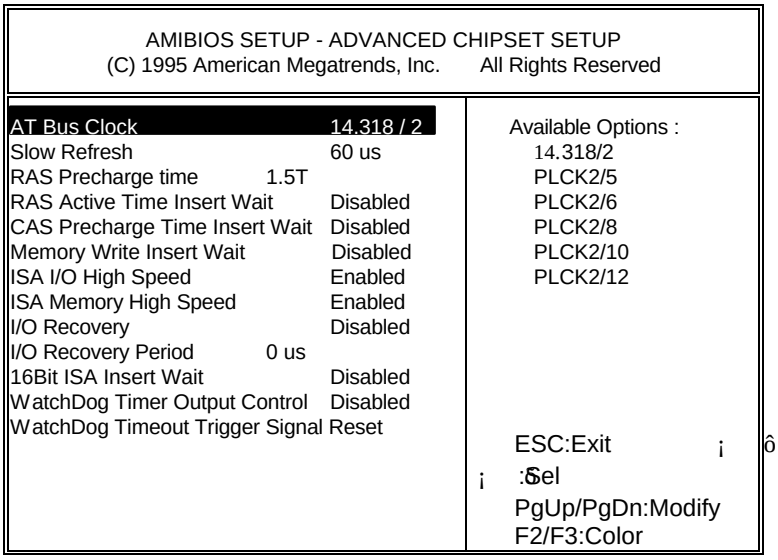

Figure 4-4 BIOS : Advanced Chipset Setup

(1) AT Bus Clock

This option sets the polling clock speed of ISA Bus (PC/104).

Note: 1. PCLK means the CPU inputs clock.

2. Acrosser recommends user setting at the range of 8MHz to 10MHz.

(2) Slow Refresh

This option sets the DRAM refresh cycle time.

(3) RAS Precharge time

The DRAM RAS precharge time.

(4) Time Insert Wait

The DRAM time insert wait: RAS Active and CAS Precharge function setting.

(5) ISA High Speed

The Speed field shows the speed at which the processor runs internally.

(6) I/O Recovery

If I/O Recovery Feature options is ***Enabled***, the BIOS inserts a delay time between two I/O commands. The delay time is defined in I/O Recovery Period option.

4.5 PERIPHERAL SETUP

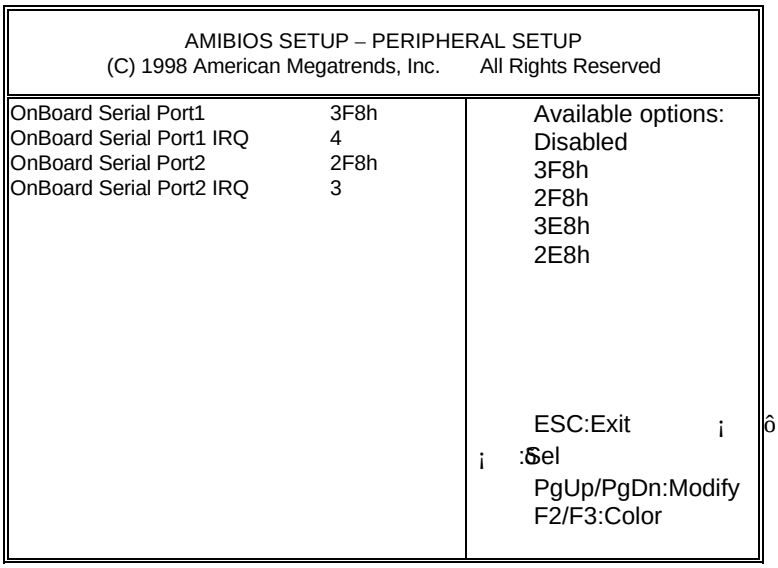

Figure 4-5 BIOS : Peripheral Setup

4.6 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. User can set either a Supervisor password or a User password.

4.6.1 Setting Password

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after BIOS completes. The next time the system boots, you are prompted for the password function is present and is enabled.

Enter new supervisor password:

4.6.2 Password Checking

The password check option is enabled in Advanced Setup by choosing either ***Always*** (the password prompt appears every time the system is powered on) or ***Setup*** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. User can enter a password by typing on the keyboard. As user select Supervisor or User. The BIOS prompts for a password, user must set the Supervisor password before user can set the User password. Enter a 1-6 character

password. The password does not appear on the screen when typed. Make sure you write it down.

4.7 LOAD DEFAULT SETTING

In this section permit user to select a group of setting for all BIOS Setup options. Not only can you use these items to quickly set system configuration parameters, you can choose a group of setting s that have a better chance of working when the system is having configuration related problems.

4.7.1 Auto Configuration with Optimal Setting

User can load the optimal default settings for the BIOS. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the Optimal settings are loaded automatically.

```
Load high performance settings (Y/N) ?
```

4.7.2 Auto Configuration with Fail Safe Setting

User can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.

The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

```
Load failsafe settings (Y/N)?
```

4.8 BIOS EXIT

This section is used to exit the BIOS main menu in two type situation. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

4.8.1 Save Settings and Exit

This item set in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS.The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you to Save data to CMOS and Exit the Setup.

Save current settings and exit (Y/N) ?

4.8.2 Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to Abandon all Data and Exit Setup.

Quit without saving (Y/N) ?