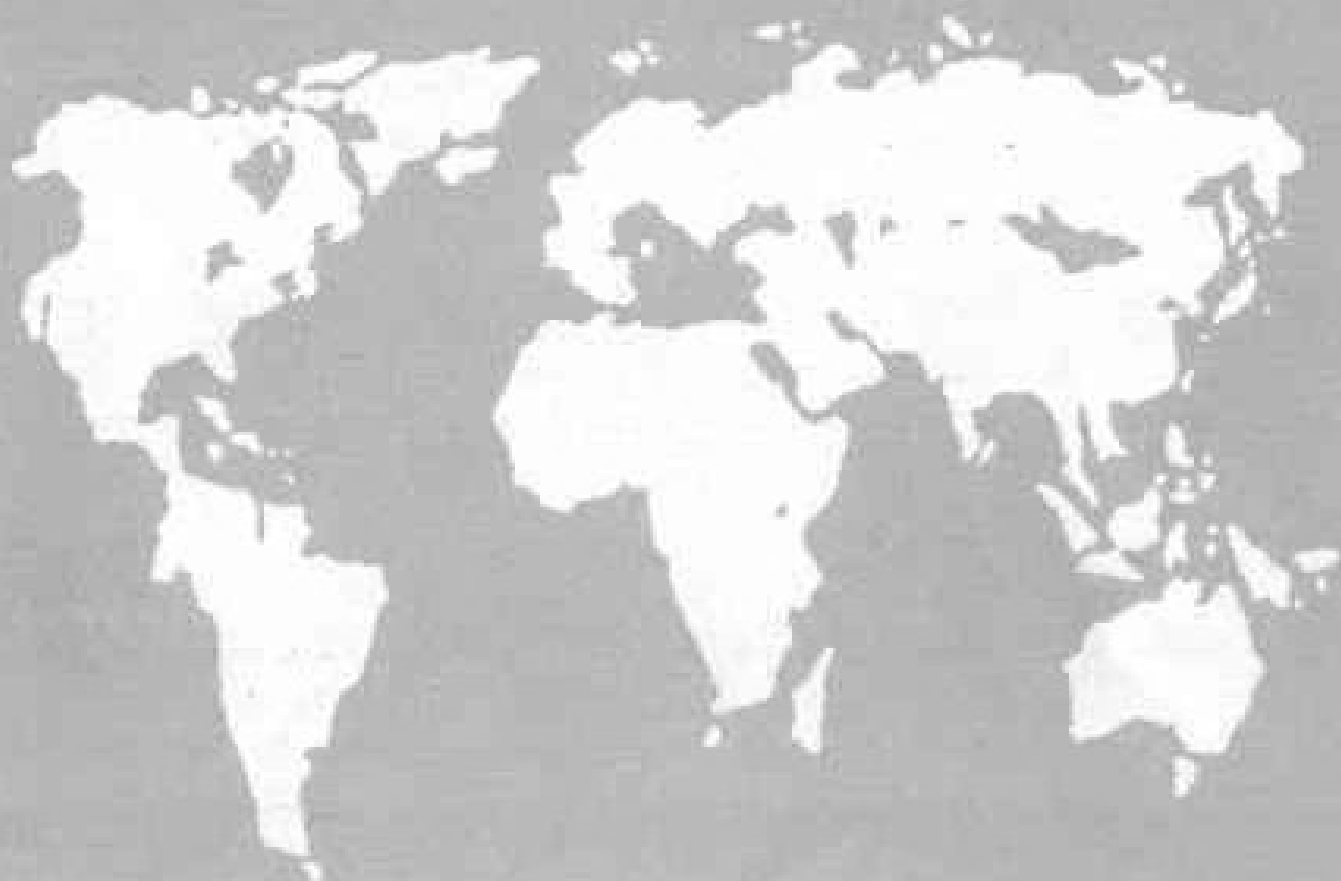


**INTEL 82430I PCI BUS  
MAIN BOARD  
USER'S MANUAL  
(Green function)**



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# CHAPTER 1.

## 1. INTRODUCTION

INTEL 82437FX  
INTEL 82371FB  
INTEL 82438FX  
SMC FDC37C665

SYSTEM CONTROLLER (TSC)  
PCI ISA IDE XCELERATOR (PIIX)  
DATA PATH UNIT (TDP)  
FDC, PARALLEL, SERIAL,

The INTEL 82430I board is a baby size main board integrated by INTEL 82437FX, 82438FX and 82371FB PCiset & SMC I/O FDC37C665GT chipset. The INTEL 82430FX PCiset forms a Host-to-PCI bridge and provides the second level cache control and a full function 64-bit data path to main memory. The TSC integrates the cache and main memory DRAM control function and provides bus control for transfer between the CPU, cache, main memory, and the PCI bus. The second level (L2) cache controllers support a write-back cache policy for cache size of 256K Byte and 512K Byte. Tag RAM is used for address tag and an internal Tag RAM for the cache line status bits. For the TSC's DRAM controller four rows are supported for up to 128M Byte of main memory. The TSC's optimiz<sup>h</sup> PCI interface allows the CPU to sustain the highest possible bandwidth to the graphics frame buffer at all frequencies. Using the snoop ahead feature, The TSC allows PCI masters to achieve full PCI bandwidth. The TDPs provide the data paths between the CPU/cache, main memory, and PCI. For increased system performance, the TDPs contain read prefetch and post write buffers. SMC I/O chipset provides two FDC (360K, 720K, 1.2M, 1.44M, 2.88M) , two serial port compatible UARTS, one multi-mode parallel port for SPP, EPP, ECP

## 2. SPECIFICATION

**CPU:**  
INTEL PENTIUM 75/90/100/120 /180 MHZ VRA/VRE SPEC.

**CACHE:**

256K/512K Asynchronous SRAM

256K (two piece 32K X 32 bit) Synchronous

Pipelined burst SRAM

Provides Write Back

**MEMORY:**

72 pins SIMM module x 4 UP TO 128M Byte

EDO and Fast Page DRAM module supported.

**IDE:**

Support dual PIO and BUS Master IDE

Up to mode 4 timing, Transfer rate to 22M Byte/s

Support Enhance IDE Hard disk x 4 or IDE CD-ROM

**I/O:**

FDC x 2 (360K/720K/1.2M/1.44M/2.88M)

Two serial port for UARTS(16C550)

One parallel port for SPP/EPP/ECP

Jumper setting by BIOS setup

PS2 mouse supported

**PCI:**

32 bit X 3 slots for PCI ver 2.0

**ISA:**

16 bit X 5 slots

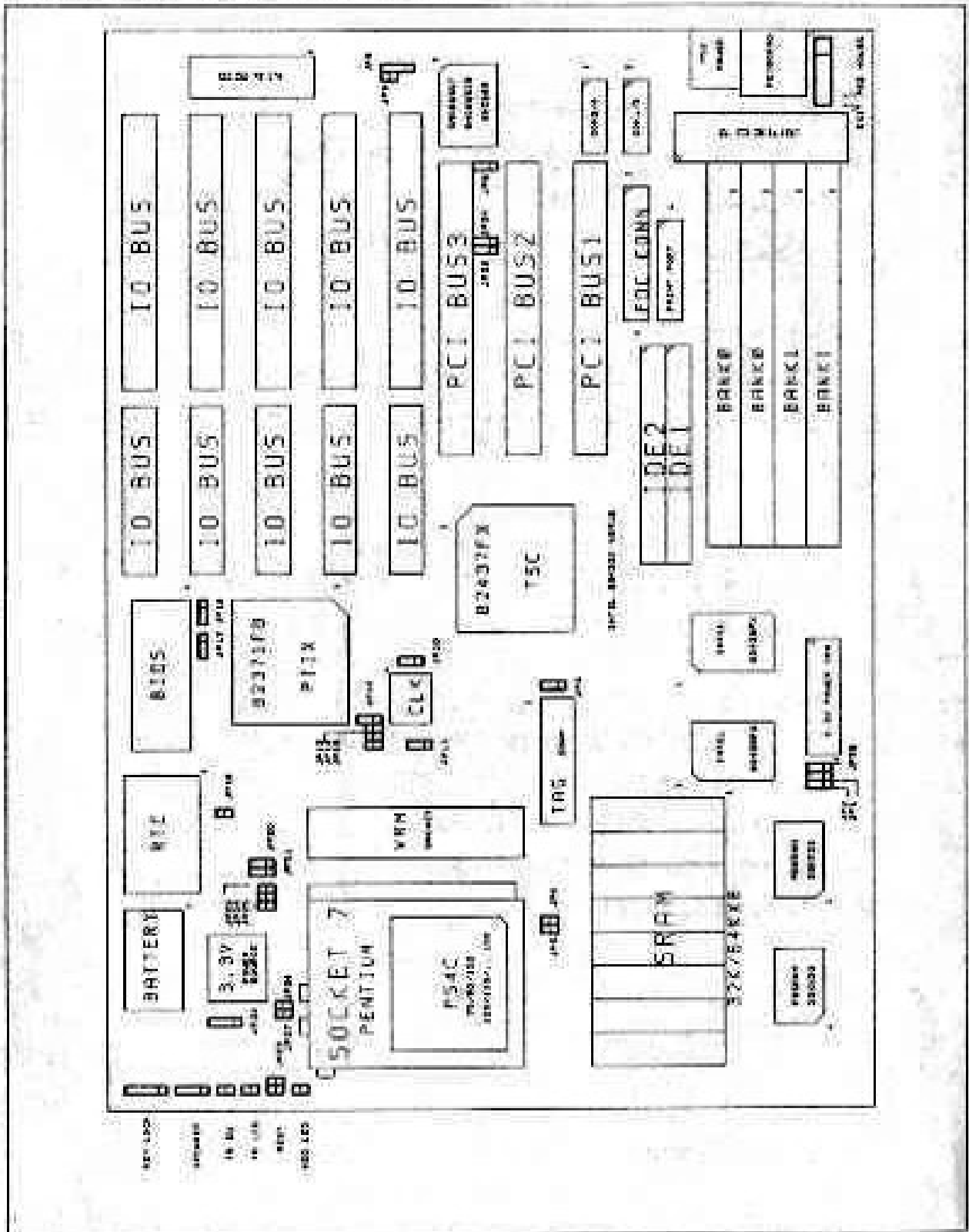
**BIOS:**

AWARD BIOS

Support "plug and play" function

# CHAPTER 2.

## Hardware Configuration & Jumper Layout



## CHAPTER 3.

### JUMPER SETTING

#### 1. Clock Select

CLOCK FREQUENCY	50MHZ	60MHZ	66MHZ
JP13	ON	ON	ON
JP14	OFF	OFF	ON
JP15	OFF	ON	ON
CPU TYPE	Pentium 75MHZ M16X86 100MHZ AMD5K 75MHZ	Pentium 90MHZ Pentium 120MHZ Pentium 150MHZ Pentium 180MHZ M16X86 120MHZ	Pentium 100MHZ Pentium 133MHZ Pentium 166MHZ Pentium 200MHZ

IF You want to use Pentium 120/133 MHZ, please reference JP25, JP29 setting.

#### 2. Bus Frequency

JP29	JP25	CPU-TO-BUS CLOCK	
OFF	OFF	3/2 (X1.5 default)	(for AMD5186-P75)
OFF	ON	2/1 (X2)	for pentium 120/133 M16X86 100/120
ON	ON	5/2 (X2.5)	for pentium 150/166
ON	OFF	3/1 (X3)	for pentium 180/200

The CPU-to-BUS frequency ratio is defined by bus frequency.

#### 3. Cache Memory Configuration

L2 CACHE SIZE	256K	512K	PBSRAM
JP3	2-3	1-2	2-3
JP20	1-2	2-3	1-2
JP21	1-2	2-3	1-2
TAG size (U20)	8K * 8 16K * 8 32K * 8	16K * 8 32K * 8	8K * 8 16K * 8 32K * 8

\*PBSRAM .Pipelined Burst SRAM

#### 4. CPU Internal Cache Control

L1 CACHE	W/T (WRITE THROUGH)	W/B (WRITE BACK)
JP23	ON	OFF (default)

#### 5. CPU NA# (Next Address)

PIPE LINE	DISABLE	ENABLE
JP24	OFF	ON (default)

#### 6 VR/VRE Voltage Spec.

JP32	CPU VLOTAGE
1-2 3-4	3.3 V (default)
1-2	3.45V
ALL OFF	3.6 V

NOTE: Standard Spec is 3.135 - 3.465V

VR Spec is 3.300 - 3.465V

VRE Spec is 3.450 - 3.600V

Please reference INTEL Pentium Processor spec.

#### 7 BIOS Option

TYPE	JP16	JP17
EPROM	1-2	1-2
5V FLASH ROM	1-2	2-3
12V FLASH ROM	2-3	2-3

#### 8. AT Bus Clock Select.

JP 12	AT CLOCK
1-2	PCI CLOCK/3
2-3 (default)	PCI CLOCK/4

#### 9. I/O Jumper Setting

ON BOARD I/O CHIPSET FUNCTION	ENABLE	DISABLE
JP6	1-2	2-3

## 10. Other Jumper Setting

JUMPER	SETTING	FUNCTION
TW LED		Turbo LED
HDD LED		Hard disk detect LED
RESET		Reset switch
SPEAKER		Speaker connector
KEY LOCK		Keyboard lock
JP10	1-2 (default)	CPU & SYSTEM CLK-PCI CLK X 2
	2-3	CPU & SYSTEM CLK-PCI CLK
J11		External battery connector
JP18	Break function	Connect to case turbo push button as a triggler switch (on then off), switch that system go into green mode immediately by hardware
JP11	1-2 (default)	CPU clock voltage 5 V
	2-3	CPU clock Voltage 3.3 V
JP9	on	For DALLAS CMOS DATA clear
JP30	2-3	For RTC power pin
JP31	on	JP30 (off) first and JP31 (on) then clear RTC CMOS data
J1		External PS2 mouse connector
JP4, JP5 JP26, JP27	on (default)	For P54C CPU voltage
	off	For P55CT CPU with VRM module
JP1, JP2	1-2 (default)	SRAM 5V voltage
	2-3	SRAM 3.3V voltage
JP35	1-2 (default)	ASYNC SRAM
	2-3	PBSRAM Board



## CHAPTER 4.

### BIOS CMOS SETUP

ROM PCI/ISA BIOS  
CMOS SETUP UTILITY  
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP BIOS FEATURES SETUP CHIPSET FEATURES SETUP POWER MANAGEMENT SETUP PCI CONFIGURATION SETUP LOAD BIOS DEFAULTS LOAD SETUP DEFAULTS	PASSWORD SETTING IDE HDD AUTO DETECTION HDD LOW LEVEL FORMAT SAVE & EXIT SETUP EXIT WITHOUT SAVING
ESC : Quit	↑ ↓ ← → : Select Item
F10 : Save & Exit Setup	(Shift) F2 : Change Color
Time, Date, Hard Disk Type	

### 1. STANDARD CMOS SETUP

ROM PCI/ISA BIOS  
STANDARD CMOS SETUP UTILITY  
AWARD SOFTWARE, INC.

Date(mm:dd:yy) : Wed , Jun 1, 1995						
Time(hh:mm:ss) : 00 : 00 : 00						
<b>HARD DISK</b>						
-----						
Primary Master : 00er (428MB)	899 15 65535 808 62 NORMAL					
Primary Slave : None ( 0MB)						
Secondary Master : None ( 0MB)						
Secondary Slave : None ( 0MB)						
Drive A : 1.2M , 5.25 in						
Drive B : 1.44M , 3.5 in						
Video : EGA/VGA						
Halt on : All Errors						
<table border="1" style="margin-left: auto; margin-right: auto;"><tr><td>Base Memory : 640K</td></tr><tr><td>Extended Memory : 15360K</td></tr><tr><td>Other Memory : 384K</td></tr><tr><td>-----</td></tr><tr><td>Total Memory : 16384K</td></tr></table>		Base Memory : 640K	Extended Memory : 15360K	Other Memory : 384K	-----	Total Memory : 16384K
Base Memory : 640K						
Extended Memory : 15360K						
Other Memory : 384K						
-----						
Total Memory : 16384K						
ESC : Quit	↑ ↓ ← → : Select Item	PU/PD/+/- : Modify				
F1 : Help	(Shift) F2 : Change Color					



### 3. CHIPSET FEATURES SETUP

ROM PCI/ISA BIOS  
 CHIPSET FEATURES SETUP  
 AWARD SOFTWARE, INC.

DRAM RAS# Precharge Time : 4	Onboard PDD Controller : Enabled
DRAM R/W Leadoff Time : 8/6	Onboard Serial Port 1 : COM1
DRAM RAS TO CAS Delay : 3	Onboard Serial Port 2 : COM2
DRAM Read Burst Timing : X2222	Onboard Parallel Port : 378H
DRAM Write Burst Timing : X3333	Parallel Port Mode : Normal
System BIOS Cacheable : Disabled	
Video BIOS Cacheable : Disabled	
Memory Hole At 15M-16M : Disabled	
IDE HDD Blank Mode : Enabled	
IDE Primary Master PIO : Auto	
IDE Primary Slave PIO : Auto	
IDE Secondary Master PIO : Auto	
IDE Secondary Slave PIO : Auto	
On-Chip Primary PCI IDE : Enabled	
On-Chip Secondary PCI IDE : Enabled	
PCI Slot IDE 2nd Channel : Enabled	

ESC:Quit    ↑ ↓ → ← :Select Item  
 F1:Help    PU/PD/+/- :Modify  
 F5:Old Values (Shift)F2:Color  
 F6:Load BIOS Defaults  
 F7:Load Setup Defaults

DRAM RAS# Precharge Time [The DRAM Precharge time by RAS.]

*RAS = Row address strobe* : 3 *45ns*  
*CAS = Column address strobe* : 4 (default) *60ns*

DRAM R/W Leadoff Time [The DRAM leadoff timing for page/row miss cycles Controls the MA setup to the first CAS# assertion.]

*105/75 ns*  
*120/90 ns*  
 : 7/5  
 : 8/6 (default)

DRAM RAS TO CAS Delay [Control the DRAM page miss and row miss leadoff timing.]

: 2 *30ns*  
 : 3 (default) *45ns*

DRAM Read Burst Timing [The timing used depends on the type of DRAM on a per-basis. The DRAM read burst timing are controlled by register.]

*at 66MHz bus*  
*30ns* ← : X2222 (default)  
*45ns* : X3333  
*60ns* : X4444

DRAM Write Burst Timing [Slower rate may be required in certain system designs to support layout with longer trace length or slower DRAM. The DRAM write burst timing are controlled by register.]

: X2222

	<ul style="list-style-type: none"> <li>: X3333 (default)</li> <li>: X4444</li> </ul>	
System BIOS Cacheable	[Define whether system BIOS area cacheable or not.] <ul style="list-style-type: none"> <li>: Enabled</li> <li>: Disabled (default)</li> </ul>	
Video BIOS Cacheable	[Define whether video BIOS area cacheable or not.] <ul style="list-style-type: none"> <li>: Enabled</li> <li>: Disabled (default)</li> </ul>	
Memory Hole AT 15M-16M	[This field enable a memory hole in main memory space. CPU cycles matching an enabled hold are passed on to PCI. Note that a selected hole is not remapped. Note this field should not be changed while the L2 cache is enable.] <ul style="list-style-type: none"> <li>: Enabled</li> <li>: Disable (default)</li> </ul>	hd ⊗
IDE HDD Block Mode	[This feature enhance hard disk performance by making multi sector transfer, instead of one sector per transfer. Most IDE drivers, except very early designs, can use this feature.] <ul style="list-style-type: none"> <li>: Enabled (default)</li> <li>: Disabled</li> </ul>	s ⊗ p ⊗ ⊗
IDE Primary Master PIO	[Detect your Primary Master hard disk device.] <ul style="list-style-type: none"> <li>: AUTO (default)</li> <li>: Mode 0,1,2,3,4</li> </ul>	⊗
IDE Primary Slave PIO	[Detect your Primary Slave hard disk device.] <ul style="list-style-type: none"> <li>: AUTO (default)</li> <li>: Mode 0,1,2,3,4</li> </ul>	
IDE Secondary Master PIO	[Detect your Secondary Master hard disk device.] <ul style="list-style-type: none"> <li>: AUTO (default)</li> <li>: Mode 0,1,2,3,4</li> </ul>	⊗
IDE Secondary Slave PIO	[Detect your Secondary Slave hard disk device.] <ul style="list-style-type: none"> <li>: AUTO (default)</li> <li>: Mode 0,1,2,3,4</li> </ul>	⊗

**On-Chip Primary PCI IDE** [Select use Chip support Primary PCI IDE.]  
 : Enabled (default)  
 : Disabled

**On-Chip Secondary PCI IDE** [Select use Chip support Secondary PCI IDE.]  
 : Enabled (default)  
 : Disabled

**PCI slot IDE 2nd Channel** [Use external IDE. AS ISA IDE or PCI IDE.]  
 : Enabled (default)  
 : Disabled

**On-board FDD Controller** : Enabled (default)  
 : Disabled

**On-board Serial Port 1** : COM1 (default)  
 : COM2  
 : COM3  
 : COM4  
 : Disabled

**On-board Serial Port 2** : COM1  
 : COM2 (default)  
 : COM3  
 : COM4  
 : Disabled

**On-board Parallel Port** : 378H (default)  
 : 278H  
 : 3BCH  
 : Disabled

**On-board Parallel Mode** : Normal (default)  
 : EPP  
 : ECP  
 : ECP+EPP

#### 4. POWER MANAGEMENT SETUP

ROM PC/ISA BIOS  
POWER MANAGEMENT SETUP  
AWARD SOFTWARE, INC.

Power Management	:User define	IPQ3 (COM2)	:On
PM Control by APM	:Yes	IPQ4 (COM1)	:On
Video off Method	:Blank Screen	IPQ5 (LPT2)	:On
Doze Mode	:5 min.	IPQ6 (Floppy Disk)	:On
Standby Mode	:1 min.	IPQ7 (LPT1)	:On
Suspend Mode	:1 min.	IPQ8 (RTC Alarm)	:Off
HDD Power Down	:Disabled	IPQ9 (IRQ2 Redir)	:On
IRQ3 (Wake-up Event)	:On	IPQ10 (Reserved)	:On
IRQ4 (Wake-up Event)	:On	IPQ11 (Reserved)	:On
IRQ5 (Wake-up Event)	:On	IPQ12 (PS/2 Mouse)	:On
IRQ12 (Wake-up Event)	:On	IPQ13 (Coprocessor)	:On
		IPQ14 (Hard Disk)	:On
		IPQ15 (Reserved)	:On
Power Down Activities		ESC:Quit      ↑ ↓ → ← :Select Item	
-----		F1 :Help      PU/PD/+/- :Modifs	
COM Port Accessed	:On	F5 :Old Values (Shift)F2 :Color	
LPT Port Accessed	:On	F8 :Load BIOS Defaults	
Drive Port Accessed	:On	P7 :Load Setup Defaults	

#### POWER MANAGEMENT:

- Disable : Global Power Management will be disabled.
- User Define: Users can configure their own power management.
- Min.Saving : Pre-define timer value are used such that all timers are in their MAX.value.
- Max.Saving : Pre-define timer value are used such that all timers are in their MIN.value.

#### PM Control by APM :

- No : System BIOS will ignore APM.
- Yes: System BIOS will wait for APM's prompt before it enter any PM mode, e.g. DOZE, STANDBY or SUSPEND.

- \*\*\*\* NOTE \*\*\*\*
1. If APM is installed, & if there is a task running, even the timer is time out, the APM will not prompt the BIOS to put the system into any power saving mode!
  2. If APM is not installed, this option has no effect.

Video Off Method :  
 Blank Screen : The system BIOS will only blank off the screen when disabled.

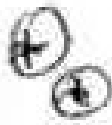
V/H SYNC+Blank : BIOS will also turn off the V/H SYNC signal from VGA card to monitor.

DPMS : Display Power Management by VGA card support.

Doze Mode : disabled , 1 Min --- 1 Hour  
 Standby Mode : disabled , 1 Min --- 1 Hour  
 Suspend Mode : disabled , 1 Min --- 1 Hour  
 HDD Power Down : disabled , 1 Min --- 15 Min

Wake-up Event : To IRQ3, IRQ4 , IRQ8 , IRQ12 check point.  
 Any activity. The system will wake up.

Power down Activities : To COM ports, LPT ports and Drive ports  
 IRQ3.....IRQ15 check point Then Into Green function.



## 5. PCI CONFIGURATION SETUP

ROM PCI/ISA BIOS  
PCI CONFIGURATION SETUP  
AWARD SOFTWARE, INC.

PnP BIOS Auto Config	: Disabled	
Slot 1 Using INT#	: Auto	
Slot 2 Using INT#	: Auto	
Slot 3 Using INT#	: Auto	
1st Available IRQ	: 10	
2nd Available IRQ	: 11	
3rd Available IRQ	: 9	
4th Available IRQ	: 12	
PCI IRQ Activated By	: Level	ESC:Quit      ↑ ↓ → ← :Select Item
PCI IDE Map To	: PCI-Auto	F1 :Help      PII/PD/+/- :Modify
Primary IDE INT#	: A	F5 :Old Values (Shift)F2 :Color
Secondary IDE INT#	: B	F6 :Load BIOS Defaults
		F7 :Load Setup Defaults

Slot (1-3) Using Int# : Auto (A, B, C, D)  
(1-4) Available IRQ : ( NA, 3, 4, 5, 7, 9, 10, 11, 12, 13, 14, 15)  
PCI IRQ Activated By : Level  
PCI IDE IRQ Map To : PCI-AUTO (PCI-SLOT 1,2,3)  
Primary IDE INT# : A ( B, C, D)  
Secondary IDE INT# : B ( B, C, D)

PCI Slots routing method :  
PCI 1: A, B, C, D  
PCI 2: B, C, D, A  
PCI 3: C, D, A, B

## 6. LOAD BIOS DEFAULTS

"LOAD BIOS DEFAULTS" loads default values permanently recorded in the BIOS ROM. If the stored record created by the Setup Utility becomes corrupted (and therefore unusable), these defaults will load automatically when you turn on the computer. These settings are non-optimal and turn off all high performance features. This is useful if you are having problems with your mainboard and need to debug or trouble shooting the source.

The defaults loaded only affect the BIOS Features Setup and Chipset Features Setup screens. There is no effect on the Standard CMOS Setup. To use this feature, highlight it on the main screen and press <Enter>. A line will appear on screen asking if you want to load the BIOS default values. Press the <Y> key and then press the <Enter> key. The BIOS defaults will then load. Press <N> if you don't want to process.



## **7. LOAD SETUP DEFAULTS**

"LOAD SETUP DEFAULTS" loads optimized settings which are stored in the BIOS ROM.

The auto-configured settings only affect the BIOS Feature Setup and Chipset Features Setup screens. There is no effect on the Standard CMOS Setup. To use this feature, highlight it on the main screen and press the <Enter> key. A line will appear on screen asking if you want to load the Setup default values. Press the <Y> key and then press the <Enter> key. The Setup defaults will then load. Press <N> if you don't want to process.

## **8.PASSWORD SETTING**

The "PASSWORD SETTING" utility sets the password. The mainboard may be shipped with the default password "award", or with the password disabled. If you want to change the password, you must first enter the current password ("award" in this case). Then at the prompt, type your new password. The password is case sensitive and you can use up to 8 alphanumeric characters. Press <Enter> after the password. At the next prompt, confirm the new password by typing it and pressing <Enter> again. When you're done, the screen automatically reverts to the main screen. Remember, When you use this feature, the "Security Option" line in BIOS FEATURES SETUP will determine whether the password will be required.

To disable the password, press the <Enter> key instead of entering a new password when the "Enter Password" dialog box appears. A message will appear confirming that the password is disabled. You may receive your mainboard set up this way.