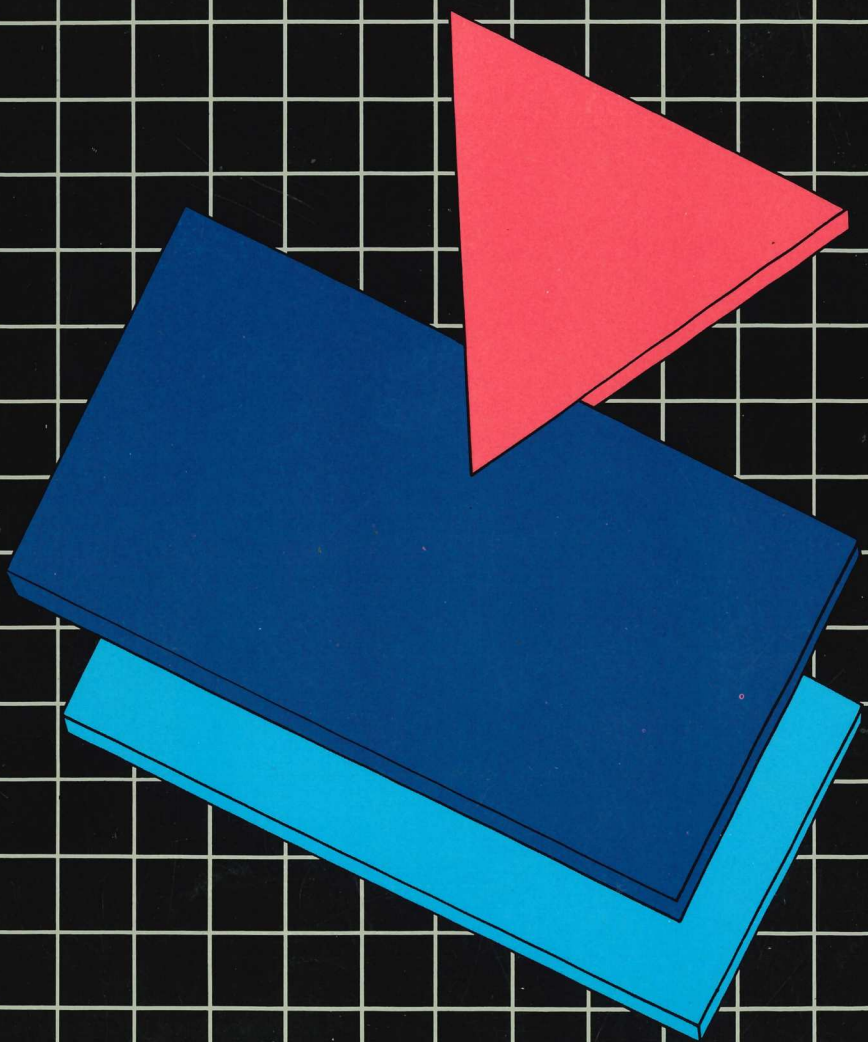
386SX



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CHAPTER 1
THE SYSTEM INFORMATION

1.1 SPECIFICATIONS:

- INTEL 16MHz 80386SX for 16MHz system operation. With 0/1 wait states for 100ns RAM-CHIPS
- Supports the INTEL 80387SX co-processor
- Page interleaved memory supports single bank page mode, and also 2 way and 4 way page interleaved mode.
- Integrates Lotus-Intel-MicroSoft Expended Memory Specification (LIM EMS) memory controller on board, to support EMS 4.0.
- Support 1M Byte up to 8M Byte of RAM, on board.
- Support different Kinds of RAM CARD.
- System speed switchable by H/W, S/W and keyboard
- Light indicator for system speed
- Real time clock/calendar with CMOS RAM and backup battery

1.2 CHIPSET OVERVIEW

The system is designed for 16MHz operation. It is based on the AT system design, including the CS8221 P9 CHIPSet (TM) and provides complete support for the IBM PC/AT bus.

The CS8221 P9 CHIPSet (TM) consists of the 82C211 CPU/Bus controller, the 82C212 Page/ Interleave and EMS Memory controller, the 82C215 Data/Address buffer and the 82C206 Integrated Peripherals Controller (IPC).

The P9 CHIPSet (TM) supports the local CPU bus, a 16 bit system memory bus, and the AT buses as shown in the P9 System Block Diagram. The 82C211 provides synchronization and control signals for all buses. The 82C211 also provides an independent AT bus clock and allows for dynamic selection between the processor clock and the user selectable At bus clock. Command delays and wait states are software configurable, providing flexibility for slow or fast peripheral boards.

The 82C212 Page/Interleave and EMS Memory controller provides an interleaved memory sub-system design with page mode operation. It supports up to 8MB of on-board DRAM with combinations of 64Kbit, 256Kbit and 1MBit DRAMs. The processor can operate at 16MHz with 0.5-0.7 wait state memory accesses, using 100 ns DRAMs. This is possible through the Page Interleaved memory scheme. The Shadow RAM feature allows faster execution of code stored in EPROM. By down loading code from EPROM to RAM. The RAM then shadows the EPROM for futher code execution. In a DOS environment, memory above 1Mb can be treated as LIM EMS memory.

The 82C215 Data/Address buffer provides the buffering and latching between the local CPU address bus and the Peripheral address bus. It also provides buffering between the local CPU data bus and the memory data bus. The parity bit generation and error detection logic resides in the 82C215.

CHAPTER 2
CONNECTORS AND JUMPER SETTINGS:

(SEE APPENDIX G FOR LOCATIONS , PAGE 57~59)

JP1 — HARD WARE RESET [RESET]

PIN	FUNCTION
1	POWER GOOD SIGNAL
2	GROUND

JP2 — POWER LED & KEY LOCK CONNECTOR [KEY-LOCK]

PIN	FUNCTION
1	POWER LED
2	—
3	GROUND
4	KEYLOCK
5	GROUND

JP3 — SPEAKER CONNECTOR [SPEAKER]

PIN	FUNCTION
1	SPEAKER SIGNAL
2	—
3	GROUND
4	+5V

JP4 — TURBO SWITCH [TURBO-SW]

PIN	FUNCTION
SHORT:	TURBO MODE
OPEN:	NORMAL MODE

JP5 — TURBO LED CONNECT [TURBO-LED]

PIN	FUNCTION
1	+5V
2	GROUND

JP6 — EXTERNAL BATTERY CONNECTOR [EXT-BAT]
*USE INTERNAL BATTERY 2,3 PIN HAVE TO BE SHORTED

PIN	FUNCTION
1	BATTERY +6V DC
2	—
3	—
4	GROUND

JP7 — BATTERY SELECT (BAT-SEL)

1, 2 PIN SHORT FOR USING EXTERNAL BATTERY (6V)
2, 3 PIN SHORT FOR USING INTERNAL BATTERY (3.6V)

JP8 — 80387SX CLOCK MODE (N9CLK)

OPEN: FASTER 387 SPEED (SYNC MODE)
SHORT: NORMAL 387 SPEED (ASYNC MODE)

JP9 — 80387SX ENABLE/DISABLE (N9 SELECT)
OPEN: 80387SX ENABLE
SHORT: 80387SX DISABLE

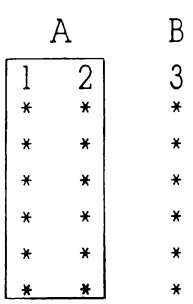
JP10 — ENABLE PIPELINE FOR 80386SX (PIPE LINE)

SHOULD BE SHORTED (JUMPERED)

JP11 — DISPLAY TYPE SELECT (COLOR/MONO)

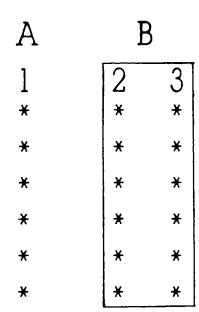
OPEN: MONOCHROME DISPLAY
SHORT: COLOR DISPLAY

JP12 — A/B JUMPERS (SELECT A/B JUMPERS FOR RAM INSTALLATION)



SELECT A JUMPERS

USE DIP RAM ON BANK 0/1, AS LO-BANK.
AND RAM MODULE ON BANK 2/3, AS HI-BANK.



SELECT B JUMPERS

USE DIP RAM ON BANK 0/1, AS LO-BANK.
OR RAM MODULE ON BANK 0/1, AS LO-BANK.

KB — KEYBOARD CONNECTOR

PIN	FUNCTION
1	KEYBOARD CLOCK
2	KEYBOARD DATA
3	—
4	GROUND
5	+5V

PS1/PS2 — SWITCHING POWER SUPPLY CONNECTOR

PIN	FUNCTION
1	POWER GOOD
2	+5V
3	+12V
4	−12V
5	GROUND
6	GROUND
1	GROUND
2	GROUND
3	−5V
4	+5V
5	+5V
6	+5V

CHAPTER 3
INSTALLATION MEMORY AND CO-PROCESSOR

3.1 HOW TO INSTALL THE CO-PROCESSOR

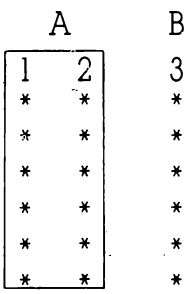
The motherboard has one PLCC carrier for an 80387SX co-processor, The 80387SX can be operated under two modes, synchronous or asynchronous mode.

When the 80387SX has installed, JP8 (N9 SELECT) MUST BE OPENED. And you can use the JP9 (N9 clock) to select the operating mode, synchronous or asynchronous mode. When using the synchronous mode, the co-processor is running with the 80386SX CPU clock, otherwise using the asynchronous mode, the co-procerssor is running under 16 MHz.

3.2 HOW TO INSTALL MEMORY (SEE APPENDIX G ON PAGE 58, 59)

The motherboard supports two kinds of memory: DIP socket on memory card and SIP socket on motherboard. it can configure 512K Byte upto 8M Byte memory.
The possible configurations of memory are listed as below.

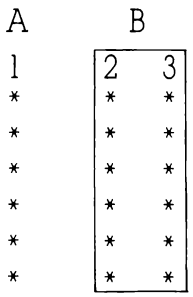
A/B JUMPERS (SELECT A/B JUMPERS FOR RAM INSTALLATION)



SELECT A JUMPERS

USE DIP RAM ON BANK 0/1, AS LO-BANK.
AND RAM MODULE ON BANK 2/3, AS HI-BANK.

	(DIP RAM)		(RAM MODULE)		
	BANK 0	BANK 1	BANK 2	BANK 3	TOTAL SIZE
1.	41256	0	0	0	512K
2.	41256	4164	0	0	640K
3.	41256	41256	0	0	1M
4.	41256	41256	41256	0	1.5M
5.	41256	4164	41256	41256	1.64M
6.	41256	41256	41256	41256	2M
7.	411000	0	0	0	2M
8.	41256	41256	411000	0	3M
9.	411000	411000	0	0	4M
10.	41256	4164	411000	411000	4.64M
11.	41256	41256	411000	411000	5M
12.	411000	411000	411000	0	6M
13.	411000	411000	411000	411000	8M



SELECT B JUMPERS

USE DIP RAM ON BANK 0/1, AS LO-BANK.
OR RAM MODULE ON BANK 0/1, AS LO-BANK.

	(DIP RAM OR RAM MODULE)		
	BANK 0	BANK 1	TOTAL SIZE
1.	41256	0	512K
2.	41256	4164	640K
3.	41256	41256	1M
4.	411000	0	2M
5.	411000	411000	4M

CHAPTER 4
STANDARD CMOS SETUP

STARTING UP THE SYSTEM

Power up the system and wait for the system to show up the system activity on the screen.

MEMORY TEST BYPASS

The system performs diagnostics of the system and displays the size of the memory being tested.

Note that you can bypass the memory test by pressing the <ESC> key. This option would be quite useful when the memory on the system is quite large. You should hit the <ESC> Key When the message **press<ESC>KEY to by pass MEMORY test** appears on the screen.

SELECT THE SETUP

Immediately after the memory and cache test, you will get the following prompt on the screen:

Press <Del> key to run SETUP/EXTD-SET

If you hit <DEL> key to the following message, it appears on the screen:

EXIT FOR BOOT.
→ STAND-SETUP
EXTD-SETUP
Use "↓", "↑" arrow key to choose "STAND-SETUP."
then you can set the CMOS data.

STANDARD CMOS SETUP

Time/Date Setup

Move the cursor using the arrow keys to the date field. At the bottom of the screen you will see:

Month: Jan, Feb, ...Dec.
Date: 01, 02, 03,.....31
Year: 1901, 1902,.....2099

Use the PgUp & PgDn keys to adjust each entry in the field. Move the cursor to the time field and you will see at the bottom of the screen:

Time is 24 hour format:—
Hour: (00-23), Minute: (00-59), Second: (00-59)
(1:30 AM=01:30:00), (1:30 PM=13:30:00)

Use the PgUp & PgDn Keys to correct the time.

DISKETTE DRIVE SETUP

Move the cursor to the diskette drive field and you will see at the bottom of the screen:

Options are: —
360 KB 5¼", 1.2 MB 5¼",
720 KB 3½", 1.44 MB 3½", Not Installed

Use the PgUp & PgDn Keys to select the desived drive type, N.B. The BIOS will automatically detect the presence of a 40 track 360K Disketle Drive, however, you must select the correct drive type for 80 track drives.

FIXED DRIVE SETUP: (See Appendix F for alisting)

Move the cursor to the Fixed Drive field and at the bottom of the screen you will see:

FIXED type=01,.....46, USER defined type = 47,
For type 47 Enter: Cyln, Head, Wpcom, Lzone, Sec,
(Wpcom is 0 for ALL, 65535 for NONE)

Use the PgUp & PgDn Keys to select one Drive Type (1-46) which matches the Parameters of the Fixed Drive installed.
If no Drive is fitted select "Not Installed" (type 0),

N.B. It is essential that the correct number of Heads and Cylinders is chosen with the Drive type to match the parameters of the installed Drive. Failure to do so may cause improper operation or damage to the Drive.

DISPLAY KEYBOARD SETUP

Move the cursor to the Display Adapter field and select one option from the list at the bottom of the screen, using the PgUp & PgDn keys.

Options are:—
Monochrome, Color 40x25,
VGA or EGA, Color 80x25, Not Installed

Then move the cursor to the keyboard field and select "Installed" using the PgUp or PgDn Keys.

SCRATCH PAD SETUP:

The Option after the keyboard field is the BIOS Scratch RAM area. It is recommended the "1" option be selected using the PgUp or PgDn Keys.

CHAPTER 5
EASY EXTENDED SETUP

THE EXTENDED SETUP FOR AMI BIOS

*** IMPORTANT ***

If a mistake is made during the altering of the extended setup and the motherboard will no tre-boot. Then press and hold the <INS> key while powr is re-applied. This will clear all of the setup.

Press the <DEL> key after the memory count-up after power-up or cold boot, or immeadiately after a warm boot, when this message appears:

Press <DEL> key to run SETUP/EXTD-SET

and answer <Y>es to the question:

Want to run SETUP/EXTD-SET (Y/N)? Y

from the setup main menu select the extended setup option.

Exit for boot
Stnd-setup
Extd-setup ◄———

use the cursor and <ENTER> keys to make the selection.

on the screen the extended setup menu will appear:

NEAT CHIPSET SETUP PROGRAM
MAIN MENU

EASY NEAT CHIPSET REGISTER SETUP ◄———
ADVANCED NEAT CHIPSET REGISTER SETUP
ENABLE/DISABLE VIDEO AND MAIN BIOS SHADOW
WRITE CMOS REGISTERS AND EXIT
DO NOT CHANGE CMOS AND EXIT

Choose the "Easy neat chipset register setup" option using the cursor and <ENTER> keys.

On the screen the easy setup menu will appear. This menu tabulates the major system setup topics. Moving the cursor to a topic and using the <PgUp> and <PgDn> keys will enable the settings to be modified.

MEMORY CONFIGURATION

BANK	ENABLE/DISABLE	DRAM TYPE	WAIT STATES
0	ENABLE	256K	0 WAIT STATE
1	ENABLE	256K	0 WAIT STATE
2	DISABLE	256K	0 WAIT STATE
3	DISABLE	256K	0 WAIT STATE

CLOCK SOURCE

PROCESSOR CLOCK	BUS CLOCK	DMA CLOCK
CLK2IN	ATCLK	SCLK/2

SHADOW RAM/INTERLEAVE

F0000H, 64K	C0000H, 16K	C4000H, 16K	INTERLEAVE
ENABLED	ENABLED	ENABLED	ENABLED
!MAIN BIOS!	!EGA/VGA BIOS!	!VGA BIOS!	

* These fields are the shadow bios' enables, they are not all essential but if enabled they can improve system performance over normal rom bios. Refer to the Appendix C on the shadow ram facility.

These are the recommended settings for 1 MB memory of 256K 100nS drams (16 MHz)

IF 1MB OF MEMORY IS INSTALLED THEN THE SETUP SCREEN SHOULD APPEAR LIKE THIS :

MEMORY CONFIGURATION

BANK	ENABLE/DISABLE	DRAM TYPE	WAIT STATES
0	ENABLE	256K	0 WAIT STATE
1	ENABLE	256K	0 WAIT STATE
2	DISABLE		0 WAIT STATE
3	DISABLE		0 WAIT STATE

CLOCK SOURCE

PROCESSOR CLOCK	BUS CLOCK	DMA CLOCK
CLK2IN	ATCLK	SCLK/2

SHADOW RAM/INTERLEAVE

F0000H, 64K	C0000H, 16K	C4000H, 16K	INTERLEAVE
ENABLED	ENABLED	ENABLED	ENABLED
!MAIN BIOS!	!EGA/VGA BIOS!	!VGA BIOS!	

* These fields are the shadow bios' enables, they are not all essential but if enabled they can improve system performance over normal rom bios. Refer to the Appendix C on the shadow ram facility.

These are the recommended settings for 1 MB memory of 256K 100nS drams (16 MHz)

NOTES: 1. These values can be changed by moving the cursor to the desired field and using the <PgUp>/<PgDn> keys to change the setting.
2. When finished setting use the <ESC> key to return to the main menu.
3. Move the cursor to the field: "Write cmos registers and exit" then press <ENTER>. This will save the settings and re-boot.
4. Re-enter the first setup menu using the <DEL> key after memory count-up. Then choose the standard setup and Re-Do the normal setup E.G. time/date/hard-disk/memory etc.

CHAPTER 6
SETTING THE SHADOW RAM

For an explanation of shadow ram mapping refer to appendix C

6.1 TO INSTALL THE SHADOW RAM FOLLOW THESE STEPS:

*** IMPORTANT ***

If a mistake is made during the altering of the extended setup and the motherboard will no re-boot. Then press and hold the <INS> key while powr is re-applied. This will clear all of the setup.

STEP 1: ENTER THE EXTENDED REGISTER SETUP

1. **Press the** <DEL> key after the memory count-up after power-up or cold boot, or immeadiately after a warm boot, when this message appears:

Press <DEL> key to run SETUP/EXTD-SET

Want to run SETUP/EXTD-SET (Y/N)? Y

and answer <Y>es to the question:

2. From the setup main menu select the extended setup option.

Exit for boot
Stnd-setup
Extd-setup ◄————

use the cursor and <ENTER> keys to make the selection.

3. On the screen the extended setup menu will appear:

NEAT CHIPSET SETUP PROGRAM
MAIN MENU

EASY NEAT CHIPSET REGISTER SETUP
ADVANCED NEAT CHIPSET REGISTER SETUP
ENABLE/DISABLE VIDEO AND MAIN BIOS SHADOW ◄————
WRITE CMOS REGISTERS AND EXIT
DO NOT CHANGE CMOS AND EXIT

Choose the "Easy neat chipset register setup" option using the cursor and <ENTER> keys.

4. On the screen you will see the option table:

SETUP SHADOW RAM FOR 212B	
SHADOW FOR MAIN BIOS RAM F0000H, 64K -> 1	<- SET TO "1"
SHADOW FOR VIDEO BIOS RAM C0000H, 16K -> 1	<- SET TO "1"
SHADOW FOR VIDEO BIOS RAM C4000H, 16K -> 1	<- SET TO "1"

SHADOW FOR ROM BIOX
1=SHADOW ENABLE
0=SHADOW DISABLE

Move the cursor through the fields and set to "1" by using the <PgUp> and <PgDn> keys.

5. When finished press the <ESC> key to return to the main setup menu.

* If you have 2MB dram installed then you may exit menu here to re-boot. Choose the "write cmos registers and exit" option from the menu.

* If you have 1MB total dram installed and you do not have any extended memory split or any ems memory then you may exit here to re-boot. Choose the "write cmos registers and exit" option from the menu.

* If you have 1MB dram installed and the high memory (384M), above the 640K base memory, is re-allocated as extended memory. Then you will have to de-allocate this extended memory so that it may be used as shadow ram.

STEP 2: DE-ALLOCATING EXTENDED MEMORY FOR 1MB ONLY DRAM (TOTAL) SYSTEMS

1. From the extended setup main menu choose the "advanced neat chipset register setup" option using the cursor and <ENTER> key.

2. On the screen the contents of the chipset registers will be displayed

```
                BITS:      7        —        0

82C211          60H ->     00   0 0 R 0 R 0
                61H ->     1 0 01   01    01
                62H ->     RR   11   11   00

82C212B         64H ->     0     01     RRRRR
                65H ->     0 0 0 0 1 1 1 0
                66H ->     1 0 0       RRRRR
                67H ->     0 0 0 0 0 0 0 0
                68H ->     0 0 0 0 0 0 0 0
                69H ->     0 0 0 0 0 0 0 0
                6AH ->     10    .1      RRRR
                6BH ->     1 0 0 0   10   11
                                 ↑    ↑
                                 |    └──────────── DISABLE EMS
                                 └──────────────── DE-ALLOCATE HIGH
                                                   MEMORY (384K)

                6CH ->     00     0  0  RRRR
                6DH ->     0100          0000
                6EH ->     00     00  00  00
                6FH ->     000   0 R   1 1 R

82C206          01  ->     11   00   00   0 0
```

The <PgUp> and <PgDn> keys will modify the register settings.

***** WARNING *****

Be careful not to accidently modify any other settings while moving the cursor through the registers.

Set this bit to "0" (no re-allocation) using the <PgUp> or <PgDn> keys.

3. Move the cursor to bit 4 of the same regisrter and disable any ems. Set bit 4 = "0"

4. Press teh <ESC> key to return to the main menu.

STEP 3: FINAL CHECK AND ALTER STANDARD SETUP.

1. Re-enter the shadow ram table to check the shadow ram settings. Then return to the extended setup main menu.

2. Save the register settings using the "write cmos registers and exit" option in the main menu.

3. The system will re-boot. When the memory count-up is complete press the <DEL> key after the memory count-up after power-up or cold boot, or immeadiately after a warm boot, when this message appears:

   Press <Del> key to run SETUP/EXIT-SET

   Want to run SETUP/EXTD-SET (Y/N)?

   and answer <Y>es to the question:

4. From the setup main menu select the standard setup option.

   Exit for boot
   Stnd-setup ◄————————
   Extd-setup

   Use the cursor and <ENTER> keys to make the selection.

5. Check the system memory configuration (IN THE UPPER RIGHT CORNER OF THE SCREEN). The setup should show 640K base memory and 0K extended memory. If not, exit and Re-Do the register setup.

CHAPTER 7
HOW TO SET THE EMS

7.1 TO USE THE P9 MOTHERBOARD EMS CAPABILITY FOLLOW THESE STEPS:

*** IMPORTANT ***

If a mistake is made during the altering of the extended setup and the motherboard will no re-boot. Then press and hold the <INS> key while powr is re-applied. This will clear all of the setup.

For 1MB dram total installed:

STEP 1: IF YOU HAVE THE SHADOW RAM ENABLED

1. **Press the** <DEL> key after the memory count-up after power-up or cold boot, or immeadiately after a warm boot, when this message appears:

   Press <DEL> key to run SETUP/EXTD-SET

   Want to run SETUP/EXTD-SET (Y/N)? Y

   and answer <Y>es to the question:

2. From the setup main menu select the extended setup option.

   Exit for boot
   Stnd-setup
   Extd-setup ◄————

   use the cursor and <ENTER> keys to make the selection.

3. On the screen the extended setup menu will appear:

NEAT CHIPSET SETUP PROGRAM
MAIN MENU

EASY NEAT CHIPSET REGISTER SETUP
ADVANCED NEAT CHIPSET REGISTER SETUP
ENABLE/DISABLE VIDEO AND MAIN BIOS SHADOW ◄————
WRITE CMOS REGISTERS AND EXIT
DO NOT CHANGE CMOS AND EXIT

Choose the "Easy neat chipset register setup" option using the cursor and <ENTER> keys.

4. On the screen you will see the option table:

SETUP SHADOW RAM FOR 212B	
SHADOW FOR MAIN BIOS RAM F0000H, 64K -> 1	<- SET TO "1"
SHADOW FOR VIDEO BIOS RAM C0000H, 16K -> 1	<- SET TO "1"
SHADOW FOR VIDEO BIOS RAM C4000H, 16K -> 1	<- SET TO "1"

SHADOW FOR ROM BIOX
1=SHADOW ENABLE
0=SHADOW DISABLE

Use the <PgUp>/<PgDn> key to disable all shadow ram mappings.

5. use the <ESC> key to return to the main menu.

STEP 2:

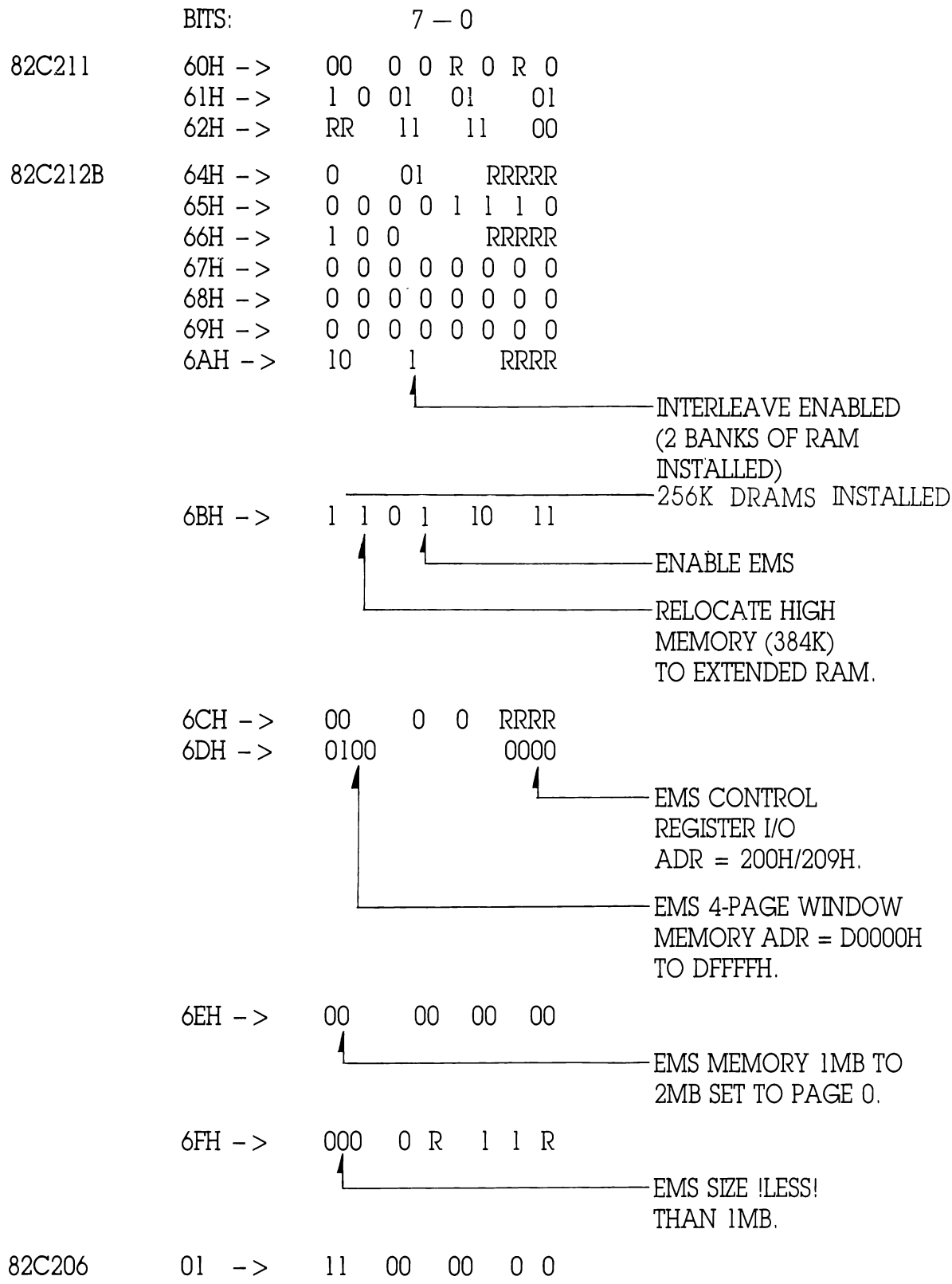
1. From the main menu of the extended setup choose the option:

NEAT CHIPSET SETUP PROGRAM
MAIN MENU

EASY NEAT CHIPSET REIGSTER SETUP
→ ADVANCED NEAT CHIPSET REGISTER SETUP
ENABLE/DIABLE VIDEO AND MAIN BIOS SHADOW
WRITE CMOS REGISTERS AND EXIT
DO NOT CHANGE CMOS AND EXIT

Choose the advanced neat chipset register setup using the cursor and <ENTER> keys.

2. On the screen you will see the register settings for the chips & technology chipset I.E. the 82C211, 82C212B and 82C206. Which should appear like this:



The <PgUp> and <PgDn> keys will modify the register settings.

*** WARNING ***

Be careful not to accidently modify any other settings while moving the cursor throught the registers.

3. Move the cursor to the register 6BH of the chip 82C212B. Enable relocation of the ram above 640K to the extended ram addres. Bit 6 = "1".

4. Move the cursor to bit 4 of the same register (6BH). Enable the ems conversion. Bit 4 = "1".

5. Move the cursor to bit 3 of the same register (6BH). Set the ems wait states to 2 waits. Bit 3 = "10".

6. Move the cursor to the register 6DH of the chip 82C212B. Set the ems base register address to D0000H, D4000H, D0000H, DC000H. Bits 7-4 are "0100"

7. Move the cursor to bit 3 - 0 of the same register (6BH). This is ems page reg I/O address it should be set to 200H/209h. Bits 3-0 are "0000".

*** WARNING ***

If any non-standard card or peripheral is installed which normally used the memory locations D000:000H to D000:FFFFH (D0000H page 64k space) or the I/O port address 200H or 209H. then:

1. You must cunsult the card/peripheral supplier to have the memory or I/O allocation changed.

or,

2. The bits of register 6DH can be changed to fix the ems controller with a more suitable location.

8. Move the cursor to register 6EH, the ems page addressing. Set ems page 0 to address the ems memory 1M to 2M. bits 7 & 6 = "00".

9. Move the cursor to register 6FH, bits 7-5 are the ems size register. Set the bits to "000" I.E. total less than 1MB installed.

10. Re-check the registers to ensure the correct settings have been done to the correct register bits.

11. Press the <ESC> key to return to the main menu and choose the option "write coms registers and exit" using the cursor and <ENTER> key. The system should re-boot.

STEP 3: RESETTING THE STANDARD SETUP

1. If you previously had the high 384K of ram (above the 640K base) re-allocated as extended memory then you will have to Re-Do the standard setup, in order to re-define the system memory configuration. It instead, you has the memory above the 640K base utilised as shadow ram, or not utilised at all, then re-entering the standard setup will not be necessary.

2. Re-boot the system. When the memory count-up is complete press the <DEL> key after the memory count-up after power-up or cold boot, or immeadiately after a warm boot, when this message appears:

   Press <Del> key to run SETUP/EXTD-SET

   Want to run SETUP/EXTD-SET (Y/N)? Y

   and answer <Y>es to the question:

3. From the setup main menu select the standard setup option.

   Exit for boot
   Stand-setup ◄————————
   Extd-setup

   use the cursor and <ENTER> keys to make the selection.

4. Check the system memory configuration (IN THE UPPER RIGHT CORNER OF THE SCREEN). The setup should show 640K base memory and 0K extended memory. If not, exit and Re-Do the register setup.

SET 4:

1. To use the ems one final step required is to install the ems software driver supplied on the diskette packaged with the motherboard. Remove this diskette and place in the diskette drive A:

2. Check to see if the file EMM.SYS is present on this diskette.

If you have a hard drive:

3. Copy the ems driver to the root directory of the hard drive:

   A: > COPY A: EMM.SYS C:

If you have only diskette drives:

4. Place the diskette containing the ems driver in drive B: (OR A: IF ONLY ONE DRIVE IS INSTALLED). If you have a boot diskette place it in drive A: Copy the driver to the boot diskette.

   B: >COPY B: EMM.SYS A:

NOW MOVE BACK TO THE BOOT DRIVE:

5. Create an entry into the Config.Sys file to cause dos to load the.driver on boot-up. From the root directory of the boot drive type:

   Copy con Config.Sys
   Device = EMM.SYS — D
   ^Z

   N.B.

   1. This will detroy any previous Config.Sys fle if one exists. To alter the contents of an existing Config.Sys to include the line "Device = Emm.SYS /D" use a line editor such as Edlin.Com (REFER DOS MANUAL FOR EXPLANATION OF OPERATION).

   2. ^Z represents depressing the control <Ctrl> and <Z> keys simultaneously.

6. If you require a non-standard memory or I/O address for the ems driver to avoid conflict with some other peripheral or card installed, then the ems driver can be set to different locations using software switches at the end of the line "device = EMM.SYS –D". Refer to the explanation note contained on the diskette which has the ems driver. This file named "EMM4xx.DOC" can be printed using the command.

   A:>TYPE A: EMM4XX.doc

   and use the <Pause> key to pause the display. <ENTER> key to restart.

7. When finished re-boot off the modified boot drive. The ems driver software will test the ems memory availble when loading, and display each available page on the screen. Should the driver report "no ems found" or "ems incorrectly installed" then the above procedure should be repeated to correctly set up the motherboard.

7.2 FOR 2MB DRAM TOTAL INSTALLED:

STEP 1:

1. Press the <DEL> key after the memory count-up after power-up or cold boot, or immeadiately after a warm boot, when this message appears:

   Press <Del> key to run SETUP/EXTD-SET

   Want to run SETUP/EXTD-SET (Y/n)? Y

   and answer <Y>es to the question:

2. From the setup main menu select the extended setup option.
   Exit for boot
   Stnd-setup
   Extd-setup

   use the cursor and <ENTER> keys to make the selection.

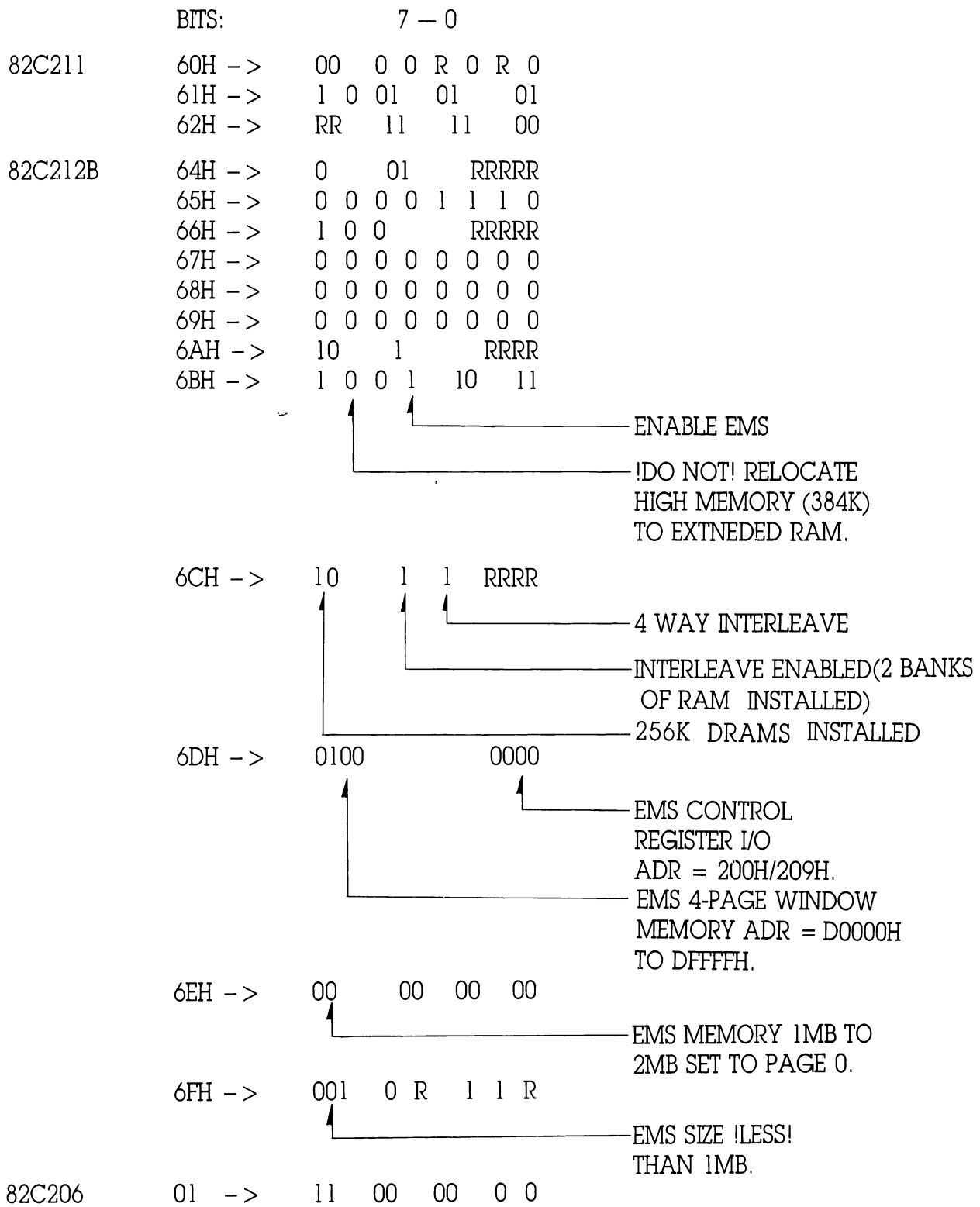
3. On the screen the extended setup menu will appear:

NEAT CHIPSET SETUP PROGRAM
MAIN MENU

EASY NEAT CHIPSET REGISTER SETUP
ADVANCED NEAT CHIPSET REGISTER SETUP ←
ENABLE/DISABLE VIDEO AND MAIN BIOS SHADOW
WRITE CMOS REGISTERS AND EXIT
DO NOT CHANGE CMOS AND EXIT

Choose the advanced neat chipset register setup using the cursor and <ENTER> keys.

4.On the screen you will see the register settings for the chips & technology chipset I.E. the 82C211, 82C212B and 82C206. Which should appear like this:



The <PgUp> and <PgDn> keys will modify the register settings.

*** WARNING ***

Be careful not to accidently modify any other settings while moving the cursor throught the registers.

5. Move the cursor to the register 6BH of the chip 82C212B. Enable relocation of the ram above 640K to the extended ram addres. Bit 6 = "1".

6. Move the cursor to bit 4 of the same register (6BH). Enable the ems conversion. Bit 4 = "1".

7. Move the cursor to bit 3 of the same register (6BH). Set the ems wait states to 2 waits. Bit 3 = "10".

8. Move the cursor to the register 6CH bit 5 and 4. Set both bits to "1" to enable 4-way interleaving plus page-mode addressing.

9. Move the cursor to the register 6DH of the chip 82C212 B. Set the ems base register address to D0000H, D4000H, D8000H, Dc000H. Bits 7-4 are "0100".

10. Move the cursor to bit 3-0 of the same register (6BH). This is ems page reg I/O address it should be set to 200H/20 9H. Bits 3-0 are "000".

*** WARNING ***

If any non-standard card or peripheral is installed which normally used the memory locations D000:000H to D000:FFFFH (D0000H page 64k space) or the I/O port address 200H or 209H. then:

1. You must cunsult the card/peripheral supplier to have the memory or I/O allocation changed.

or,

2. The bits of register 6DH can be changed to fix the ems controller with a more suitable location.

11. Move the cursor to register 6EH, the ems page addressing. Set ems page 0 to address the ems memory 1M to 2M. bits 7 & 6 = "00".

12. Move the cursor to register 6FH, bits 7-5 are the ems size register. Set the bits to "001" I.E. total less than 1MB installed.

13. Re-check the registers to ensure the correct settings have been done to the correct register bits.

14. Press the <ESC> key to return to the main menu and choose the option "write coms registers and exit" using the cursor and <ENTER> key. The system should re-boot.

STEP 2: RESETTING THE STANDARD SETUP

1. If you previously had the high 384K of ram (above the 640K base) re-allocated as extended memory then you will have to Re-Do the standard setup, in order to re-define the system memory configuration. It instead, you has the memory above the 640K base utilised as shadow ram, or not utilised at all, then re-entering the standard setup will not be necessary.

2. Re-boot the system. When the memory count-up is complete press the <DEL> key after the memory count-up after power-up or cold boot, or immeadiately after a warm boot, when this message appears:

   Press <Del> key to run SETUP/EXTD-SET

   Want to run SETUP/EXTD-SET (Y/N)? Y

   and answer <Y>es to the question:

3. From the setup main menu select the standard setup option.

   Exit for boot
   Stand-setup
   Extd-setup

   use the cursor and <ENTER> keys to make the selection.

4. Check the system memory configuration (IN THE UPPER RIGHT CORNER OF THE SCREEN). The setup should show 640K base memory and 0K extended memory. If not, exit and Re-Do the register setup.

SET 3:

1. To use the ems one final step required is to install the ems software driver supplied on the diskette packaged with the motherboard. Remove this diskette and place in the diskette drive A:

2. Check to see if the file EMM.SYS is present on this diskette.

If you have a hard drive:

3. Copy the ems driver to the root directory of the hard drive:

   A: > COPY A: EMM.SYS C:

If you have only diskette drives:

4. Place the diskette containing the ems driver in drive B: (OR A: IF ONLY ONE DRIVE IS INSTALLED). If you have a boot diskette place it in drive A: Copy the driver to the boot diskette.

```
B: >COPY B: EMM.SYS A:
```

NOW MOVE BACK TO THE BOOT DRIVE:

5. Create an entry into the Config.Sys file to cause dos to load the driver on boot-up. From the root directory of the boot drive type:

```
Copy con Config.Sys
Device = EMM.SYS — D
Z
```

N.B.

1. This will detroy any previous Config.Sys fle if one exists. To alter the contents of an existing Config.Sys to include the line "Device = Emm.SYS /D" use a line editor such as Edlin.Com (REFER DOS MANUAL FOR EXPLANATION OF OPERATION).

2. Z represents depressing the control <Ctrl> and <Z> keys simultaneously.

6. If you require a non-standard memory or I/O address for the ems driver to avoid conflict with some other peripheral or card installed, then the ems driver can be set to different locations using software switches at the end of the line "device = EMM.SYS –D". Refer to the explanation note contained on the diskette which has the ems driver. This file named "EMM4xx.DOC" can be printed using the command.

```
A:>TYPE A:  EMM4XX.doc
```

and use the <Pause> key to pause the display. <ENTER> key to restart.

7. When finished re-boot off the modified boot drive. The ems driver software will test the ems memory availble when loading, and display each available page on the screen. Should the driver report "no ems found" or "ems incorrectly installed" then the above procedure should be repeated to correctly set up the motherboard.

SPPENDIX A

P9 CHIPSET 82C211 CONFIGURATION REGISTERS

There are three bytes of configuration registers in the 82C211; RA0,RA1 and RA2. An indexing scheme is used to reduce the I/O ports required to access all the registers required for the P9 CHIPSET. Port 22H is used as an indexing register and Port 23H is used as the data register. The index value is placed in port 22H to access a particular register and the data to be read from or written to that register is located in port 23H. Every access to port 23H must be preceded by a write of the index value to port 22H, even if the same register data is being accessed again.
All bits marked as Reserved are set to zero by default and must be maintained that way during write operations.

P9 CHIPSET 82C212B CONFIGURATION REGISTERS3

There are twelve configuration and diagnostics registers in the 82C212, RB0-RB11. These are accessed through I/O ports 22H and 23H normally found in the interrupt controller module of the 82C206IPC. An indexing scheme is used to reduce the number of I/O addresses required to access all of the registers needed to configure and control the memory controller. Port 22H is used as an index register that points to the required data value accessed through port 23H. A write of the index value for the required data is performed to location 22H. This is then decoded and controls the multiplexers gating the appropriate register to the output bus. Every access to port 23H must be preceded by a write of the index value to port22H, even if the same data register is being accessed again. All bits marked as Reserved are set to zero by default and must be maintained that way during write operations.

All reserved bits are set to zero by default and when written to, must be set to zero. Table 1 lists the three registers:

Table 1. RA0, RA1, and RA2

Register Number	Register Name	Index
RA0	PROCCLK Selector	60H
RA1	Command Delay	61H
RA2	Wait State/BCLK Selector	62H

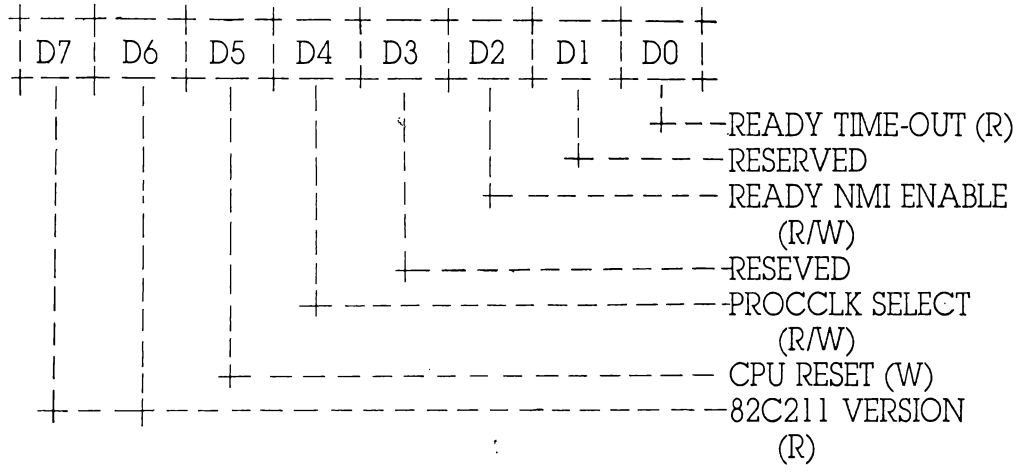
must be maintained that way during write operations. Table 3 lists these registers.

Table 3. RB0 to BR11 Registers

Register Number	Register Name	Index
RB0	Version	64H
RB1	ROM Configuration	65H
RB2	Memory Enable-1	66H
RB3	Memory Enable-2	67H
RB4	Memory Enable-3	68H
RB5	Memory Enable-4	69H
RB6	Bank 0/1 enable	6AH
RB7	DRAM Configuration	6BH
RB8	Bank 2/3 Enable	6CH
RB9	EMS Base Address	6DH
RB10	EMS Address Extesion	6EH
RB11	Miscellaneous	6FH

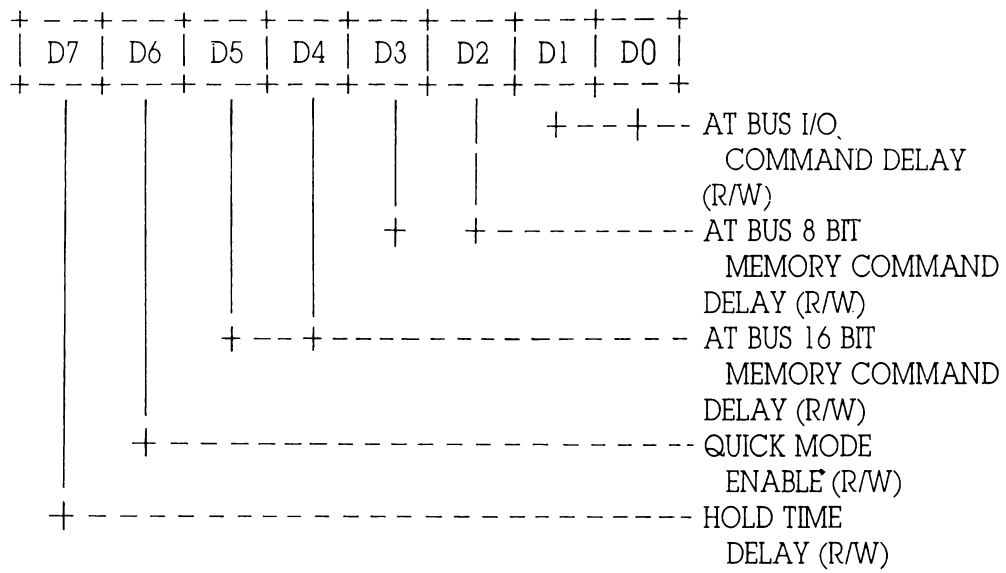
— Register Description

PROCCLK Register RA0
Index egister port: 22H
Data Register Port 23H
Index: **60H**



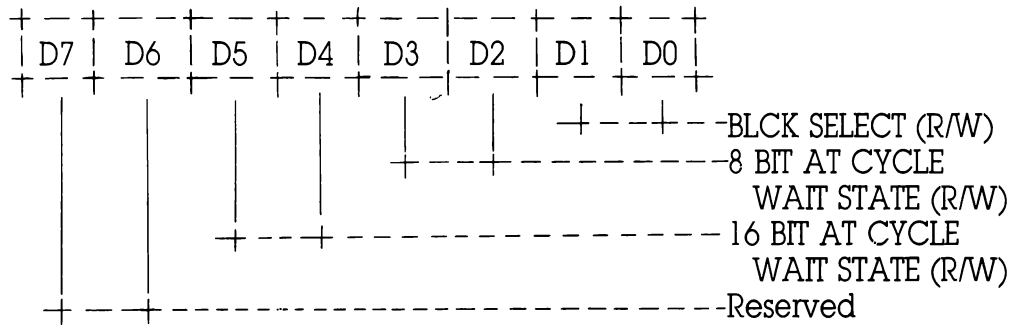
Bits	Function
7,6	72C211 revision number. 00 is the initial number.
5	Alternate CPU reset. A low to high transition in this bit activates a CPU reset. Once active, it remains active for 16 PROCCLK cycles and then goes low.
4	Processor clock select is by default set to zero and selects PROCCLK=CLK2IN. If high, is selects PROCCLK=BCLK. Prefered Setting=CLK 2IN
3	Reserved.
2	Local bus READY timeout NMI enable. A one enables the NMI and a zero disables it. Default is 0
1	Reserved.
0	Local bus READY TIMEOUT. A one indicates that READY timeout has occurred 128 PROCLK cycles after-AF16 has been asserted. A zero indicates that READY time out has not occured.

Command Delay Register RA1
Index register port: 22H
Data register port: 23H
Index: **61H**



Bits	Function
1, 0	AT Bus I/O cycle command delay. Specifies between 0 to 3 BCLK cycle command delays for AT I/O cycles. Default is 1.
3, 2	AT Bus 8 bit memory command delay. Specifies between 0 to 3 BCLK cycle command delay for 8 bit AT memory cycle. Default is 1.
5, 4	AT Bus 16 bit memory command delay. Specifies between 0 and 3 BCLK cycle command delays for 16 bit AT memory cycles. Default is 0.
6	Quick mode enable. A zero enables Quick mode a one disables it. Default is 1.
7	Address hold time delay. A one enables extra address bus hold time and a zero disables it. Default is 0.

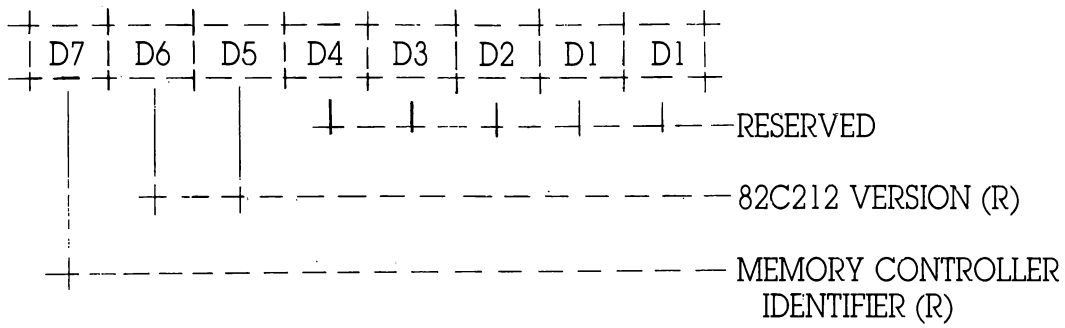
Wait States Register RA2
Index register port: 22H
Data register port: 23H
Index: **62H**



Bit	Function
1, 0	Bus clock (bclk) source select. Default is 00. 00 BLCK = CLK2IN/2 01 BCLK = CLK2IN 10 BCLK = ATCLK 11 Reserved
3, 2	8 BIT at cycle wait state generation. Default is 4 00 2 wait states 01 3 wait states 10 4 wait states 11 5 wait states
5, 4	16 bit at cycle wait state generation. Default is 1 00 0 wait states 01 1 wait state 10 2 wait states 11 3 wait states
7, 6	Reserved

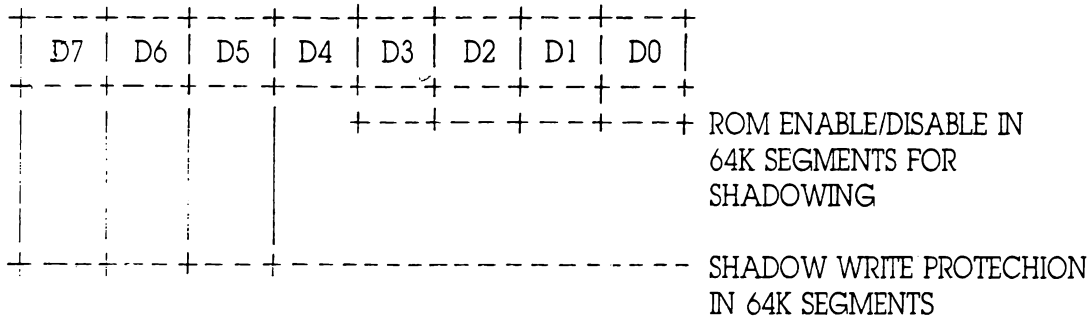
REGISTER DESCRIPTION

Version Register RB0
Index register port: 22H
Data register port: 23H
Index: **64H**



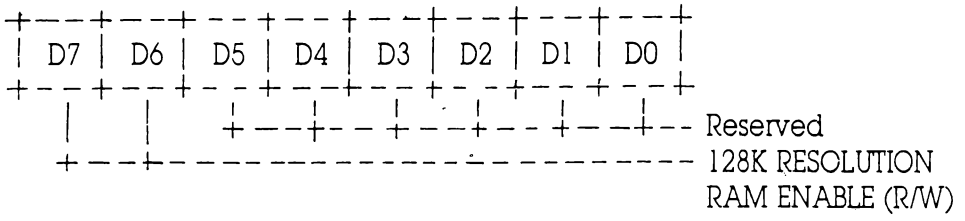
Bits	Function
7	NEAT memory controller indentifier. 0 = 72C212
6, 5	82C212 revision number. 00 = initial revision number, 01 = 'B' revision
4-0	Reserved

ROM configuration Register RB1
Index register port: 22H
Data register port: 23H (R/W)
Index: **65H**



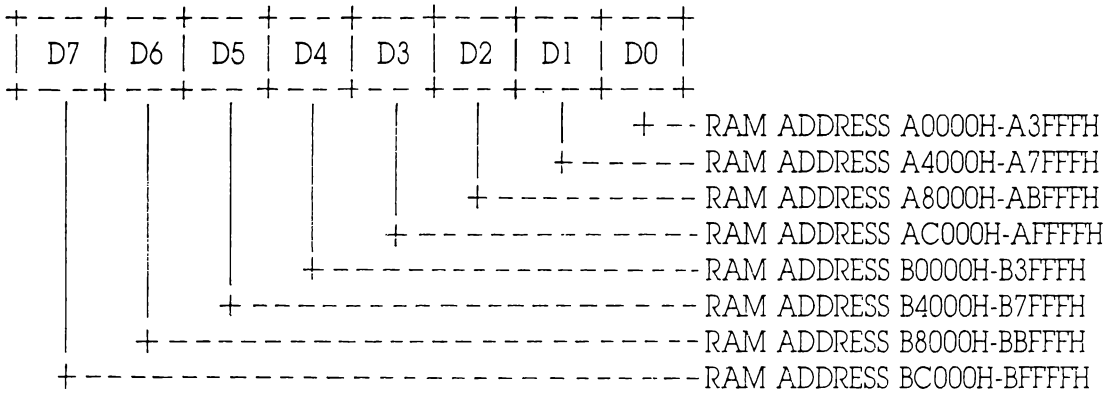
Bits	Function
0	ROM at F0000H-FFFFFH (BIOS). Default = 0 = ROM enabled - ROMCS is generated.
1	ROM at E0000H-EFFFFH. Default = 1 = ROM disabled. Shadow RAM enabled. ROMCS is not generated unless bit is set to 0.
2	ROM at D0000H-DFFFFH. Default = 1 = ROM disabled. Shadow RAM enabled. ROMCS is not generated unless bit is set to 0.
3	ROM at C0000H-CFFFFH (EGA). Default = 1 = ROM Disabled. Shadow RAM enabled. - ROMCS is not generated unless bit is set to 0.
4	Shadow RAM at F0000H-FFFFFH in Read/Write mode. 0 = Read/Write (default). 1 = Read only (Write protected).
5	Shadow RAM at E0000H-EFFFFH in Read/Write mode. 0 = Read/write (default). 1 = Read only (write protected).
6	Shadow RAM at D0000H-DFFFFH in Read/Write mode. 0 = Read/write (default). 1 = Read only (write protected).
7	Shadow RAM at C0000H-CFFFFH in Read/write mode. 0 = Read/write (default). 1 = Read only (Write portected).

Memory Enable-1 Register RB2
Index register port: 22H
Data register port: 23H
Index: **66H**



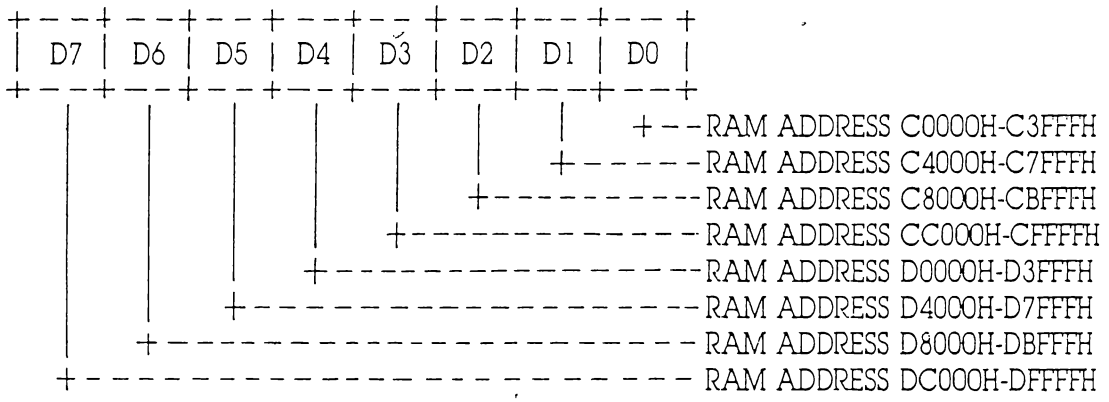
Bits	Function
0-6	Reserved
7	Address map RAM on system board in 80000H-9FFFFH area. 0 = Address is on the I/O channel (Default). 1 = Address is on the system board is put out by the 82C212.

Memory Enable Register-2 RB3
Index register port: 22H
Data register port: 23H (R/W)
Index: **67H**



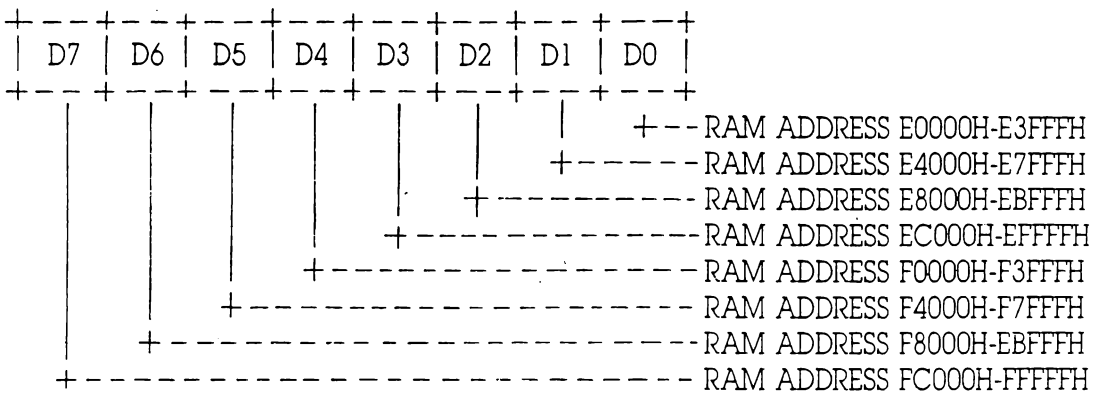
Bits	Function
0	Enable shadow RAM in A0000H-A3FFFH area. Disable = 0 Enable = 1
1	Enable Shadow RAM in A4000H-A7FFFH area. Disable = 0 Enable = 1
2	Enable Shadow RAM in A8000H-ABFFFH area. Disable = 0 Enable = 1
3	Enable Shadow RAM in AC000H-AFFFFH area. Disable = 0 Enable = 1
4	Enable Shadow RAM in B0000H-B3FFFH area. Disable = 0 Enable = 1
5	Enable Shadow RAM in B4000H-B7FFFH area. Disable = 0 Enable = 1
6	Enable Shadow RAM in B8000H-BBFFFH area. Disable = 0 Enable = 1
7	Enable Shadow RAM in BC000H-BFFFFH area. Disable = 0 Enable = 1

Memory Enable-3 Register RB4
Index register port: 22H
Data register port: 23H (R/W)
Index: **68H**



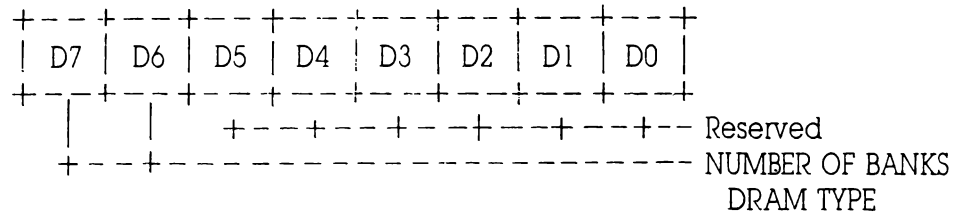
Bits	Function
0	Enable shadow RAM in C0000H-C3FFFH area. Disable = 0 Enable = 1
1	Enable Shadow RAM in C40000H-C7FFFH area. Disable = 0 Enable = 1
2	Enable Shadow RAM in C8000H-CBFFFH area. Disable = 0 Enable = 1
3	Enable Shadow RAM in CC000H-CFFFFH area. Disable = 0 Enable = 1
4	Enable Shadow RAM in D4000H-D3FFFH area. Disable = 0 Enable = 1
5	Enable Shadow RAM in D4000H-D7FFFH area. Disable = 0 Enable = 1
6	Enable Shadow RAM in D8000H-DBFFFH area. Disable = 0 Enable = 1
7	Enable Shadow RAM in DC000H-DFFFFH area. Disable = 0 Enable = 1

Memory Enable-4 Register (RB5)
Index register port: 22H
Data register port: 23H (R/W)
Index: **69H**



Bits	Function
0	Enable shadow RAM in E0000H-E3FFFH area. Disable = 0 Enable = 1
1	Enable Shadow RAM in E4000H-E7FFFH area. Disable = 0 Enable = 1
2	Enable Shadow RAM in E8000H-EBFFFH area. Disable = 0 Enable = 1
3	Enable Shadow RAM in EC000H-EFFFFH area. Disable = 0 Enable = 1
4	Enable Shadow RAM in F0000H-F3FFFH area. Disable = 0 Enable = 1
5	Enable Shadow RAM in F4000H-F7FFFH area. Disable = 0 Enable = 1
6	Enable Shaodw RAM in F8000H-FBFFFH area. Disable = 0 Enable = 1
7	Enable Shadow RAM in FC000H-FFFFFH area. Disable = 0 Enable = 1

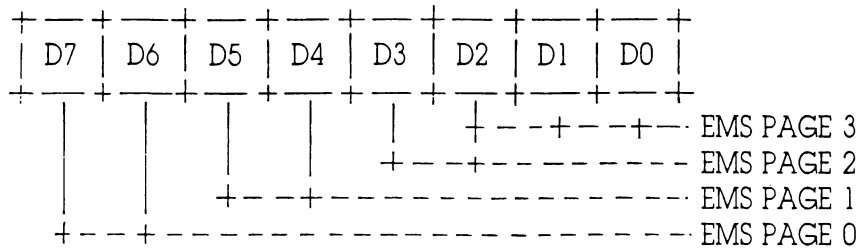
Bank0/1 Enable Register RB6
Index register port: 22H
Data register port: 23H
Index: **6AH**



Bits	Function
0-4	Reserved
5	Number of RAM banks used. 0 = 1 bank. non-interleaved mode (Default) 1 = 2 banks
7, 6	These bits contain the information for the DRAM types used on the system board. POST/BIOS should use the DRAM configuration data stored in the CMOS RAM of the 82C206 IPC.

7	6	DRAM Types
0	0	Disabled
0	1	256K and 64K bit DRAMs used (for 640Kbyte combination only)
1	0	256K bit DRAMs used (Default)
1	1	1M bit DRAMs used

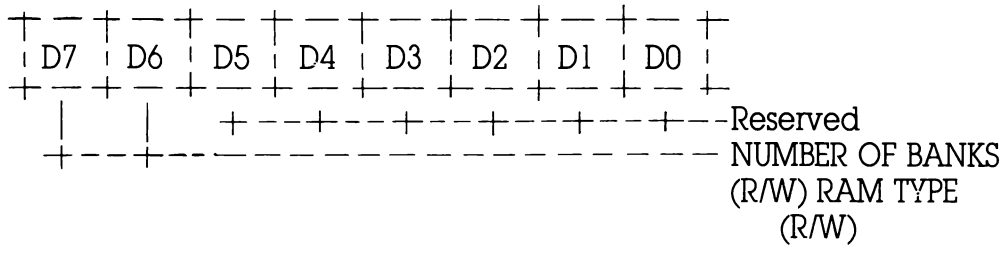
EMS Address Extention Register RB10
Index register port: 22H
Data register port: 23H
Index: **6EH**



Bits	Function		
1, 0	EMS Page 3 address extension bits.		
	1	0	Block of EMS Memory
	0	0	1 Mbyte to 2 Mbyte
	0	1	2 Mbyte to 4 Mbyte
	1	0	4 Mbyte to 6 Mbyte
	1	1	6 Mbyte to 8 Mbyte
3, 2	EMS Page 2 address extension bits.		
	3	2	Block of EMS Memory
	0	0	1 Mbyte to 2 Mbyte
	0	1	2 Mbyte to 4 Mbyte
	1	0	4 Mbyte to 6 Mbyte
	1	1	6 Mbyte to 8 Mbyte
5, 4	EMS Page 1 address extension bits.		
	5	4	Block of EMS Memory
	0	0	1 Mbyte to 2 Mbyte
	0	1	2 Mbyte to 4 Mbyte
	1	0	4 Mbyte to 6 Mbyte
	1	1	6 Mbyte to 8 Mbyte
7, 6	EMS Page 0 address extension bits.		
	7	6	Block of EMS Memory
	0	0	1 Mbyte to 2 Mbyte
	0	1	2 Mbyte to 4 Mbyte
	1	0	4 Mbyte to 6 Mbyte
	1	1	6 Mbyte to 8 Mbyte

Bits	Function
5	RAM access wait states. If set to 0, accesses have 0 wait states. If set to 1 (Default), accesses will have 1 wait state.
6	640Kbyte to 1Mbyte RAM relocation bit. A zero does not relocate local RAM. A one (Default) relocates local RAM from 080000H-09FFFFH to 100000H-11FFFFH, provided total local RAM is 1 Mbyte only.
7	Page/Interleaved mode enable. A0 disables the page/interleaved mode, allowing useage of normal mode for the DRAMs (Default). A 1 enables page/ interleaved mode for the DRAMs.

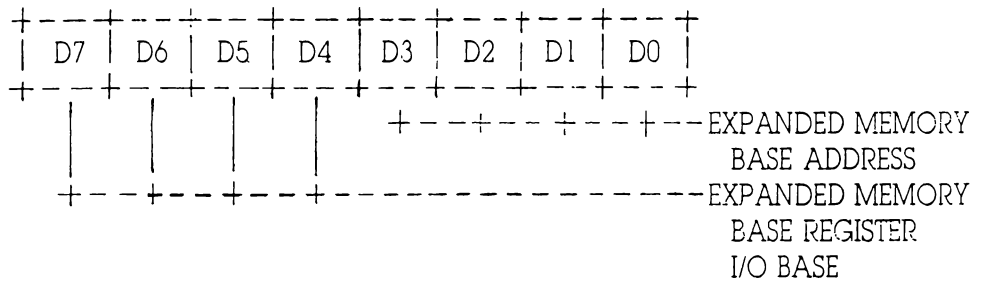
Band 2/3 Enable Register RB8
Index register port: 22H
Data register port: 23H
Index: **6CH**



Bits	Function
0-3	Reserved
4	2 or 4 Way Interleave, 4 Way Intrleave is Recommended.
5	Number of local RAM Banks used. 0 = 1 Bank used, non-interleaved mode only (Default). 1 = 2 Banks used.
7, 6	These bits indicate the local DRAM type as listed:

7	6	RAM Type
0	0	None (Default)
0	1	Reserved
1	0	256 Kbit
1	1	1 Mbit

EMS Base Address Register RB9
Index registr port: 22H
Data register port: 23H (R/W)
Index: **6DH**



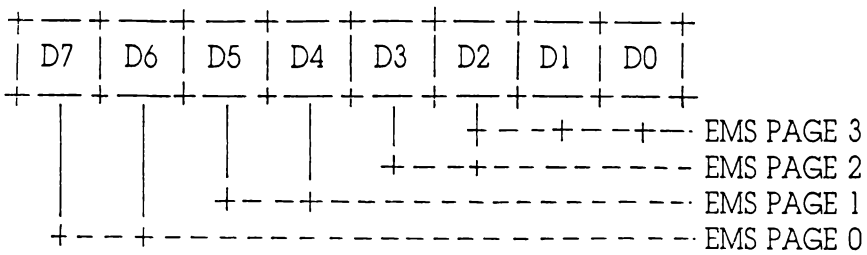
Bits	Function
0-3	These bits are used for the EMS page register I/O base address. The bits are encoded as follows. with unused combinations being reserved:

3	2	1	0	I/O Base
0	0	0	0	208H/209H
0	0	0	1	218H/219H
0	1	0	1	258H/259H
0	1	1	0	268H/269H
1	0	1	0	2A8H/2A9H
1	0	1	1	2B8H/2B9H
1	1	1	0	2E8H/2E9H

Bits	Function
7-4	These bits are used for selecting the expanded memory base addresses. They are encoded as follows, with all unused combinations being reserved:

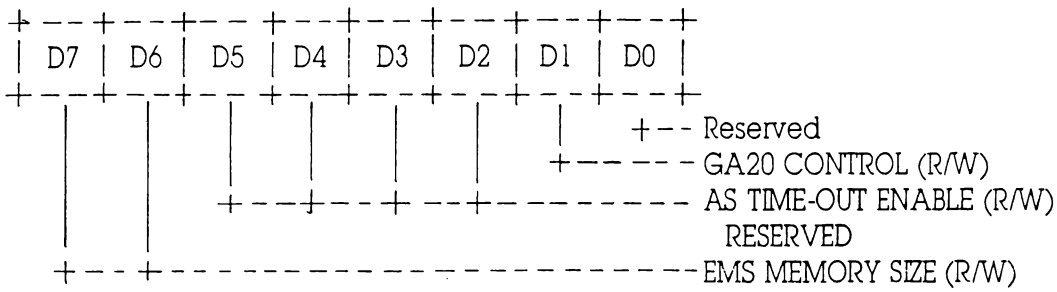
7	6	5	4	EMS Base Addresses
0	0	0	0	C0000H, C4000H, C8000H, CC000H
0	0	0	1	C4000H, C8000H, CC000H, D0000H
0	0	1	0	C8000H, CC000H, D0000H, D4000H
0	0	1	1	CC000H, D4000H, D4000H, D8000H
0	1	0	0	D0000H, D4000H, D8000H, DC000H
0	1	0	1	D4000H, D8000H, DC000H, E0000H
0	1	1	0	D8000H, DC000H, E0000H, E4000H
0	1	1	1	DC000H, E0000H, E4000H, E8000H
1	0	0	0	E0000H, E4000H, E8000H, EC000H

EMS Address Extention Register RB10
Index register port: 22H
Data register port: 23H
Index: **6EH**



Bits	Function		
1, 0	EMS Page 3 address extension bits.		
	1	0	Block of EMS Memory
	0	0	1 Mbyte to 2 Mbyte
	0	1	2 Mbyte to 4 Mbyte
	1	0	4 Mbyte to 6 Mbyte
	1	1	6 Mbyte to 8 Mbyte
3, 2	EMS Page 2 address extension bits.		
	3	2	Block of EMS Memory
	0	0	1 Mbyte to 2 Mbyte
	0	1	2 Mbyte to 4 Mbyte
	1	0	4 Mbyte to 6 Mbyte
	1	1	6 Mbyte to 8 Mbyte
5, 4	EMS Page 1 address extension bits.		
	5	4	Block of EMS Memory
	0	0	1 Mbyte to 2 Mbyte
	0	1	2 Mbyte to 4 Mbyte
	1	0	4 Mbyte to 6 Mbyte
	1	1	6 Mbyte to 8 Mbyte
7, 6	EMS Page 0 address extension bits.		
	7	6	Block of EMS Memory
	0	0	1 Mbyte to 2 Mbyte
	0	1	2 Mbyte to 4 Mbyte
	1	0	4 Mbyte to 6 Mbyte
	1	1	6 Mbyte to 8 Mbyte

Miscellaneous Register RB12
Index register port: 22H
Data register port: 23H
Index: **6FH**



Bits	Function
0	Reserved
1	This bit is used for Address line A20 control and provides OS/2 optimization while switching between user and protected modes. The bit defaults to 0 and enables CPUA20 onto A20. If set to 1, it sets A20 = 0
2	This bit is used to enable the RAS time-out counter for page mode operation. The counter is disabled if set to 0 (Default) and is enabled if set to 1.
3, 4	Reserved
7-5	These bits are used to set the EMS memory space according to the following coding:

7	6	5	EMS Memory Size
0	0	0	1 Mbyte to 1.5 Mbytes (0.5 MB)
0	0	1	1 Mbyte to 2 Mbytes (1 MB)
0	1	0	1 Mbyte to 3 Mbytes (2 MB)
0	1	1	1 Mbyte to 4 Mbytes (3 MB)
1	0	0	1 Mbyte to 5 Mbytes (4 MB)
1	0	1	1 Mbyte to 6 Mbytes (5 MB)
1	1	0	1 Mbyte to 7 Mbytes (6 MB)
1	1	1	1 Mbyte to 8 Mbytes (7 MB)

APPENDIX B

82C212 PAGE/INTERLEAVE AND EMS MEMORY CONTROLLER

The 82C212 performs the memory control function in the system.

The 82C212 organizes memory as banks of 18 bit modules consisting of 16 bits of data and 2 bits of parity, information. The 16 bits of data are split into high and lower bytes with one parity bit for each byte. The minimum configuration can be a single bank operating in non interleaved mode or can be a pair of DRAM banks operating in two way interleaved mode, the DRAMs within a pair of banks must be indentical.

However, each bank of DRAM pairs can be different from other pairs. For example, Banks 0,1,2 & 3 may have 256K by 4-bit DRAM and Banks 4,5 etc could have 1M by 1 bit DRAMs. A typical system may be shipped with one or two banks of smaller DRAM types (e.g. 256 by 4-bit DRAMs) and later upgraded with additional pairs of banks of larger DRAMs (e.g. 1M by 1 bit DRAMs)

Page/Interleaved Operation

The 82C212 uses a page/interleaved design that is different from most interleaved memory designs. Typical two way interleaving schemes use two banks of DRAMs with even word addresses on one bank and odd word addresses on the other bank. If memory accesses are sequential, the RAS precharge time of one bank overlaps the access time of the other bank. Typically, programs consist of instruction fetches interspersed with operand accesses. The instruction fetches tend to be sequential and the operand accesses tend to be random.

Figure 1 is a sequence diagram for a memory interleaved scheme using two banks 0 and 1. The - RAS signals of the two banks are interleaved so that the RAS precharge time (Trp) of one bank is used for the - RAS active time in the other bank. This requires sequential accesses it is possible to get wait states due to a "miss". Typically this results in a 50% hit ratio (possible zero wait state accesses).

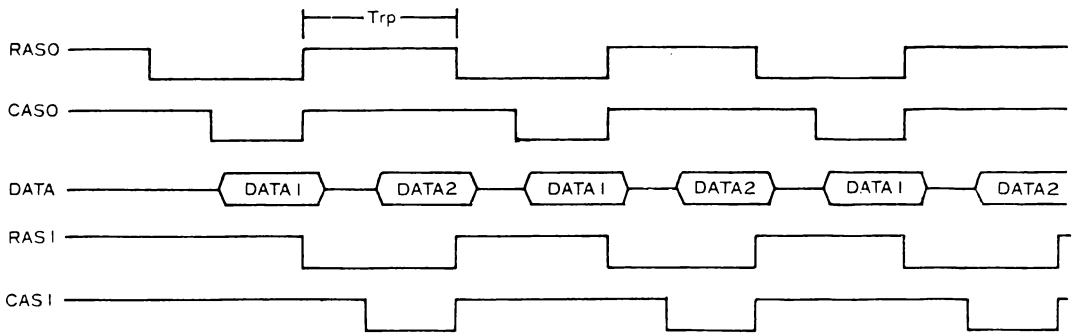


Figure 1. DRAM Interleaved Operation

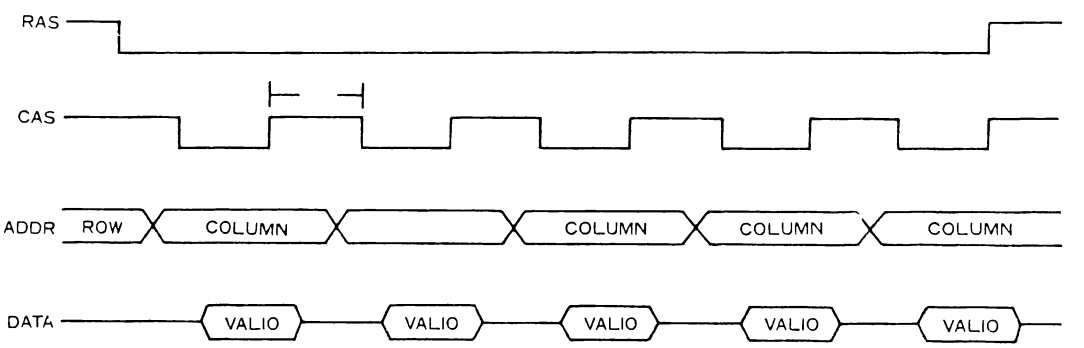


Figure 2. DRAM Page Mode Operation

Figure 2 is a sequence diagram of a paged mode DRAM operation. In paged mode DRAMS, once a row access has been made, it is possible to acess subsequent column address within that row, without the - RAS precharge penalty. However, after a - RAS active timeout, there is a - RAS precharge period which typically occurs every 10 microseconds. Since the CAS precharge time Top is small, it is possible to make fast random accesses within a selected row. Typically, page mode access times are half the normal DRAM access times. For 256K x 1 DRAMs, each row has 512 bits. If eighteen 256K x 1 bit DRAMs are used to implement a bank, a page would have 512 x 2 bites (excluding 2 bits for parity) = 1 Kbytes. Thus paged mode DRAMs could be interleaved at 1 Kbyte boundaries rather than 2 byte boundaries as in the regular interleaved mode operation. Any access to the currently active - RAS page would occur in a short page access time and any subsequent access could be anywhere in the same 1 Kbyte boundary, without incurring any penalty due to - RAS precharge. If memory is configured to take advantage of this DRAM organization, significantly better performance can be achieved over normal interleaving because:

1. Page mode access time is shorter than normal DRAM access time. This allows more time in the DRAM critical paths, to achieve penalty free accesses or 'hits'.

2. The possibility of the next access being fast is significantly higher than in a regular interleaving scheme. This is because instructions and data tend to cluster together by principle of locality of reference.

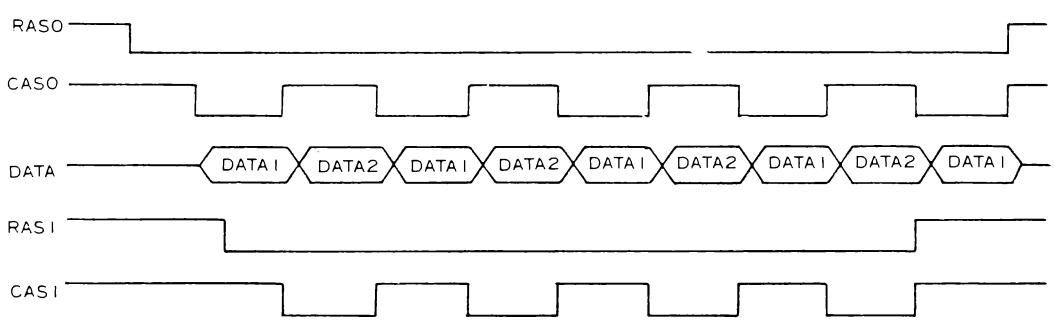


Figure 3. DRAM Page/Interleave Operation

Figure 3 is a sequence diagram of a two way Page/Interleaved scheme using page mode DRAMs. As seen, it is possible to make zero wait state accesses between the two banks 0 and 1, by overlapping - CAS precharge time of once bank with - CAS active time of the other bank. The DRAM - RAS lines for both banks can be held active till the - RAS active timeout period, at which time a - RAS precharge for that bank is required. Typical hit ratios higher than 80% are possible using this scheme. With the 82C212 memory controller, using the page/interleaved scheme, 150 nanosecond access time DRAMs can be used at 12MHz and 100 nanosecond access time DRAMs at 16MHz.

APPENDIX C

MEMORY MAPPING AND REFRESH LOGIC

The 82C212 has an extensive set of memory mapping registers for various memory organizations. Through the memory mapping logic, for up to 1 Mbyte of system RAM, it is possible to map RAM that overlaps the EPROM area (640Kbyte-1Mbyte) above the 1Mbyte area, as shown in Figure 4. Hence, for 1Mbyte of on board RAM, the software can address it from 0 to 640Kbytes and from 1 Mbyte to 1.384 Mbytes. The EPROM can be addressed from the 640 Kbyte area to the 1Mbyte area.

For normal mode of operation, only one bank of DRAMs may be used. However, for the page/interleaved mode of operation, RAM bank pairs must be used.

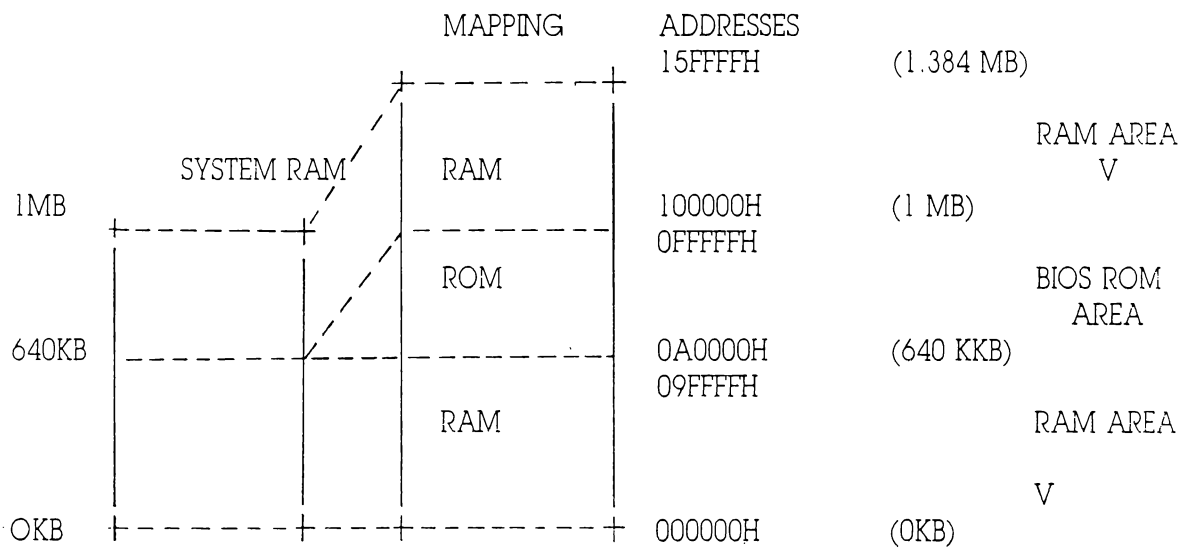


Figure 4. System RAM/ROM Mapping for 1MB System RAM

SHADOW RAM FEATURE

For efficient execution of BIOS, it is preferable to execute BIOS code through RAM rather than through slower EPROMS. The 82C212 provides the shadow RAM feature which if enabled allows the BIOS code to be executed from address as the BIOS EPROM The software should transfer code stored in the BIOS EPROMs to the system RAM, before enabling the shadow RAM feature. This feature significantly improves the performance in BIOS-call intensive applications. Performance improvements as high as 300 to 400% have been observed in benckmark tests on the shadow RAM. The shadow RAM feature is invoked by enabling the corresponding bits in the ROM enable register and the RAM mapping register.

If more than 1 Mbyte of system RAM exists, it is mapped as shown in Figure 5. if the shadow RAM feature is not invoked. This means that RAM in the 640K byte to 1 Mbyte area cannot be accessed.

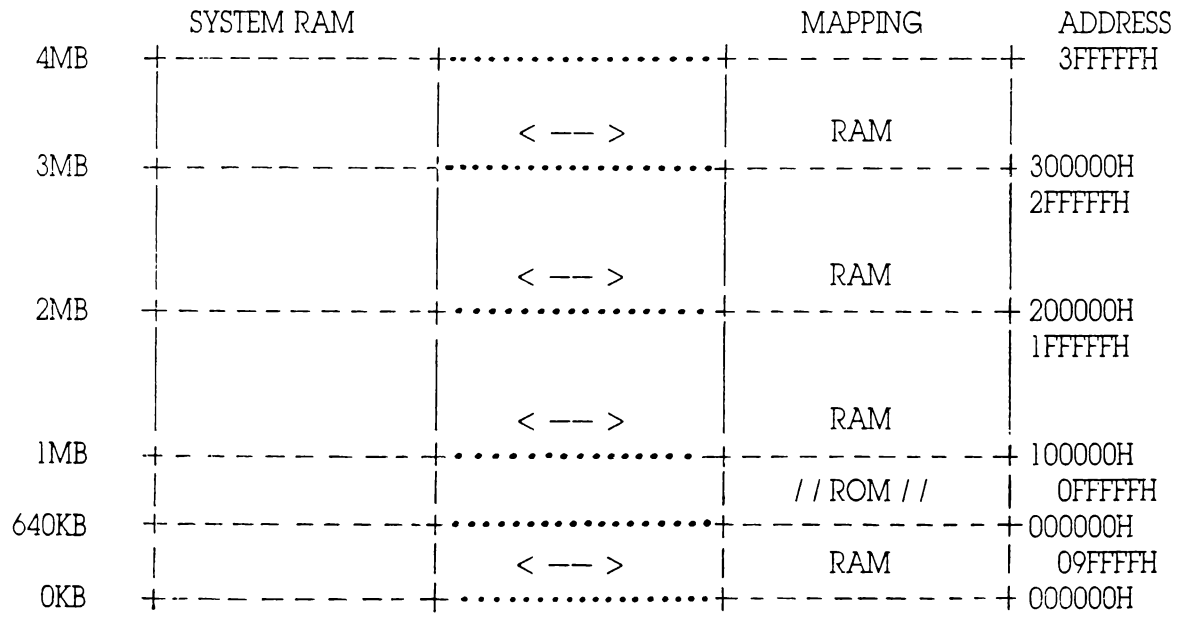


Figure 5. RAM/ROM Mapping Without Shadow RAM (More Than 1MB of RAM)

If the shadow RAM feature is used, then the RAM is mapped as

shown in Figure 6 , overlapping or Shadowing the EPROM area. In both cases, for accesses beyond the 1 Mbyte address range, the processor is switched from real to protected mode from BIOS.

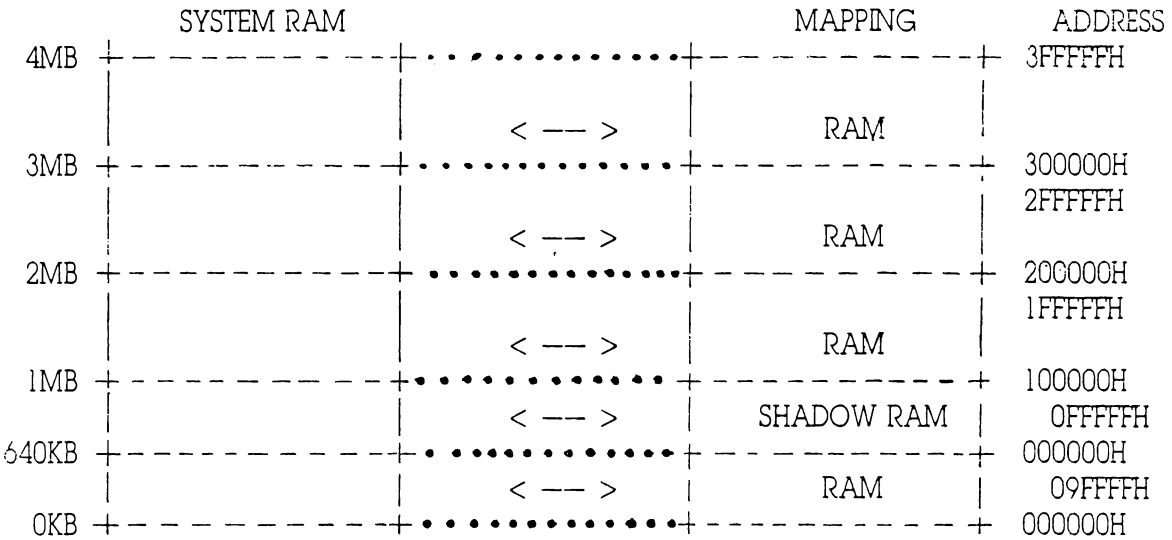
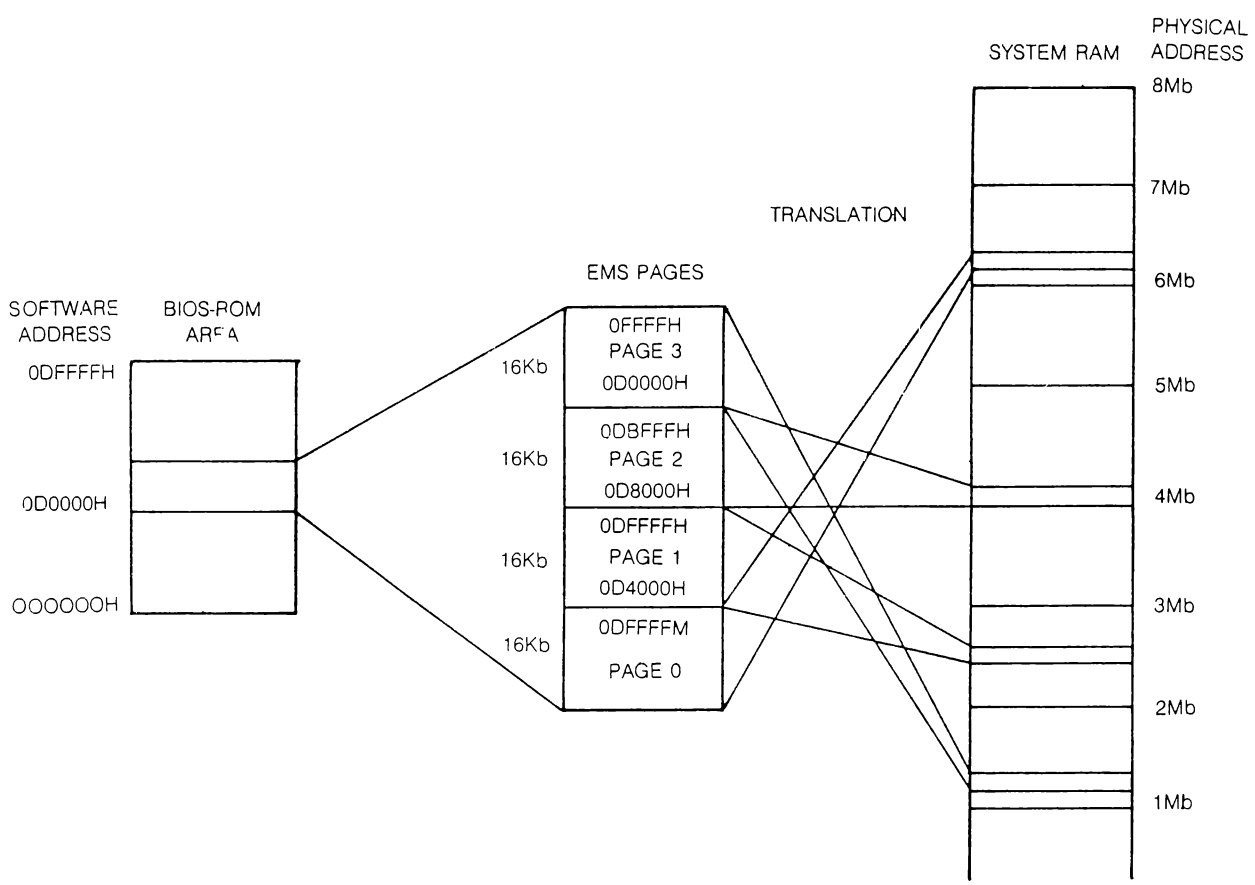


Figure 6. RAM Mapping with Shadow RAM (More Than 1MB of RAM)

APPENDIX D

EMS ADDRESS TRANSLATION LOGIC

Expanded Memory System or EMS is a memory mapping scheme used to map a 64 Kbyte block of memory in the EPROM area D0000H-DFFFFH to anywhere in the 1 Mbyte 8 Mbyte area This 64 Kbyte memory block is segmented into four 16 Kbyte pages. Through a translation cable, each 16 Kbyte segment can be mapped any where in the 1 Mbyte to 8 Mbyte area. Sin e the 82C212 uses the translation table in the EMS mode, address lines A14 to A22 are translatied by the appropriate EMS mapping register. Hence, this scheme does not require switching between user and protected mod. Figure 7 shows the EMS organization with a possible translation scheme. It is possible for the 82C212 to map this 64Kbyte block to anywhere in the 0 to 8 Mbyte area. However, it is desirable to map this block above the 1 Mbyte area in order to not use the RAM space in the 0 the 640 Kbyte area. Although the EMS scheme translates the 64 Kbyte block in the D0000H-DFFFFH area, it is possible to select a 64K byte block from any other area.



EMS Mapping

APPENDIX E

Fatal Errors

Beep Count	Meaning
1	DRAM refresh failure.
2	Parity Circuit failure.
3	Base 64KB RAM failure.
4	System Timer failure.
5	Processor Failure.
6	Keyboard Controller - Gate A20 error.
7	Virtual Mode Exception Error.
8	Display Memory R/W Test Failure. (*)
9	ROM-BIOS Check Sum Failure.

(*) Non-Fatal Error.

APPENDIX F

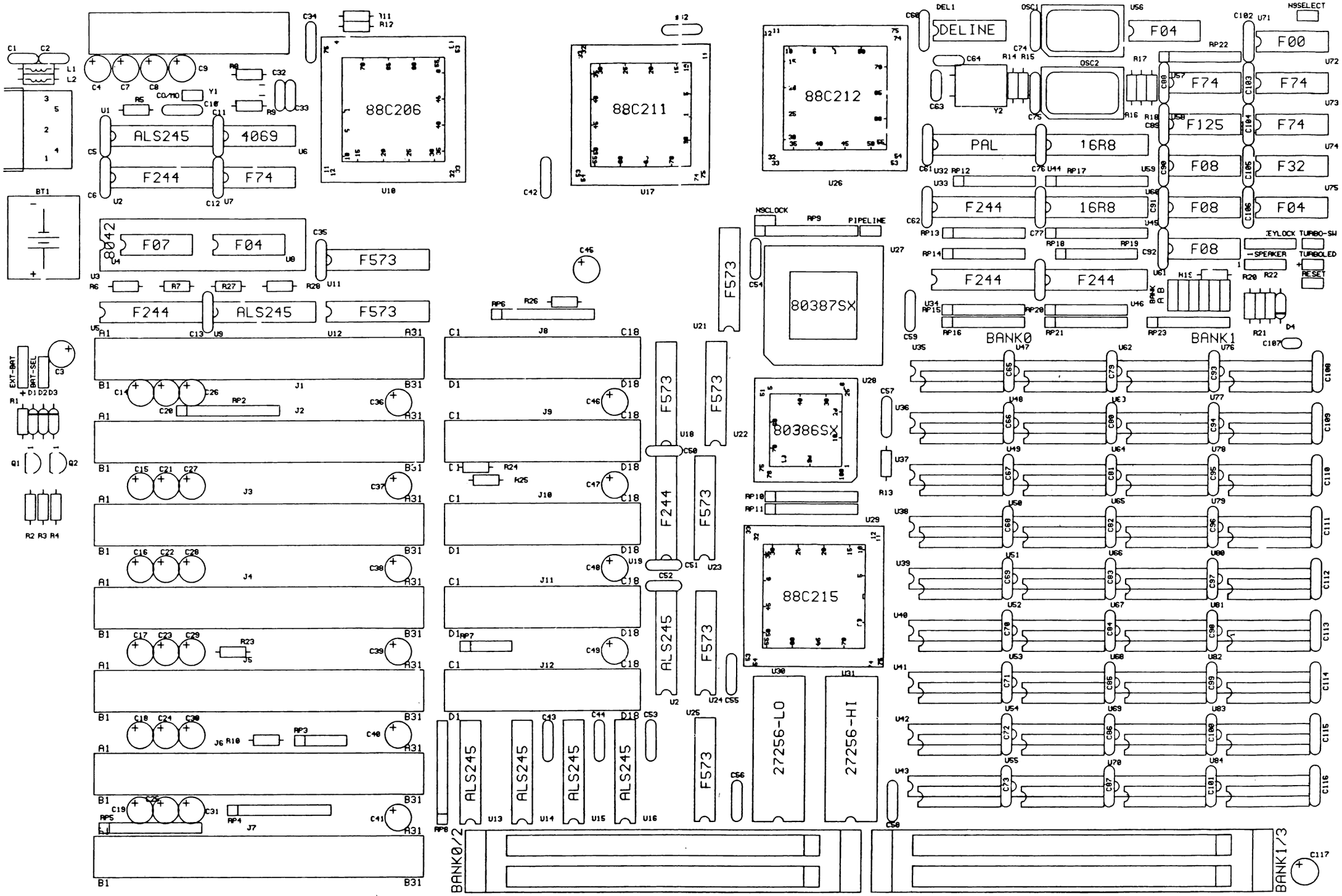
HARD DISK DRIVE TYPE TABLE

Type	Cylinders	Heads	Write-precomp	Landing-zone	Capacity
1	306	4	128	305	10 MB
2	615	4	300	615	21 MB
3	615	6	300	615	31 MB
4	940	8	512	940	64 MB
5	940	6	512	940	48 MB
6	615	4	NONE	615	21 MB
7	462	8	256	511	31 MB
8	733	5	NONE	733	31 MB
9	900	15	NONE	901	115 MB
10	820	3	NONE	820	21 MB
11	855	5	NONE	855	36 MB
12	855	7	NONE	855	51 MB
13	306	8	128	319	21 MB
14	733	7	NNE	733	44 MB
15	000	0	000	000	
16	612	4	ALL CYLS	663	21 MB
17	977	5	300	977	42 MB
18	977	7	NONE	977	58 MB
19	1024	7	512	1023	61 MB
20	733	5	300	732	31 MB
21	733	7	300	732	42 MB
22	733	5	300	733	31 MB
23	306	4	ALL CYLS	336	10 MB
24	925	7	ALL CYLS	925	56 MB
25	925	9	NONE	925	72 MB
26	754	7	754	754	46 MB
27	754	11	NONE	754	72 MB
28	699	7	256	699	42 MB
29	823	10	NONE	823	71 MB
30	918	7	918	918	55 MB
31	1024	11	NONE	1024	98 MB
32	1024	15	NONE	1024	133 MB
33	1024	5	1024	1024	44 MB
34	612	2	128	612	10 MB
35	1024	9	NONE	1024	80 MB
36	1024	8	512	1024	71 MB
37	615	8	128	615	42 MB
38	987	8	987	987	25 MB
39	987	7	987	987	60 MB
40	820	6	820	820	42 MB
41	977	5	977	977	42 MB
42	981	5	981	981	42 MB
43	830	7	512	830	50 MB
44	830	10	NONE	830	72 MB
45	917	15	NONE	918	115 MB
46	000	00	000	000	

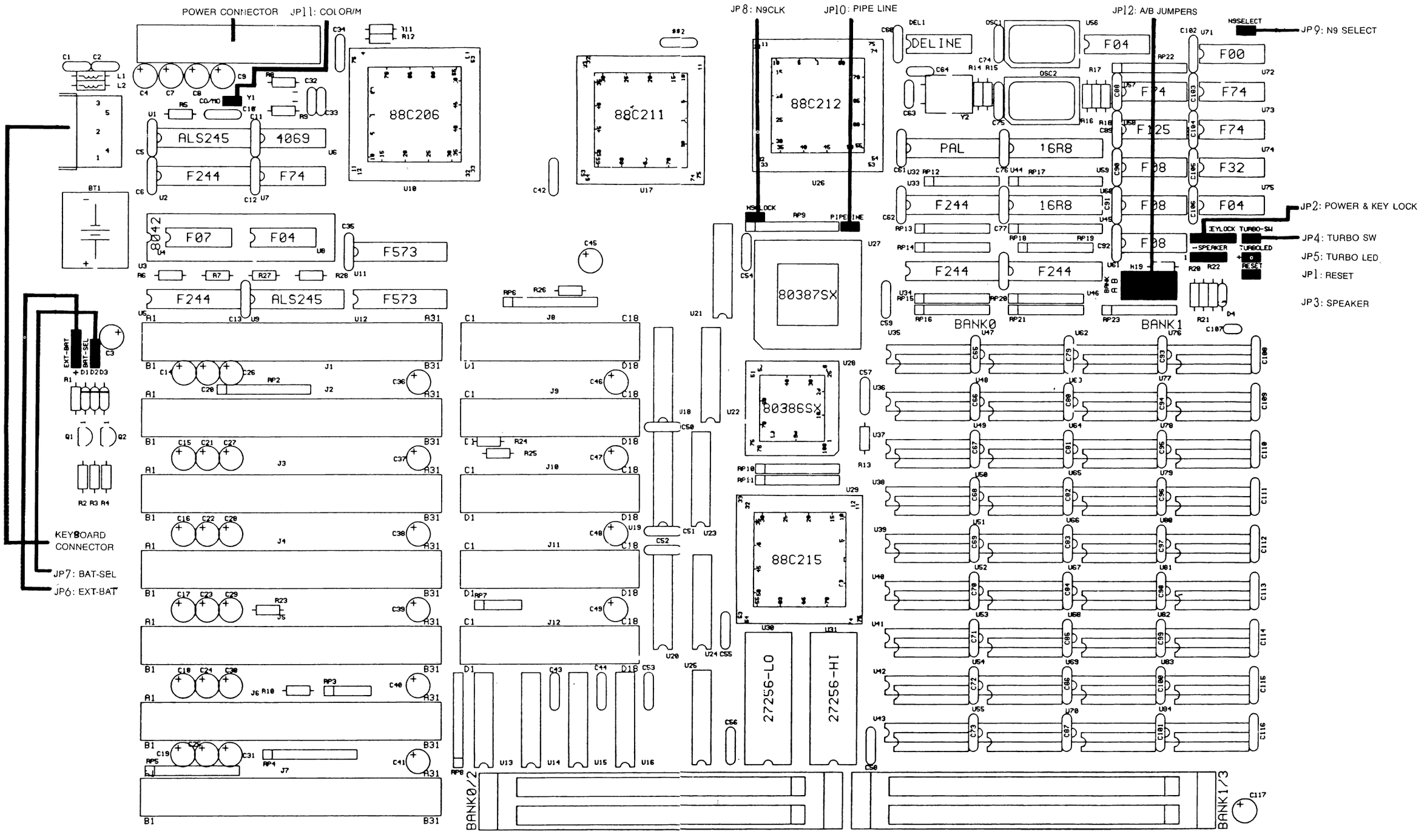
APPENDIX G

QUICK JUMPER SETTING AND MAIN BOARD CIRCUIT DIAGRAM

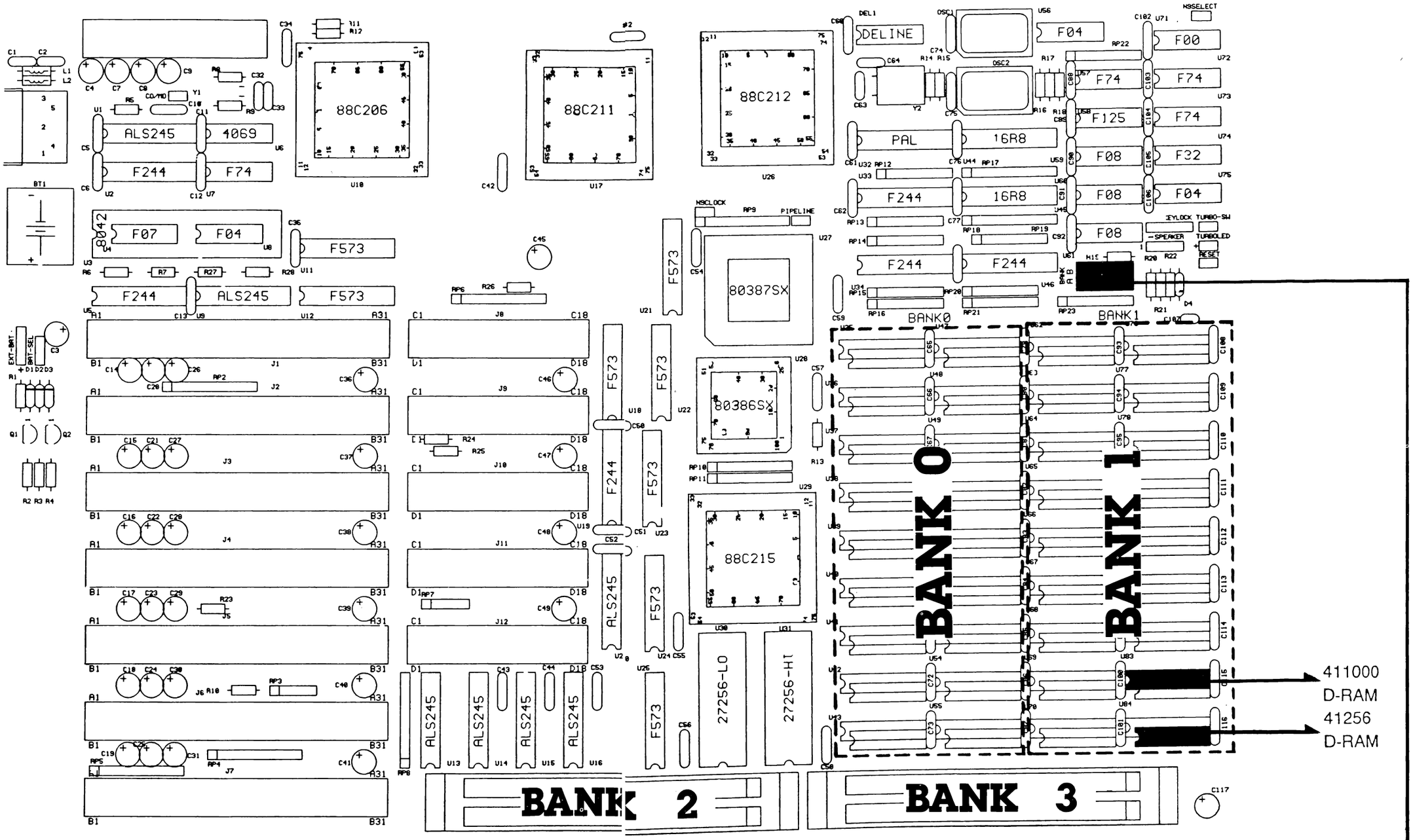
COMPONENTS LOCATIONS



JUMPERS AND CONNECTORS SETTING



BANK LOCATION



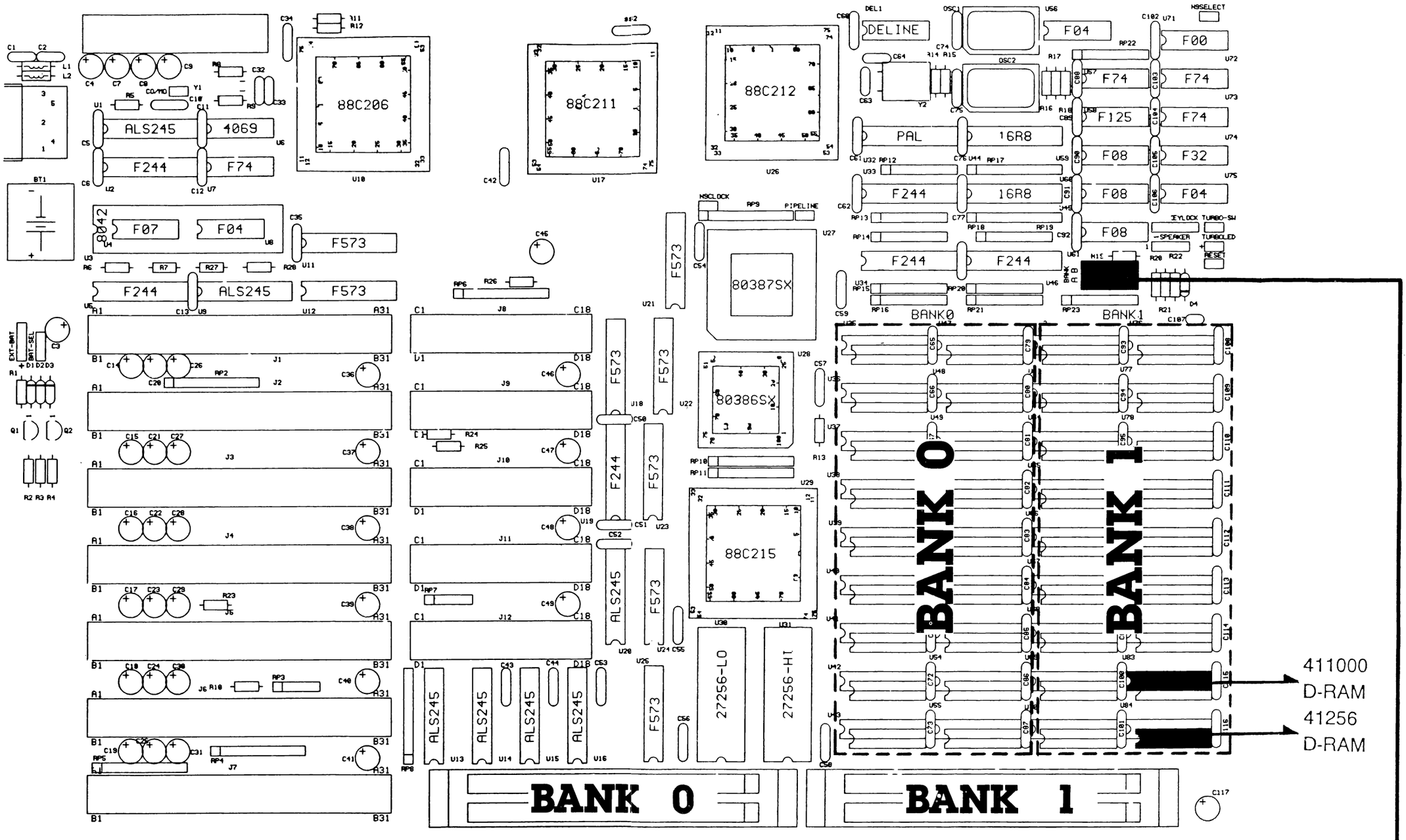
A/B JUMPERS (SELECT A/B JUMPERS FOR RAM INSTALLATION)

A		B
1	2	3
*	*	*
*	*	*
*	*	*
*	*	*
*	*	*
*	*	*

SELECT A JUMPERS

USE DIP RAM ON BANK 0/1, AS LO-BANK.
AND RAM MODULE ON BANK 2/3, AS HI-BANK.

BANK LOCATIONS

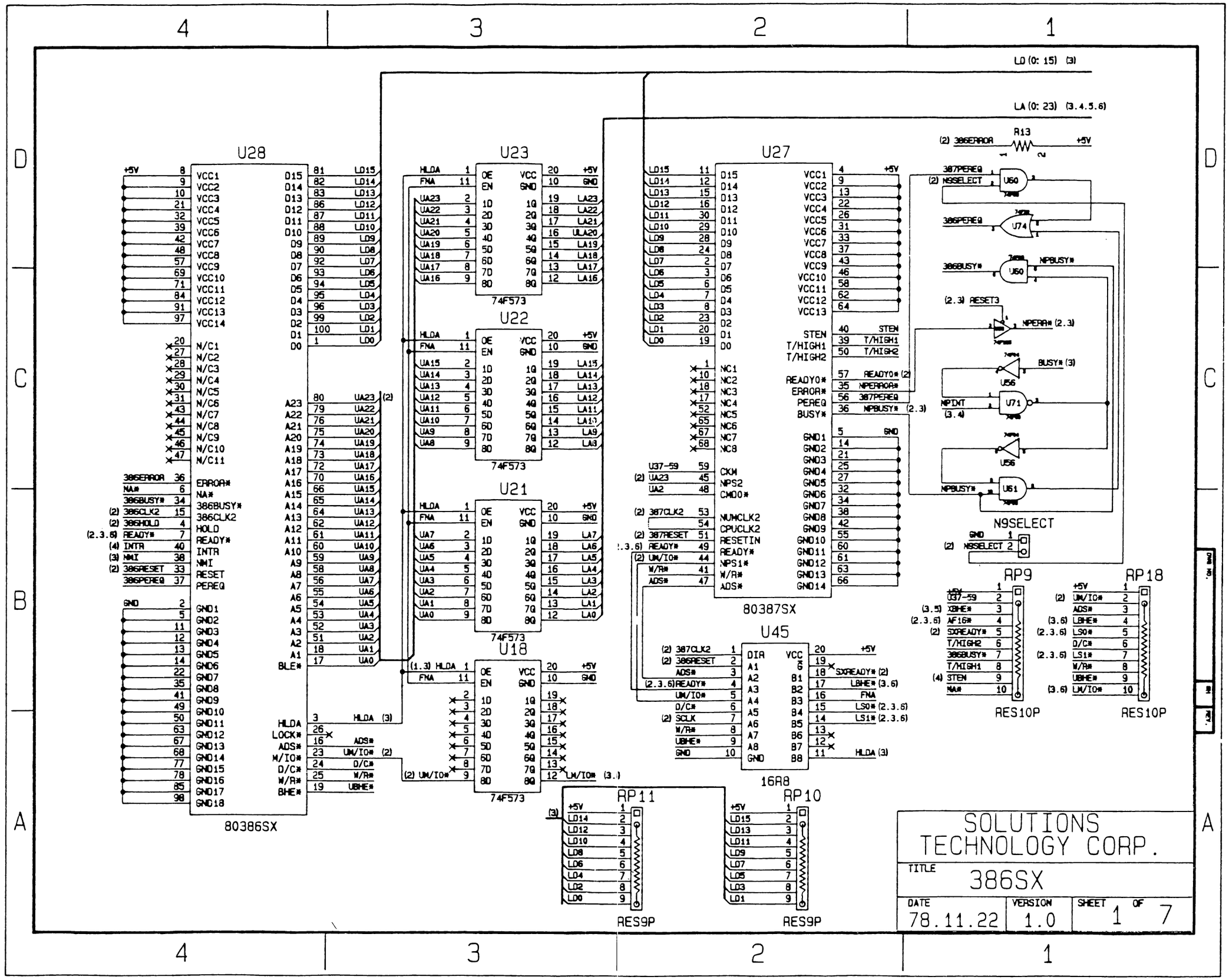


A/B JUMPERS (SELECT A/B JUMPERS FOR RAM INSTALLATION)

A	B
1	2 3
*	* *
*	* *
*	* *
*	* *
*	* *
*	* *

SELECT B JUMPERS

USE DIP RAM ON BANK 0/1, AS LO-BANK.
OR RAMMODULE ON BANK 0/1, AS LO-BANK. only


LD (0: 15) (3)
LA (0: 23) (3.4.5.6)
U28
80386SX
U23
U22
U21
U18
74F573
U27
80387SX
U45
16R8
R13
(2) 386ERROR
+5V
387PEREQ
(2) N9SELECT
U60
U74
386PEREQ
386BUSY#
NPBUSY#
(2.3) RESET3
NPERR# (2.3)
BUSY# (3)
U56
U71
NPINT
(3.4)
U51
N9SELECT
(2) N9SELECT
RP9
RP18
RES10P
RP11
RP10
RES9P
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TECHNOLOGY CORP.
TITLE
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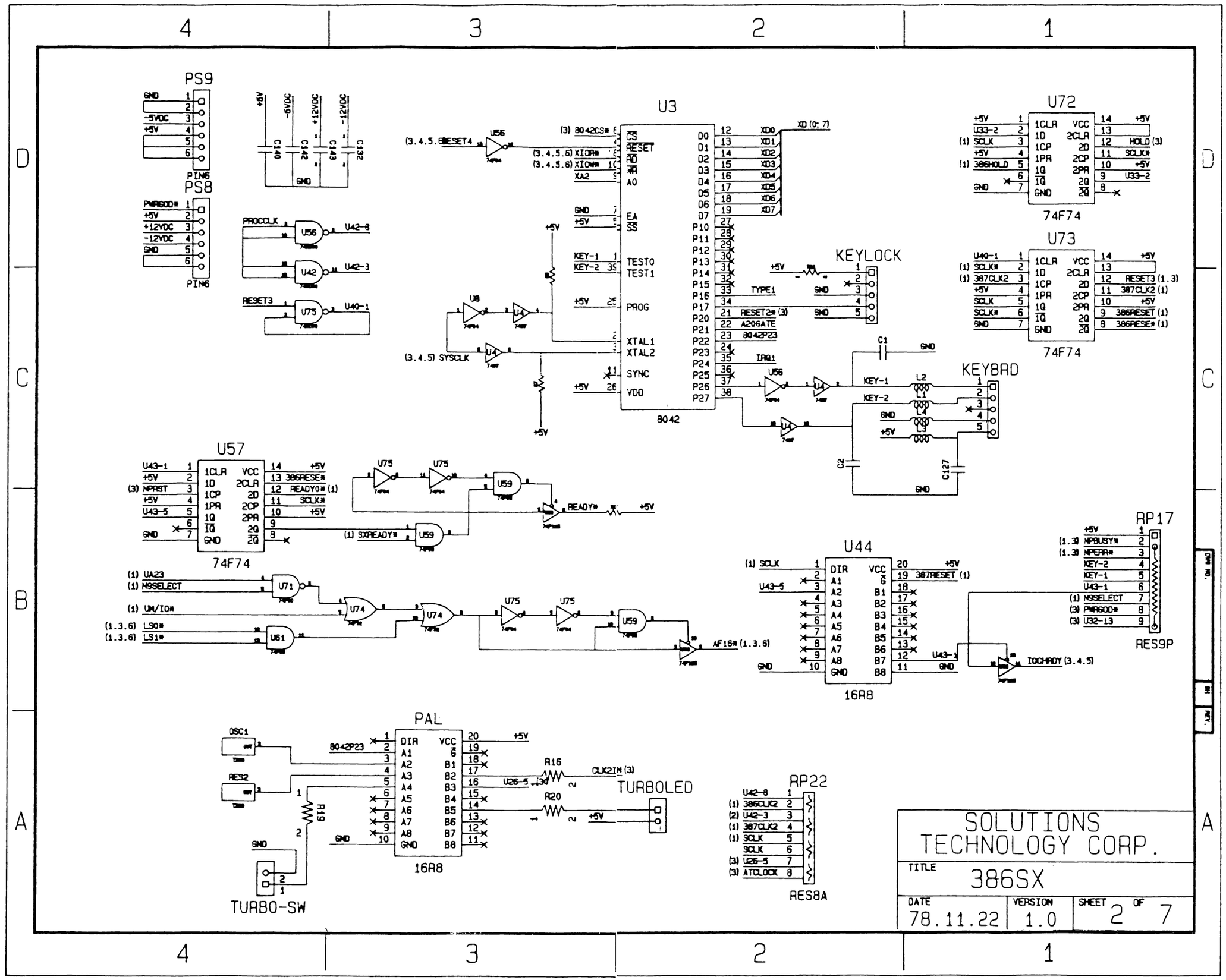
DATE
78.11.22
VERSION
1.0
SHEET
1 OF 7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PS8
PIN6
U3
8042
U72
74F74
U73
74F74
KEYLOCK
KEYBRD
U57
74F74
U44
16R8
RP17
RES9P
PAL
16R8
TURBO-SW
RP22
RES8A
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DATE
78.11.22
VERSION
1.0
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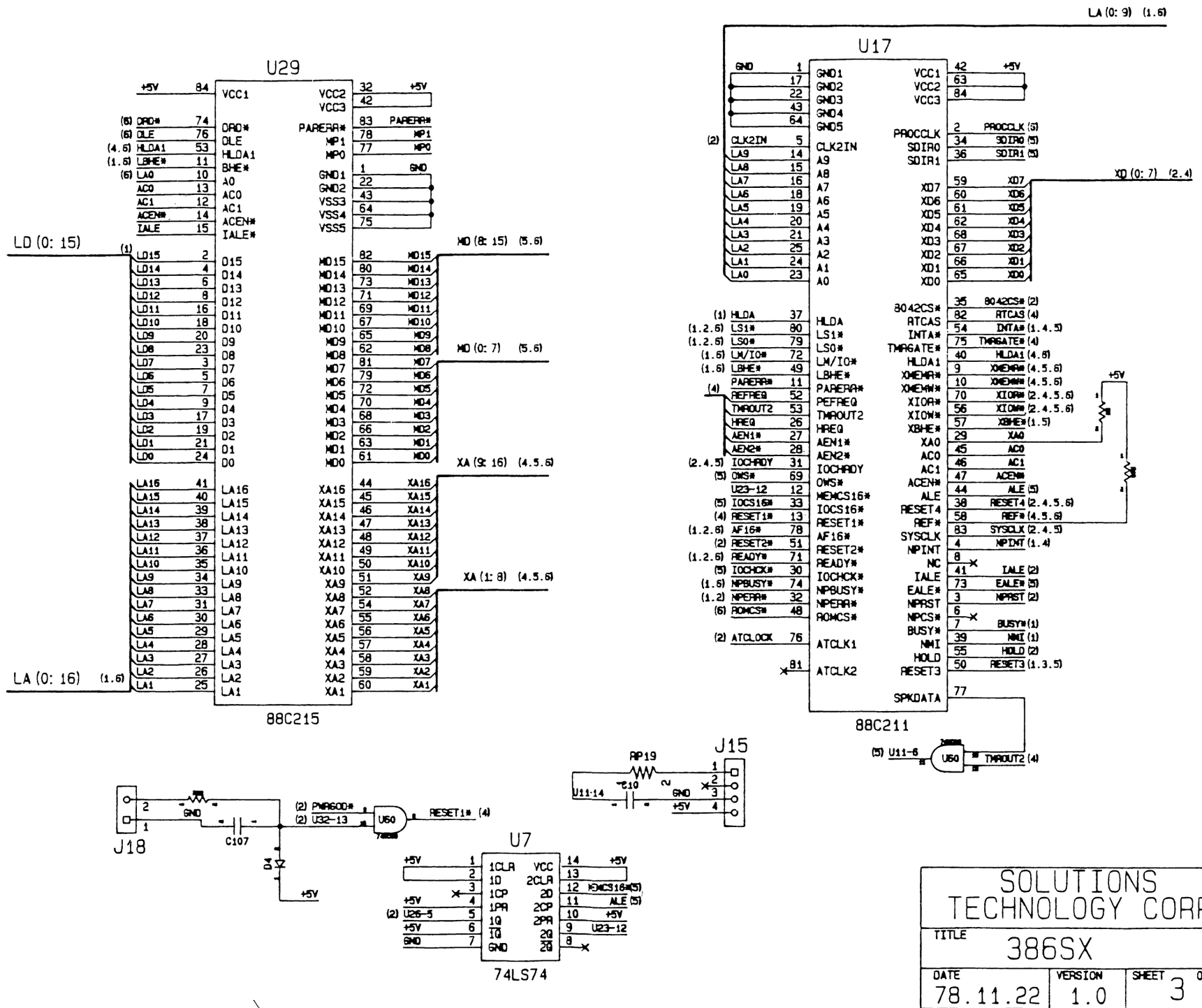
2
OF
7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88C215
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MD (8: 15) (5.6)
MD (0: 7) (5.6)
XA (9: 16) (4.5.6)
XA (1: 8) (4.5.6)
LA (0: 16) (1.6)
U17
88C211
LA (0: 9) (1.6)
XD (0: 7) (2.4)
J18
C107
J15
RP19
C10
U7
74LS74
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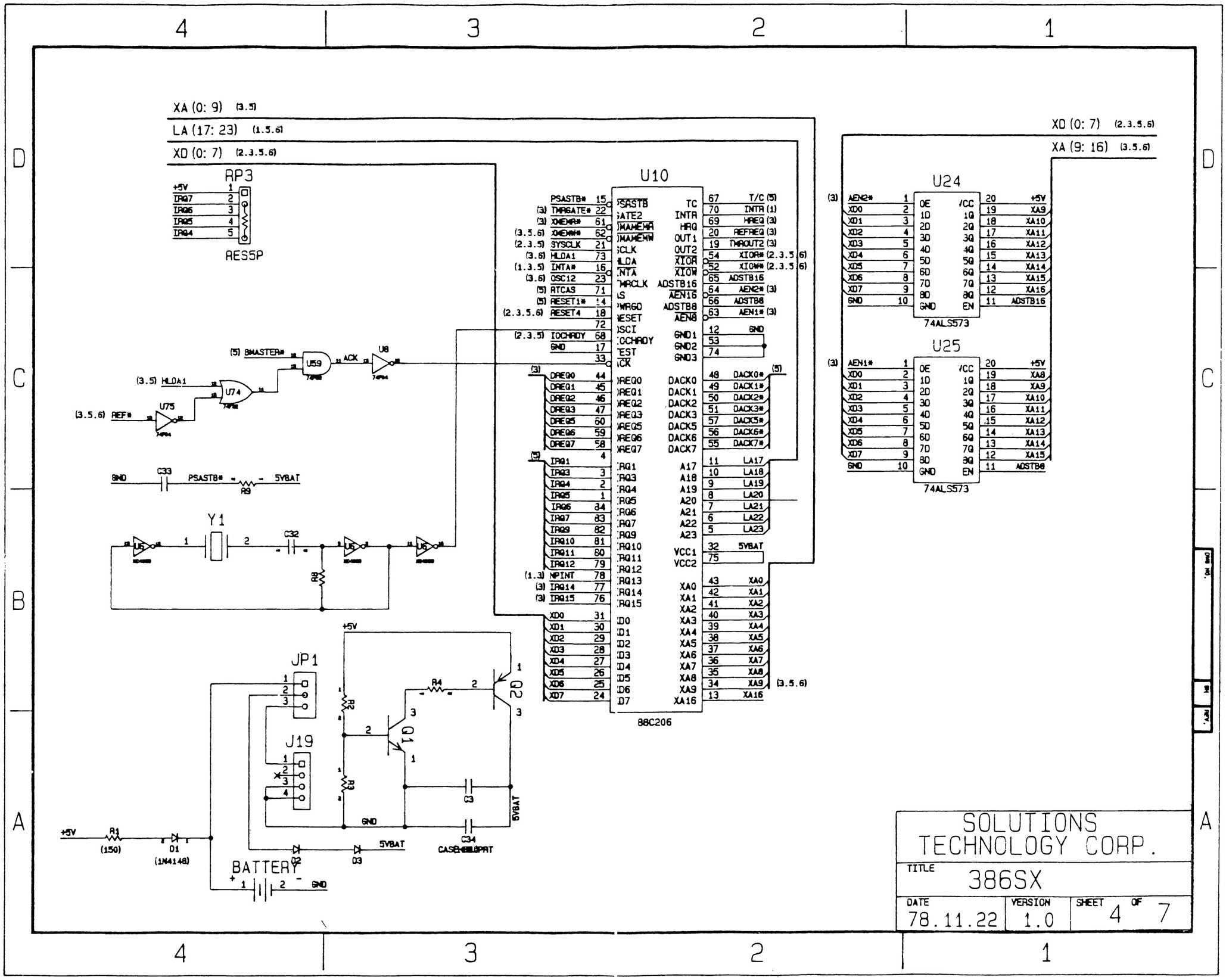
DATE
78.11.22
VERSION
1.0
SHEET 3 OF 7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LA (17: 23) (1.5.6)
XD (0: 7) (2.3.5.6)
RP3
RES5P
U10
88C206
U24
74ALS573
U25
74ALS573
XD (0: 7) (2.3.5.6)
XA (9: 16) (3.5.6)
U59
U74
U75
U8
Y1
C33
C32
R9
R8
JP1
J19
Q1
Q2
R1
R2
R3
R4
D1
(1N4148)
D2
D3
C3
C34
BATTERY
5VBAT
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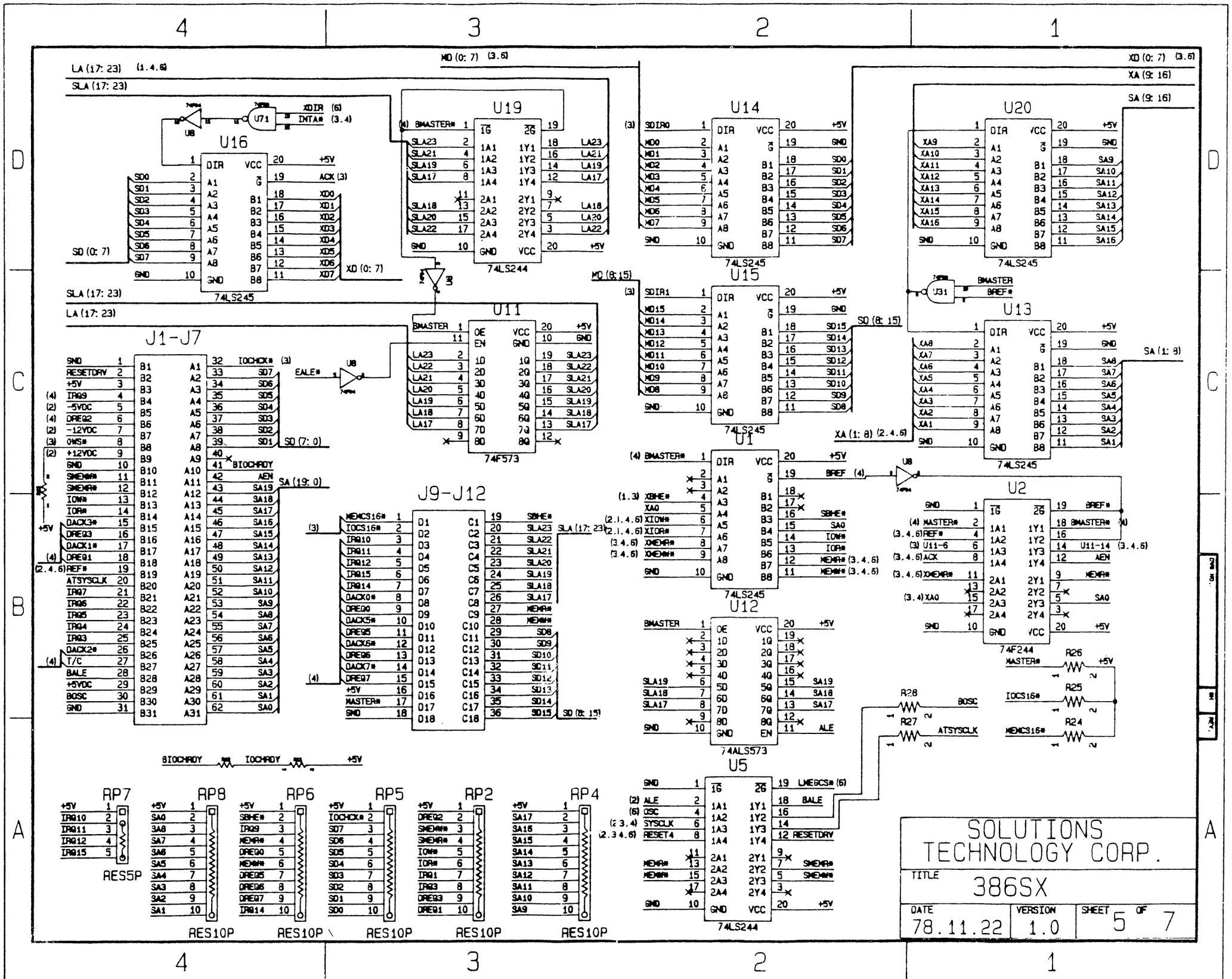
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SLA (17: 23)
MD (0: 7) (3.6)
XD (0: 7) (3.6)
XA (9: 16)
SA (9: 16)
U16
74LS245
U19
74LS244
U14
74LS245
U20
74LS245
U15
74LS245
U31
BMASTER
BREF#
U13
74LS245
U11
74F573
J1-J7
J9-J12
U1
74LS245
U2
74F244
U12
74ALS573
U5
74LS244
XA (1: 8) (2.4.6)
SA (1: 8)
SD (8: 15)
SD (0: 7)
SA (19: 0)
SLA (17: 23)
BIOCHRDY
IOCHRDY
+5V
RP7
RP8
RP6
RP5
RP2
RP4
RES5P
RES10P
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386SX
DATE
78.11.22
VERSION
1.0
SHEET
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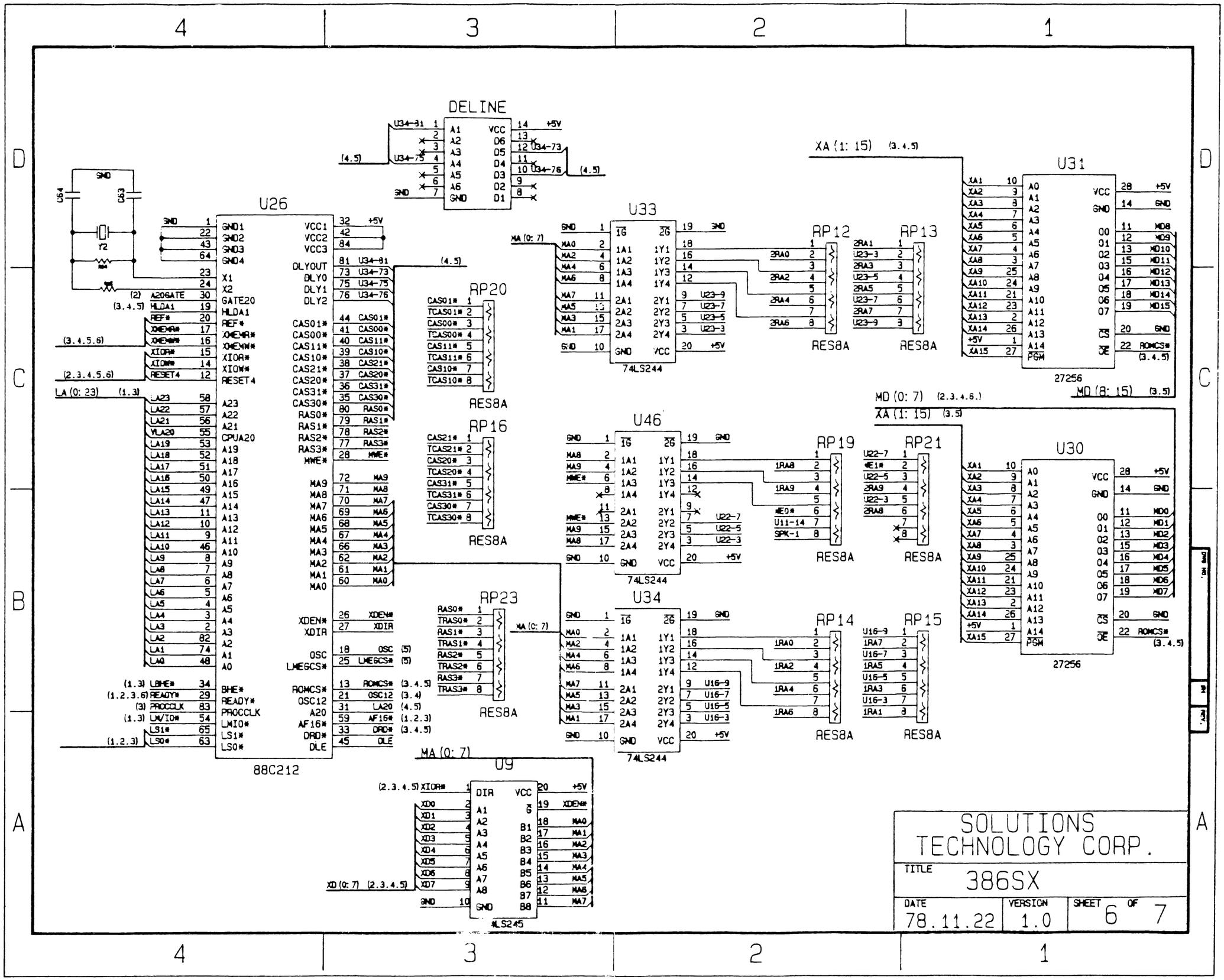
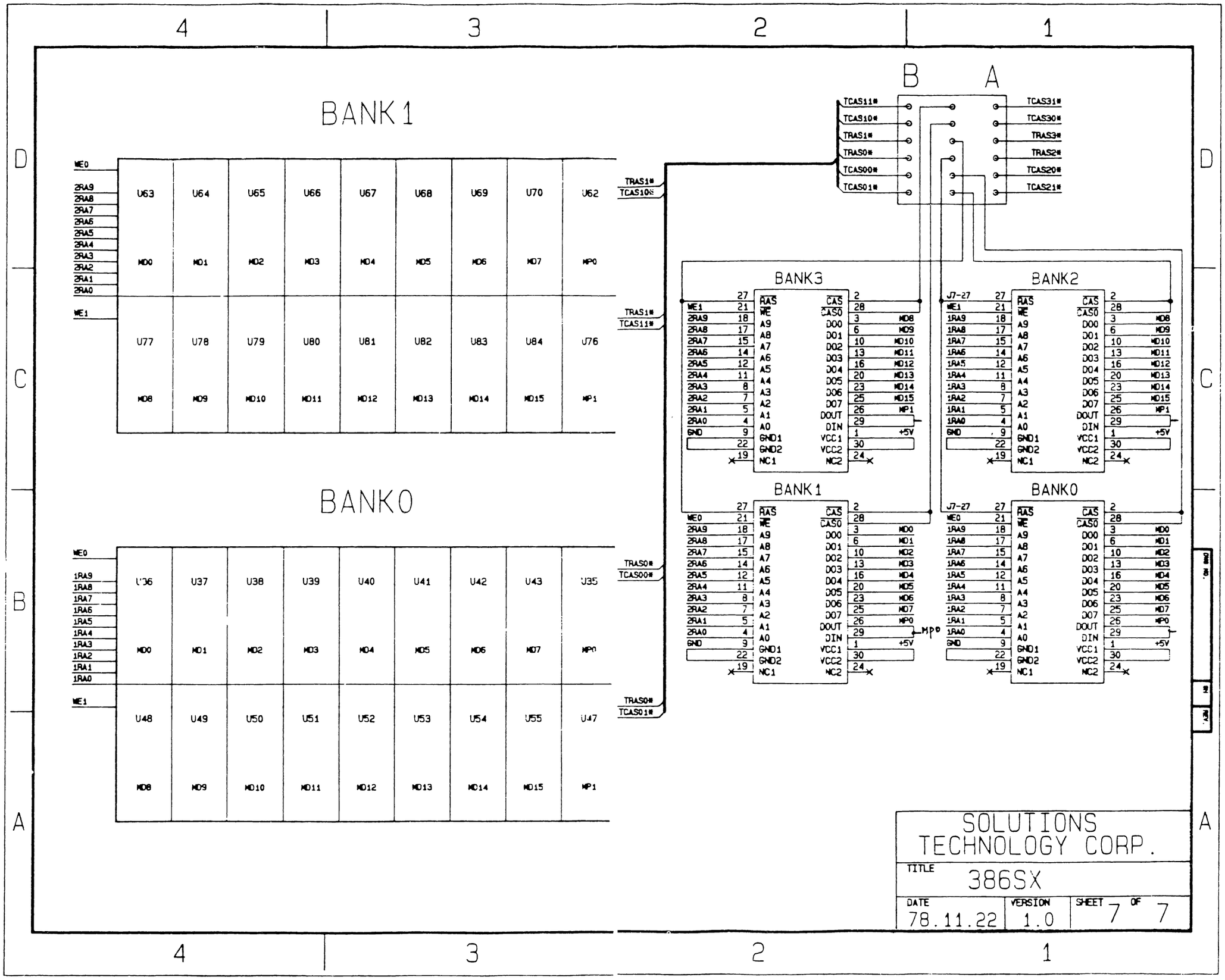
OF
7


DELINE
U26
88C212
U33
74LS244
U31
27256
U46
74LS244
U34
74LS244
U30
27256
U9
74LS245
RP20
RES8A
RP16
RES8A
RP23
RES8A
RP12
RES8A
RP13
RES8A
RP19
RES8A
RP21
RES8A
RP14
RES8A
RP15
RES8A
XA (1: 15) (3.4.5)
MD (0: 7) (2.3.4.6.)
MD (8: 15) (3.5)
XA (1: 15) (3.5)
MA (0: 7)
LA (0: 23) (1.3)
XD (0: 7) (2.3.4.5)
SOLUTIONS
TECHNOLOGY CORP.
TITLE
386SX
DATE
78.11.22
VERSION
1.0
SHEET
6 OF 7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2RA8
2RA7
2RA6
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2RA4
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2RA2
2RA1
2RA0
U63 U64 U65 U66 U67 U68 U69 U70 U62
MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7 MP0
WE1
U77 U78 U79 U80 U81 U82 U83 U84 U76
MD8 MD9 MD10 MD11 MD12 MD13 MD14 MD15 MP1
TRAS1#
TCAS10#
TRAS1#
TCAS11#
BANK0
WE0
1RA9
1RA8
1RA7
1RA6
1RA5
1RA4
1RA3
1RA2
1RA1
1RA0
U36 U37 U38 U39 U40 U41 U42 U43 U35
MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7 MP0
WE1
U48 U49 U50 U51 U52 U53 U54 U55 U47
MD8 MD9 MD10 MD11 MD12 MD13 MD14 MD15 MP1
TRAS0#
TCAS00#
TRAS0#
TCAS01#
B A
TCAS11#
TCAS10#
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TRAS0#
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TCAS01#
TCAS31#
TCAS30#
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TRAS2#
TCAS20#
TCAS21#
BANK3
BANK2
BANK1
BANK0
RAS
CAS
WE
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
GND1
GND2
NC1
VCC1
VCC2
NC2
DOUT
DIN
+5V
MP0
SOLUTIONS
TECHNOLOGY CORP.
TITLE
386SX
DATE
78.11.22
VERSION
1.0
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