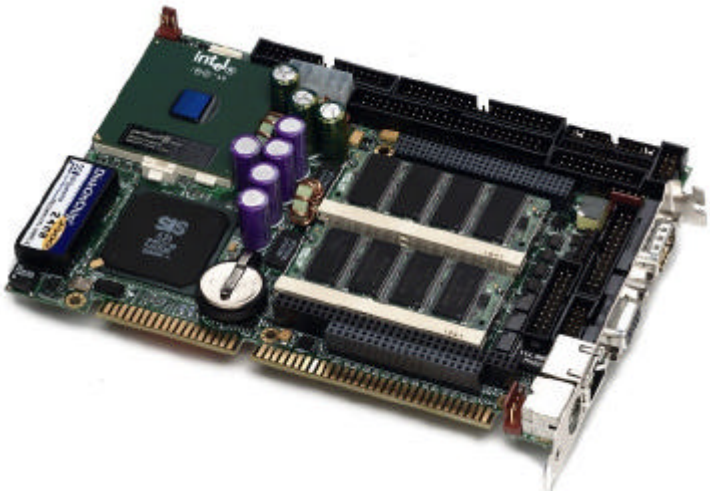
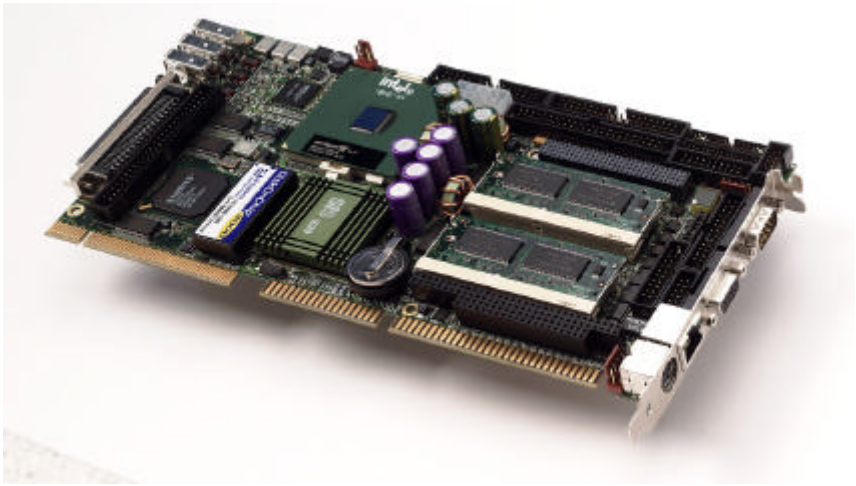
User's Hardware Manual

786LCD/S, 786LCD/MG, 786LCD/3.5", 786LCD/ST

Boards





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Document revision history.

Revision	Date	By	Comment
0.1	14. Oct. 1999	SJA	First initial draft
0.2	20. Feb. 2000	SJA	First draft for pilot release
1.0	20. Jul. 2000	SJA	Entire manual updated for production release
1.1	12. Jan 2001	CLI	Power Connector (PWRCON) pin row correction (p. 48) and ISA BUS limitations. (p. 8, 89). Various other corrections and updates.
1.2	20. Feb 2001	PJA	786LCD/3.5" information added.
1.3	20. Aug. 2002	JSN	Corrections and 786LCD/ST information added.
1.4	14. Nov. 2002	JSN	Minor corrections and Ezra-T support added.

Life Support Policy

KONTRON Technology's PRODUCTS ARE NOT FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT EXPRESS WRITTEN APPROVAL OF THE GENERAL MANAGER OF KONTRON Technology A/S.

As used herein :

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into body, or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labelling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Kontron Technology Technical Support and Services

If you have questions about installing or using your Kontron Technology Product, check this User's Manual first – you will find answers to most questions here. To obtain support, please contact your local Distributor or Field Application Engineer (FAE).

Before Contacting Support:
Before requesting technical support be prepared to provide as much information as possible:

- CPU Board
  1. Type.
  2. Part-number (Number starting with "56").
  3. Serial Number.
- Configuration
  1. CPU Type, Clock speed.
  2. DRAM Type and Size.
  3. BIOS Revision (Find the Version Info in the BIOS Setup in the Kontron Section).
  4. BIOS Settings different than *Default* Settings (Refer to the Software Manual).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
  3. Attached Hardware: Harddisks, Floppy, LCD Panels etc.

Table of contents

1. Introduction

This manual describes the 786LCD/S, 786LCD/ST, 786LCD/MG, and 786LCD/3.5” boards made by KONTRON Technology A/S. The boards will also be denoted 786LCD or 786 family if no differentiation is required.

All boards are to be used with the Celeron or the Pentium III processor from Intel.

Use of this manual implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the 786 Board’s special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in chapter 2 before switching-on the power.

All configuration and setup of the CPU board is either done automatically or by the user in the CMOS setup menus. No jumper configuration is required.

2. Installation procedure

2.1 Check the Kit Contents

The standard shipment should contain the following items :

1.) 786LCD/S, 786LCD/ST, 786LCD/MG or 786LCD/3.5” Board.
2.) Power supply Cable for Power Connector (PWRCON).

For OEM shipments this contents list may be different than listed.

The optional accessory for the 786LCD/S, /ST, /MG, and /3.5” boards is currently:
1.) 786LCD Audio, SPDIF, IrDA module (720901) for installing in the Bracket connectors (BRACK2 & BRACK2).
2.) 786LCD Audio, SPDIF module (720902) for installing in the Bracket connectors (BRACK2 & BRACK2).
3.) 786LCD DVI, TV-out module (720906) for installing in the Video Interface Module SODIMM144 connector.
4.) 786LCD Panellink Module (720907) for installing in the Video Interface Module SODIMM144 connector.
5.) 786LCD DVI-S100 Module (720908) for installing in the Video Interface Module SODIMM144 connector.
6.) 786LCD LCDADPT 3V3 module (720910) for installing in the Video Interface Module SODIMM144 connector for support of Direct LCD connections on 786LCD/3.5” boards.

The available cable and driver kit (726560) for the 786LCD/S, /ST and /MG contain:
1.) Standard Hardisk Cable (726510) for Harddisk Connector (IDE1).
2.) Harddisk Cable, Ultra DMA66 (726510) for Harddisk Connector (IDE1).
3.) Harddisk Cable, 2mm to 3.5” Disks (726520) for Harddisk Connector (IDE2).
4.) Floppy Cable (726530) for Floppy Connector (FLOPPY).
5.) Y-Cable for Keyboard and PS2-mouse (726540) for MINI-DIN Connector (KBD).
6.) 786LCD Manual and Driver CDROM (726600).

Additional the following cable(s) are available for the 786LCD/S, /ST and /MG, but not included the kit:
7.) Harddisk Cable, 2mm to 2.5” Disks (726520) for Harddisk Connector (IDE2).
8.) USB Bracket (726400) for Connector (USB).
9.) COM2 / Centronic Bracket (721030) for Connectors (COM2 & PRINTER).
10.) 786LCD COM3/4 Bracket (721033) for Connector (COM3/4).
11.) PS/2 Mouse Bracket (721040) for Connector (JPMSE).

The available cable and driver kit (726562) for the 786LCD/3.5" contain:
1.) Standard Hardisk Cable (726510) for Harddisk Connector (IDE1).
2.) Harddisk Cable, Ultra DMA66 (726510) for Harddisk Connector (IDE1).
3.) Harddisk Cable, 2mm to 3.5" Disks (726520) for Harddisk Connector (IDE2).
4.) Floppy Cable (2mm) for Floppy Connector (FLOPPY).
5.) Serial Port 2 Cable (2mm) for COM2 Connector (COM2).
6.) Parallel Port Cable (2mm) for LPT Connector (PRINTER).
7.) Y-Cable for Keyboard and PS2-mouse (726540) for MINI-DIN Connector (KBD).
8.) 786LCD Manual and Driver CDROM (726600).

Additional the following cable(s) are available, but not included the kit:
9.) Harddisk Cable, 2mm to 2.5" Disks (726520) for Harddisk Connector (IDE2).
10.) USB Bracket (726400) for Connector (USB).
11.) PS/2 Mouse Bracket (721040) for Connector (JPMSE).

The following list is available for all 786LCD Boards:
1.) Intel Celeron or Intel Pentium III processor for installing in Socket370 (contact sales dep. for availability of different types).
2.) 786LCD Active Cooler, +5V, RPM output (40200121) for processors in PPGA, FC-PGA and FC-PGA2 Package.
3.) SDRAM module(s) for SODIMM144 sockets.
4.) M-Systems DiskOnChip 2000 for DiskOnChip Socket (786LCD/S, /ST and /MG only).
5.) Compact Flash card for insertion in Compact Flash Connector (CFLASH).
6.) Mounting tool for CPU (40100001).

For an updated accessory list for the 786LCD Product Family please check the Kontron Technology WorldWideWeb: www.inside.dk or contact the Distributor or FAE. Updated drivers and manuals are also available here.

2.2 Installing the Board

To get the board running, follow these steps. In some cases the boards shipped from Kontron Technology will have CPU, SDRAM and Cooler mounted. In this case Step 2-4 can be skipped.

1. Turn off the power supply.

2. Insert the SDRAM module(s). Be careful to push it in the slot(s) before rotating it into position. The locking mechanism will typically make a *click* when the module is locked in position. If only one module is going to be installed, it **must** be placed in the SODIMM connector closest to the PC-AT edge connector on 786LCD/S, /ST and /MG boards. On 786LCD/3.5" boards the SDRAM module must be installed in the slot closest to the PC104+ connector. **It is very important to use SDRAM modules that comply to the Intel SO-DIMM Specification Revision 1.0.** The maximum width of the SODIMM modules is 1". For a list of approved SDRAM modules contact your Distributur or FAE.

3. Install the processor. Pin 1 (marked with a chamfered corner and possibly a dot) shall be opposite to the power connector on 786LCD/S, /ST and /MG boards and closest to the power connector on the 786LCD/3.5" board. Use a screwdriver or CPU lock tool (available from Kontron Technology) as indicated to lock the CPU in place, the tab at the arrow (below) must be closed (figure 1). Place CPU lock (shipped with board) to secure the CPU socket from opening.

Mounting on 786LCD/S, /ST and /MG Board

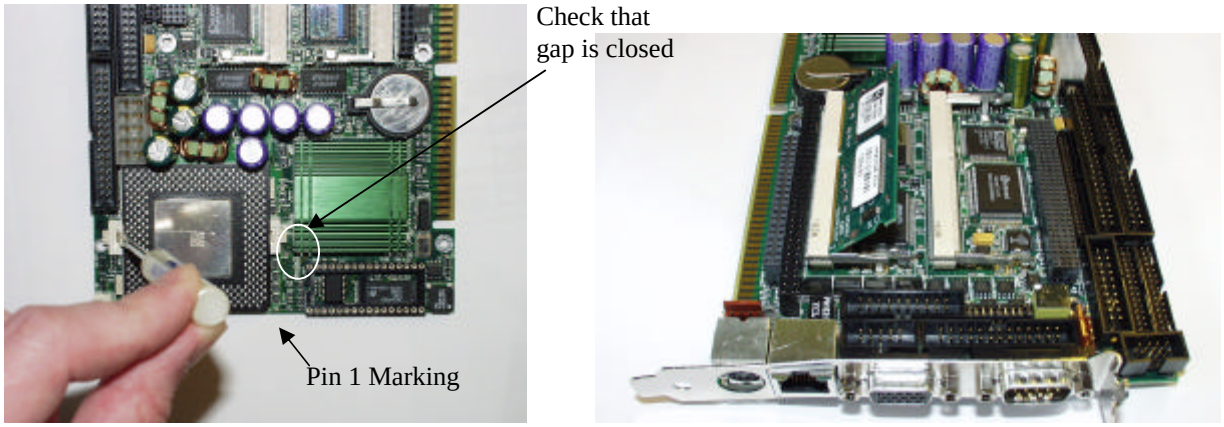
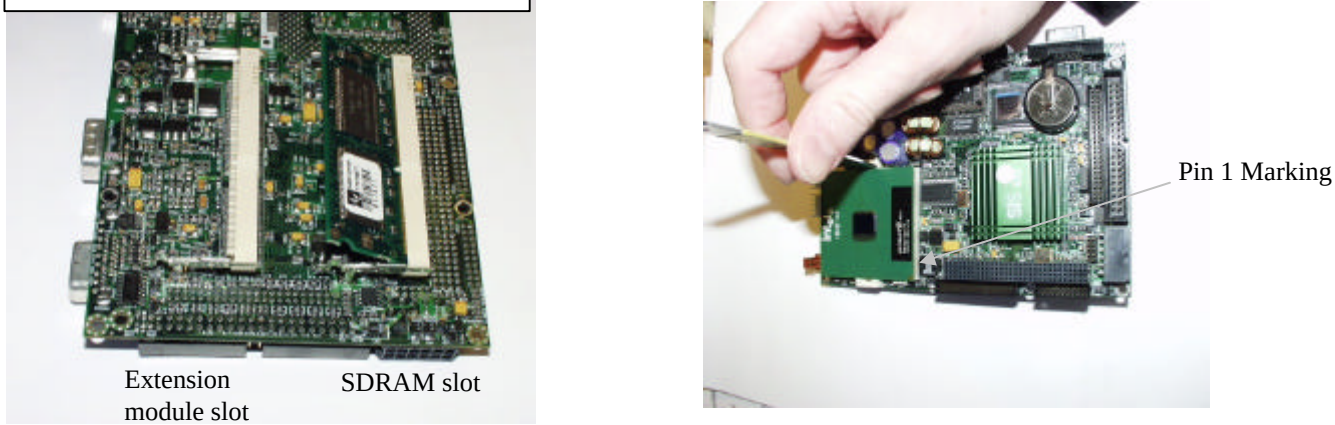


Fig.1

Mounting on 786LCD/3.5" Board



4. Mount the Fan on the top of the processor and connect it to the JPFAN connector.

5. Insert all external cables for hard disk, floppy, keyboard etc. except for flat panel. **A CRT monitor must be connected in order to change CMOS settings to flat panel support**. To achieve UDMA-66 performance on the IDE interface (and UDMA-100 on 786LCD/ST), 80poled UDMA cables **must** be used. If using the IDE_Two connector care should be taken in correct orientation when attaching the female cable. The cables that Kontron provide do not have a key. There is possibility of damage to the HDD or PCB if the cable is not orientated correct.

6. Connect power supply to the board by the PWRCON connector and insert the board in a backplane if required. The PWRCON **must** be used for proper board operation. For 786LCD/S, /ST and /MG boards the –12V can be supplied through the Blue wire shipped with the Power Supply Cable, but is only used for supplying external ISA devices.

7. Turn on the power.

8. Enter the BIOS setup by pressing the "F2" key during boot up. Setup the Processor clock speed in the Main menu. Refer to the Software Manual for details.

9. If Flat Panel Display is to be utilised, make sure the Panel type and Panel voltage in the BIOS setup in the Inside Utilities menu is correct before turning off the power and connecting the display cable.

Note: In case of corrupt CMOS settings the board may display an error message followed by "Press F1 to continue". To clear the non-PnP part of the CMOS (ESCD area – Extended System Configuration Data area) enter the Advanced menu and set "Reset Configuration Data" to *Yes*.
To reset the CMOS settings to BIOS defaults, press the Escape key during boot.
To clear all CMOS settings, including Password protection, remove the battery for approximately 1 minute then reinsert it.

2.3 Requirement according to EN60950 :

Users of 786LCD boards should take care when designing chassis interface connectors in order to fulfill the EN60950 standard :

When an interface/connector has a VCC (or other power) pin, that is directly connected to the VCC (or other) plane :

To protect the external power lines of peripheral devices the customer has to take care about :

- That the wires have the right diameter to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

Lithium Battery precautions:

CAUTION! Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by manyfacturer. Dispose of used batteries according to the manufacturer's instructions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

3. System specification

3.1 Configuration overview

Model	786LCD/S	786LCD/MG	786LCD/3.5”	786LCD/ST
Processor	Intel Celeron (Mendocino) Intel Celeron (CuMine) Intel Pentium III (CuMine)	Intel Celeron (Mendocino) Intel Celeron (CuMine) Intel Pentium III (CuMine)	Intel Celeron (Mendocino) Intel Celeron (CuMine) Intel Pentium III (CuMine)	Intel Celeron (CuMine) Intel Pentium III (CuMine) Intel Pentium III (Tualatin) VIA C3 Ezra-T
Processor frequency	up to 1 GHz	up to 1 GHz	up to 1 GHz	up to 1.4 GHz
Front Side Bus	66/100 MHz	66/100 MHz	66/100/133 MHz	66/100/133 MHz
Chipset				
Memory SDRAM	2 pcs. SODIMM	2 pcs. SODIMM	1 pcs. SODIMM	2 pcs. SODIMM
Memory speed	66/100 MHz	66/100 MHz	66/100/133 MHz	66/100/133 MHz
Suspend to RAM	Yes	Yes	Yes	Yes
IDE Ultra DMA66	2 x 2 drives	2 x 2 drives	2 x 2 drives	2 x 2 drives (UDMA-100)
PC99 compliant	Yes	Yes	Yes	Yes
PCI 2.2 compliant	Yes	Yes	Yes	Yes
Graphics	128 Bit 3D accelerator	128 Bit 3D accelerator	128 Bit 3D accelerator	128 Bit 3D accelerator
AGP 2.0 compliant	Yes	Yes	Yes	Yes
Video Memory (Shared)	Up to 64 MB SDRAM	Up to 64 MB SDRAM	Up to 64 MB SDRAM	Up to 64 MB SDRAM
Analog Video resolution	Up to 1920x1440, 16bit colors	Up to 1920x1440, 16bit colors	Up to 1920x1440, 16bit colors	Up to 1920x1440, 16bit colors
DVD	Hardware accelerated	Hardware accelerated	Hardware accelerated	Hardware accelerated
DirectX compliant	Yes	Yes	Yes	Yes
Parallel Panel support	TFT 24 bit	TFT 24 bit	TFT 24 bit	TFT 24 bit
Panellink, DFP, DVI, LVDS.	Video Interface modules	Video Interface modules	Video Interface modules	Video Interface modules
Dual CRT controller	Video Interface module	Video Interface module	Video Interface module	Video Interface module
Communication				
Ethernet	10Base-T / 100Base-TX	10Base-T / 100Base-TX	10Base-T / 100Base-TX	10Base-T / 100Base-TX
Wake on LAN	Yes	Yes	Yes	Yes
Serial ports	3*RS232, 1*RS232/485	3*RS232, 1*RS232/485	2*RS232	3*RS232, 1*RS232/485
Parallel port	STD / ECP / EPP	STD / ECP / EPP	STD / ECP / EPP	STD / ECP / EPP
USB channels	2 channel onboard 3 ch.on Bracket Module	2 channel onboard 3 ch.on Bracket Module	2 channel onboard 3 ch.on Bracket Module	2 channel onboard 3 ch.on Bracket Module
IrDA v.1.1, Customer IR	Bracket Module	Bracket Module	Bracket Module	Bracket Module
Sound				
AC97/98	Yes	Yes	Yes	Yes
SoundBlaster PRO/16 compliant	Yes	Yes	Yes	Yes
DirectSound compliant	Yes	Yes	Yes	Yes
VirtualAC3 surround sound	Bracket Module	Bracket Module	Bracket Module	Bracket Module
SPDIF Interface	Bracket Module	Bracket Module	Bracket Module	Bracket Module

Other				
ISAMAX	Yes Limited ISA Support	Yes Limited ISA Support	No ISA	Yes Full ISA Support
PC104	PC104+ Limited ISA Support	PC104 Limited ISA Support	PCI only	PC104+ Full ISA Support
M-System	Yes	Yes	No	Yes
Compact Flash	Yes; Type I	Yes; Type I	Yes; Type I, II	Yes; Type I, II
Supervision, voltages, fan, temperature, watchdog	Yes	Yes	Yes	Yes
SCSI	No	Ultra2, 80MB/s	No	No
Firewire, IEEE1394	No	2 ch. 400Mbps.	No	No
BIOS	Phoenix / KONTRON	Phoenix / KONTRON	Phoenix / KONTRON	Phoenix / KONTRON
Power Management	ACPI 1.0, APM 1.2	ACPI 1.0, APM 1.2	ACPI 1.0, APM 1.2	ACPI 1.0, APM 1.2
EMI	EN-55022/ EN-50082	EN-55022/ EN-50082	EN-55022/ EN-50082	EN-55022/ EN-50082
Operating Temp.	0 - 60 °C.	0 – 60 °C.	0 – 60 °C.	0 - 60 °C.
Dimensions	190 x 123 mm 7.4" x 4.8"	250 x 123 mm 9.8" x 4.8"	145 x 102 mm 5.7" x 4.0"	190 x 123 mm 7.4" x 4.8"

3.2 Component main data

The main data for the functions and components on the board are listed below. Availability of some of the features depends on the configuration as listed above. For further details, refer to chapter 3.4 and the connector definitions in chapter 5.

Processor	Socket 370 based : Intel Celeron Mendocino, Intel Celeron CuMine, Intel Pentium III CuMine, Intel Pentium III Tualatin and VIA C3 Ezra-T supported depending on board type. Please refer to processor support table in section 3.3.
Core Chipsets	SiS630 Single Chipset and SiS950 Super I/O.
SDRAM memory	1 or 2 pcs. SODIMM 144 pin sockets. Support memory bus speeds 66/100/133 MHz (Board specific). Size: Up to 1.0 GB supported, but only 512MB support verified due to availability of SDRAM. (Board specific). Synchronous Host/DRAM clock scheme. Suspend-to-RAM (STR) support. Two programmable PCI hole areas. Operating voltage: 3.3V.
Graphics	Advanced hardware 2D/3D 128 bit Video/Graphics Accelerators. UltraAGP, AGP 4x-like performance with up to 2 GB/s memory bandwidth. AGP v.2.0 compliant. Tightly coupled 64 bits 133 MHz host interface to VGA with pipelined process to speed up GUI performance and video playback frame rate. Up to 64 MB shared system memory area. Peak polygon rate : 4M polygon/s @ 1 pixel/polygon with 16 bpp, bilinear textured, Z buffered and alpha blended. Supports up to 2048x2048 texture size. Built-in 8 KB texture cache. Supports Flat and Gouraud shading. Supports 16/24/32 bpp Z buffer integer/floating formats. Supports MIPMAP with point-sampled, linear and tri-linear texture filtering. Supports Fogging and Alpha blending. Supports Specula lighting. Support full scene anti-aliasing. Build-in hardware DVD accelerator. MPEG-2 ISO/IEC 13818-2 MP@ML and MPEG-1 ISO/IEC 11172-2 standards compliant.

	Supports direct DVD to TV playback. Supports RBG555, RGB565, YUV422 and YUV420 video playback formats. Supports VESA standard super high resolution graphic modes : • 640x480 16/256/32K/64K/16M colors 120 Hz NI. • 800x600 16/256/32K/64K/16M colors 120 Hz NI. • 1024x768 256/32K/64K/16M colors 120 Hz NI. • 1280x1024 256/32K/64K/16M colors 120 Hz NI. • 1600x1200 256/32K/64K/16M colors 100 Hz NI. • 1920x1200 256/32K/64K/16M colors 80 Hz NI. Supports virtual screen up to 4096x4096. Built-in programmable 24-bit true-color RAMDAC with up to 270 MHz pixel clock. Support DDC1, DDC2B and DDC3.0 specifications. Built-in secondary graphic controller for independent secondary : • CRT • LCD via parallel interface. • LCD via Panellink or LVDS interface. • TV digital output. Fully DirectX 8.1 compliant. Supports DCI drivers. Support Direct Draw drivers.
PCI IDE controller	Supports PCI bus mastering. Ultra DMA 33/66 MHz (786LCD/S, /MG, /3.5") Ultra DMA 100 MHz (786LCD/ST) PIO mode 0, 1, 2, 3, 4. Multiword DMA mode 0, 1, 2. Two independent IDE channels each with 16 DW FIFO. Connectors for direct support of 3½" and 2½" drives.
Ethernet	Supports 10Base-T and 100base-TX High performance 32-bit PCI bus master architecture with integrated DMA controller for low CPU and bus utilization. IEEE 802.3 and 802.3u standard compatible. Full and half-duplex mode for both 10 and 100 Mbps. Wake on LAN support.
USB	OpenHCI host controller with root hub. Two independent USB host controllers with 5 USB channels together. 12 Mb bandwidth for each host controller.

Audio	AC97/98 support with full duplex, independent sample rate converter for audio recording and playback. SoundBlaster Pro/16 compatible. 32-Voice DirectSound 3D accelerator with IID, IAD and Doppler effects on 3D positional audio buffer. VirtualAC3 support with external circuit. SPDIF output. Complete DirectX driver suite for Win 98/2000/XP.
SCSI	Symbios SYM53C895A controller. High performance SCSI core. Supports wide Ultra2 SCSI synchronous transfers up to 80MB/s. Performs PCI zero wait-state bus master data bursts faster than 110MB/s (@ 33MHz). Universal transceivers supports Low Voltage Differential and High Voltage Single-ended devices.
Firewire, IEEE1394	NEC µPD72872controller. 2 channels with up to 400Mbps. Compliant with Link Layer Services as described in IEEE1394 rel. 1.0. Compliant with Physical Layer Services and Protocol enhancement as described in P1394a draft 2.0. Built-in transmit and receive FIFO'es (1024/2048 bytes). Supports PCI 32bit Master mode interface. Driver support for Win98, Win2K, WinXP (not WinNT)
On-board Peripheral interfaces	AT-keyboard interface, PS/2 mouse interface, 1xRS232 or RS422/485 interface. 3xRS232 ports. All RS232/RS485 ports are controlled by NS16550 comp. UART. 1 x Parallel printer interface (Centronic, ECP, EPP mode). Floppy drive interface (2 x 360kB to 2.88MB). Compact flash connector for flash disk.
Supervision	Supervision of power supplies, including 10 different voltages. Fan monitoring and control (PWM). Temperature supervision of CPU. A watchdog timer is provided to reboot in case of system lockup.
Real-Time-Clock and CMOS memory	System configuration, date and time are maintained by CMOS memory with battery backup. SecureCMOS option for Flash backup of system configuration data.
M-systems Disk on Chip	A DIP32 socket is provided to support the M-systems Disk on Chip 2000 flash disk system (Board specific).

ISA-bus	The ISA bus is made available on the Edge connector and by the PC104 bus connector. *Note: For 786LCD/S and /MG the ISA bus supports only 8 Bit I/O and Memory cycles. (See 5.17.4 ISA Bus limitation.)* *For 786LCD/ST the ISA support complies to IEEE-996, but it limited in bandwidth for 16-bit transfers.*
PCI-bus	A PC104+ extension compliant to the *PC104Plus Specification v1.0* provides a PCI bus with support for up to 3 bus masters. The bus operates at 3.3V signal levels. A 5V supply is provided in the connector. 3.3V supply is provided for light loads.
BIOS	Phoenix PICO BIOS v. 4.0. KONTRON Technology BIOS extensions.
Plug and Play features	PCI and ISA plug and play provided by BIOS On-board I/O devices are reallocated if other devices are found.
Power supply	External power supplies: VCC Supply: +5V +5%/-2.5% VCC3V3 Supply +3.3V +5%/-5% (786LCD/3.5” only) Onboard +/-12V supplies for internal use.
Power Consumption	Approximately 25-35 W depending on CPU and clock speed selected.
Battery	Exchangeable 3.0V Lithium battery for onboard RTC. Manufacturer Toshiba / Part-number CR2032. Approximate 9 years retention. **CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer’s instructions.**
Environmental Conditions	**Operating**: 0°C – 60°C operating temperature (forced cooling). It is the customer’s responsibility to provide sufficient airflow to/from the board. 10% - 90% relative humidity (non-condensing) **Storage**: -10°C – 85°C 5% - 95% relative humidity (non-condensing)
EMI	All Peripheral interfaces intended for connection to external equipment are EMI protected.

3.3 Processor support table.

Speed	Code Names	Intel Single Pack Product Order Code	Intel OEM Product Order Code	786LCD/3.5"	786LCD/MG	786LCD/S	786LCD/ST
Intel® Pentium® Processors							
1.40 GHz with 133 MHz FSB	Tualatin	BX80530C1400512	RK80530KZ017512	no	no	no	yes
1.26 GHz with 133 MHz FSB*	Tualatin	BX80530C1266512	RK80530KZ012512	no	no	no	yes
1.20 GHz with 133 MHz FSB	Tualatin	BX80530C1200256	RK80530PZ009256	no	no	no	yes
1.13 GHz with 133 MHz FSB	Tualatin	BX80530C1133512	RK80530KZ006512	no	no	no	yes
1.13 GHz with 133 MHz FSB	Tualatin	BX80530C1133256	RK80530PZ006256	no	no	no	yes
1.10 GHz with 100 MHz FSB	Coppermine	N/A	RB80526PY005256	no	no	no	yes
1 GHz with 133MHz FSB*	Coppermine	BX80526C1000256	RB80526PZ001256	yes	yes	no	yes
1 GHz with 100 MHz FSB*	Coppermine	N/A	RB80526PY001256	yes	yes	yes	yes
933MHz with 133 MHz FSB	Coppermine	BX80526C933256E	RB80526PZ933256	yes	yes	no	yes
900 MHz with 100MHz FSB	Coppermine	N/A	RB80526PY900256	yes	yes	yes	yes
866MHz with 133 MHz FSB*	Coppermine	BX80526C866256E	RB80526PZ866256	yes	yes	no	yes
850MHz with 100 MHz FSB*	Coppermine	BX80526F850256E	RB80526PY850256	yes	yes	yes	yes
800MHz with 133 MHz FSB	Coppermine	BX80526C800256E	RB80526PZ800256	yes	yes	no	yes
800MHz with 100 MHz FSB	Coppermine	BX80526F800256E	RB80526PY800256	yes	yes	yes	yes
750MHz with 100 MHz FSB	Coppermine	BX80526F750256E	RB80526PY750256	yes	yes	yes	yes
733MHz with 133 MHz FSB*	Coppermine	BX80526F733256E	RB80526PZ733256	yes	yes	no	yes
700MHz with 100 MHz FSB*	Coppermine	BX80526F700256E	RB80526PY700256	yes	yes	yes	yes
667MHz with 133 MHz FSB	Coppermine	BX80526F667256E	RB80526PZ667256	yes	yes	no	yes
650MHz with 100 MHz FSB	Coppermine	BX80526F650256E	RB80526PY650256	yes	yes	yes	yes
600MHz with 133 MHz FSB	Coppermine	BX80526C600256E	RB80526PZ600256	yes	yes	no	yes
600MHz with 100 MHz FSB*	Coppermine	BX80526F600256E	RB80526PY600256	yes	yes	yes	yes
550MHz with 100 MHz FSB	Coppermine	BX80526F550256E	RB80526PY550256	yes	yes	yes	yes
533MHz with 133 MHz FSB	Coppermine	BX80526F533256E	RB80526PZ533256	yes	yes	no	yes
500MHz with 100 MHz FSB	Coppermine	BX80526F500256E	RB80526PY500256	yes	yes	yes	yes
Intel® Celeron® Processors							
1.3 GHz with 100 MHz FSB	Tualatin	BX80530F1300256	RK80530RY013256	no	no	no	yes
1.2 GHz with 100 MHz FSB*	Tualatin	BX80530F1200256	RK80530RY009256	no	no	no	yes
1.10A GHz with 100 MHz FSB	Tualatin	BX80530F1100256	RK80530RY005256	no	no	no	yes
1.1 GHz with 100 MHz FSB	Coppermine	BX80526F1100128	RB80526RY005128	yes	yes	yes	yes
1A GHz with 100 MHz FSB	Tualatin	BX80530F1000256	RK80530RY001256	no	no	no	Yes
1.0 GHz with 100 MHz FSB	Coppermine	BX80526F1000128	RB80526RY001128	yes	yes	yes	yes
950 MHz with 100 MHz FSB	Coppermine	BX80526F950128	RB80526RY950128	yes	yes	yes	yes
900 MHz with 100 MHz FSB	Coppermine	BX80526F900128	RB80526RY900128	yes	yes	yes	yes
850 MHz with 100 MHz FSB*	Coppermine	BX80526F850128	RB80526RY850128	yes	yes	yes	yes
800 MHz with 100 MHz FSB	Coppermine	BX80526F800128	RB80526RX800128	yes	yes	yes	yes
766 MHz with 66 MHz FSB	Coppermine	BX80526F766128	RB80526RX766128	yes	yes	yes	yes
733 MHz with 66 MHz FSB*	Coppermine	BX80526F733128	RB80526RX733128	yes	yes	yes	yes
700 MHz with 66 MHz FSB	Coppermine	BX80526F700128	RB80526RX700128	yes	yes	yes	yes
667 MHz with 66 MHz FSB	Coppermine	BX80526F667128	RB80526RX667128	yes	yes	yes	yes
633 MHz with 66 MHz FSB	Coppermine	BX80526F633128	RB80526RX633128	yes	yes	yes	yes
600 MHz with 66 MHz FSB	Coppermine	BX80526F600128	RB80526RX600128	yes	yes	yes	yes
566 MHz with 66 MHz FSB*	Coppermine	BX80526F566128	RB80526RX566128	yes	yes	yes	yes
533 MHz with 66 MHz FSB	Mendocino	BX80524P533128	FV80524RX533128	yes	yes	yes	no
500 MHz with 66 MHz FSB	Mendocino	BX80524P500128	FV80524RX500128	yes	yes	yes	no
466 MHz with 66 MHz FSB	Mendocino	BX80524P466128	FV80524RX466128	yes	yes	yes	no
433 MHz with 66 MHz FSB*	Mendocino	BX80524P433128	FV80524RX433128	yes	yes	yes	no
400 MHz with 66 MHz FSB	Mendocino	BX80524P400128	FV80524RX400128	yes	yes	yes	no
366 MHz with 66 MHz FSB*	Mendocino	BX80524P5366128	FV80524RX366128	yes	yes	yes	no
333 MHz wih 66 MHz FSB	Mendocino	BX80524P333128	FV80524RX333128	yes	yes	yes	no
300 MHz with 66 MHz FSB	Mendocino	BX80524P300128	FV80524RX300128	yes	yes	yes	no
VIA Processors							
VIA C3 Ezra-T 800/133MHz	Ezra-T			No	No	No	Yes
VIA C3 Ezra-T 866/133MHz	Ezra-T			No	No	No	Yes
VIA C3 Ezra-T 933/133MHz	Ezra-T			No	No	No	Yes

*) Intel Embedded Processor

Notes:

1.) Not all processors listed have been verified on the 786LCD series boards.

2.) Early BIOS version may not be prepared for showing correct CPU clock speed during boot. In all cases CPU will run at correct clock speed with FSB setup, no matter the displayed frequency.

3.) Processors above 1GHz may have restricted operating temperature range depending on the cooler used from Kontron.

3.4 System overview

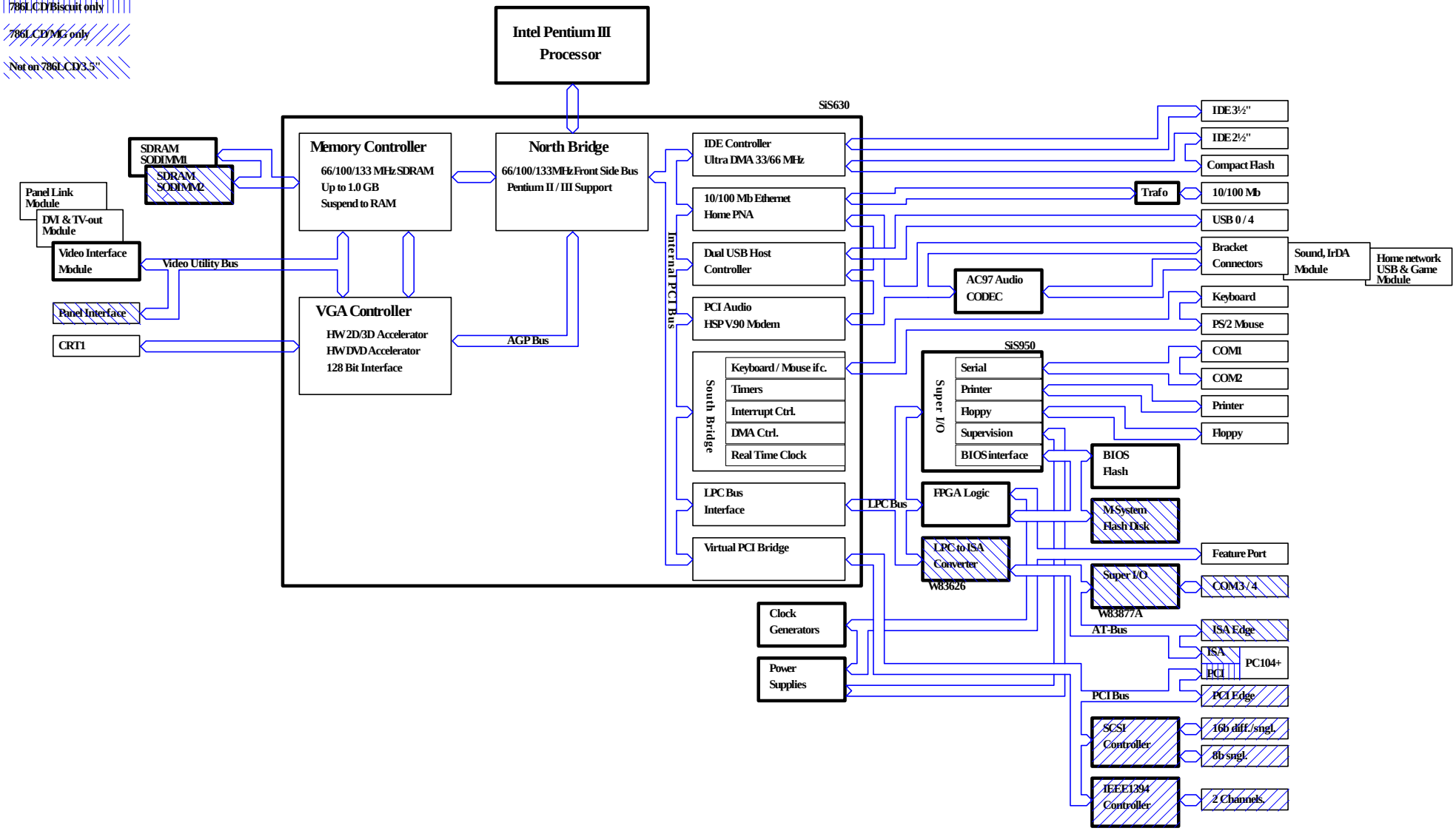
The block diagram below shows the architecture and main components of the 786LCD boards.

The two key components on the board are the SiS 630 Chipset and the SiS 950 companion chip.

All shaded components are optional and are therefore only provided in some configurations.

The following sections will provide additional details about the functions of the board, shaded paragraphs indicate that the availability will depend on the model; check the differences in section 3.1.

786LCD Family Block Diagram



3.4.1 Processor.

The 786LCD/S, /MG and /3.5" boards are designed to operate with Intel Celeron (Mendocino and CuMine) and Intel Pentium III (CuMine) processors. The 786LCD/ST is designed to operate with Intel Celeron (CuMine), Intel Pentium III (CuMine and Tualatin) and VIA C3 Ezra-T processors. The boards are equipped with a screwdriver actuated Socket370 designed for Intels PGA370 housed processors.
The processor interfaces the chipset though a GTL+ or AGTL+ (Pentium III) bus. The processor Front Side Bus can operate at frequencies of 66, 100 or 133 MHz. The processor core frequency is set by a internally hard-strapped multiplier.

3.4.2 SiS630 Chipset.

The SiS630 is one of the most integrated chipset available on the market. The chipset is manufactured in a 0.18u process to keep power consumption low.
The SiS630 chipset integrates :

- Celeron / Pentium III (Tualatin on 786LCD/ST) host bus interface.
- VGA controller with HW accelerator for 2D/3D and DVD.
- Memory controller for SDRAM support up to 1GB.
- IDE Controller, Ultra DMA 33/66(/100 on 786LCD/ST).
- 10/100Mb Ethernet with integrated PHY.
- Dual USB host controller with support of totally 5 USB channels.
- PCI Audio controller.
- PCI South Bridge.
- Virtuel PCI Bridge to allow externally connected PCI devices.
- LPC (Low Pin Count) interface.

3.4.3 SDRAM interface.

The 786LCD boards include 1 or 2 pcs. SODIMM144 connectors for support of SDRAM memory modules. The module supply is 3.3V and the memory speed can be either 66, 100 or 133 MHz.
The DRAM controller supports modules based on 16Mb, 64Mb, 128Mb, 256Mb or 512Mb SDRAM technology (only up to 256MB modules are currently qualified).
NOTE: that limitations apply to the SDRAM support; request details from Kontron Technology.
The main memory also contains the VGA memory. The VGA controller is tightly coupled to the DRAM controller through a highly optimized arbitration unit. The VGA memory size can be selected from 2MB to 64MB.
The boards supports Suspend to RAM feature, where the complete operating system can close down with all previous settings stored in SDRAM, while the rest of the board is powered down. Extremely fast restart is possible from this Suspend mode.

3.4.4 VGA Controller.

Controller

The SiS630 chipset integrates a powerful graphic controller. The graphic controller is connected through an internal AGPx2 bus. The controller has a 128 bit engine with hardware 2D/3D accelerators. The controller also includes a hardware assisted DVD decoder, which enables smooth video playback with minimal CPU load. The graphic controller uses up to 64MB memory from system memory as video memory. A tightly coupled interface to the DRAM controller ensures performance as high as normally only seen with separate video frame buffer memory. The controller has the capability two drive two separate display devices with individual images. The second display device can be either CRT, parallel connected flat panel, Panellink or LVDS connected flat panel, Television or DVI equipped display devices.

Panel interfaces

The 786LCD boards offer a very flexible interface for supporting flat panels and other devices. The graphic controller outputs data for the second display device on the Video Utility Bus. This bus can be used for the following options :

- 24 bit TFT flat panels can be connected directly in parallel to the Video Utility Bus through the 50-pin PANEL connector on the 786LCD/S, /MG and /ST boards and through the LCDADPT module (inserted in the SODIMM144 connector) on the 786LCD/3.5” boards..

A Video Module Connector (SODIMM144) is located on the backside of the board in the bracket end. Different Video Modules can be installed for various interfaces :

- A SiS301 based Video Module supports DVI connector (CRT2 and Panellink) and TV-out in Composite or S-Video format.
- Silicon Image Panellink Transmitter module for internal or external connection of Panellink interfaced flat panels.
- Texas / National LVDS Transmitter module for internal or external connection of LVDS interfaced flat panels.

3.4.4.1 Supported Video Resolutions.

The supported resolutions depend on various parameters:

1. Memory clock speed (66/100/133MHz).
2. Selected mode in O/S Driver:
   - Single display mode
   - Mirror display mode
     - Primary display
     - Secondary display
   - Multiple display mode *
     - Primary display
     - Secondary display

Please note that certain restrictions exist for resolution and colour depth when playing MPEG2 formats. To support DVD HW playback the sufficient bandwidth is required. There are three factors which determine the bandwidth: resolution, refresh rate and colordepth.
Modes marked with bold text support HW DVD playback capability.
Please note that in multiple display mode, DVD playback is only supported on the primary display device, and not on the secondary device.

*Multiple display mode is not supported for Win2000 and WinNT.

The tables below list the supported resolutions with the given conditions.

	System Memory Clock=66Mhz **Video memory size=8MB or above.**					
Single Display Output Mode	**Resolution**	**Bpp**	**CRT1 at single mode**	**CRT2 at single mode**	**LCD at single mode**	**TV-out at single mode**
	640x480	8	60 72 75 85 100 120 160 200	60 72 75 85 100 120 160 200	60 70 75	60 (NTSC) or 50 (PAL)
		16	60 72 75 85 100 120 160 200	60 72 75 85 100 120 160 200	60 70 75	60 (NTSC) or 50 (PAL)
		32	60 72 75 85 100 120 160	60 72 75 85 100	60 70 75	60 (NTSC) or 50 (PAL)
	800x600	8	56 60 72 75 85 100 120 160	56 60 72 75 85 100 120 160	60 70 75	60 (NTSC) or 50 (PAL)
		16	56 60 72 75 85 100 120 160	56 60 72 75 85 100 120 160	60 70 75	60 (NTSC) or 50 (PAL)
		32	56 60 72 75 85 100 120	56 60 72 75	60 70 75	60 (NTSC) or 50 (PAL)
	1024x768	8	43 60 70 75 85 100 120	60 70 75 85 100 120	60 70 75	
		16	43 60 70 75 85 100 120	60 70 75 85 100	60 70 75	
		32	43 60 70 75			
	1280x1024	8	43 60 75 85	60	60	
		16	43 60 75 85			
		32	43			
	1600x1200	8	60 65 70 75 85			
		16	60			
	1920x1440	8	60			

Mirror Display Output Mode

System Memory Clock=66Mhz **Video memory size=8MB or above.**			
CRT2 selected as secondary display.			
Resolution	**Bpp**	**CRT1 at Mirror mode**	**CRT2 at Mirror mode**
640x480	8	60 72 75 85 100 120 160 200	60 72 75 85 100 120 160 200
	16	60 72 75 85 100 120 160	60 72 75 85 100 120
	32	60 72 75 85	60
800x600	8	56 60 72 75 85 100 120 160	56 60 72 75 85 100 120 160
	16	56 60 72 75 85 100 120	56 60 72 75 85
1024x768	8	43 60 70 75 85 100 120	60 70 75 85 100
LCD selected as secondary display.			
Resolution	**Bpp**	**CRT1 at Mirror mode**	**LCD at Mirror mode**
640x480	8	60 72 75 85 100 120 160 200	60 70 75
	16	60 72 75 85 100 120 160 200	60 70 75
	32	60 72 75 85 100	60
800x600	8	56 60 72 75 85 100 120 160	60 70 75
	16	56 60 72 75 85 100 120	60 70 75
1024x768	8	43 60 70 75 85 100 120	60 70 75
TV-Out selected as secondary display.			
Resolution	**Bpp**	**CRT1 at Mirror mode**	**TV-out at Mirror mode**
640x480	8	60 72 75 85 100 120 160 200	60 (NTSC) or 50 (PAL)
	16	60 72 75 85 100 120 160 200	60 (NTSC) or 50 (PAL)
800x600	8	56 60 72 75 85 100 120 160	60 (NTSC) or 50 (PAL)
	16	56 60 72 75 85 100 120	60 (NTSC) or 50 (PAL)

Multiple Monitor Output Mode

System Memory Clock=66Mhz **Video memory size=8MB or above.**			
CRT2 selected as secondary display.			
Resolution	**Bpp**	**CRT1 at MM mode**	**CRT2 at MM mode**
640x480	8	60 72 75 85 100 120 160 200	60 72 75 85 100 120 160 200
	16	60 72 75 85 100 120 160	60 72 75 85 100 120
	32	60 72 75 85	60
800x600	8	56 60 72 75 85 100 120 160	56 60 72 75 85 100 120 160
	16	56 60 72 75 85 100 120	56 60 72 75 85
	32	56 60	
1024x768	8	43 60 70 75 85 100 120	60 70 75 85 100
	16	43 60 70 75	
1280x1024	8	43 60 75 85	
	16	43	
1600x1200	8	60	
LCD selected as secondary display.			
Resolution	**Bpp**	**CRT1 at MM mode**	**LCD at MM mode**
640x480	8	60 72 75 85 100 120 160 200	60 70 75
	16	60 72 75 85 100 120 160 200	60 70 75
	32	60 72 75 85 100	60
800x600	8	56 60 72 75 85 100 120 160	60 70 75
	16	56 60 72 75 85 100 120	60 70 75
	32	56 60	0
1024x768	8	43 60 70 75 85 100 120	60 70 75
	16	43 60 70 75	
	32	43	
1280x1024	8	43 60 75 85	
	16	43	
1600x1200	8	60 65	

Cont'd

Multiple Monitor Output	TV-Out selected as secondary display.			
	Resolution	**Bpp**	**CRT1 at MM mode**	**TV-out at MM mode**
	640x480	8	60 72 75 85 100 120 160 200	60 (NTSC) or 50 (PAL)
		16	60 72 75 85 100 120 160 200	60 (NTSC) or 50 (PAL)
		32	60 72 75 85 100	
	800x600	8	56 60 72 75 85 100 120 160	60 (NTSC) or 50 (PAL)
		16	56 60 72 75 85 100 120	60 (NTSC) or 50 (PAL)
		32	56 60	
	1024x768	8	43 60 70 75 85 100 120	
		16	43 60 70 75	
		32	43	
	1280x1024	8	43 60 75 85	
		16	43	
	1600x1200	8	60 65	

Single Display Output Mode	**System Memory Clock=100Mhz** **Video memory size=16MB or above.**					
	Resolution	**Bpp**	**CRT1 at single mode**	**CRT2 at single mode**	**LCD at single mode**	**TV-out at single mode**
	640x480	8	**60 72 75 85 100 120 160** 200	**60 72 75 85** 100 120 160 200	**60 70 75**	**60** (NTSC) or **50** (PAL)
		16	**60 72 75 85 100 120 160** 200	**60 72 75 85** 100 120 160 200	**60 70 75**	**60** (NTSC) or **50** (PAL)
		32	**60 72 75 85 100 120 160** 200	**60 72 75 85** 100 120 160	**60 70 75**	**60** (NTSC) or **50** (PAL)
	800x600	8	**56 60 72 75 85 100 120** 160	**56 60 72 75 85** 100 120 160	**60 70 75**	**60** (NTSC) or **50** (PAL)
		16	**56 60 72 75 85 100 120** 160	**56 60 72 75 85** 100 120 160	**60 70 75**	**60** (NTSC) or **50** (PAL)
		32	**56 60 72 75 85 100 120** 160	**56 60 72 75 85** 100 120	**60 70 75**	**60** (NTSC) or **50** (PAL)
	1024x768	8	43 **60 70 75 85 100** 120	**60 70 75 85** 100 120	**60 70 75**	
		16	43 **60 70 75 85 100** 120	**60 70 75 85** 100 120	**60 70 75**	
		32	43 **60 70 75 85 100**	**60 70 75**	**60 70 75**	
	1280x1024	8	43 **60 75** 85	**60**	60	
		16	43 **60 75** 85	**60**	60	
		32	43 **60**			
	1600x1200	8	60 65 70 75 85			
		16	60 65 70 75 85			
	1920x1440	8	60			
		16	60			

Mirror Display Output Mode

System Memory Clock=100Mhz

Video memory size=16MB or above.

CRT2 selected as secondary display.

Resolution	Bpp	CRT1 at Mirror mode	CRT2 at Mirror mode
640x480	8	**60 72 75 85 100 120 160** 200	**60 72 75 85 100 120 160** 200
	16	**60 72 75 85 100 120 160** 200	**60 72 75 85 100 120 160** 200
	32	**60 72 75 85 100 120**	**60 72 75 85 100**
800x600	8	**56 60 72 75 85 100 120** 160	**56 60 72 75 85 100 120** 160
	16	56 60 72 75 85 100 120 160	56 60 72 75 85 100 120
	32	56 60 72 75 85	56 60
1024x768	8	43 60 70 75 85 100 120	60 70 75 85 100 120
	16	43 60 70 75 85 100	60 70 75

LCD selected as secondary display.

Resolution	Bpp	CRT1 at Mirror mode	LCD at Mirror mode
640x480	8	**60 72 75 85 100 120 160** 200	**60 70 75**
	16	**60 72 75 85 100 120 160** 200	**60 70 75**
	32	60 72 75 85 100 120 160	60 70 75
800x600	8	**56 60 72 75 85 100 120** 160	**60 70 75**
	16	**56 60 72 75 85 100 120** 160	**60 70 75**
	32	56 60 72 75 85	60
1024x768	8	43 **60 70 75 85 100** 120	**60 70 75**
	16	43 **60 70 75 85 100** 120	**60 70 75**

TV-Out selected as secondary display.

Resolution	Bpp	CRT1 at Mirror mode	TV-out at Mirror mode
640x480	8	**60 72 75 85 100 120 160** 200	**60** (NTSC) or **50** (PAL)
	16	**60 72 75 85 100 120 160** 200	**60** (NTSC) or **50** (PAL)
800x600	8	**56 60 72 75 85 100 120** 160	**60** (NTSC) or **50** (PAL)
	16	56 60 72 75 85 100 120 160	**60** (NTSC) or **50** (PAL)

Multiple Monitor Output Mode

System Memory Clock=100Mhz

Video memory size=16MB or above.

CRT2 selected as secondary display.

Resolution	Bpp	CRT1 at MM mode	CRT2 at MM mode
640x480	8	**60 72 75 85 100 120 160** 200	**60 72 75 85** 100 120 160 200
	16	**60 72 75 85 100 120 160** 200	**60 72 75 85** 100 120 160 200
	32	**60 72 75 85 100 120**	**60 72 75 85**
800x600	8	**56 60 72 75 85 100 120** 160	**56 60 72 75 85** 100 120 160
	16	56 60 72 75 85 100 120 160	**56 60 72 75 85** 100 120
	32	56 60 72 75 85	56 60
1024x768	8	43 60 70 75 85 100 120	**60 70 75 85** 100 120
	16	43 60 70 75 85 100	60 70 75
	32	43	
1280x1024	8	43 60 75 85	
	16	43 60	
1600x1200	8	60 65 70 75 85	
1920x1440	8	60	

Multiple Monitor Output Mode

LCD selected as secondary display.

Resolution	Bpp	CRT1 at MM mode	LCD at MM mode
640x480	8	**60 72 75 85 100 120 160** 200	**60 70 75**
	16	**60 72 75 85 100 120 160** 200	**60 70 75**
	32	**60 72 75 85 100 120** 160	60 70 75
800x600	8	**56 60 72 75 85 100 120** 160	**60 70 75**
	16	**56 60 72 75 85 100 120** 160	**60 70 75**
	32	56 60 72 75 85	60
1024x768	8	43 **60 70 75 85 100** 120	**60 70 75**
	16	43 60 70 75 85 100 120	60 70 75
	32	43 60	
1280x1024	8	43 60 75 85	
	16	43 60 75	
1600x1200	8	60 65 70 75 85	
1920x1440	8	60	

TV-Out selected as secondary display.

Resolution	Bpp	CRT1 at MM mode	TV-out at MM mode
640x480	8	**60 72 75 85 100 120 160** 200	**60** (NTSC) or **50** (PAL)
	16	**60 72 75 85 100 120 160** 200	**60** (NTSC) or **50** (PAL)
	32	**60 72 75 85 100 120** 160	
800x600	8	**56 60 72 75 85 100 120** 160	**60** (NTSC) or **50** (PAL)
	16	**56 60 72 75 85 100 120** 160	**60** (NTSC) or **50** (PAL)
	32	56 60 72 75 85	
1024x768	8	43 60 70 75 85 100 120	
	16	43 60 70 75 85 100 120	
	32	43 60	
1280x1024	8	43 60 75 85	
	16	43 60 75	
1600x1200	8	60 65 70 75 85	
1920x1440	8	60	

Single Display Output Mode

System Memory Clock=133Mhz

Video memory size=16MB or above.

Resolution	Bpp	CRT1 at single mode	CRT2 at single mode	LCD at single mode	TV-out at single mode
640x480	8	**60 72 75 85 100 120 160** 200	**60 72 75 85** 100 120 160 200	**60 70 75**	**60** (NTSC) or **50** (PAL)
	16	**60 72 75 85 100 120 160** 200	**60 72 75 85** 100 120 160 200	**60 70 75**	**60** (NTSC) or **50** (PAL)
	32	**60 72 75 85 100 120 160** 200	**60 72 75 85** 100 120 160 200	**60 70 75**	**60** (NTSC) or **50** (PAL)
800x600	8	**56 60 72 75 85 100 120** 160	**56 60 72 75 85** 100 120 160	**60 70 75**	**60** (NTSC) or **50** (PAL)
	16	**56 60 72 75 85 100 120** 160	**56 60 72 75 85** 100 120 160	**60 70 75**	**60** (NTSC) or **50** (PAL)
	32	**56 60 72 75 85 100 120** 160	**56 60 72 75 85** 100 120 160	**60 70 75**	**60** (NTSC) or **50** (PAL)
1024x768	8	43 **60 70 75 85 100** 120	**60 70 75 85** 100 120	**60 70 75**	
	16	43 **60 70 75 85 100** 120	**60 70 75 85** 100 120	**60 70 75**	
	32	43 **60 70 75 85 100** 120	**60 70 75 85** 100	**60 70 75**	
1280x1024	8	43 **60 75** 85	**60**	60	
	16	43 **60 75** 85	**60**	60	
	32	43 **60 75** 85	**60**	60	
1600x1200	8	60 65 70 75 85			
	16	60 65 70 75 85			
	32	60			
1920x1440	8	60			
	16	60			

Mirror Display Output Mode

System Memory Clock=133Mhz

Video memory size=16MB or above.

CRT2 selected as secondary display.

Resolution	Bpp	CRT1 at Mirror mode	CRT2 at Mirror mode
640x480	8	**60 72 75 85 100 120 160** 200	**60 72 75 85 100 120 160** 200
	16	**60 72 75 85 100 120 160** 200	**60 72 75 85 100 120 160** 200
	32	**60 72 75 85 100 120 160**	**60 72 75 85 100 120 160**
800x600	8	**56 60 72 75 85 100 120** 160	56 60 72 75 85 100 120 160
	16	**56 60 72 75 85 100 120** 160	56 60 72 75 85 100 120 160
	32	**56 60 72 75 85 100 120**	56 60 72 75 85
1024x768	8	43 **60 70 75 85 100** 120	60 70 75 85 100 120
	16	43 **60 70 75 85 100** 120	60 70 75 85 100

LCD selected as secondary display.

Resolution	Bpp	CRT1 at Mirror mode	LCD at Mirror mode
640x480	8	**60 72 75 85 100 120 160** 200	**60 70 75**
	16	**60 72 75 85 100 120 160** 200	**60 70 75**
	32	60 72 75 85 100 120 160 200	60 70 75
800x600	8	**56 60 72 75 85 100 120** 160	**60 70 75**
	16	**56 60 72 75 85 100 120** 160	**60 70 75**
	32	56 60 72 75 85 100 120	60 70 75
1024x768	8	43 **60 70 75 85 100** 120	**60 70 75**
	16	43 **60 70 75 85 100** 120	**60 70 75**

TV-Out selected as secondary display.

Resolution	Bpp	CRT1 at Mirror mode	TV-out at Mirror mode
640x480	8	**60 72 75 85 100 120 160** 200	**60** (NTSC) or **50** (PAL)
	16	**60 72 75 85 100 120 160** 200	**60** (NTSC) or **50** (PAL)
	32	**60 72 75 85 100 120 160** 200	**60** (NTSC) or **50** (PAL)
800x600	8	**56 60 72 75 85 100 120** 160	**60** (NTSC) or **50** (PAL)
	16	**56 60 72 75 85 100 120** 160	**60** (NTSC) or **50** (PAL)
	32	**56 60 72 75 85 100 120**	**60** (NTSC) or **50** (PAL)

Multiple Monitor Output Mode

System Memory Clock=133Mhz

Video memory size=16MB or above.

CRT2 selected as secondary display.

Resolution	Bpp	CRT1 at MM mode	CRT2 at MM mode
640x480	8	**60 72 75 85 100 120 160** 200	**60 72 75 85** 100 120 160 200
	16	**60 72 75 85 100 120 160** 200	**60 72 75 85** 100 120 160 200
	32	**60 72 75 85 100 120 160**	**60 72 75** 85 100 120
800x600	8	**56 60 72 75 85 100 120** 160	**56 60 72 75 85** 100 120 160
	16	**56 60 72 75 85 100 120** 160	**56 60 72 75** 85 100 120 160
	32	**56 60 72 75 85 100 120**	**56** 60 72 75 85
1024x768	8	43 **60 70 75 85 100** 120	**60 70 75 85** 100 120
	16	43 **60 70 75** 85 100 120	**60 70 75** 85 100
	32	43 **60 70 75**	
1280x1024	8	43 **60** 75 85	
	16	43 60 75 85	
	32	43	
1600x1200	8	60 65 70 75 85	
	16	60	
1920x1440	8	60	

Multiple Monitor Output Mode

LCD selected as secondary display.

Resolution	Bpp	CRT1 at MM mode	LCD at MM mode
640x480	8	**60 72 75 85 100 120 160** 200	**60 70 75**
	16	**60 72 75 85 100 120 160** 200	**60 70 75**
	32	**60 72 75 85 100 120** 160 200	**60 70 75**
800x600	8	**56 60 72 75 85 100 120** 160	**60 70 75**
	16	**56 60 72 75 85 100 120** 160	**60 70 75**
	32	**56 60 72 75** 85 100 120	**60 70 75**
1024x768	8	43 **60 70 75 85 100** 120	**60 70 75**
	16	43 **60 70 75 85** 100 120	**60 70 75**
	32	43 60 70 75	
1280x1024	8	43 **60 75** 85	
	16	43 60 75 85	
	32	43	
1600x1200	8	60 65 70 75 85	
	16	60 65	
1920x1440	8	60	

TV-Out selected as secondary display.

Resolution	Bpp	CRT1 at MM mode	TV-out at MM mode
640x480	8	**60 72 75 85 100 120 160** 200	**60** (NTSC) or **50** (PAL)
	16	**60 72 75 85 100 120** 160 200	**60** (NTSC) or **50** (PAL)
	32	**60 72 75 85 100** 120 160 200	**60** (NTSC) or **50** (PAL)
800x600	8	**56 60 72 75 85 100** 120 160	**60** (NTSC) or **50** (PAL)
	16	**56 60 72 75 85 100** 120 160	**60** (NTSC) or **50** (PAL)
	32	**56 60 72 75** 85 100 120	**60** (NTSC) or **50** (PAL)
1024x768	8	43 **60 70 75 85 100** 120	
	16	43 **60 70 75 85 100** 120	
	32	43 60 70 75	
1280x1024	8	43 **60 75** 85	
	16	43 60 75	
	32	43	
1600x1200	8	60 65 70 75 85	
	16	60 65	
1920x1440	8	60	

3.4.5 IDE interface.

The SiS630 chip provides a primary as well as a secondary IDE controller, which supports Ultra DMA33/66 mode and PCI bus mastering for the data transfer. PIO mode 0, 1, 2, 3, 4 and Multi Word DMA mode 0, 1, 2 is supported. The 786LCD/ST further supports Ultra DMA100 mode.
A standard IDC40 connector (2.54mm. pitch) is used for the primary controller and an IDC44 connector (2mm. pitch) for the secondary controller. There are currently no UDMA66/100 cable available for the secondary IDE 2mm connector limiting the maximum supported rate to UDMA33.
A compact flash connector on the backside of the board is also attached to the secondary controller.

3.4.6 Ethernet.

The Ethernet interface is based on the SiS630 internal Ethernet controller supporting 10MBit as well as 100Mbit Base-T interface.
The controller is attached to the PCI bus and uses PCI bus mastering for data transfer. The CPU is thereby not loaded during the actual transfer.
Network activity LED is located in the RJ45 connector.

3.4.7 USB interface.

Two separate USB OpenHCI Host controllers are integrated in the SiS630. The controllers supports together 5 USB channels. Two channels (one from each controller) are available in 2x4 pinrow for USB connector bracket attachment. The remaining 3 channels are available in the Bracket Connectors.
In order to meet the requirements of USB v.1.1 standard, the SB5V supply to the board must be at least 5.00V

3.4.8 Audio.

The SiS630 chip provides onboard audio support by means of an AC97 codec interface. The onboard audio codec provides mixing of the analog signals as well as Digital/analog conversion. The following analog interfaces are provided in the Bracket Connectors.

- Line-in, stereo.
- CR-ROM input, stereo.
- Microphone, single input with microphone bias circuit.
- Lineout, stereo.

By applying a Sound Bracket Module the signals can be accessed through standard audio phone plugs and additionally Speakerout (stereo) and SPDIF output will be available.
The SPDIF optical output can be connected to external high-power / high-quality AC3 amplifier for 3D Surround Sound.

3.4.9 Super I/O controllers.

The 786LCD board includes two Super I/O controllers with the following functions :

SiS950

This is the main IO controller with the following features:
- COM1. A RS485/RS232 driver is used providing RS232, RS422/RS485.
- COM2. Operates in RS232 mode.
- LPT. Support for SPP, EPP and ECP modes.
- Standard Floppy Disk Controller.
- Environment Controller for temperature, voltage and Fan supervision/control.
- Game- and MIDI-port support.
- Bus interface to BIOS and M-System Flash.

Winbond W83877ATF (on 786LCD/S and 786LCD/MG)
This device provides additionally two COM-ports (COM3 and COM4) with RS232 support. An advanced IR controller is also integrated in this device. The IR interface shares the controller of COM4.

Winbond W83697HF (on 786LCD/ST)
This device provides additionally two COM-ports (COM3 and COM4) with RS232 support. An advanced IR controller is also integrated in this device. The IR interface shares the controller of COM4.

3.4.10 M-System and SRAM support.

Access to the BIOS and M-system disk on chip socket is controlled by the SiS950 and a FPGA on the board. In this way, it is possible to provide an address window for the disk on chip support. Information on DOC2000 devices may be found on http://www.m-sys.com.
The M-systems socket may additionally be used to bootstrap the system if the on-board BIOS should be erased. This requires an external flash BIOS (e.g Atmel 29C040A) inserted with a 3.3KΩ pull-down on the chip select signal (CS Pin 22, GND Pin 16). Contact Support for instructions on bootstrapping.

3.4.11 Power supplies.

The 786LCD/s, /ST and 786LCD/MG boards are designed to operate on a 5V DC only supply. Onboard circuit is included to support ATX power supply alike functions such as OS controlled suspend and power-off. An ideal power supply for the 786 board offers good efficience at both high load (15-40W) when the board is operating, as well as at low load (< 1W) during board standby. The 786LCD/3.5” requires 5V and 3V3 to operate. This can be handled by using a standard ATX supply. See section 4.6 for details on power consumption.

3.4.12 PCI bus.

The PCI-bus on the board is provided by the SiS630 chipset and will always run at 33MHz.
The SiS630 provides support for up to 3 external bus masters. On 786LCD/S, /ST and 786LCD/3.5" these signals are used for supporting the PC104+ bus.
On the 786LCD/MG which includes the PIC-MG interface additionally 4 sets of bus master signals are generated by means of an arbiter connected to one set of bus-master signals on the SiS630.
The arbitration algorithm being used provides a fair and equal arbitration for each of the PIC-MG bus-masters. The SCSI controller and the IEEE1394 controller on the 786LCD/MG is directly connected to one of the SiS630 bus-master signals.
The PCI interface provided in the PC104+ connector complies with the PC/104+ specification version 1.0 February 1997 [2].
The PC104+ and the PIC-MG specification essentially define another physical interface to the PCI-bus defined in the PCI v2.1 specification [5].

Note: Some of the signals in the PCI interface is pulled up to +5V. Devices connected to the PCI interface must be +5V tolerant.

3.4.13 ISA bus.

The SiS630 chipset do not include a PC-AT interface, but only a LPC (Low Pin Count) interface.
In order to support the PC-AT interface on the 786LCD/S, /ST and 786LCD/MG boards a LPC to ISA converter chip is added. This converter chip provides a limited ISA interface, with no ISA master mode support or support for 16 Bit I/O and Memory cycles. 16 Bit DMA cycles are supported. For further details see section 5.17.4 ISA Bus limitations.
On the 786LCD/ST board additional handling is added for support of all 8 and 16-bit cycles of the IEEE-996 standard. Due to the nature of the LPC bus, the bandwidth of 16 bit I/O and Memory cycles will only be half of a non-LPC ISA solution.

ISA master mode allows an ISA board to grant the bus and get the bus master status. The bus master has the ability to generate bus cycles and transferring data without involvement of the CPU or DMA (Direct memory access). ISA boards that utilise the bus master mode are less common today and is not supported on the 786LCD series.

On 786LCD/3.5" the ISA bus can be accessed through the LPC interface, but it will require external circuitry to convert to a 16bit ISA bus.

Note: Use of PC104 devices and Serial Ports.
In order to allow room for connecting Serial Port C+D to the 786LCD/S, 786LCD/ST, 786LCD/MG boards, PC104 connector spacers must be used for the PC104 devices.

3.4.14 SCSI controller.

SCSI Standards

To help understand the terminology of the many different SCSI standards this chapter outlines the terms as endorsed by the SCSI Trade Association.
The SCSI standards are grouped based on two parameters: the SCSI Bus Width and Bus Speed, refer to the table.

STA Terms	SCSI Bus Width, Bits	SCSI Bus Speed, MBytes/second

SCSI-1	8	5
Fast SCSI	8	10
Fast Wide SCSI	16	20
Ultra SCSI	8	20
Wide Ultra SCSI	16	40
Wide Ultra2 SCSI	16	80

To describe the available bandwidth the terms Fast, Ultra and Ultra2 are used where each new term indicates a doubling in bandwidth compared to the previous. So the maximum transfer rate of the Ultra SCSI is twice that of a Fast SCSI and the Ultra2 rate twice the rate of an Ultra. The Bus Width is described by either the absence of a word or the word Wide. The absence means an 8-bit bus and Wide a 16-bit bus where the difference is a doubling in transfer rate.

In the world of SCSI standards the names SCSI-1, SCSI-2 and SCSI-3 are often used as well. The borders between these are often fuzzy, as manufactures have implemented parts of the suggested SCSI-3 standards in their SCSI-2 devices.

The major additional functions of the SCSI-2 standard compared to SCSI-1 is the option of Fast and Wide SCSI enabling transfer rates of up to 20 Mbytes/sec. Also the SCSI-2 standard demands that active termination is used. The SCSI-3 standards are still in development, but some of the features included will be the Ultra SCSI option allowing for transfers of up to 40 Mbytes/second, which have already been realised by most hard disk manufactures as an extension to the SCSI-2 Fast and Wide. Shown in the table is also the Ultra2 option which doubles the Ultra Bus speed by using low voltage differential transceivers (LVD).

All the SCSI standards shown in the table are supported by Kontron Technology's 786MG board. The chart below shows the corresponding bus length and maximum number of devices on a single SCSI line. Both Asynchronous and Synchronous devices can be used.

SCSI standard	Maximum Bus Length, Meters	Maximum number of Devices
SCSI-1	6	8
Fast SCSI	3	8
Fast Wide SCSI	3	16
Ultra SCSI	1.5	8
Ultra SCSI	3	4
Wide Utra SCSI	1.5	8
Wide Utra2 SCSI (LVD)	25	15

SCSI Installation

Kontron Technology's 786MG board provides a PCI-to-Ultra2 SCSI host adapter onboard. The board utilise SYMBIOS's SYM53C895A chip for the SCSI operations and is supported major operating systems: DOS/Windows and NT.

The SCSI host adapter can handle up to 15 devices, either

- 7 standard narrow internal and 8 standard wide internal/external or
- 15 standard wide internal/external SCSI devices.

Ultra2 SCSI devices is only supported in the 68-pin connector. It is not posible to mix Single Ended and Low Voltage Differential devices, even not when connected to different connector.

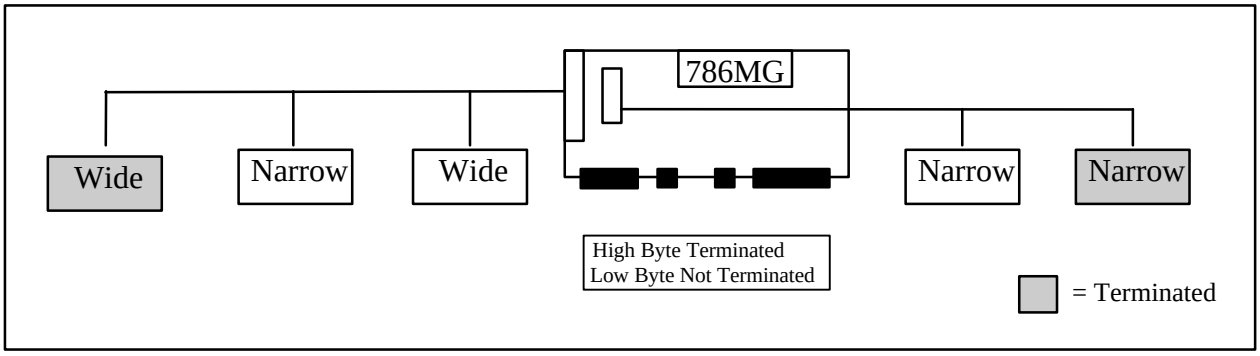
The cabling required is a 50-pin internal SCSI cable (type A) for connection of 8-bit devices to the onboard 50-pin universal header; use only keyed connectors like AMP P/N 1-746195-2 or equal. For Wide SCSI devices a 68-pin internal/external cable (type P) is used with a DB68HP connector AMP P/N 786090-7 or equivalent.

The requirements regarding termination in the SCSI standards prescribe the use of active termination at the extreme ends of the SCSI bus. Depending on how the 786MG board is connected the termination onboard should be asserted/not asserted as shown in the following table.

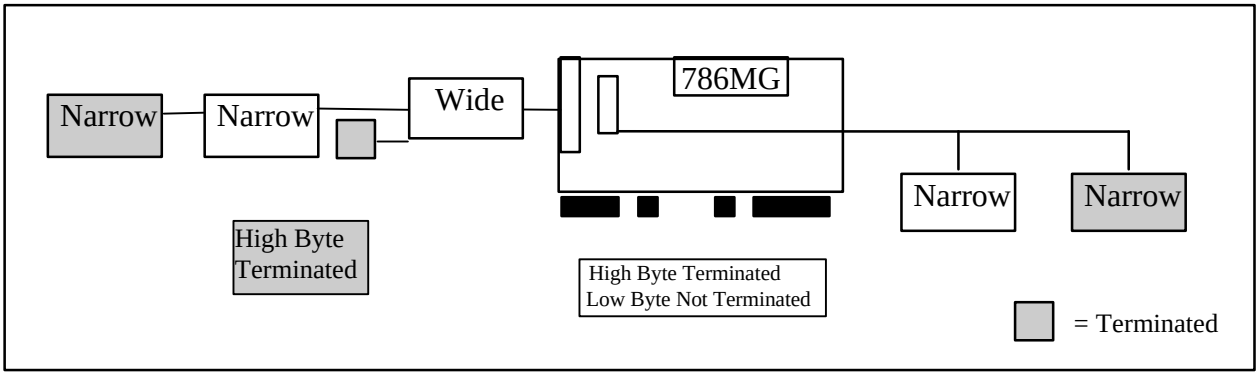
	Termination	
Cable connected	Low Byte	High Byte
Type A	Asserted	Asserted
Type P	Asserted	Asserted
Type A and P	Not Asserted	Asserted

The termination enabling/disabling is handled automatically by a ground sensing onboard circuit detecting if one or both connectors are used. To use 8-bit devices on the 68-pin Wide SCSI connector special consideration must be taken if external devices are used. The high byte must be active terminated in the converter connector going from 68-pins to 50-pins. Here Adaptec's ACK-68P-50P-E could be used. For internal devices connected to 68-pin Wide SCSI connector the high byte should not be terminated before the end of the cable. If the last device is not Wide, a terminator should be placed at the end of the cable (ACK-W2W-5IT). A converter connector going from 68-pins to 50-pins without termination could be ACK-68P-50P-IU. The configurations are illustrated in the figures below.

Internal Devices connected:



External Devices connected:



3.4.15 IEEE1394 controller.

The NEC µPD72872 is used as onboard IEEE1394 controller. The controller complies with the P1394a draft 2.0 specification and the OpenHCI IEEE1394 1.0. Two ports are supported with speeds up to 400Mb/s. Compliant with Physical Layer Services and Protocol enhancement as defined in P1394a draft 2.0 (Data Rate 100/200/400 Mb/s).
The controller supports PCI bus mastering.
The operating systems support include Windows98 and WindowsXP (WindowsNT drivers not available).

4. System Resources

4.1 Memory Map

The following table indicates memory map for the **786LCD** boards. The address ranges specifies the runtime code length.

Address Range	Length	Description	Note
00000000-000002FFh	768 bytes	BIOS Interrupt Vector Table	
00000300-000003FFh	256 bytes	BIOS Stack Area	
00000400-000004FFh	256 bytes	BIOS Data Area	
00000500-0009FFFFh	639 Kbytes	Application Memory. Used by the operating system, device drivers and TSRs	
000A0000-000BFFFFh	128 Kbytes	Video memory page	1
000C0000-000CBFFFh	48 Kbytes	Video BIOS ROM	1
000CC000-000CFFFFh	16 Kbytes	Occupied by Network Boot Extension or SCSI BIOS if enabled	2, 3
000D0000-000D3FFFh	16 Kbytes	Occupied by Network Boot Extension if Network Boot and SCSI is enabled	
000D0000-000DBFFFh	48 Kbytes	Available for external ROM BIOS Extensions	
000DC000-000DFFFFh	16 Kbytes	Occupied by USB support if enabled	
000E0000-000E3FFFh	16 Kbytes	Occupied by M-System support if enabled.	
000E4000-000FFFFFh	112 Kbytes	System BIOS ROM	
00100000-1FFFFFFFh	511 Mbytes	Application Memory. Accessible through EMM-handler or as Extended memory	
FFFF0000-FFFFFFFFh	64 Kbytes	System BIOS ROM (mirrored)	

Note:

1. Used by the on-board VGA controller, if enabled.
2. Net Boot ROM is enabled by setting “Network Boot” **as enabled** in the BIOS Boot menu.
3. SCSI BIOS only applies to 786LCD/MG Boards.

4.2 PCI Devices

The table below lists the mapping and ID's of PCI devices on the 786LCD boards.
The availability of the shaded devices will depend on the actual board type and it's configuration.

Bus #	Device #	Function #	Vendor ID	Device ID	IDSEL	Chip	Device Function
Bus 0	Device 0	Function 0	1039h	0630h	AD11	SiS630	North Bridge
Bus 0	Device 0	Function 1	1039h	5513h	AD11	SiS630	PCI IDE
Bus 1	Device 0	Function 0	1039h	6300h	AD11	SiS630	GUI / AGP
Bus 0	Device 1	Function 0	1039h	0008h	AD12	SiS630	LPC
Bus 0	Device 1	Function 1	1039h	0900h	AD12	SiS630	LAN
Bus 0	Device 1	Function 2	1039h	7001h	AD12	SiS630	USB 0
Bus 0	Device 1	Function 3	1039h	7001h	AD12	SiS630	USB 1
Bus 0	Device 1	Function 4	1039h	7018h	AD12	SiS630	H/W Audio
Bus 0	Device 1	Function 6	1039h	7013h	AD12	SiS630	S/W Modem
Bus 0	Device 2	Function 0	1039h	6001h	AD13	SiS630	Virtual PCI Bridge
Bus 0	Device 8	Function 0	1000h	0012h	AD19	53C895A	SCSI controller
Bus 0	Device 9	Function 0	1033h	00CEh	AD18	uPD72872	IEEE1394 ctrl.
Bus 0	Device 9				AD20		PC104+ Board 0
Bus 0	Device 10				AD21		PC104+ Board 1
Bus 0	Device 11				AD22		PC104+ Board 2
Bus 0	Device 12				AD23		PC104+ Board 3
Bus 0	Device 20				AD31		PIC-MG Board 0
Bus 0	Device 19				AD30		PIC-MG Board 1
Bus 0	Device 18				AD29		PIC-MG Board 2
Bus 0	Device 17				AD28		PIC-MG Board 3

4.3 ISA I/O - Map.

The 786LCD boards incorporate a ISA Bus interface with support for ISA slave mode devices only. The drive capabilities allow for up to five external ISA slots to be driven without external data buffers. The accessible I/O area on the ISA-bus is 64Kbytes with 16 address bits and the accessible Memory area is 16Mbytes with 24 address bits.
Certain I/O addresses are subject to change during boot as PnP managers may relocate devices or functions. The addresses shown in the table are typical locations

I/O Port	Access	Read/ Write	Description
0000h – 001Fh are used by the 8237 Compatible DMA Controller 1			
DMA Current Address and Byte Count Registers Ch.3-0			
0000h	PCI/ISA	R/W	DMA channel 0 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
0001h	PCI/ISA	R/W	DMA channel 0 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
0002h	PCI/ISA	R/W	DMA channel 1 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
0003h	PCI/ISA	R/W	DMA channel 1 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
0004h	PCI/ISA	R/W	DMA channel 2 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
0005h	PCI/ISA	R/W	DMA channel 2 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
0006h	PCI/ISA	R/W	DMA channel 3 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
0007h	PCI/ISA	R/W	DMA channel 3 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
DMA Status and Command Register Ch.3-0			
0008h	PCI/ISA	R	DMA channels 3-0 status register Bit 7 1 Channel 3 request Bit 6 1 Channel 2 request Bit 5 1 Channel 1 request Bit 4 1 Channel 0 request Bit 3 1 Terminal count on channel 3 Bit 2 1 Terminal count on channel 2 Bit 1 1 Terminal count on channel 1 Bit 0 1 Terminal count on channel 0
0008h	PCI/ISA	W	DMA channels 3-0 command register Bit 7 0 DACK# sense active low 1 DACK# sense active high Bit 6 0 DREQ sense active high 1 DREQ sense active low Bit 5 0 Late write selection 1 Extended write selection Bit 4 0 Fixed priority 1 Rotating priority Bit 3 0 Normal timing 1 Compressed timing Bit 2 0 Enable controller 1 Disable controller Bit 1 0 Reserved. Must be 0. Bit 0 0 Reserved. Must be 0.
DMA Request Register			
0009h	PCI/ISA	W	DMA write request register, Channels 3-0 Bits 7-3 0 Reserved. Must be 0. Bit 2 0 Resets individual DMA Channel Service SW Request Bit 1-0 1 Sets the request bit. 00 DMA Channel 0 select 01 DMA Channel 1 select 10 DMA Channel 2 select 11 DMA Channel 3 select

DMA Mask Register			
000Ah	PCI/ISA	W	DMA channel 3-0 mask register Bits 7-3 - Reserved. Must be 0. Bit 2 0 Enable DREQ for the selected channel. 1 Disable DREQ for the selected channel. Bit 1-0 Channel select 00 Channel 0 01 Channel 1 10 Channel 2 11 Channel 3
DMA Channel Mode Register			
000Bh	PCI/ISA	W	DMA channel 3-0 write mode register Bits 7-6 Transfer Mode select 00 Demand mode 01 Single mode 10 Block mode 11 Cascade mode Bit 5 0 Address increment 1 Address decrement Bit 4 0 Disable auto-initialization 1 Enable auto-initialization Bit 3-2 Select type of operation 00 Verify operation 01 Memory write 10 Memory read 11 Reserved Bits 1-0 Channel select 00 Channel 0 01 Channel 1 10 Channel 2 11 Channel 3
Misc. DMA Registers			
000Ch	PCI/ISA	W	DMA 1 Clear byte pointer flip/flop. Channels 3-0. Command enabled with a write to the I/O port address.
000Dh	PCI/ISA	W	DMA 1 Master Clear Register. Channels 3-0. Same effect as HW reset. Command enabled with a write to the I/O port address.
000Eh	PCI/ISA	W	DMA 1 Clear Mask Register. Channels 3-0. Enables acceptance of DMA requests for all four channels. Command enabled with a write to the I/O port address.
000Fh	PCI/ISA	R/W	DMA 1 Mask Register, read/write all mask bits. Channels 3-0. Bits 7-4 0 Reserved. Must be 0. Channel Mask Bits Bit 3 0 Disable ch. 3 DREQ 1 Enable ch. 3 DREQ Bit 2 0 Disable ch. 2 DREQ 1 Enable ch. 2 DREQ Bit 1 0 Disable ch. 1 DREQ 1 Enable ch. 1 DREQ Bit 0 0 Disable ch. 0 DREQ 1 Enable ch. 0 DREQ
0020h – 0021h are used by the 8259 compatible Programmable interrupt controller 1			
Int. 1 Control			
0020h	PCI/ISA	W	Initialization Command Word 1 Register. Set Bit 4 to 1 to access ICW1. Bit 7-5 000 Reserved. Set to 0. Bit 4 1 ICW1 Select. Must be 1 to select ICW1. Bit 3 0 Edge Trigger Mode 1 Level Trigger Mode Bit 2 0 8 byte Vector Address Intervals 1 4 byte Vector Address Intervals Bit 1 0 Cascade Mode. Must be 0. Bit 0 1 ICW4 Write Required. Must be set to 1.

0020h	PCI/ISA	W	Operational Control Word 2 Register. Set Bits 4 and 3 to 00 to access OCW2. Bits 7-5 000 Rotate in automatic EOI mode (clear) 001 Non-specific EOI 010 No Action. 011 Specific EOI (bits [2:0] must be valid) 100 Rotate in automatic EOI mode (set) 101 Rotate on non-specific EOI command 110 Set priority command (bits [2:0] must be valid) 111 Rotate on specific EOI command Bits 4-3 00 OCW2 Select. Must be 00 to select OCW2. Bits 2-1 nnn The interrupt request to which the command applies
0020h	PCI/ISA	W	Operational Control Word 3 Register. Set Bits 4 and 3 to 01 to access OCW3. Bit 7 0 Reserved. Must be 0. Bit 6-5 00 No Action. 01 Normal mask mode. 10 No Action. 11 Enter special mask mode. Bit 4-3 01 Must be programmed to 01 to select OCW3 Bit 2 0 No poll command. 1 Poll command. Next I/O read to irq controller is treated as highest priority request. Bit 1-0 00 No Action. 01 No Action. 10 Read interrupt request register on next read of port 0020h. 11 Read interrupt in-service register on next read of port 0020h.
0020h	PCI/ISA	R	IRQ and IS read to port 0020h following write to OCW3. Interrupt request register: Bits 7-0 0 No active request for the corresponding interrupt line. 1 Active request for the corresponding interrupt line. Interrupt in-service register: Bits 7-0 0 The corresponding interrupt line is not being serviced. 1 The corresponding interrupt line is being serviced.
Int. 1 Mask.			
0021h	PCI/ISA	W	Initialization Command Word 2-4. Following a write to the ICW1 a initialization sequence with three I/O writes to respectively ICW2, ICW3 and ICW4 Initialization Command Word 2: Bits 7-3 nnnnn Address lines A7-A3 of the base vector address for the 000 interrupt controller. Bits 2-0 Interrupt Request Level. Must be programmed to all 0s. Initialization Command Word 3: Bits 7-3 Reserved. Must be 0s. Bit 2 Cascaded Mode Enable Bit 0 Reserved. Must be all 0s. Initialization Comand Word 4: Bits 7-5 000 Reserved (should be zeroes). Bit 4 0 No special fully-nested mode. 1 Special fully-nested mode. Bit 3-2 00 Buffered Mode. Must be programmed to 00 selecting Non-buffered mode. Bit 1 0 Normal EOI. 1 Auto EOI. Bit 0 0 8085 mode. 1 8086 and 8080 mode. (Intel Architecture Based system).
0021h	PCI/ISA	R/W	Operation Command Word 1 (OCW1) Bit 7 0 Enable IRQ7 interrupt Bit 6 0 Enable IRQ6 interrupt Bit 5 0 Enable IRQ5 interrupt Bit 4 0 Enable IRQ4 interrupt Bit 3 0 Enable IRQ3 interrupt Bit 2 0 Enable IRQ2 interrupt Bit 1 0 Enable IRQ1 interrupt Bit 0 0 Enable IRQ0 interrupt
002Eh-002Fh are used by SiS950 I/O Ctrl. Configuration Registers.			
002Eh		R/W	Config Port / Index Port.
002Fh		R/W	Data Port.

0040h – 0043h are used by the 82C54 compatible Programmable timer 1

Timer Counter 1 : Counter 0-2 Count			
0040h	PCI/ISA	R	Programmable interval timer counter 0 status byte format register. This status byte can be read following an Interval Timer Read Back Command. Bit 7 Counter Out Pin State 0 Pin is 0 1 Pin is 1 Bit 6 Count Register Status 0 Count has been transferred from CR to CE and is available for reading. 1 Count has not been transferred from CR to CE and is not yet available for reading. Bits 5-4 Read/Write Selection Status 00 Counter Latch Command 01 R/W Least Significant Byte (LSB) 10 R/W Most Significant Byte (MSB) 11 R/W LSB then MSB. Bits 3-1 Mode Selection Status 000 Mode 0 selected 001 Mode 1 selected x01 Mode 2 selected x11 Mode 3 selected 100 Mode 4 selected 101 Mode 5 selected Bit 0 Countdown Type Status 0 Binary countdown 1 Binary coded decimal (BCD) countdown
0040h	PCI/ISA	W	Counter 0 Access Ports register. Bits 7-0 - Used to program 16-bit Count register. The order of programming LSB and MSB is defined with the Interval Counter Control Register.
0041h	PCI/ISA	R	Programmable timer counter 1 status byte format register. Equivalent to counter 0 byte definition.
0041h	PCI/ISA	R/W	Counter 1 Access Ports register. Equivalent to counter 0 byte definition.
0042h	PCI/ISA	R	Programmable timer counter 2 status byte format register. Equivalent to counter 0 byte definition.
0042h	PCI/ISA	R/W	Counter 2 Access Ports register. Equivalent to counter 0 byte definition.
Timer Counter 1 Command Mode			
0043h	PCI/ISA	W	Programmable timer mode port. Control word register for counters 0, 1 and 2 Bits 7-6 00 Counter 0 select 01 Counter 1 select 10 Counter 2 select 11 Read Back Command Bits 5-4 00 Counter latch command 01 R/W counter bits LSB only 10 R/W counter bits MSB only 11 R/W counter bits LSB first, then bits MSB Bits 3-1 Counter Mode Selection 000 Mode 0 Out signal on end of count. 001 Mode 1 Hardware retriggerable one-shot X10 Mode 2 Rate generator (divide by n counter) X11 Mode 3 Square wave output 100 Mode 4 Software triggered strobe 101 Mode 5 Hardware triggered strobe Bit 0 0 Binary counter is 16 bits (count max. 2^{16}) 1 Binary code decimal (BCD) counter (count max. 2^4)
Read Back Command			
0043h	PCI/ISA	W	Read Back Command for counters 0,1 and 2. Must follow a write to Control word register. The requested count or status may be read by access to the counter's I/O address. Bit 7-6 00 Read Back Command. Bit 5 0 Current count will be latched. 1 Current count will not be latched. Bit 4 0 Status of selected counters will be latched. 1 Status of selected counters will not be latched. Bit 3-1 001 Counter 0 Select. 010 Counter 1 Select. 100 Counter 2 Select. Bit 0 0 Reserved. Must be 0.
Counter Latch Command			
0043h	PCI/ISA	W	Counter Latch Command for counters 0,1 and 2. Must follow a write to Control word register. The requested count or status may be read by access to the counter's I/O address. Bit 7-6 00 Latch counter 0 select. 01 Latch counter 1 select. 10 Latch counter 2 select. 11 Read back command. Bit 5-4 00 Counter Latch Command. Bit 3-0 0 Reserved. Don't care.

004Eh – 004Fh are used by LPC – ISA Converter Configuration Registers.			
004Eh	PCI/ISA	R/W	Index Register
004Fh	PCI/ISA	R/W	Data Register

0060h & 0064h are used by the 8042 compatible keyboard-controller.			
Keyboard controller data port.			
0060h	PCI/ISA	R	Keyboard input buffer. A read of address 60h resets IRQ1 and IRQ12 (if enabled). Bit 7 0 Keyboard inhibited Bit 6 0 Primary display is VGA 1 Primary display is MDA Bit 5 0 System BIOS performs diagnostics on the motherboard in an Infinite loop. 1 Any other diagnostic function Bit 4 Motherboard RAM 0 256 kB 1 >= 512 kB Bit 3-1 - Reserved Bit 0 0 The motherboard passed the diagnostics tests when diagnostic mode was enabled.
0060h	PCI/ISA	W	Keyboard output port. Bit 7 0 Keyboard data is being transferred Bit 6 0 The keyboard clock signal is being used in data transfer Bit 5 0 PC-type mouse being used 1 PS/2-type mouse being used Bit 4 0 Output buffer full, IRQ1 generated 1 Output buffer not full Bit 3-2 - Reserved Bit 1 0 The system processor address 20 line is inhibited on the system bus 1 Address line 20 in not inhibited Bit 0 0 Reset system processor 1 This bit should always be kept at 1

0061h is used by NMI Status and Control.			
0061h	PCI/ISA	R/W	NMI Status and Control
		R	Bit 7 0 This bit must be 0 when writing to port 61h. 1 This bit is set if PCI device or main memory detects a system board error and pulses the PCI PERR#/SERR# line.
		R	Bit 6 0 This bit must be 0 when writing to port 61h. 1 This bit is set if an expansion board asserts IOCHK# on the ISA Bus.
		R	Bit 5 0 This bit must be 0 when writing to port 61h. 1 This bit reflects the Counter 2 OUT signal state.
		R	Bit 4 0 This bit must be 0 when writing to port 61h. 1 The Refresh Cycle Toggle bit toggles from 0 to 1 or 1 to 0 following every refresh cycle.
		R/W	Bit 3 0 Enable IOCHK# NMIs. 1 Clear and disable IOCHK# NMIs.
		R/W	Bit 2 0 Enable PCI SERR#. 1 Clear and disable PCI SERR#.
		R/W	Bit 1 0 Speaker Output is 0. 1 Speaker Output is the Counter 2 OUT signal value.
		R/W	Bit 0 0 Timer Counter 2 Disable. 1 Timer Counter 2 Enable.

0060h & 0064h are used by the 8042 compatible keyboard-controller.			
0064h	PCI/ISA	R	Keyboard controller status. Bit 7 0 No parity error 1 Parity error on last byte of transmission from keyboard Bit 6 0 No timeout 1 Received a timeout on last transmission Bit 5 0 No timeout 1 Transmission from keyboard controller to keyboard timed out Bit 4 0 Keyboard inhibited 1 Keyboard not inhibited Bit 3 0 Data. System writes to input buffer via I/O port 0060h 1 Command. System writes to input buffer via I/O port 0064h Bit 2 0 System flag status. Set to 0 after a power on reset. 1 The keyboard controller sets this bit according to the command from the system. Bit 1 0 Input buffer (0060h or 0064h) is empty 1 Input buffer full Bit 0 0 Output buffer has no data 1 Output buffer full
0064h	PCI/ISA	W	Keyboard Command Write

0070h – 0071h are used by the RTC clock and CMOS RAM.			
0070h	PCI/ISA	W	Real Time Clock (CMOS RAM) address register and NMI mask Bit 7 0 NMI disabled 1 NMI enabled Bits 6-0 n x 7 CMOS RAM index address register
0071h	PCI/ISA	R/W	CMOS RAM data register port
0080h is used for power-on diagnostics port.			
0080h	PCI/ISA	R	Manufacturing test port (POST checkpoints can be accessed via this port)
0080h	PCI/ISA	R/W	Temporary storage for additional DMA page register
0081h - 008Fh are used for DMA control.			
0081h	PCI/ISA	R/W	DMA channel 2 Address bits [23:16]
0082h	PCI/ISA	R/W	DMA channel 3 Address bits [23:16]
0083h	PCI/ISA	R/W	DMA channel 1 Address bits [23:16]
0084h	PCI/ISA	R/W	Additional DMA page register (Reserved)
0085h	PCI/ISA	R/W	Additional DMA page register (Reserved)
0086h	PCI/ISA	R/W	Additional DMA page register (Reserved)
0087h	PCI/ISA	R/W	DMA channel 0 Address bits [23:16]
0088h	PCI/ISA	R/W	Additional DMA page register (Reserved)
0089h	PCI/ISA	R/W	DMA channel 6 Address bits [23:16]
008Ah	PCI/ISA	R/W	DMA channel 7 Address bits [23:16]
008Bh	PCI/ISA	R/W	DMA channel 5 Address bits [23:16]
008Ch	PCI/ISA	R/W	Additional DMA page register (Reserved)
008Dh	PCI/ISA	R/W	Additional DMA page register (Reserved)
008Eh	PCI/ISA	R/W	Additional DMA page register (Reserved)
008Fh	PCI/ISA	R/W	DMA low page register refresh
0092h is used for the Peripheral controller Fast GateA20 and Keyboard reset.			
0092h	PCI/ISA	R/W	Port 92 Register. Bits 7-2 - Reserved. Bit 1 - Fast gate A20 option 0 CPU address wrap around 1MB boundary 1 No wrap around. Bit 0 1 Force a Fast CPU reset, for protected mode switchings.

00A0h-00A1h are used for Programmable interrupt controller 2. Except for the differences noted below, the bit definitions are the same as those for addresses 0020h-0021h.			
Int. 2 Control			
00A0h	PCI/ISA	R/W	Programmable interrupt controller 2
Int. 2 Mask			
00A1h	PCI/ISA	R/W	Programmable interrupt controller 2 mask (OCW1) Bit 7 0 Enable IRQ15 interrupt Bit 6 0 Enable IRQ14 interrupt Bit 5 0 Enable IRQ13 interrupt Bit 4 0 Enable IRQ12 interrupt Bit 3 0 Enable IRQ11 interrupt Bit 2 0 Enable IRQ10 interrupt Bit 1 0 Enable IRQ9 interrupt Bit 0 0 Enable IRQ8 interrupt
00C0h - 00DFh are used by DMA controller 2.			
00C0h	PCI/ISA	R/W	DMA channel 4 Address bits [15:0] : byte 0 (low byte), followed by byte 1. Not used.
00C2h	PCI/ISA	R/W	DMA channel 4 Byte count [15:0] : byte 0 (low byte), followed by byte 1. Not used.
00C4h	PCI/ISA	R/W	DMA channel 5 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
00C6h	PCI/ISA	R/W	DMA channel 5 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
00C8h	PCI/ISA	R/W	DMA channel 6 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
00CAh	PCI/ISA	R/W	DMA channel 6 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
00CCh	PCI/ISA	R/W	DMA channel 7 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
00CEh	PCI/ISA	R/W	DMA channel 7 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
00D0h	PCI/ISA	R	DMA channel 7-4 status register Bit 7 1 Channel 7 request Bit 6 1 Channel 6 request Bit 5 1 Channel 5 request Bit 4 1 Channel 4 request Bit 3 1 Terminal count on channel 7 Bit 2 1 Terminal count on channel 6 Bit 1 1 Terminal count on channel 5 Bit 0 1 Terminal count on channel 4

00D0h	PCI/ISA	W	DMA channel 7-4 command register Bit 7 0 DACK# sense active low 1 DACK# sense active high Bit 6 0 DREQ sense active high 1 DREQ sense active low Bit 5 0 Late write selection 1 Extended write selection Bit 4 0 Fixed priority 1 Rotating priority Bit 3 0 Normal timing 1 Compressed timing Bit 2 0 Enable controller 1 Disable controller Bit 1 0 Reserved. Must be 0. Bit 0 0 Reserved. Must be 0.
00D2h	PCI/ISA	W	DMA channel 7-4 write request register Bit 7-3 0 Reserved (should all be zeroes) Bit 2 0 Resets individual DMA Channel Service SW Request 1 Sets the request bit. 00 Illegal 01 DMA Channel 5 select 10 DMA Channel 6 select 11 DMA Channel 7 select
00D4h	PCI/ISA	R/W	DMA channel 7-4 write single mask register bit Bits 7-3 0 Reserved (should all be zeroes) Bit 2 0 Clear mask bit 1 Set mask bit Bit 1-0 Channel select 00 Channel 4 01 Channel 5 10 Channel 6 11 Channel 7
00D6h	PCI/ISA	W	DMA channel 7-4 mode register Bits 7-6 Mode select 00 Demand mode 01 Single mode 10 Block mode 11 Cascade mode Bit 5 0 Address increment 1 Address decrement Bit 4 0 Disable autoinitialization 1 Enable autoinitialization Bit 3-2 Select type of operation 00 Verify operation 01 Memory write 10 Memory read 11 Reserved Bits 1-0 Channel select 00 Channel 4 01 Channel 5 10 Channel 6 11 Channel 7
00D8h	PCI/ISA	W	DMA channel 7-4 clear byte pointer flip/flop
00DAh	PCI/ISA	W	DMA channel 7-4 master clear
00DCh	PCI/ISA	W	DMA channel 7-4 clear mask register
00DEh	PCI/ISA	W	DMA channel 7-4 write mask register
00F1h – 00FFh KONTRON Technology On-board control registers.			
00F0h	PCI/ISA	R/W	Coprocessor Error Register
00F1h	PCI/ISA	R	Supervision Status Register Bit 7-4 - Key words must be written to these bits to enable writes in arrea 0F5-0Feh. Bit 3-2 - Reserved Bit 1-0 - Might be used for RS485 control, if selected in BIOS setup. Bit 1 0 Disable TxD+/- RS485 driver. 1 Enable TxD+/- RS485 driver. Bit 0 0 Disable CTS+/- RS485 driver. 1 Enable CTS+/- RS485 driver.
00F2h	PCI/ISA	R	Revision Information Register Bit 7-4 - PCB Revision Bit 3-0 - FPGA Revision
00F3h	PCI/ISA	R/W	Feature Port GPIO Configuration Bit 7 0 GPIO7 is operating as input (default). 1 GPIO7 is operating as output. Bit 6-0 - Configuration of GPIO6-0 as for GPIO7 above.

00F4h	PCI/ISA	R/W	Feature Port GPIO Data Bit 7-0 - Read data from or write data to GPIO7-0
00F5h-00FFh	PCI/ISA	R/W	Reserved for Kontron Technology use.

0100h – 03FFh On-board peripherals and PC-AT / PC104 Adapter boards.

0170h - 0177h may be used by on-board hard disk controller for secondary (1) IDE port.

Depends on choice made in Main setup.
The bit definitions for these addresses are the same as those for addresses 01F0h-01F7h.

0170h	PCI/ISA	R/W	Hard disk 1 data register base port
0171h	PCI/ISA	R	Hard disk 1 error register
0171h	PCI/ISA	W	Hard disk 1 write pre-compensations register
0172h	PCI/ISA	R/W	Hard disk 1 sector count
0173h	PCI/ISA	R/W	Hard disk 1 sector number
0174h	PCI/ISA	R/W	Hard disk 1 number of cylinders, low byte
0175h	PCI/ISA	R/W	Hard disk 1 number of cylinders, high byte
0176h	PCI/ISA	R/W	Hard disk 1 drive/head register
0177h	PCI/ISA	R	Hard disk 1 status register
0177h	PCI/ISA	W	Hard disk drive 1 command register

01F0h - 01F7h may be used by on-board hard disk controller for primary (1) IDE port.

Depends on choice made in Main setup.

01F0h	PCI/ISA	R/W	Hard disk 0 data register base port
01F1h	PCI/ISA	R	Hard disk 0 error register **Diagnostic mode** Bits 7-3 - Reserved Bits 2-0 - Diagnostics mode errors 001 No errors 010 Controller error 011 Sector buffer error 100 ECC device error 101 Control processor error **Operation mode** Bit 7 0 Block is not bad 1 Bad block detected Bit 6 0 No error 1 Uncorrectable ECC error Bit 5 - Reserved Bit 4 0 ID not found 1 ID found Bit 3 - Reserved Bit 2 0 Command aborted 1 Command completed Bit 1 0 Track 000 found 1 Track 000 not found Bit 0 0 DAM found (CP-3002 is always 0) 1 DAM not found
01F1h	PCI/ISA	W	Hard disk 0 write pre-compensations register
01F2h	PCI/ISA	R/W	Hard disk 0 sector count
01F3h	PCI/ISA	R/W	Hard disk 0 sector number
01F4h	PCI/ISA	R/W	Hard disk 0 number of cylinders, low byte
01F5h	PCI/ISA	R/W	Hard disk 0 number of cylinders, high byte
01F6h	PCI/ISA	R/W	Hard disk 0 drive/head register Bit 7 1 Reserved Bit 6 0 Reserved Bit 5 1 Reserved Bit 4 - Drive select 0 First hard disk drive 1 Second hard disk drive Bit 3-0 nnnn Head select bits
01F7h	PCI/ISA	R	Hard disk 0 status register Bit 7 1 Controller is executing a command Bit 6 1 Drive is ready Bit 5 1 Write fault Bit 4 1 Seek complete Bit 3 1 Sector buffer requires servicing Bit 2 1 Disk data read corrected Bit 1 1 An index. Set to 1 each disk revolution Bit 0 1 Previous command ended with an error
01F7h	PCI/ISA	W	Hard disk drive 0 command register

0200h – 0201h may be used by SiS950 Game Port			
0200h	PCI/ISA	-	Reserved
0201h	PCIISA	W	A wite triggers the 4 coordinate timers to high output
0201h	PCI/ISA	R	Bit 7 0 Joystick B, Button 2 activated Bit 6 0 Joystick B, Button 1 activated Bit 5 0 Joystick B, Coordinate Y, timer de-activated Bit 4 0 Joystick B, Coordinate X, timer de-activated Bit 3 0 Joystick A, Button 2 activated Bit 2 0 Joystick A, Button 1 activated Bit 1 0 Joystick A, Coordinate Y, timer de-activated Bit 0 0 Joystick A, Coordinate X, timer de-activated
0220h - 022Fh may be used by on-board Audio Support (SB16 Compatible) Depends on choice made in Advanced setup			
0220h	PCI/ISA	R	Left FM Status port
0220h	PCI/ISA	W	Left FM Register Status port
0221h	PCI/ISA	W	Left FM Data port
0222h	PCI/ISA	R	Right FM Status port
0222h	PCI/ISA	W	Right FM Register status port
0223h	PCI/ISA	W	Right FM Status port
0224h	PCI/ISA	W	Mixer Register Address Register Data 00h Bit 7-0 Data reset 02h Bit 7-0 Reserved 04h Bit 7-4 Voice Volume Left Bit 3-0 Voice Volume Right 06h Bit 7-0 Reserved 08h Bit 7-0 Reserved 0Ah Bit 2-0 Microphone Mixing 0Ch Bit 2-1 Input Select 0Eh Bit 1 VSTC
			20h Bit 7-0 Reserved 22h Bit 7-4 Master Volume Left Bit 3-0 Master Volume Right 24h Bit 7-0 Reserved 26h Bit 7-4 FM Volume Left Bit 3-0 FM Volume Right 28h Bit 7-4 CD Volume Left Bit 3-0 CD Volume Right 2Ah Bit 7-0 Reserved 2Ch Bit 7-0 Reserved 2Eh Bit 7-4 Line Volume Left Bit 3-0 Line Volume Right
0225h	PCI/ISA	R/W	Mixer Data port
0226h	PCI/ISA	W	Reset
0228h	PCI/ISA	R	FM Status port
0229h	PCI/ISA	W	FM Data port
022Ah	PCI/ISA	R	Read Data port
022Ch	PCI/ISA	W	Command/Write Data
022Ch	PCI/ISA	R	Write Buffer Status (bit 7)
022Eh	PCI/ISA	R	Data Available Status (bit 7)
0240h – 024Fh may be used by on-board Audio Support (SB16 Compatible) Depends on choice made in Advanced setup			
0240h-024Fh	PCI/ISA	-	The bit definitions for these addresses are the same as those for addresses 0220h-022Fh.
0250h – 0252h are used by I/O cntl. 2. Configuration Registers			
0250h	PCI/ISA	R/W	Extended Functions Enable Register
0251h	PCI/ISA	R/W	Extended Functions Index Register
0252h	PCI/ISA	R/W	Extended Functions Data Register
0260h – 026Fh may be used by on-board Audio Support (SB16 Compatible) Depends on choice made in Advanced setup			
0260h-026Fh	PCI/ISA	-	The bit definitions for these addresses are the same as those for addresses 0220h-022Fh.

0278h – 027Fh may be used by on-board peripheral controller as Parallel port 2. Depends on choice made in Advanced setup. The bit definitions for these addresses are the same as those for addresses 0378h-037Fh.			
0278h	PCI/ISA	R/W	Parallel port 2, data
0279h	PCI/ISA	R/W	Parallel port 2, status
027Ah	PCI/ISA	R/W	Parallel port 2, control
027Bh	PCI/ISA	R/W	Parallel port 2, EPP address port
027Ch	PCI/ISA	R/W	Parallel port 2, EPP data port 0
027Dh	PCI/ISA	R/W	Parallel port 2, EPP data port 1
027Eh	PCI/ISA	R/W	Parallel port 2, EPP data port 2
027Fh	PCI/ISA	R/W	Parallel port 2, EPP data port 3
0280h - 028Fh may be used by on-board Audio Support (SB16 Compatible) Depends on choice made in Advanced setup			
0280h-028Fh	PCI/ISA	-	The bit definitions for these addresses are the same as those for addresses 0220h-022Fh.
0290h – 0297h may be used by SiS950 Environment Controller			
0290h-0294h	PCI/ISA	-	Reserved
0295h	PCI/ISA	R/W	Address register of environment controller
0296h	PCI/ISA	R/W	Data Register of environment controller
0297h	PCI/ISA	-	Reserved
02E8h – 02EFh may be used by on-board peripheral controller as Serial port 4. Depends on choice made in Advanced setup. The bit definitions for these addresses are the same as those for addresses 03F8h-03FFh.			
02E8h	PCI/ISA	R	Receiver buffer register, when DLAB is 0
02E8h	PCI/ISA	W	Transmitter buffer register, when DLAB is 0
02E8h	PCI/ISA	R/W	Divisor latch LSB, when DLAB is 1
02E9h	PCI/ISA	R/W	Divisor latch MSB, when DLAB is 1
02E9h	PCI/ISA	R/W	Interrupt enable register, when DLAB is 0
02Eah	PCI/ISA	R	Interrupt identification register
02Eah	PCI/ISA	W	FIFO control register
02Ebh	PCI/ISA	R/W	Line control register
02Ech	PCI/ISA	R/W	Modem control register
02Edh	PCI/ISA	R/W	Line status register
02Eeh	PCI/ISA	R/W	Modem status register
02Efh	PCI/ISA	R/W	Scratch pad register
02F8h - 02FFh may be used by on-board peripheral controller as Serial port 2. Depends on choice made in Advanced setup. The bit definitions for these addresses are the same as those for addresses 03F8h-03FFh.			
02F8h	PCI/ISA	R	Receiver buffer register, when DLAB is 0
02F8h	PCI/ISA	W	Transmitter buffer register, when DLAB is 0
02F8h	PCI/ISA	R/W	Divisor latch LSB, when DLAB is 1
02F9h	PCI/ISA	R/W	Divisor latch MSB, when DLAB is 1
02F9h	PCI/ISA	R/W	Interrupt enable register, when DLAB is 0
02Fah	PCI/ISA	R	Interrupt identification register
02Fah	PCI/ISA	W	FIFO control register
02FBh	PCI/ISA	R/W	Line control register
02FCh	PCI/ISA	R/W	Modem control register
02FDh	PCI/ISA	R/W	Line status register
02Feh	PCI/ISA	R/W	Modem status register
02FFh	PCI/ISA	R/W	Scratch pad register
0300h – 0307h may be used by SiS950 CIR Controller			
0300h	PCI/ISA	R/W	CIR Data Register
0301h	PCI/ISA	R/W	CIR Iterrupt Enable Register
0302h	PCI/ISA	R/W	CIR Receiver Control Register
0303h	PCI/ISA	R/W	CIR Transmitter Control Register 1
0304h	PCI/ISA	R/W	CIR Transmitter Control Register 2
0305h	PCI/ISA	R	CIR Transmitter Status Register
0306h	PCI/ISA	R	CIR Receiver Status Register
0305h	PCI/ISA	R/W	CIR Baud Rate Divisor Low Byte Register
0306h	PCI/ISA	R/W	CIR Baud Rate Divisor High Byte Register
0307h	PCI/ISA	R/W	CIR Interrupt identification Register

0310h – 0311h may be used by SiS950 MIDI Port					
0310h	PCI/ISA	R/W	MIDI Data Port		
0311h	PCI/ISA	W	MIDI Instruction Command		
0311h	PCI/ISA	R	Bit 7	0	Data in Receive Buffer
				1	Receive Buffer Empty
			Bit 6	0	Transmit Buffer not full
				1	Transmit Buffer full
			Bit 5-0	111111	Reserved, return all one's.

0370h - 0377h may be used by on-board peripheral controller as Floppy disk controller port 2. Depends on choice made in Advanced setup. The bit definitions for these addresses are the same as those for addresses 03F0h-03F7h.			
0370h	PCI/ISA	R	Status Register A (SRA)
0371h	PCI/ISA	R	Status Register B (SRB)
0372h	PCI/ISA	R/W	Floppy disk controller output register (DOR)
0373h	PCI/ISA	R/W	Tape Drive Register (TSR)
0374h	PCI/ISA	R	Floppy disk controller status register (MSR)
0374h	PCI/ISA	W	Data Rate Select Register (DSR)
0375h	PCI/ISA	R/W	Floppy disk controller data register (FIFO)
0376h	PCI/ISA	-	Reserved
0377h	PCI/ISA	R	Digital input register (DIR)
0377h	PCI/ISA	W	Hard disk status register (CCR)

0374 – 0377h may be used by on-board IDE controller as Secondary IDE Control Block.			
0374h	PCI/ISA	-	Reserved.
0375h	PCI/ISA	-	Reserved.
0376h	PCI/ISA	R/W	Alt. Status/ Device control.
0377h	PCI/ISA	R/W	Forward to ISA (floppy)

0378h - 037Fh may be used by on-board peripheral controller as Parallel port 1. Depends on choice made in Advanced setup.					
0378h	PCI/ISA	R/W	Parallel port 1, data		
0379h	PCI/ISA	R	Parallel port 1, status		
			Bit 7	0	Busy
			Bit 6	0	Acknowledge
			Bit 5	1	Out of paper
			Bit 4	1	Printer is selected
			Bit 3	0	Error
			Bits 2-1	11	Reserved
			Bit 0	1	EPP timeout
037Ah	PCI/ISA	R/W	Parallel port 1, control		
			Bits 7-6	00	Reserved
			Bit 5	0	Data port direction, output data to printer
				1	Data port direction, input data from printer
			Bit 4	1	Enable IRQ
			Bit 3	1	Select printer
			Bit 2	0	Initialize printer
			Bit 1	1	Automatic line feed
			Bit 0	1	Strobe
037Bh	PCI/ISA	R/W	Parallel port 1, EPP address port		
037Ch	PCI/ISA	R/W	Parallel port 1, EPP data port 0		
037Dh	PCI/ISA	R/W	Parallel port 1, EPP data port 1		
037Eh	PCI/ISA	R/W	Parallel port 1, EPP data port 2		
037Fh	PCI/ISA	R/W	Parallel port 1, EPP data port 3		

03B0h – 03BBh may be used by on-board Video controller.			
03B0h - 03BFh are used by on-board Video controller in monochrome modes.			
03B0h-03B3h		R/W	Reserved for MDA/Hercules
03B4h		R/W	MDA CRTC index register

03B5h		R/W	MDA CRTC data register
03B6h-03B7h		R/W	Reserved for MDA/Hercules
03B8h		R/W	Hercules mode register
03BAh		R	Status register
03BAh		W	Feature control register

03BCh – 03BFh may be used for off-board Parallel port 3.

The bit definitions for these addresses are the same as those for addresses 0378h-037Fh.

03BC-03BFh		R/W	Available for off-board parallel port 3.

03C0h - 03CFh are used by on-board Video controller in color and monochrome modes.

03C0h		R/W	Attribute controller Index / Data
03C1h		R/W	Attribute/ Alternate controller Data
03C2h		R	Input Status Register
03C2h		W	Miscellaneous Output Register
03C3h		R/W	Video Subsystem enable
03C4h		R/W	Sequencer index
03C5h		R/W	Sequencer data
03C6h		R/W	Color palette mask
03C7h		R	Color palette state
03C7h		W	Color palette read mode index
03C8h		R/W	Color palette write mode index
03C9h		R/W	Color palette data
03CAh		R	Feature Control register
03CCh		R	Miscellaneous output register
03CEh		R/W	Graphics controller index
03CFh		R/W	Graphics controller data

03D4h - 03DFh are used by on-board Video controller in color modes.

03D4h		R/W	CRTC Index
03D5h		R/W	CRTC Data
03D6h		R/W	Reserved
03D7h		R/W	Reserved
03D8h		R/W	CGA mode register
03D9h		R/W	CGA color register
03DAh		R	Status register
03DAh		W	Feature control register
03DBh		W	Clear light pen FF (ignored)
03DCh		W	Set light pen FF (ignored)

03E8h - 03EFh may be used by on-board peripheral controller as Serial port 3.

Depends on choice made in Advanced setup.

The bit definitions for these addresses are the same as those for addresses 03F8h-03FFh.

03E8h	PCI/ISA	R	Receiver buffer register, when DLAB is 0
03E8h	PCI/ISA	W	Transmitter buffer register, when DLAB is 0
03E8h	PCI/ISA	R/W	Divisor latch LSB, when DLAB is 1
03E9h	PCI/ISA	R/W	Divisor latch MSB, when DLAB is 1
03E9h	PCI/ISA	R/W	Interrupt enable register, when DLAB is 0
03EAh	PCI/ISA	R	Interrupt identification register
03EAh	PCI/ISA	W	FIFO control register
03EBh	PCI/ISA	R/W	Line control register
03ECh	PCI/ISA	R/W	Modem control register
03EDh	PCI/ISA	R/W	Line status register
03EEh	PCI/ISA	R/W	Modem status register
03EFh	PCI/ISA	R/W	Scratch pad register

03F0h - 03F7h may be used by SiS950 peripheral controller as Floppy disk controller port 1.

Depends on choice made in Advanced setup.

03F0h	PCI/ISA	R	Status Register A (SRA)
03F1h	PCI/ISA	R	Status Register B (SRB)
03F2h	PCI/ISA	R/W	Floppy disk controller output register Bits 7-6 00 Reserved (should be zeroes) Bit 5 1 Enable motor on floppy drive B Bit 4 1 Enable motor on floppy drive A Bit 3 1 Enable Interrupt and DMA for floppy drives Bit 2 0 Controller reset Bit 1 0 Reserved (should be zero) Bit 0 0 Select floppy drive A 1 Select floppy drive B

03F4h	PCI/ISA	R	Floppy disk controller status register Bit 7 1 Data register is ready Bit 6 0 Transfer from system to controller 1 Transfer from controller to system Bit 5 1 Non-DMA mode Bit 4 1 Floppy disk controller busy Bits 3-2 xx Reserved Bit 1 1 Drive B is busy Bit 0 1 Drive A is busy
03F5h	PCI/ISA	R/W	Floppy disk controller data register (FIFO)
03F7h	PCI/ISA	R	Digital input register Bit 7 n Diskette change line inverted Bits 6-0 nx7 These bits may be driven by the hard disk status register depending on configuration

03F4h – 03F7h may be used by on-board IDE controller as Primary IDE Control Block.

03F4h	PCI/ISA	-	Reserved.
03F5h	PCI/ISA	-	Reserved.
03F6h	PCI/ISA	R/W	Alt Status / Device control.
03F7h	PCI/ISA	R/W	Forward to ISA (Floppy).

03F8h - 03FFh may be used by on-board peripheral controller as Serial port 1.

Depends on choice made in Advanced setup.

03F8h	PCI/ISA	R	Receiver buffer register (contains the received character). Bit 0, the least significant bit, is received first. Only this register function when DLAB is 0
03F8h	PCI/ISA	W	Transmitter buffer register (contains the character to be sent). Bit 0, the least significant bit, is send first. Only this register function when DLAB is 0
03F8h	PCI/ISA	R/W	Divisor latch LSB, when DLAB is 1. Settings shown below
03F9h	PCI/ISA	R/W	Divisor latch MSB, when DLAB is 1. Settings shown below

Desired Baud rate	Divisor Used	Divisor latch MSB	Divisor latch LSB
50	2304	9	0
75	1536	6	0
110	1047	4	23
150	768	3	0
300	384	1	128
600	192	0	192
1200	96	0	96
2400	48	0	48
4800	24	0	24
9600	12	0	12
19200	6	0	6
38400	3	0	3
56000	2	0	2
115200	1	0	1

03F9h	PCI/ISA	R/W	Interrupt enable register, when DLAB is 0 Bits 7-4 xxxx Reserved Bit 3 1 Modem status interrupt enable Bit 2 1 Receiver line status interrupt enable Bit 1 1 Transmitter holding register empty interrupt enable Bit 0 1 Received data available interrupt enable
03FAh	PCI/ISA	R	Interrupt identification register, information about a pending interrupt is stored here. When the ID register is addressed, the highest priority interrupt is held and no other interrupts are acknowledged until the microprocessor services that interrupt Bits 7-4 xxxx Reserved Bit 3-0 0xx1 No interrupts 0110 Receiver line status (highest priority) 0100 Received data available 1100 Character timeout indication (FIFO mode only) 0010 Transmitter holding register empty 0000 Modem status (lowest priority)
03FAh	PCI/ISA	W	FIFO control register Bits 7-6 - Receive FIFO interrupt trigger level 00 1 byte 01 4 bytes 10 8 bytes 11 14 bytes Bits 5-3 xxx Reserved Bit 2 1 Clears the transmit FIFO, self-clearing bit Bit 1 1 Clears the receive FIFO, self-clearing bit Bit 0 1 Enable transmit and receive FIFOs

03FBh	PCI/ISA	R/W	Line control register Bit 7 - Divisor Latch Access Bit (DLAB) 0 Access receiver buffer, transmitter holding register 1 Access divisor latches Bit 6 1 Set break control. Serial output forced to spacing state and remains there Bit 5 1 Odd parity Bit 4 1 Even parity select Bit 3 1 Parity enable Bit 2 - Number of stop bits per character 0 One stop bit 1 1½ stop bits if 5-bit word length is selected, 2 stop bits if 6,7 or 8-bit word length is selected Bit 1-0 - Number of bits per character 00 5-bit word length 01 6-bit word length 10 7-bit word length 11 8-bit word length
03FCh	PCI/ISA	R/W	Modem control register Bits 7-5 xxx Reserved Bit 4 1 Loop mode enabled. The output from the transmitter shift register is looped back to the receiver shift register input Bit 3 1 Enable PC-AT interrupt (OUT2) Bit 2 1 Force OUT1 active, no function at this bit Bit 1 1 Force Request To Send active Bit 0 1 Force Data Terminal Ready active
03FDh	PCI/ISA	R/W	Line status register Bit 7 1 In FIFO mode, this bit indicates at least one receive error in the FIFO. It is cleared when the CPU reads LSR, if the are no more errors in the FIFO Bit 6 1 Transmitter shift and holding registers empty Bit 5 1 Transmitter holding register empty. The controller is ready to accept a new character Bit 4 1 Break interrupt. The last received character was a break character Bit 3 1 Framing error. The stop bit that follows the last parity or data bit is zero. Bit 2 1 Parity error. The character has incorrect parity Bit 1 1 Overrun error. A character was sent to the receiver buffer before the previous character was read by the CPU Bit 0 1 Data Ready. A complete incoming character has been received and sent to the receiver buffer register
03FEh	PCI/ISA	R/W	Modem status register Bit 7 1 Data Carrier Detect Bit 6 1 Ring Indicator Bit 5 1 Data Set Ready Bit 4 1 Clear To Send Bit 3 1 Delta Data Carrier Detect Bit 2 1 Trailing edge Ring Indicator Bit 1 1 Delta Data Set Ready Bit 0 1 Delta Clear To Send
03FFh	PCI/ISA	R/W	Scratch pad register
0481h-048Bh are used by DMA High Page Registers			
0481h	PCI/ISA	R/W	DMA Channel 2 Address bits [31:24], register cleared on any access to Port 081h
0482h	PCI/ISA	R/W	DMA Channel 3 Address bits [31:24], register cleared on any access to Port 082h
0483h	PCI/ISA	R/W	DMA Channel 1 Address bits [31:24], register cleared on any access to Port 083h
0487h	PCI/ISA	R/W	DMA Channel 0 Address bits [31:24], register cleared on any access to Port 087h
0489h	PCI/ISA	R/W	DMA Channel 6 Address bits [31:24], register cleared on any access to Port 089h
048Ah	PCI/ISA	R/W	DMA Channel 7 Address bits [31:24], register cleared on any access to Port 08Ah
048Bh	PCI/ISA	R/W	DMA Channel 5 Address bits [31:24], register cleared on any access to Port 08Bh
04D0h-04D1h are used by onboard Interrupt Controller			
04D0h	PCI/ISA	R/W	Interrupt Cntrl 1 (IRQ7-3) Edge/level control. Bit 7 0 IRQ7 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ7 Level sensitivity. Bit 6 0 IRQ6 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ6 Level sensitivity. Bit 5 0 IRQ5 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ5 Level sensitivity. Bit 4 0 IRQ4 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ4 Level sensitivity. Bit 3 0 IRQ3 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ3 Level sensitivity. Bit 2-0 000 Reserved. Set to 0.

04D1h	PCI/ISA	R/W	Interrupt Cntrl 2 (IRQ15-9) Edge/level control.		
			Bit 7	0	IRQ15 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting.
				1	IRQ15 Level sensitivity.
			Bit 6	0	IRQ14 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting.
				1	IRQ14 Level sensitivity.
			Bit 5	0	Reserved. Set to 0.
			Bit 4	0	IRQ12 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting.
				1	IRQ12 Level sensitivity.
			Bit 3	0	IRQ11 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting.
				1	IRQ11 Level sensitivity.
			Bit 2	0	IRQ10 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting.
				1	IRQ10 Level sensitivity.
			Bit 1	0	IRQ9 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting.
				1	IRQ9 Level sensitivity.
			Bit 0	0	Reserved. Set to 0.

4.4 Interrupt Usage.

The SiS630 chipset provides an ISA compatible interrupt controller with functionality as two 82C59 interrupt controllers. The two controllers are cascaded to provide 13 external interrupts. Onboard devices use most of these, but a few are available through the PC-AT interface or as INTA-D on the PC104+ / PICMG connector.
The actual interrupt settings depend on the PnP handler; the scheme below indicates the typical settings.

IRQ	Onboard system parity errors and IOCHCHK signal activation	Onboard Timer 0 Interrupt	Onboard Keyboard Interrupt	Used for Cascading IRQ8-IRQ15	May be used by onboard Serial Port A	May be used by onboard Serial Port B / IrDA Port	May be used by onboard Serial Port C	May be used by onboard Serial Port D /IrDA Port. 786LCD/S, /MG only	May be used by onboard Serial Port D /IrDA Port. 786LCD/ST only	May be used by onboard Parallel Port	May be used by onboard Floppy disk Controller	Used by onboard Real Time Clock Alarm	May be used by onboard P/S 2 support	Used for Onboard co-processor support	May be used by primary harddisk controller	May be used by secondary harddisk controller	May be used for onboard Sound System	May be used by onboard USB controller	May be used by onboard Ethernet controller	May be used by onboard Environment Controller	May be used by onboard MIDI Port	May be used by onboard SCSI Controller	May be used by onboard IEEE1394 Controller	Available in PC-AT Bus or on PC104+ / PCI-MG connector (PCI-bus) as IRQA-IRQD depending on selections in the BIOS	Notes
NMI	•																								
IRQ0		•																							
IRQ1			•																						
IRQ2				•																					
IRQ3					•	•	•	•	•															•	1, 2
IRQ4					•	•																		•	1, 2
IRQ5							•	•		•														•	1, 2
IRQ6											•													•	1, 2
IRQ7									•	•														•	1, 2
IRQ8												•													
IRQ9																	•	•	•	•	•	•	•	•	1, 2
IRQ10																	•	•	•	•	•	•	•	•	1, 2
IRQ11								•									•	•	•	•	•	•	•	•	1, 2
IRQ12													•											•	1
IRQ13														•											
IRQ14															•									•	1
IRQ15																•								•	1

Notes:

1. Availability of the shaded IRQs depends on the setting in the BIOS. According to the PCI Standard, PCI Interrupts IRQA-IRQD can be shared.
2. These interrupt lines are managed by the PnP handler and are subject to change during system initialisation.

4.5 DMA-channel Usage.

The DMA circuitry incorporates the functionality of two 82C37 DMA controllers with seven programmable channels. The controllers are referenced DMA Controller 1 for channels 0-3 and DMA Controller 2 for channels 4-7. Channel 4 is by default used to cascade the two controllers. Channels 0-3 are hardwired to 8-bit count-by-bytes transfers and channels 5-7 to 16-bit count-by-bytes transfers.
The SiS630 chipset provides 32-bit address range support with the 16 least significant bits [15:0] in the Current register, bits [23:16] in the Low Page register, and bits [31:24] in the High Page register.

DMA- Channel	May be used by onboard Floppy disk controller	May be used by onboard Parallel Port in ECP mode	Used for cascading	May be used for onboard IrDA Controller. Two ch. mght be used for TX&RX	May be used for onboard Sound System in 16bit DMA mode	May be used for onboard Sound System in 8bit DMA mode	Available in PC-AT Bus depending on selections in the BIOS	Notes
DRQ0				•		•	•	1
DRQ1		•		•		•	•	1
DRQ2	•						•	1
DRQ3		•		•		•	•	1
DRQ4			•					
DRQ5					•		•	1
DRQ6					•		•	1
DRQ7					•		•	1

Notes:

1. The availability of the shaded DMA-channels depends on the choices made in the BIOS Advanced setup screen. The DMA-channels are fully usable in PC-AT bus if the corresponding on-board unit is disabled in the setup screen.

4.6 Power Consumption.

This section describes static and dynamic power consumption on the 786LCD/S and 786LCD/3.5" boards in different configurations.

Configurations:

786LCD/S

- Configuration 1: PIII 700/100MHz, 2x 64MB SDRAM (100MHz)
- Configuration 2: Celeron 633/66MHz (FC-PGA), 2x64MB SDRAM (66MHz)

786LCD/3.5"

- Configuration 3: PIII 700/100MHz (FC-PGA), 1x128MB SDRAM (100MHz)

Additional hardware common to all configurations:

- 5V active cooler (Kontron Technology)
- PS/2 keyboard and mouse

Configuration	DOS Prompt	WIN98 Idle	WIN98 Full load*
Static power consumption			
Config 1	24.4W	12.9W	appr. 30W
Config 2	23.2W	12.8W	appr. 27W
Config 3	-	-	-
• VCC	15.5W	4.8W	18W
• VCC3	5.3W	4.3W	8.9W
Dynamic power consumption**			
Config 1	-	3.3W	5.7W
Config 3	-	-	-
• VCC	-	5.8W	5.6W
• VCC3	-	0.4W	4.1W

*) 3Dmark2000 from MadOnion (www.madonion.com) and BurnInTest ver. 2.1 pro from Passmark (www.passmark.com) w. (100% duty cycle) on CRT, HD, FD and (Ethernet, COM1 & LPT w. loop-back)

**) The dynamic power consumption is aquired from measuring the ac-voltage across a 50mO resistor in series on the voltage supply line.

5. Connector Definitions

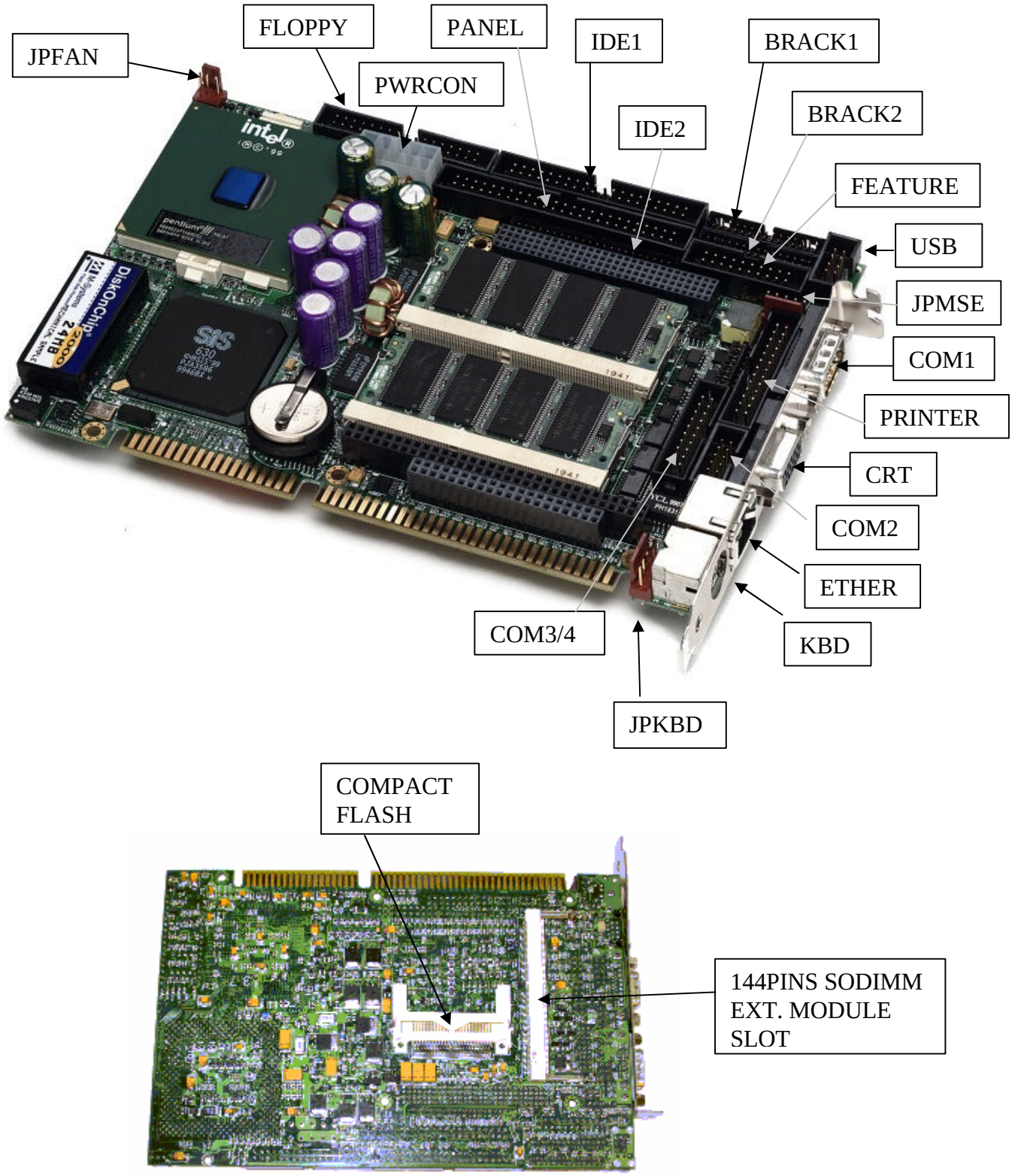
The following sections provide pin definitions and detailed description of all on-board connectors.
For a list of internal, mating connectors refer to page 106.
The connector definitions follows the following notation:

Column name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation "XX#" states that the signal "XX" is active low.
Type	AI : Analog Input. AO : Analog Output. I : Input, TTL compatible if nothing else stated. IO : Input / Output. TTL compatible if nothing else stated. IOT : Bi-directional tristate IO pin. IS : Schmitt-trigger input, TTL compatible. IOC : Input / open-collector Output, TTL compatible. NC : Pin not connected. O : Output, TTL compatible. OC : Output, open-collector or open-drain, TTL compatible. OT : Output with tri-state capability, TTL compatible. PWR : Power supply or ground reference pins.
Ioh/Iol	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.

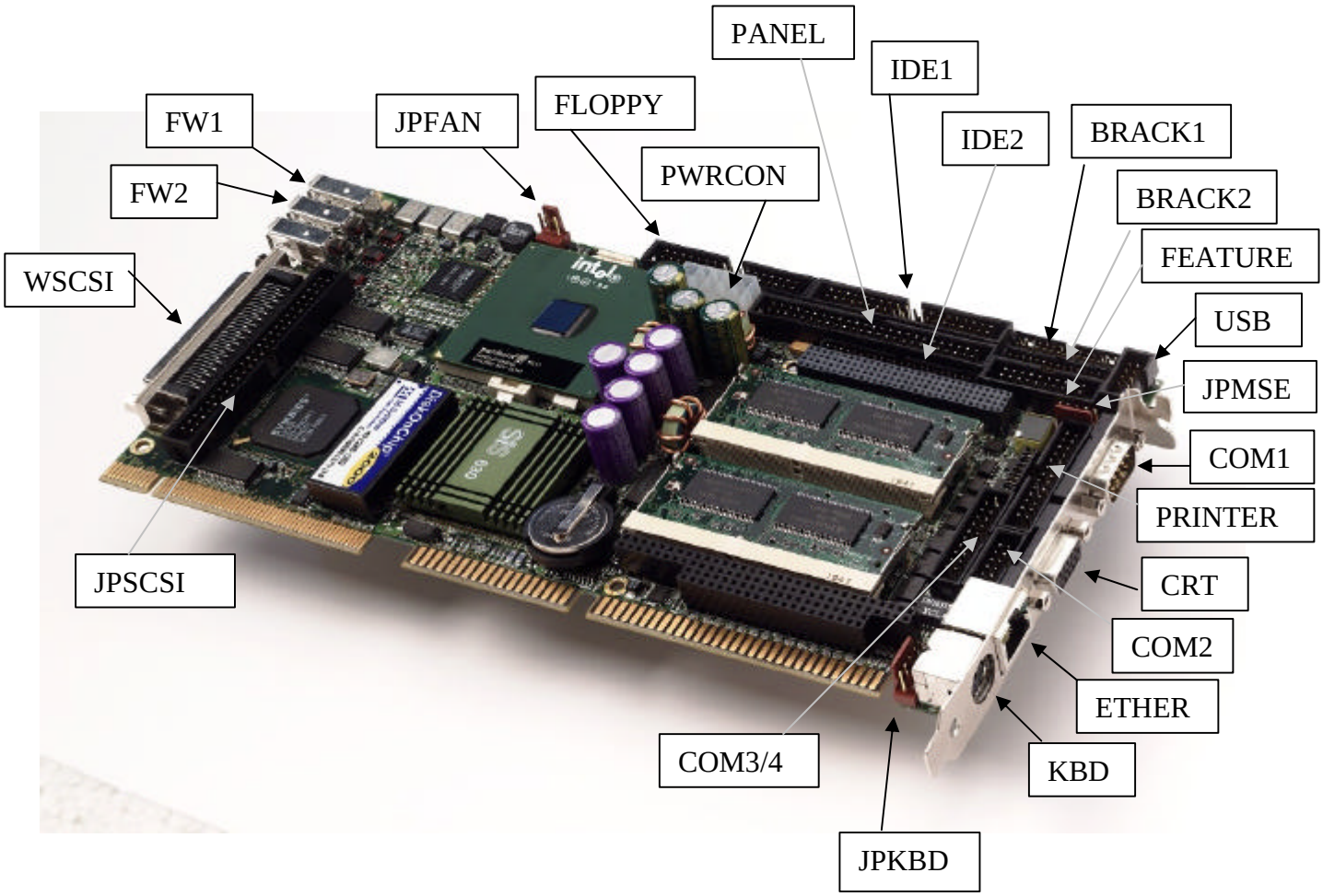
The abbreviation *TBD* is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

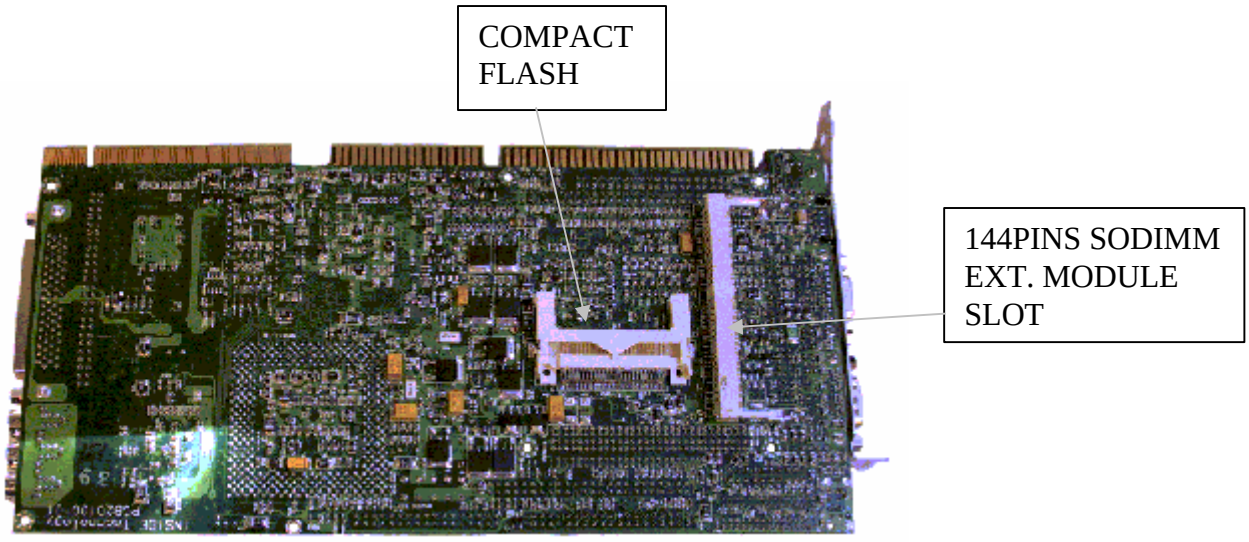
5.1 Connector layout

5.1.1 786LCD/S and 786LCD/ST

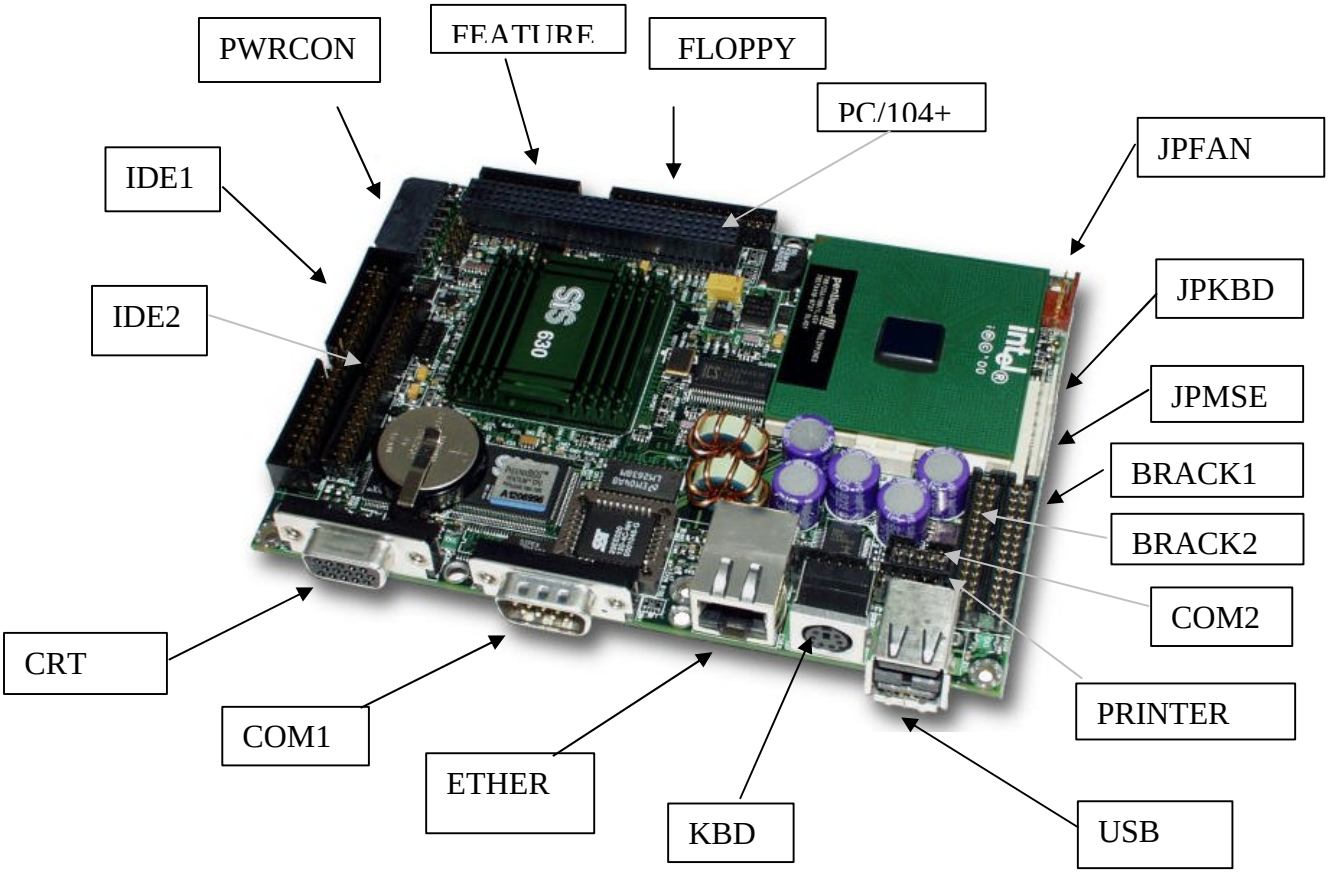


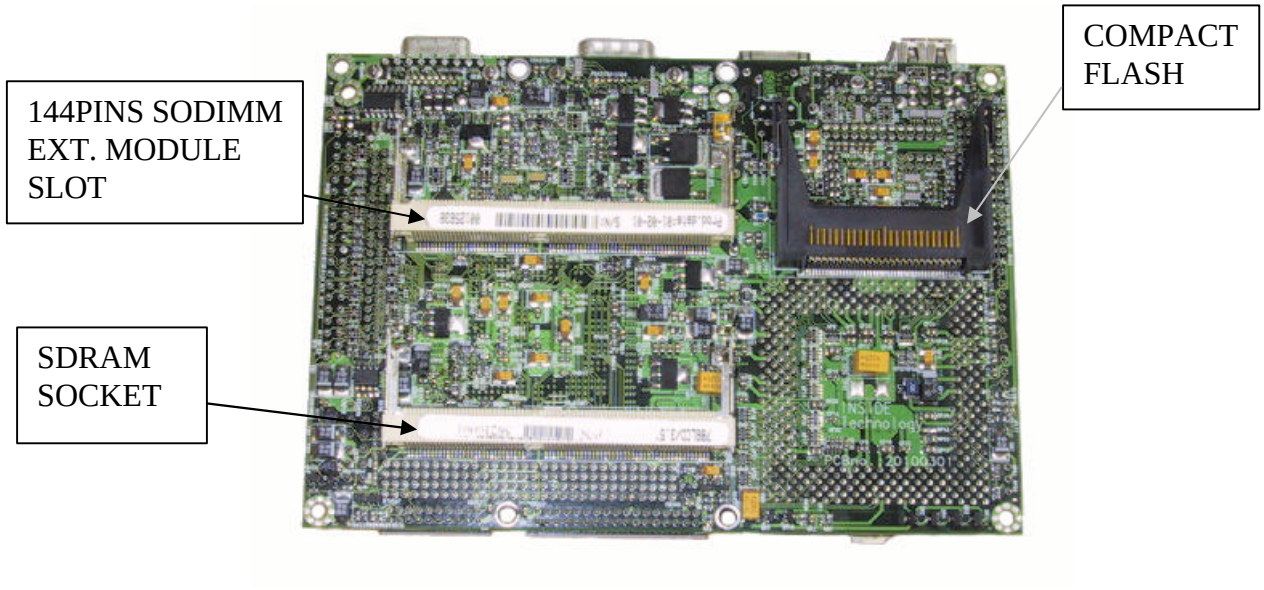
5.1.2 786LCD/MG





5.1.3 786LCD/3.5”





5.1.4 Power Connector (PWRCON)

Although power may be provided to the board by means of an ISA backplane on 786LCD/S and /MG, it is always required to use the onboard power connector.

Power Connector 786LCD/S and 786LCD/MG

Note	Pull U/D	Ioh/Iot	Type	Signal	PIN		Signal	Type	Ioh/Iot	Pull U/D	Note
1				+12Ve	1	2	-12Ve				1
2				SB5V	3	4	GND				
2				SB5V	5	6	GND				
3				SB5V	7	8	GND				
3				SB5V	9	10	GND				

Note:
1. +/-12Ve is not used onboard, but only directed to PC-AT and PC104 connectors.
2. These pins are used for supply of the onboard 5V circuits.
3. These pins are used for supply of the onboard switch mode regulators.

Power Connector 786LCD/3.5"

The Power connector for the 786LCD/3.5" board fits a standard ATX Power supply.

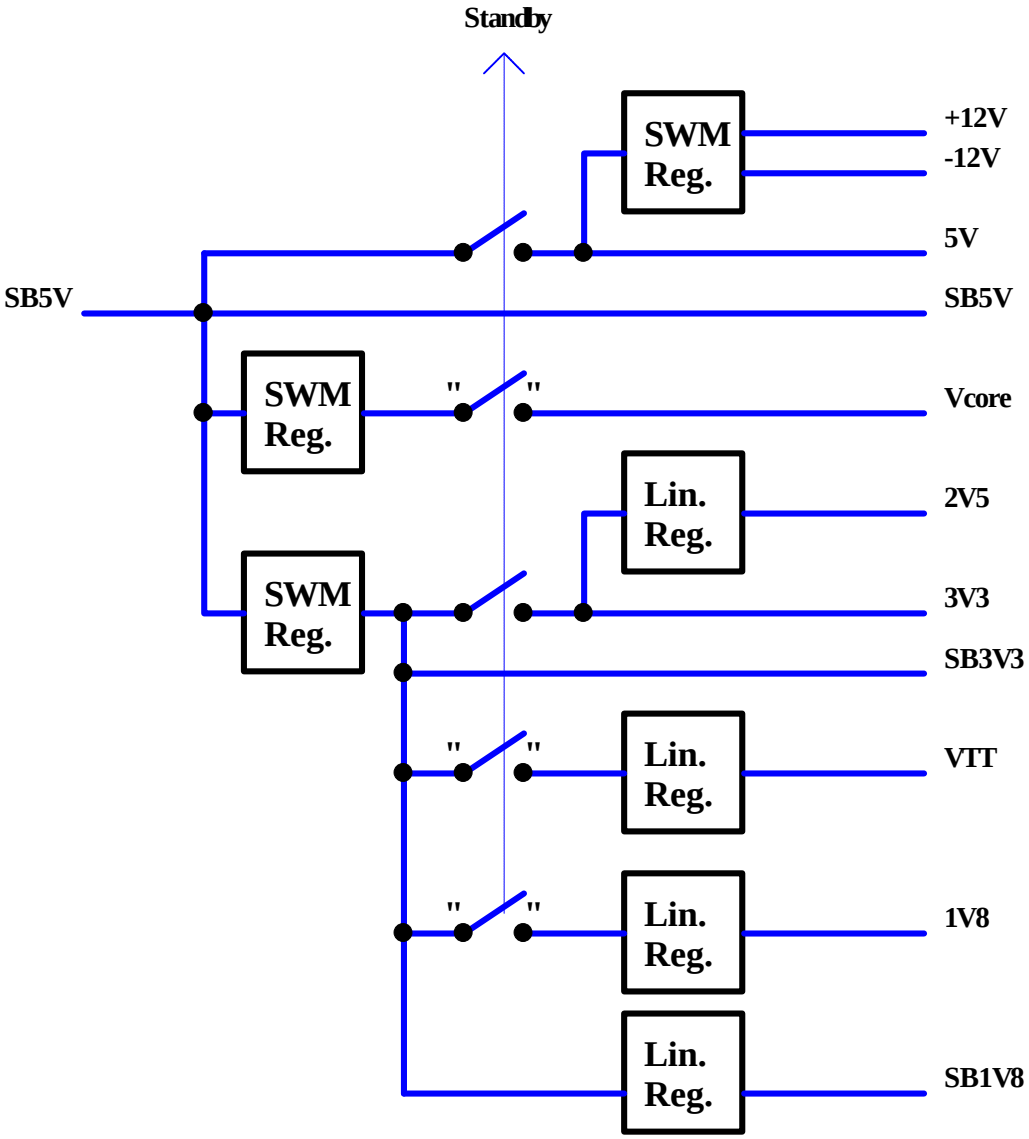
Note	Pull U/D	Ioh/Iot	Type	Signal	PIN		Signal	Type	Ioh/Iot	Pull U/D	Note
4				3V3	2	1	3V3				
4				3V3	4	3	GND				
				GND	6	5	GND				
4				+5V	8	7	+5V				4
2	2K7	/24	OC	PS-ON	10	9	SB5V				3
1				-12Ve	12	11	+12Ve				1

Note:
1. +/12Ve is not used onboard, but only directed to PC104+ connector.
2. The PS-ON is used by the 786LCD/3.5" board to turn the ATX supply ON/OFF.
3. The SB5V is used to supply onboard standby circuit.
4. Both +5V and +3.3V are required to operate the board.

The requirements to the supply voltages are as follows:

Supply	Min	Max	Note
3V3	3.14V	3.46V	Used on 786LCD/3.5" only.
SB5V	4.76V	5.25V	Minimum voltage should be 4.875V for compliance with IEEE-996 Standard.
+12Ve	11.4V	12.6V	Should be ±5% for compliance with IEEE-996 Standard.
–12Ve	–12.6V	–11.4V	Should be ±5% for compliance with IEEE-996 Standard.

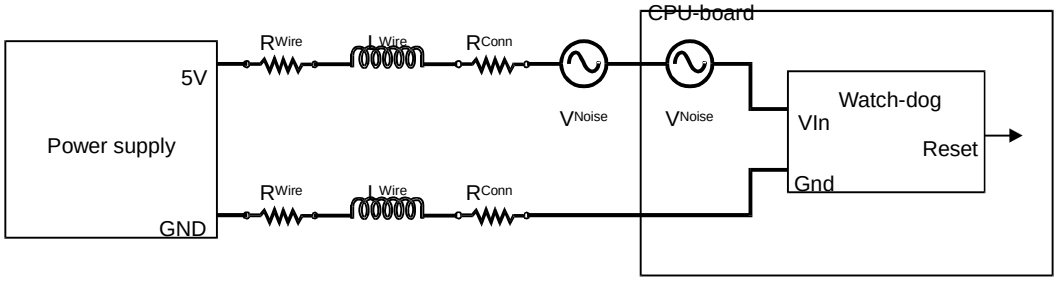
5.1.5 786LCD/S and /MG onboard power supply circuit.



5.1.6 Power supply recommendations.

In order to ensure safe operation of the board, the onboard hardware watchdog monitors the supply voltage and asserts reset when the 5V supply is below 4.76V (max). This ensures that the board is running only while the components operate in their specified voltage range. This voltage limit obviously applies to the voltage seen at the supply to the watch-dog on the board.

In order to meet the minimum 5V requirement, the voltage should be higher at the power supply due to losses from the power supply to the board as illustrated below:



The physical equivalent of the components is as follows:

R_{Conn}	Contact resistance in connectors
R_{Wire}	Wire resistance
L_{Wire}	Inductance of wires
V_{Noise}	Noise in supply introduced by the board, the power supply itself and by other equipment attached to the 5V supply

It is obviously desirable to reduce the contribution of all these components to maintain a voltage above 4.76V at any time. To achieve this, the following guidelines should be observed:

- Use wire with a high copper cross-section area to reduce the resistance and inductance.
- Reduce wire length and number of connectors to a minimum.
- Let power and ground wires follow each other in order to reduce inductance.
- Provide a good voltage margin in order to provide the best possible immunity to load transients and noise generated by the CPU board and other devices attached to the supply. A voltage of 5.0V measured on the board is recommended.

In systems with a high current draw, it should be considered to use power supplies with voltage sense. If the loads additionally have very different connection lengths from a common node and/or very different loads, it should additionally be considered to use power supplies with individual outputs.

5.2 Keyboard and PS/2 mouse connectors

Attachment of a keyboard or PS/2 mouse adapter may be done by means of pinrows (JPKBD, JPMSE) or by means of a combined PS/2 mouse and keyboard connector (KBD).
Both interfaces utilise open-drain signalling with on-board pull-up. Although this interface from a hardware point of view allows multiple devices, it cannot be guaranteed since the keyboard and mouse protocol is not prepared for multiple devices.

The PS/2 mouse and keyboard is supplied from 5V_SB in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A fuse, which is supervised by the chipset.

The signals of the PS/2 mouse interface are:

MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.

The signals of the keyboard interface are:

KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

The connectors are defined in the following sections.

5.2.1 MINI-DIN combined keyboard and mouse Connector (KBD)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	10K	TBD	IOC	MSCLK	6 5	KBDCLK	IOC	TBD	10K	
	-	-	PWR	SB5V	4 3	GND	PWR	-	-	
	10K	TBD	IOC	MSDAT	2 1	KBDDAT	IOC	TBD	10K	

5.2.2 Pin-row Keyboard Connector (JPKBD)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOC	TBD	10K	
2	KBDDAT	IOC	TBD	10K	
3	NC	-	-	-	
4	GND	PWR	-	-	
5	SB5V	PWR	-	-	

5.2.3 Pin-row PS/2 Mouse Connector (JPMSE)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	MSCLK	IOC	TBD	10K	
2	MSDAT	IOC	TBD	10K	
3	NC	-	-	-	
4	GND	PWR	-	-	
5	SB5V	PWR	-	-	

5.3 Display Connectors

The 786 board family provides onboard two basic types of interfaces to a display: Analog CRT interface and a digital interface typically used with flat panels.

5.3.1 CRT Connector (CRT)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN			Signal	Type	Ioh/Iol	Pull U/D	Note
						6		ANA-GND	PWR	-	-	
	/75R	*	A0	RED	1		11	NC	-	-	-	
						7		ANA-GND	PWR	-	-	
	/75R	*	A0	GREEN	2		12	DDCDAT	IO	TBD	2K2	
						8		ANA-GND	PWR	-	-	
	/75R	*	A0	BLUE	3		13	HSYNC	O	TBD		
						9		5V	PWR	-	-	1
	-	-	-	NC	4		14	VSYNC	O	TBD		
						10		DIG-GND	PWR	-	-	
	-	-	PWR	DIG-GND	5		15	DDCCLK	IO	TBD	2K2	

Note :

1. 5V supply is shared with supply pins in COM2 and COM3/4 headers. The common fuse is 1.1A, and the supply is supervised by the chipset.

5.3.2 Signal Description - CRT Connector

HSYNC	CRT horizontal synchronisation output.
VSYNC	CRT vertical synchronisation output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red colour signal to the CRT. For 75 Ohm cable impedance.
GREEN	Analog output carrying the green colour signal to the CRT. For 75 Ohm cable impedance.
BLUE	Analog output carrying the blue colour signal to the CRT. For 75 Ohm cable impedance.
DIG-GND	Ground reference for HSYNC and VSYNC.
ANA-GND	Ground reference for RED, GREEN, and BLUE.

5.3.3 Flat Panel Connector (PANEL)

Note	Type	Signal	Pin		Signal	Type	Note
	PWR	LCDVCC	1	2	LCDVCC	PWR	
		NC	3	4	ENVCC	OT	
		NC	5	6	GND	PWR	
	OT	DE	7	8	ENBKL	O	
	PWR	GND	9	10	LP	OT	
	OT	FLM	11	12	GND	PWR	
	OT	SHFCLK	13	14	GND	PWR	
	OT	P0	15	16	P1	OT	
	PWR	GND	17	18	P2	OT	
	OT	P3	19	20	GND	PWR	
	OT	P4	21	22	P5	OT	
	PWR	GND	23	24	P6	OT	
	OT	P7	25	26	GND	PWR	
	OT	P8	27	28	P9	OT	
	PWR	GND	29	30	P10	OT	
	OT	P11	31	32	GND	PWR	
	OT	P12	33	34	P13	OT	
	PWR	GND	35	36	P14	OT	
	OT	P15	37	38	GND	PWR	
		NC	39	40	NC		
	OT	P16	41	42	P17	OT	
	OT	P18	43	44	P19	OT	
	PWR	GND	45	46	P20	OT	
	OT	P21	47	48	P22	OT	
	OT	P23	49	50	GND	PWR	

The PANEL connector is only available on 786LCD/3.5” boards when using a SODIMM LCDADPT module.

5.3.4 Signal Description - Flat Panel Connector

Signal	Description
P23..0	3.3V Flat panel data output for 8, 9, 12, 16, 18 or 24 bit panels. The flat panel data and control outputs are all controlled for secure power-on/off sequencing
SHFCLK	Shift clock. Pixel clock for flat panel data.
LP	Latch Pulse. Flat panel equivalent of HSYNC (horizontal synchronisation).
FLM	First Line Marker. Flat panel equivalent of VSYNC (vertical synchronisation).
DE	Output Display Enable.
ENBKL	Enable backlight signal.
ENVCC	Enable VCC. Signal to control the panel power-on/off sequencing. A high level may be used externally to turn on the VCC (5 V or 3V3 DC) to the panel.
LCDVCC	VCC supply to the flat panel. This supply includes power-on/off sequencing. The flat panel supply may be either 5V DC or 3.3V DC depending on the CMOS configuration. Maximum load is 1A at both voltages.

Note: All flat panel signalling are 3.3V level and compliant to the standard TTL high/low voltages. Displays requiring 5V signalling (Non-TTL Compatible) can not be used.

5.3.5 SODIMM Extension Module Slot

Note	Type	Signal	Pin		Signal	Type	Note
	PWR	GND	1	2	GND	PWR	
	IOT	AD0	3	4	VBCAD	IO	
	IOT	AD1	5	6	VBCTL1	O	
	IOT	AD2	7	8	VBCTL0	O	
	IOT	AD3	9	10	VBBLANK#	O	
	PWR	VCC3	11	12	VCC3	PWR	
	IOT	AD4	13	14	P15	OT	
	IOT	AD5	15	16	P14	OT	
	IOT	AD6	17	18	P12	OT	
	IOT	AD7	19	20	P13	OT	
	PWR	GND	21	22	GND	PWR	
	IOT	C/BE0#	23	24	PREQ2#	I	
	IOT	C/BE1#	25	26	PGNT2#	OT	
	PWR	VCC3	27	28	VCC3	PWR	
	IOT	PAR	29	30	TRDY#	IOT	
	IOT	FRAME#	31	32	STOP#	IOT	
	IOT	IRDY#	33	34	DEVSEL#	IOT	
	PWR	GND	35	36	GND	PWR	
	IOT	AD8	37	38	P8	OT	
	IOT	AD9	39	40	P9	OT	
	IOT	AD10	41	42	P11	OT	
	IOT	AD11	43	44	P10	OT	
	PWR	VCC3	45	46	VCC3	PWR	
	IOT	AD12	47	48	P23	OT	
	IOT	AD13	49	50	P22	OT	
	IOT	AD14	51	52	P21	OT	
	IOT	AD15	53	54	P20	OT	
	PWR	GND	55	56	GND	PWR	
	O	CLK14M	57	58	PCIRST#	O	
	I	INTA#	59	60	MD36	IO	
		KEY			KEY		
		KEY			KEY		
	IO	PME#	61	62	VCC3	PWR	
	PWR	VCC3	63	64	VCC3	PWR	
	-	NC	65	66	NC	-	
	-	NC	67	68	VCC3	PWR	
	PWR	SB3V	69	70	CLK14M	O	
	PWR	SB3V	71	72	NC	-	
	-	NC	73	74	ENVCC	O	
	PWR	GND	75	76	GND	PWR	
	IO	MD33	77	78	ENBKL	O	
	PWR	LCDVCC	79	80	VCC	PWR	
	PWR	VCC3	81	82	VCC3	PWR	
	IOT	AD16	83	84	P19	OT	
	IOT	AD17	85	86	P16	OT	
	IOT	AD18	87	88	P17	OT	
	IOT	AD19	89	90	P18	OT	
	PWR	GND	91	92	GND	PWR	
	IOT	AD20	93	94	P0	OT	
	IOT	AD21	95	96	P1	OT	
	IOT	AD22	97	98	P2	OT	
	IOT	AD23	99	100	P3	OT	
	PWR	VCC3	101	102	VCC3	PWR	
	IOT	PERR#	103	104	SERR#	IOC	
	-	NC	105	106	NC	-	
	PWR	GND	107	108	GND	PWR	
	O	PCICLK	109	110	VBCLK	I	
	O	VBHCLK	111	112	VGCLK	O	
	PWR	VCC3	113	114	VCC3	PWR	
	IOT	C/BE2#	115	116	NC	-	
	IOT	C/BE3#	117	118	NC	-	
	PWR	GND	119	120	GND	PWR	
	IOT	AD24	121	122	P4	OT	
	IOT	AD25	123	124	P5	OT	
	IOT	AD26	125	126	P6	OT	
	IOT	AD27	127	128	P7	OT	
	PWR	VCC3	129	130	VCC3	PWR	
	IO	DDCDAT2	131	132	AD28	IOT	
	O	DDCCLK2	133	134	AD29	IOT	
	IO	VBVSYNC	135	136	AD30	IOT	
	IO	VBHSYNC	137	138	AD31	IOT	
	PWR	GND	139	140	GND	PWR	
	O	SMCLK2	141	142	SMDAT2	IO	
	PWR	VCC3	143	144	VCC3	PWR	

5.3.6 Signal Description – SODIMM Extension Module Slot

For a description of PCI interface signals (AD[0..31], PAR, FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, PERR#, SERR#, C/BE[0..3]#, PREQ2#, PGNT2#, PCIRST#, INTA#) please refer to section 5.17.3 for a detailed description.

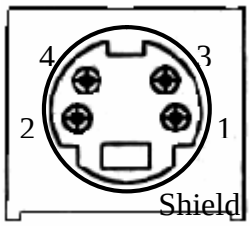
Signal	Description
VBCAD	Register programming serial bus: command/address/data (SIS301)
VBHCLK	Register programming serial bus: clock (SIS301)
VBCTL0	Video control bit0 from primary VGA to SIS301
VBCTL1	Video control bit1 from primary VGA to SIS301
VBCLK	Clock output to primary VGA from SIS301
VGCLK	Clock input from primary VGA to SIS301
VBHSYNC	Horizontal Sync: from primary VGA to SIS301 in slave mode, from SIS301 to primary VGA in master mode.
VBVSYNC	Vertical Sync: from primary VGA to SIS301 in slave mode, from SIS301 to primary VGA in master mode.
VBBLANK#	Data valid indication bit. VBBLANK# is high when input video data are valid. From primary VGA to SIS301
MD33	HW Trap used for module detection
MD36	HW Trap used for module detection
CLK14M	14.31818MHz Reference clock
DDCDAT2	Secondary DDC data
DDCCLK2	Secondary DDC clock
SMDAT2	Secondary SMBus data
SMCLK2	Secondary SMBus clock
PME#	PCI Bus Wakeup Event Reporting .
P[0..23]	3.3V Flat panel data output for 8, 9, 12, 16, 18 or 24 bit panels. The flat panel data and control outputs are all controlled for secure power-on/off sequencing
ENVCC	Enable VCC. Signal to control the panel power-on/off sequencing. A high level may be used externally to turn on the VCC (5 V or 3V3 DC) to the panel.
ENBKL	Enable backlight signal.
LCDVCC	VCC supply to the flat panel. This supply includes power-on/off sequencing. The flat panel supply may be either 5V DC or 3.3V DC depending on the CMOS configuration. Maximum load is 1A at both voltages.
VCC3	+3.3V
SB3V	+3.3V Standby Voltage
VCC	+5V

5.3.7 786LCD DVI, TV-out module.

To show the various display settings in Win95/98, select Control Panel, Display, Settings, Advanced to show the SIS630 Properties. The modes described in the following sections can be found in the Display mode setup.
For Win2000 the display settings can be found in the Control Panel, Display, Settings, Advanced, Utility Manager.

Connector definition

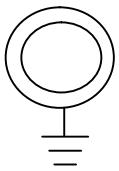
TV-Out S-Video connector



Frontview

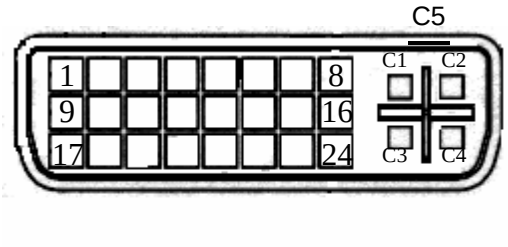
Pin No.	Signal	Type	Pull U/D	Ioh/Iol (mA)	Note
1	GND	PWR			
2	GND	PWR			
3	Y Output	AO			
4	C Output	AO			
Shield	GND	PWR			

TV-Out Phono Jack



Pin No.	Signal	Type	Pull U/D	Ioh/Iol (mA)	Note
Center	Composite Video Out	AO			
House	GND	PWR			

DVI connector



Frontview

Pin No.	Signal	Type	Pull U/D	Ioh/Iol (mA)
1	T.M.D.S. Data 2-	OT		
2	T.M.D.S. Data 2+	OT		
3	T.M.D.S. Data 2/4 Shield	PWR		
4	N.C.	-		
5	N.C.	-		
6	DDC Clock	IO	2K2	
7	DDC Data	IO	2K2	
8	Analog Vertical Sync	AO		
9	T.M.D.S. Data 1-	OT		
10	T.M.D.S. Data 1+	OT		
11	T.M.D.S. Data 1/3 Shield	PWR		
12	N.C.	-		
13	N.C.	-		
14	+5V Fused (200mA)	PWR		
15	GND (return for +5V, Hsync, VSync)	PWR		
16	Hot Plug Detect	I		
17	T.M.D.S. Data 0-	OT		
18	T.M.D.S. Data 0+	OT		
19	T.M.D.S. Data 0/5 Shield	PWR		
20	N.C.	-		
21	N.C.	-		
22	T.M.D.S. Clock Shield	PWR		
23	T.M.D.S. Clock+	OT		
24	T.M.D.S. Clock-	OT		
C1	Analog Red	AO		
C2	Analog Green	AO		
C3	Analog Blue	AO		
C4	Analog Horizontal Sync	AO		
C5	Analog Ground (analog R, G, and B return)	PWR		

5.4 Floppy Disk Connector (FLOPPY)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	1	2	DENSEL0#	OC	/48	-	
	-	-	PWR	GND	3	4	NC	-	-	-	
	-	-	PWR	GND	5	6	NC	-	-	-	
	-	-	PWR	GND	7	8	INDEX#	IS	-	330R	
	-	-	PWR	GND	9	10	MOTEA#	OC	/48	-	
	-	-	PWR	GND	11	12	DRVB#	OC	/48	-	
	-	-	PWR	GND	13	14	DRVA#	OC	/48	-	
	-	-	PWR	GND	15	16	MOTEB#	OC	/48	-	
	-	-	PWR	GND	17	18	DIR#	OC	/48	-	
	-	-	PWR	GND	19	20	STEP#	OC	/48	-	
	-	-	PWR	GND	21	22	WDATA#	OC	/48	-	
	-	-	PWR	GND	23	24	WGATE#	OC	/48	-	
	-	-	PWR	GND	25	26	TRK0#	IS	-	330R	
	-	-	PWR	GND	27	28	WPT#	IS	-	330R	
	10K	-	I	FLPPRES#	29	30	RDATA#	IS	-	330R	
	-	-	PWR	GND	31	32	SIDE1#	OC	/48	-	
	-	-	PWR	GND	33	34	DSKCHG#	IS	-	330R	

Signal Description:

RDATA#	Read Disk Data, active low, serial data input from the floppy disk drive.
WDATA#	Write Disk Data, active low, serial data output to the floppy disk drive.
WGATE#	This output signal enables the head of the selected disk drive to write to the disk.
MOTEA#	This output signal enables the motor in floppy disk drive A.
MOTEB#	This output signal enables the motor in floppy disk drive B.
DRVA#	Active low output signal to select floppy disk drive A.
DRVB#	Active low output signal to select floppy disk drive B.
SIDE1#	This output signal selects side of the disk in the selected drive.
DIR#	This signal controls the direction of the floppy disk drive head movement during a seek operation. A low level request steps through centre.
STEP#	This output signal supplies step pulses to move the head during seek operations.
DENSEL0#	This output indicates whether a low data rate (250/300kbps at low level) or a high data rate (500/1000kbps at high level) has been selected.
TRK0#	Floppy Disk Track 0, active low input to indicate that the head of the selected drive is at track 0.
INDEX#	Floppy Disk Index, active low input indicates the beginning of a disk track.
WPT#	Active low input signal indicating that the selected drive contains a write protected disk.
DSKCHG#	Input pin that senses whether the drive door has been opened or the diskette has been changed.
FLPPRES#	Floppy present. Used by the BIOS to bypass floppy detection, if no floppy is attached.

5.5 Harddisk and Compact flash interface

Two harddisk controllers are available on the board – a primary and a secondary controller. Standard 3½" harddisks or CD-ROM drives may be attached to the primary controller board by means of the 40 pin IDC connector, IDE1.
The secondary controller is shared between a compact flash connector on the bottom side of the board and the IDE2 connector, which is intended for 2½" harddisks.
The SiS630 harddisk controller supports Bus master IDE, ultra DMA 33/66 MHz and standard operation modes. Ultra DMA mode is the fastest with up to 66 MB/Sec bandwidth, to utilise this mode a special driver is required (see Software Manual). 786LCD/ST supports ultra DMA 100 mode.

NOTE: The IDE interface uses 3.3V signalling, and most IDE devices will accept this and work properly. So far the only drive known not to function is the CD-ROM drive: TEAC CD-540E 40X, which requires +5V signalling on the RESET*# pin.

NOTE: For 786LCD/S, /MG, /3.5" and /ST boards with board partnumbers: 5603xxxx, 5604xxxx, 5612xxxx, 5613xxxx, 5622xxxx, and 5607xxxx ("x"=don't care) support is not included of Compact flash disk and Secondary harddisk when connected to the board at the same time. Support of either a Compact flash, one Secondary harddisk, or two Secondary harddisks is available on all versions of the 786LCD/S boards.

The signals used for the harddisk interface are the following:

DA*2..0	Address lines, used to address the I/O registers in the IDE hard disk.
HDCS*1..0#	Hard Disk Chip-Select. HDCS0# selects the primary hard disk.
D*15..8	High part of data bus.
D*7..0	Low part of data bus.
IOR*#	I/O Read.
IOW*#	I/O Write.
IORDY*#	This signal may be driven by the hard disk to extend the current I/O cycle.
RESET*#	Reset signal to the hard disk. The signal is similar to RSTDRV in the PC-AT bus.
HDIRQ*	Interrupt line from hard disk. Routed by the SiS630 chipset to PC-AT bus interrupt.
DDREQ*	Disk DMA Request might be driven by the IDE hard disk to request bus master access to the PCI bus. The signal is used in conjunction with the PCI bus master IDE function and is not associated with any PC-AT bus compatible DMA channel.
DDACK*#	Disk DMA Acknowledge. Active low signal grants IDE bus master access to the PCI bus.
HDACT*#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signals from primary and secondary controller are routed together through diodes and passed to the connector FEATURE.

All of the above signals are compliant to [4].
"*" is "A" for primary and "B" for secondary controller.
The pinout of the connectors are defined in the following sections.

5.5.1 IDE Hard Disk Connector (IDE1)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESETA#	1	2	GND	PWR	-	-	
	/10K	TBD	IO	DA7	3	4	DA8	IO	TBD	-	
	-	TBD	IO	DA6	5	6	DA9	IO	TBD	-	
	-	TBD	IO	DA5	7	8	DA10	IO	TBD	-	
	-	TBD	IO	DA4	9	10	DA11	IO	TBD	-	
	-	TBD	IO	DA3	11	12	DA12	IO	TBD	-	
	-	TBD	IO	DA2	13	14	DA13	IO	TBD	-	
	-	TBD	IO	DA1	15	16	DA14	IO	TBD	-	
	-	TBD	IO	DA0	17	18	DA15	IO	TBD	-	
	-	-	PWR	GND	19	20	NC	-	-	-	
	/5K6	-	I	DDRQA	21	22	GND	PWR	-	-	
	-	TBD	O	IOWA#	23	24	GND	PWR	-	-	
	-	TBD	O	IORA#	25	26	GND	PWR	-	-	
	1K	-	I	IORDYA#	27	28	GND	PWR	-	-	
	-	-	O	DDACKA	29	30	GND	PWR	-	-	
	/10K	-	I	HDIRQA	31	32	NC				
	-	TBD	O	DAA1	33	34	CDLIDA	IO	-		
	-	TBD	O	DAA0	35	36	DAA2	O	TBD	-	
	-	TBD	O	HDCSA0#	37	38	HDCSA1#	O	TBD	-	
	-	-	I	HDACTA#	39	40	GND	PWR	-	-	

5.5.2 IDE Hard Disk Connector (IDE2)

This connector can be used for connection of two IDE drives, if no Compact Flash Disk is installed in CFLASH socket. Notice that the Secondary Slave device is default Disabled in the BIOS setup.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESETB#	1	2	GND	PWR	-	-	
	/10K	TBD	IO	DB7	3	4	DB8	IO	TBD	-	
	-	TBD	IO	DB6	5	6	DB9	IO	TBD	-	
	-	TBD	IO	DB5	7	8	DB10	IO	TBD	-	
	-	TBD	IO	DB4	9	10	DB11	IO	TBD	-	
	-	TBD	IO	DB3	11	12	DB12	IO	TBD	-	
	-	TBD	IO	DB2	13	14	DB13	IO	TBD	-	
	-	TBD	IO	DB1	15	16	DB14	IO	TBD	-	
	-	TBD	IO	DB0	17	18	DB15	IO	TBD	-	
	-	-	PWR	GND	19	20	NC	-	-	-	
	/5K6	-	I	DDRQB	21	22	GND	PWR	-	-	
	-	TBD	O	IOWB#	23	24	GND	PWR	-	-	
	-	TBD	O	IORB#	25	26	GND	PWR	-	-	
	1K	-	I	IORDYB#	27	28	GND	PWR	-	-	
	-	-	O	DDACKB	29	30	GND	PWR	-	-	
	/10K	-	I	HDIRQB	31	32	NC				
	-	TBD	O	DAB1	33	34	CDLIDB	IO			
	-	TBD	O	DAB0	35	36	DAB2	O	TBD	-	
	-	TBD	O	HDCSB0#	37	38	HDCSB1#	O	TBD	-	
	-	-	I	HDACTB#	39	40	GND	PWR	-	-	
			PWR	5V	41	42	5V	PWR			
			PWR	GND	43	44	NC	-	-	-	-

5.5.3 Compact Flash Socket (CFLASH)

The pinout of the compact flash connector is shown below. Pin 1 is the marked by and arrow/triangle on the connector.
If a Compact Flash Disk is installed in this socket, only one IDE drive can be connected to the IDE2 connector. Only Compact flash disks set as Master device will work on the Secondary channel.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
2	-	TBD	IO	DB3	2	1	GND	PWR	-	-	1
	-	TBD	IO	DB5	4	3	DB4	IO	TBD	-	
	/10K	TBD	IO	DB7	6	5	DB6	IO	TBD	-	
	-	-	PWR	GND	8	7	HDCSB0#	O	TBD	-	
	-	-	PWR	GND	10	9	GND	PWR	-	-	
	-	-	PWR	GND	12	11	GND	PWR	-	-	
	-	-	PWR	GND	14	13	5V	PWR	-	-	
	-	-	PWR	GND	16	15	GND	PWR	-	-	
	-	-	O	DAB2	18	17	GND	PWR	-	-	
	-	-	O	DAB0	20	19	DAB1	O	-	-	
	-	TBD	IO	D1	22	21	DB0	IO	TBD	-	
				NC	24	23	DB2	IO	TBD	-	
				NC	26	25	NC				
	-	TBD	IO	DB12	28	27	DB11	IO	TBD	-	
	-	TBD	IO	DB14	30	29	DB13	IO	TBD	-	
	-	TBD	O	HDCSB#	32	31	DB15	IO	TBD	-	
	-	TBD	O	IORB#	34	33	CDLIDB			-	
	-	-	PWR	5V	36	35	IOWB#	O	TBD	-	
	-	-	PWR	5V	38	37	IRQB	I	-	/10K	
				HDACTB#	40	39	GND	PWR			
	1K	-	I	IORDYB#	42	41	RESETB#			-	
	-	-	PWR	5V	44	43	NC				
				NC	46	45	NC				
	-	TBD	IO	DB9	48	47	DB8	IO	TBD	-	
1	-	-	PWR	GND	50	49	DB10	IO	TBD	-	2

Note:
1. Pin is longer than average length of the other pins.
2. Pin is shorter than average length of the other pins.

5.6 Printer Port Connector (PRINTER).

The printer port connector is provided as an IDC26 connector for easy adaptation to the standard DB25 pinout.

The signal definition in standard printer port mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	2K2	(24)/24	OC(O)	STB#	1	2	AFD#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD0	3	4	ERR#	I	-	2K2	
	2K2	24/24	IO	PD1	5	6	INIT#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD2	7	8	SLIN#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD3	9	10	GND	PWR	-	-	
	2K2	24/24	IO	PD4	11	12	GND	PWR	-	-	
	2K2	24/24	IO	PD5	13	14	GND	PWR	-	-	
	2K2	24/24	IO	PD6	15	16	GND	PWR	-	-	
	2K2	24/24	IO	PD7	17	18	GND	PWR	-	-	
	2K2	-	I	ACK#	19	20	GND	PWR	-	-	
	2K2	-	I	BUSY	21	22	GND	PWR	-	-	
	2K2	-	I	PE	23	24	GND	PWR	-	-	
	2K2	-	I	SLCT	25	26	GND	PWR	-	-	

If the DB25 ribbon cable adapter is used, the pinout will be as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	2K2	(24)/24	OC(O)	STB#	1						
						14	AFD#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD0	2						
						15	ERR#	I	-	2K2	
	2K2	24/24	IO	PD1	3						
						16	INIT#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD2	4						
						17	SLIN#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD3	5						
						18	GND	PWR	-	-	
	2K2	24/24	IO	PD4	6						
						19	GND	PWR	-	-	
	2K2	24/24	IO	PD5	7						
						20	GND	PWR	-	-	
	2K2	24/24	IO	PD6	8						
						21	GND	PWR	-	-	
	2K2	24/24	IO	PD7	9						
						22	GND	PWR	-	-	
	2K2	-	I	ACK#	10						
						23	GND	PWR	-	-	
	2K2	-	I	BUSY	11						
						24	GND	PWR	-	-	
	2K2	-	I	PE	12						
						25	GND	PWR	-	-	
	2K2	-	I	SLCT	13						

The interpretation of the signals in standard Centronics mode (SPP) with a printer attached is as follows:

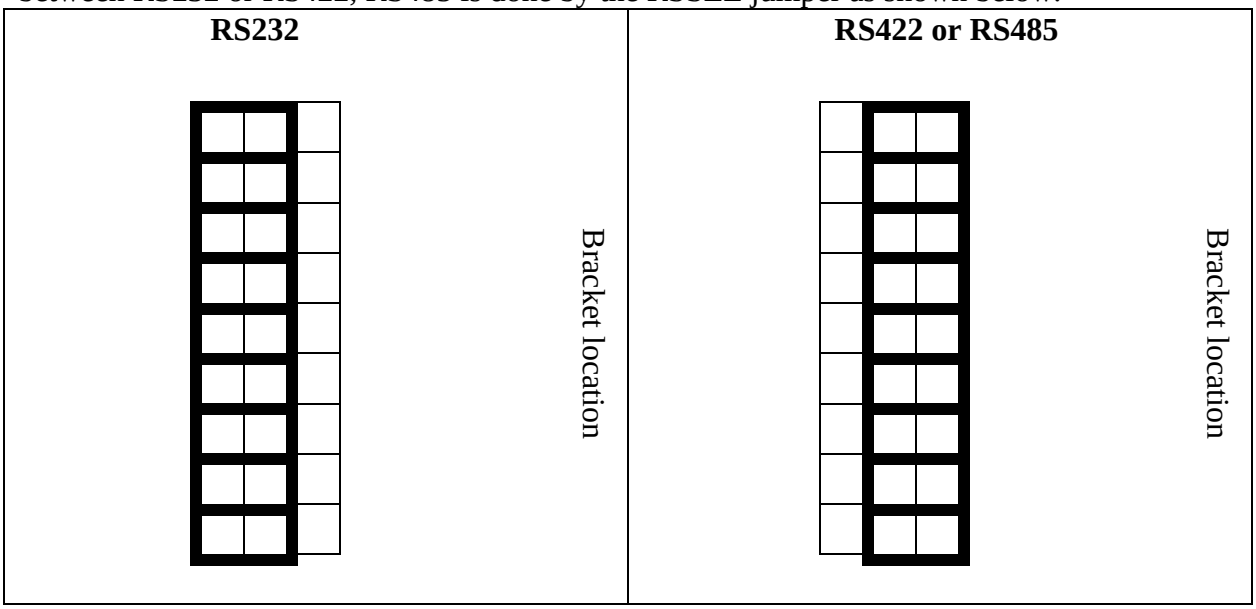
PD7..0	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Signal to select the printer sent from CPU board to printer.
SLCT	Signal from printer to indicate that the printer is selected.
STB#	This signal indicates to the printer that data at PD7..0 are valid.
BUSY	Signal from printer indicating that the printer cannot accept further data.
ACK#	Signal from printer indicating that the printer has received the data and is ready to accept further data.
INIT#	This active low output initialises (resets) the printer.
AFD#	This active low output causes the printer to add a line feed after each line printed.
ERR#	Signal from printer indicating that an error has been detected.
PE#	Signal from printer indicating that the printer is out of paper.

The printer port additionally supports operation in the EPP and ECP mode as defined in [3].

5.7 Serial Ports

4 serial ports are available on the 786LCD/S and 786LCD/MG boards and 2 are available on 786LCD/3.5" boards. RS422 or RS485 modes are not available on 786LCD/3.5" boards.

Serial Port 1 provides three selectable operation modes: RS232, RS422 or RS485 mode. Selection between RS232 or RS422, RS485 is done by the RSSEL jumper as shown below.



The default factory setting is RS232 mode.

Selection between RS422 or RS485, as well as different transmitter enabling options are controlled from the BIOS setup, please refer to the software Manual.
Serial port 2, 3 and 4 provides standard RS232 interfaces.
All serial ports operating in RS232 mode are supplied from an on-board ±12V switch mode power supply.

The typical interpretation of the signals in the COM ports in RS232 mode is as follows:

TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone-ringing signal.

The connector pinout for each operation mode is defined in the following sections.

5.7.1 Serial Port 1 DB9 Connector (COM1) in RS232 Mode

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	5						
						9	RI	I	-	/5K	
	-		O	DTR	4						
						8	CTS	I	-	/5K	
	-		O	TxD	3						
						7	RTS	O		-	
	/5K	-	I	RxD	2						
						6	DSR	I	-	/5K	
	/5K	-	I	DCD	1						

5.7.2 Serial Port 1 DB9 Connector (COM1) in RS422 Mode

RS422 mode uses differential mode signalling increasing noise immunity. Longer cables and higher transfer rates may be utilised. All differential lines should be terminated in the receiver end with a resistor matching the characteristic differential impedance of the cable. These resistors could be placed in the cable housing. For Setup of the transmitter Enabling signal refer to the software Manual. This mode is not available on 786LCD/3.5" boards.
The pinout in the RS422 mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	5						
						9	RTS+	OT		-	1
1	-		OT	TxD+	4						
						8	CTS+	I		/12K	
1	-		OT	TxD-	3						
						7	RTS-	OT		-	1
	/12K	-	I	RxD-	2						
						6	CTS-	I		/12K	
	/12K	-	I	RxD+	1						

Note :
1. These drivers (TxD and RTS) may be tri-stated so multiple drivers can be used on the same media. The controlling signal may be the RTS, DTR or in a permanently on/off configuration. The signal and polarity is selected in the BIOS setup.

5.7.3 Serial Port 1 DB9 Connector (COM1) in RS485 Mode

RS485 mode uses differential mode signalling increasing noise immunity. Longer cables and higher transfer rates may be utilised. All differential lines should be terminated in the receiver end of the network with a resistor matching the characteristic differential impedance of the cable. These resistors could be placed in the cable housing. For Setup of the transmitter Enabling signal refer to the software Manual. This mode is not available on 786LCD/3.5" boards.
The pinout in the RS485 mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	5						
						9	CTS/RTS+	I/OT		/12K	1
1	/12K		I/OT	RxD/TxD+	4						
						8	NC	-	-	-	
1	/12K		I/OT	RxD/TxD-	3						
						7	CTS/RTS-	I/OT	-	/12K	1
	-	-	-	NC	2						
						6	NC	-	-	-	
	-	-	-	NC	1						

Note :
1. These drivers (TxD and RTS) may be tri-stated so multiple drivers can be used on the same media. The controlling signal may be the RTS, DTR or in a permanently on/off configuration. The signal and polarity is selected in the BIOS setup.

5.7.4 Pin Header Serial Port 2 Connector (COM2)

The pinout of Serial port 2 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD	1	2	DSR	I	-		
		-	I	RxD	3	4	RTS	O		-	
	-		O	TxD	5	6	CTS	I	-		
	-		O	DTR	7	8	RI	I	-		
	-	-	PWR	GND	9	10	5V	PWR	-	-	1

Note :
1. 5V supply is shared with supply pins in CRT and COM3/4 header. The common fuse is 1.1A, and the supply is supervised by the chipset.

If the DB9 adapter (ribbon cable) is used, the DB9 pinout will be identical to the pinout of Serial port 1 operating in RS232 mode as defined in section 5.7.1.

5.7.5 Pin Header Serial Port 3&4 Connector (COM3/4)

The pinout of Serial port 3/4 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD3	1	2	DSR3	I	-		
		-	I	RxD3	3	4	RTS3	O		-	
	-		O	TxD3	5	6	CTS3	I	-		
	-		O	DTR3	7	8	RI3	I	-		
	-	-	PWR	GND	9	10	5V	PWR	-	-	1
		-	I	DCD4	11	12	DSR4	I	-		
		-	I	RxD4	13	14	RTS4	O		-	
	-		O	TxD4	15	16	CTS4	I	-		
	-		O	DTR4	17	18	RI4	I	-		
	-	-	PWR	GND	19	20	5V	PWR	-	-	1

Note :

1. 5V supply is shared with supply pins in CRT and COM2 header. The common fuse is 1.1A, and the supply is supervised by the chipset.

These Serial ports are not available on 786LCD/3.5” boards.

If the DB9 adapters (ribbon cable) are used, the DB9 pinouts will be identical to the pinout of Serial port 1 operating in RS232 mode as defined in section 5.7.1.

5.8 Ethernet connector (ETHER)

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used.
The pinout of the RJ45 connector is as follows:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	TXD+	O	-	-	
2	TXD-	O	-	-	
3	RXD+	I	-	-	
4		-	-	-	1
5		-	-	-	1
6	RXD-	I	-	-	
7		-	-	-	2
8		-	-	-	2

Note:

1. Pin 4 and 5 are shorted and terminated by 75Ω to a voltage potential which is common to the common-mode level of all the connector signals.
2. Pin 7 and 8 are shorted and terminated by 75Ω to a voltage potential which is common to the common-mode level of all the connector signals.

Differential mode transmission is used for the transmitter (TXD+/TXD-) and receiver (RXD+/RXD-).

Two LED's are on the RJ45 connector, one is ethernet activity indicator, the other is used as ACPI LED. When the board is in e.g. Suspend to Disk, with standby power on, the LED will be on. When board is on the LED is off.

5.9 USB Connector (USB)

The 786LCD board supports 5 USB channels managed by to separate USB host controllers.
USB channel 0, 1 and 2 is assigned to one controller and channel 3 and 4 to the other.
The USB interface provides a differential mode serial interface with transfer rates up to 12Mbps.
The interface consists of only 2 signals per channel.

In the USB connector two USB lines are provided which have data signals denoted D0+/- and D4+/-.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN CH0	PIN CH1	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	4	8	GND	PWR	-	-	
	/15K	0.25/2	IO	D0+	3	7	D4+	IO	0.25/2	/15K	
	/15K	0.25/2	IO	D0-	2	6	D4-	IO	0.25/2	/15K	
1	-	-	PWR	SB5V	1	5	SB5V	PWR	-	-	1

Note :
1. The USB 5V supply is on-board fused with a 1.1A resetable fuse. The supply is supervised by the chipset.
2. In order to meet the requirements of USB v.1.1 standard, the SB5V supply to the board must be at least 5.00V.

5.9.1 USB Signals

D0+, D0-	Differential bi-directional data signal for USB channel 0. Clock is transmitted along with the data using NRZI encoding. The signalling rate is up to 12MBs.
D4+, D4-	Differential bi-directional data signal for USB channel 1. Clock is transmitted along with the data using NRZI encoding. The signalling rate is up to 12MBs.
SB5V	5V supply for external devices. Fused with 1.1A resetable fuse.

5.10 Bracket Module Interface

The Bracket Module Interface is made by the two connectors : BRACK1 and BRACK2 which contains signals for support of the following features : Audio, Environmental Monitoring / control, 3 additional USB channels, IrDA and Game port.
The signals can be accessed using different Stackable Bracket Modules offered by KONTRON or some of the signals can be wired directly to external connectors / circuits.

5.10.1 Bracket Module Interface (BRACK1)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	AI	MIC_IN	1	2	MIC_BIAS	AI	-	-	
	-	-	PWR	A_GND	3	4	A_GND	PWR	-	-	
	-	-	AO	MONO_OUT	5	6	PHONE_IN	AI	-	-	
	-	-	AI	LINE_IN_L	7	8	LINE_IN_R	AI	-	-	
	-	-	AI	CD_IN_L	9	10	CD_IN_R	AI	-	-	
	-	-	AO	LINE_OUT_L	11	12	LINE_OUT_R	AO	-	-	
	-	-	AO	RAW_LOUT_L	13	14	RAW_LOUT_R	AO	-	-	
	-	-	PWR	CD_GND	15	16	GND	PWR	-	-	
	-	-	AI	TEMP_IN2	17	18	TEMP_GND	AI	-	-	
	-	-	AI	TEMP_IN3	19	20	SPDIF_OUT	O	TBD	-	
	-	-	PWR	5V	21	22	SB5V	PWR	-	-	
		-	I	USB_SUP	23	24	+12V	PWR	-	-	
	/15K	TBD	I/O	USB_D1+	25	26	USB_D1-	I/O	TBD	/15K	
	/15K	TBD	I/O	USB_D2+	27	28	USB_D2-	I/O	TBD	/15K	
	/15K	TBD	I/O	USB_D3+	29	30	USB_D3-	I/O	TBD	/15K	

	Audio input / output.
MIC, MIC_BIAS	The MIC signal is used for microphone input. This input is fed to the MIC1 microphone channel. MIC_BIAS provides 2.25V supplied through a 2.2kΩ resistor. This signal may be used for bias / supply of some microphone types.
PHONE_IN	Input from telephony subsystem speakerphone.
MONO_OUT	Output to telephony subsystem speakerphone.
LINE_IN_L, LINE_IN_R	Right and left line in signals.
CD_IN_L, CD_IN_R	Left and right CD audio input lines.
LINE_OUT_L, LINE_OUT_R	Right and left line out signals. Both signals are capacitor coupled and should have AGND as return.

RAW_LOUT_L, RAW_LOUT_R	Raw right and left line out signals. Both signals are DC coupled and should have capacitors / filter added externally.
AGND	Audio GND, should be used as reference for all audio signals.
CD_GND	GND reference for the CD_IN_L and CD_IN_R signals.
	SPDIF Interface.
SPDIF_OUT	S/PDIF output signal. Can be connected to external copper / optic fibre SPDIF transmitter.
	Environmental Monitoring / Control.
TEMP_IN2, TEMP_IN3	Temperature input. Might be connected to external thermistor or thermal diode. 4.096V is feed through a 30K resistor to these pins.
TEMP_GND	GND reference for temperature measurement.
	USB channels.
USB_D1+, USB_D1-, USB_D2+, USB_D2-, USB_D3+, USB_D3-	Differential bi-directional data signal for USB channel 1 to 3. Clock is transmitted along with the data using NRZI encoding. The signalling rate is up to 12MBs. Channel 1 and 2 are managed by one USB host controller and channel 3 by an other.
USB_SUP	USB power supply supervision input. Can be connected to USB supply (5V or SB5V feed through a fuse) to supervise for shorts on the USB channels.

5.10.2 Bracket Module Interface (BRACK2)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	I	RESERVED	1	2	RESERVED	I	-	-	
	-	-	I	RESERVED	3	4	RESERVED	I	-	-	
	-	-	I	RESERVED	5	6	RESERVED	I	-	-	
	-	-	I	RESERVED	7	8	RESERVED	I	-	-	
	-	-	PWR	5V	9	10	GND	PWR	-	-	
	-	25/25	O	AC_CLK	11	12	RESERVED	O	TBD	-	
	-	TBD	O	AC_RST#	13	14	AC_SYNC	O	TBD	/100K	
	/100K	TBD	O	SDATO	15	16	BIT_CLK	I	-	-	
	/100K	-	I	SDATI0	17	18	EAPD	O	TBD	-	
	/100K	-	I	SDATI1	19	20	SB3V3	PWR	-	-	
	-	-	PWR	3V3	21	22	BSERCLK	I/O	4/12	75K	
	-	TBD	O	PCIRST#	23	24	BSERDAT	I/O	4/12	75K	
	-	8/8	O	IRTX	25	26	IRRX	I	-	-	
	4K7	TBD	O	FAN_CTR2	27	28	FAN_TAC2	I	-	4K7	
	-	-	-	RESERVED	29	30	RESERVED	-	-	-	

	AC97 Interface.
	The AC97 interface can with external circuits be used to implement AC3 surround sound aplications.
AC_SYNC	48 kHz signal, which is used to synchronise CODEC's.
BIT_CLK	This signal is a 12.288 MHz serial data clock, which is generated by the primary CODEC.
SDATO	Serial data output to CODEC's.
SDATI0, SDATI1	Serial data input from primary and secondary CODEC's.
AC_RST#	Hardware reset signal for CODEC'c.
AC_CLK	24.576 MHz clock signal, which can be used for external primary CODEC'c.
EAPD	External Amplifier Power Down, output signal to external amplifier.
	Infrared Communication.
IRTX, IRRX	Infrared transmit output / receive input.
CIRTX, CIRRX	Customer Infrared transmit output / receive input.
	Environmental Monitoring / Control.
FAN_CTR2	FAN control output. Can be used with external FET circuit to perform FAN on / off / PWM control.
FAN_TAC2	FAN tachometer input. Voltage range 0-5 V.
	Other signals
PCIRST#	Reset signal from PCI-bus.
BSERCLK, BSERDAT	Serial I^2C bus signals for used on bracket modules. Alternatively these pins can act as MIDI output / input used in the Game port.

5.11 Bracket Modules

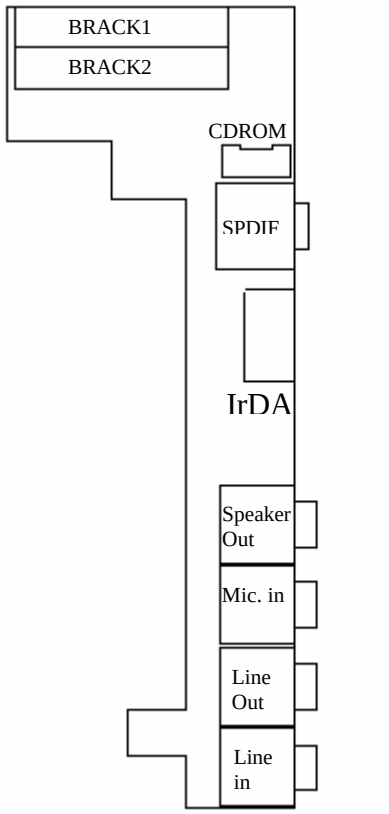
5.11.1 Sound/SPDIF/IrDA Bracket Module

The Sound/SPDIF/IrDA Bracket Module offers CDROM input, Speaker Out, Microphone in, Line In and Out. IrDA transmitter/ receiver and SPDIF fibre optic output are included on the bracket module.

Installation

To support the Audio bracket the BIOS setting Embedded Audio Device under Advanced Chipset Control, Embedded Device Menu must be set to Enabled (default).

Connector Definition



The Speaker Out connector can typically supply 200 mW per channel of continuous average power to an 8R load with 0.1% (THD).

The Microphone input is single-ended supporting most common types of microphones.
Phantom power is supplied to the connector (2.25V).

5.12 Fan connector (FAN)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
3	TAC1	PWR	-	4K7	
2	5V	PWR	100	-	
1	GND	PWR	-	-	

Signal description:

5V	5V supply for fan, can be turned on/off or modulated (PWM) by the chipset. A maximum of 400 mA can be supplied from this pin.
TAC1	Tacho signal from the fan for supervision. 0-5V levels accepted.

5.13 Feature Connector (FEATURE)

The feature connector provides a number of signals to monitor and change the board status and operation. In addition to this are 8 general-purpose inputs/outputs.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	5V	1	2	EXTRST#	I	-	2K7	
	-	4/12	O	PWRGD#	3	4	KBDLOCK#	O	4/12	-	
	2K7	-	I	EXTREQ#	5	6	PWRON#	OC	/24	2K7	
	-	-	AO	EXTSPK	7	8	BUTIN#	I	-	4K7	
	-	HD	O	HDACT#	9	10	GND	PWR	-	-	
	/10K	4/12	IO	GPIO0	11	12	GPIO1	IO	4/12	/10K	
	/10K	4/12	IO	GPIO2	13	14	GPIO3	IO	4/12	/10K	
	/10K	4/12	IO	GPIO4	15	16	GPIO5	IO	4/12	/10K	
	/10K	4/12	IO	GPIO6	17	18	GPIO7	IO	4/12	/10K	
	-	-	PWR	EXTBATT	19	20	GND	PWR	-	-	

The function of the signals is as follows:

EXTRST#	External reset input. A logic low level at this pin will reset the entire CPU board.
PWRGD#	Indicate whatever the board is reset due to power fault, supervision reset or by external reset. High: The board is reset. Low: The board is not reset due to one of the above mentioned causes.
KBDLOCK#	Keyboard Lock Input. Pull this pin low to Enable Keyboard Lock. The BIOS setting “Keyboard Lock Input” must be enabled to use this feature. This feature is **not** available on the 786LCD/ST board.
EXTREQ#	External Request Switch. This active low input signal can activate NMI-, SMI- or a standard AT-Bus IRQ-interrupt. This feature requires a vendor code and is currently not supported.
EXTSPK	An external speaker may be connected between this pin and ground. The speaker impedance must be 8 ohms or higher. For improved sound ‘quality’, an amplifier or speaker with higher impedance (150Ω or more) should be used.
HDACT#	Hard Disk Activity. This pin is a logically AND between the two HDACTx# signals in the IDE_ONE1 and IDE_TWO2 connectors. The signal is fed through a 330R series resistor for direct connection of an LED.
GPIO7..0	General Purpose Inputs / Outputs. These Signals may be controlled or observed through the use of the KONTRON API (Advanced Programmer Interface) available for Win98, WinNT, and Win2000. See Software Manual for details.
EXTBATT	An external primary cell battery can be connected between this pin and GND. The battery will not be recharged. The battery voltage should be within the range : 2.5 - 4.0 V DC. Typical current is 1 µA.
5V	5 V DC supply output for connection to LEDs or switches. No more than 100 mA DC may be drawn from this pin.
PWRON#	Active low output signal that could be used to turn external power supplies ON. The SB5V supply to the board should not be controlled externally, because power supply switches are integrated onboard. The signal will go low when BUTIN is pulsed low.
BUTIN#	This active low input signal is a part of the Power Control logic and could be connected to an external “Power On” button. The signal is internally debounced.

5.14 SCSI Interface (786LCD/MG boards only)

5.14.1 68-Pin Wide Internal and External SCSI Connector – Single Ended Mode - WSCSI

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	Gnd	1	35	DB(12)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	2	36	DB(13)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	3	37	DB(14)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	4	38	DB(15)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	5	39	DB(PH)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	6	40	DB(0)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	7	41	DB(1)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	8	42	DB(2)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	9	43	DB(3)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	10	44	DB(4)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	11	45	DB(5)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	12	46	DB(6)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	13	47	DB(7)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	14	48	DB(PL)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	15	49	Gnd Sense	PWR	-	-	
	-	-	O	Diffsens	16	50	Gnd	PWR	-	-	
2	-	-	PWR	Termpwr	17	51	Termpwr	PWR	-	-	
	-	-	PWR	Termpwr	18	52	Termpwr	PWR	-	-	
				Reserved	19	53	Reserved				
	-	-	PWR	Gnd	20	54	Gnd	PWR	-	-	
	-	-	PWR	Gnd	21	55	ATN-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	22	56	Gnd	PWR	-	-	
	-	-	PWR	Gnd	23	57	BSY-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	24	58	ACK-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	25	59	RST-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	26	60	MSG-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	27	61	SEL-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	28	62	C/D-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	29	63	REQ-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	30	64	I/O-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	31	65	DB(8)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	32	66	DB(9)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	33	67	DB(10)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	34	68	DB(11)-	OC	-/100mA	110Ω/-	1

Note 1 : Active Termination 110Ω Typical pull up to Termpwr.
Note 2 : Termpwr supplied through Schottky diode to prevent backflow of power.

5.14.2 68-Pin Wide Int. and Ext. SCSI Connector – Low Voltage Diff. Mode - WSCSI

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	105Ω	3.5mA	O	DB(12)+	1	35	DB(12)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(13)+	2	36	DB(13)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(14)+	3	37	DB(14)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(15)+	4	38	DB(15)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(PH)+	5	39	DB(PH)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(0)+	6	40	DB(0)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(1)+	7	41	DB(1)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(2)+	8	42	DB(2)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(3)+	9	43	DB(3)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(4)+	10	44	DB(4)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(5)+	11	45	DB(5)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(6)+	12	46	DB(6)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(7)+	13	47	DB(7)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(PL)+	14	48	DB(PL)-	O	3.5mA	105Ω	1
	-	-	PWR	Gnd	15	49	Gnd Sense	PWR	-	-	
	-	-	O	Diffsens	16	50	Gnd	PWR	-	-	
2	-	-	PWR	Termpwr	17	51	Termpwr	PWR	-	-	
	-	-	PWR	Termpwr	18	52	Termpwr	PWR	-	-	
				Reserved	19	53	Reserved				
	-	-	PWR	Gnd	20	54	Gnd	PWR	-	-	
	105Ω	3.5mA	O	ATN+	21	55	ATN-	O	3.5mA	105Ω	1
	-	-	PWR	Gnd	22	56	Gnd	PWR	-	-	
	105Ω	3.5mA	O	BSY+	23	57	BSY-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	ACK+	24	58	ACK-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	RST+	25	59	RST-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	MSG+	26	60	MSG-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	SEL+	27	61	SEL-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	C/D+	28	62	C/D-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	REQ+	29	63	REQ-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	I/O+	30	64	I/O-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(8)+	31	65	DB(8)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(9)+	32	66	DB(9)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(10)+	33	67	DB(10)-	O	3.5mA	105Ω	1
	105Ω	3.5mA	O	DB(11)+	34	68	DB(11)-	O	3.5mA	105Ω	1

Note 1 : Termination 105Ω differential and 150Ω common mode typical.
Note 2 : Termpwr supplied through Schottky diode to prevent backflow of power.

5.14.3 50-pin Internal SCSI-connector – Single Ended Only - JPSCSI

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	Gnd	1	2	DB(0)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	3	4	DB(1)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	5	6	DB(2)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	7	8	DB(3)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	9	10	DB(4)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	11	12	DB(5)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	13	14	DB(6)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	15	16	DB(7)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	17	18	DB(PL)-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	19	20	Gnd	PWR	-	-	
	-	-	PWR	Gnd	21	22	Gnd Sense	PWR	-	-	
	-	-	PWR	Gnd	23	24	Gnd	PWR	-	-	
	-	-	-	NC	25	26	Termpwr	PWR	-	-	2
	-	-	PWR	Gnd	27	28	Gnd	PWR	-	-	
	-	-	PWR	Gnd	29	30	Gnd	PWR	-	-	
	-	-	PWR	Gnd	31	32	ATN-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	33	34	Gnd	PWR	-	-	
	-	-	PWR	Gnd	35	36	BSY-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	37	38	ACK-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	39	40	RST-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	41	42	MSG-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	43	44	SEL-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	45	46	C/D-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	47	48	REQ-	OC	-/100mA	110Ω/-	1
	-	-	PWR	Gnd	49	50	I/O-	OC	-/100mA	110Ω/-	1

Note 1 : Active Termination 110Ω Typical pull up to Termpwr.
Note 2 : Termpwr supplied through Schottky diode to prevent backflow of power .

5.14.4 Signal Description

DATA.

DB(0)+/-..DB(7)+/-:

SCSI Low Byte Data Lines. Used for 8-bit transfers while DB(8)+/-..DB(15)+/- are floated. The SCSI Data Lines DB(0)+/-..DB(15)+/- drive the ID during Arbitration and Selection, and command and data information as well as status and messages.

DB(8)+/-..DB(15)+/-:

SCSI High Byte Data Lines. Used with Low Byte for 16-bit transfers.

COMMAND.

DB(PL)+/-:

SCSI Low Byte Parity. This bit provides odd parity for DB(0)+/-..DB(7)+/-.

DB(PH)+/-:

SCSI High Byte Parity. This bit provides odd parity for DB(8)+/-..DB(15)+/-. Floated for 8-bit transfers.

C/D+/-:

Command/Data. This control line is received when in Initiator mode or driven when in Target mode. It indicates Command or Message phase when asserted, and Data phase when deasserted. Used for 8- and 16-bit transfers.

I/O+/-:

In/Out. This control line is received when in Initiator mode or driven when in Target mode. It indicates the In direction when asserted, and the Out direction when deasserted. Used for 8- and 16-bit transfers.

MSG+/-:

Message. This control line is received when in Initiator mode or driven when in Target mode. It indicates a Message phase when asserted, and a Command or Data phase when deasserted. Used for 8- and 16-bit transfers.

REQ+/-:

Request. This control line is received by the device when in Initiator mode or driven when in Target mode. A target will assert REQ to indicate a byte is ready or is needed by the Target. Used for 8- and 16-bit transfers.

ACK+/-:

Acknowledge. This control line is received by the device when in Target mode or driven when in Initiator mode. An Initiator will assert ACK to indicate a byte is ready for or was received from the Target. Used for 8- and 16-bit transfers.

RST+/-:

Reset. This line is received and/or driven. It is interpreted as a hard reset and will clear all commands pending on the SCSI bus. Used for 8- and 16-bit transfers.

SEL+/-:

Select. This line is driven after a successful arbitration to Select as an Initiator or Reselect as a Target, otherwise it is received. Used for 8- and 16-bit transfers.

BSY+/-:

Busy. This line is driven by the Initiator as a handshake during arbitration, and received for the rest of the transfer. As a Target, it is driven also as a handshake during Arbitration, and then it is driven for the rest of the transfer. Used for 8- and 16-bit transfers.

ATN+/-:

Attention. This line is driven as an Initiator when a special condition occurs. It is received by the Target. Used for 8- and 16-bit transfers.

POWER.

TERMPWR: Termination Power.

5.15 IEEE1394 Interface (FW1 and FW2)

The 786LCD/MG board supports 2 IEEE1394 channels managed by the NEC µPD72872 controller.

FW1

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1	-	-	PWR	Vcable	1	2	GND	PWR	-	-	
	-		IO	TpB0p	3	4	TpB0n	IO		-	
	-		IO	TpA0p	5	6	TpA0n	IO		-	

Note 1 : Fused by self healing fuse with Itrip = 4A.

FW2

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1	-	-	PWR	Vcable	1	2	GND	PWR	-	-	
	-		IO	TpB1p	3	4	TpB1n	IO		-	
	-		IO	TpA1p	5	6	TpA1n	IO		-	

Note 1 : Fused by self healing fuse with Itrip = 4A.

5.15.1 Signal Description IEEE1394

Signals.

TpA0p / TpA0n :
Port 1 twisted pair A input/output positive and negative.

TpB0p / TpB0n :
Port 1 twisted pair B input/output positive and negative.

TpA1p / TpA1n :
Port 2 twisted pair A input/output positive and negative.

TpB1p / TpB1n :
Port 2 twisted pair B input/output positive and negative.

Power.

Vcable :
+12 VDC supplied through Schottky diode to prevent backflow of power and separately fused with Itrip = 4A. 12 VDC must be applied to PWRCON to enable these supplies.

5.16 ISA bus connectors

5.16.1 PC104 Connector (PC104XT & PC104AT)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	B32	A32			GND	PWR	-	-	
	-	-	PWR	GND	B31	A31			SA0	IO	24/24	8K2	
	-	12/12	O	OSC	B30	A30			SA1	IO	24/24	8K2	
	-	-	PWR	5V	B29	A29			SA2	IO	24/24	8K2	
	4K7	24/24	OT	BALE	B28	A28			SA3	IO	24/24	8K2	
	-	-	-	NC			C19	D19	GND	PWR	-	-	
	-	24/24	OT	TC	B27	A27			SA4	IO	24/24	8K2	
	8K2	24/24	IO	SD15			C18	D18	GND	PWR	-	-	
	-	24/24	O	DACK2#	B26	A26			SA5	IO	24/24	8K2	
	8K2	24/24	IO	SD14			C17	D17	MASTER#	I		1K	1
	8K2	-	I	IRQ3	B25	A25			SA6	IO	24/24	8K2	
	8K2	24/24	IO	SD13			C16	D16	5V	PWR	-	-	
	8K2	-	I	IRQ4	B24	A24			SA7	IO	24/24	8K2	
	8K2	24/24	IO	SD12			C15	D15	DRQ7	I	-	/8K2	
	8K2	-	I	IRQ5	B23	A23			SA8	IO	24/24	8K2	
	8K2	24/24	IO	SD11			C14	D14	DACK7#	O	24/24	-	
	8K2	-	I	IRQ6	B22	A22			SA9	IO	24/24	8K2	
	8K2	24/24	IO	SD10			C13	D13	DRQ6	I	-	/8K2	
	8K2	-	I	IRQ7	B21	A21			SA10	IO	24/24	8K2	
	8K2	24/24	IO	SD9			C12	D12	DACK6#	O	24/24	-	
	-	24/24	O	SYSCLK	B20	A20			SA11	IO	24/24	8K2	
	8K2	24/24	IO	SD8			C11	D11	DRQ5	I	-	/8K2	
2	1K	24/24	IO	REFRESH#	B19	A19			SA12	IO	24/24	8K2	
	8K2	24/24	IO	MEMW#			C10	D10	DACK5#	O	24/24	-	
	/8K2	-	I	DRQ1	B18	A18			SA13	IO	24/24	8K2	
	8K2	24/24	IO	MEMR#			C9	D9	DRQ0	I	-	/8K2	
	-	24/24	O	DACK1#	B17	A17			SA14	IO	24/24	8K2	
	8K2	24/24	IO	LA17			C8	D8	DACK0#	O	24/24	-	
	/8K2	-	I	DRQ3	B16	A16			SA15	IO	24/24	8K2	
	8K2	24/24	IO	LA18			C7	D7	IRQ14	I	-	8K2	
	-	24/24	O	DACK3#	B15	A15			SA16	IO	24/24	8K2	
	8K2	24/24	IO	LA19			C6	D6	IRQ15	I	-	8K2	
	8K2	24/24	IO	IOR#	B14	A14			SA17	IO	24/24	8K2	
	8K2	24/24	IO	LA20			C5	D5	IRQ12	I	-	8K2	
	8K2	24/24	IO	IOW#	B13	A13			SA18	IO	24/24	8K2	
	8K2	24/24	IO	LA21			C4	D4	IRQ11	I	-	8K2	
	1K	24/24	OT	SMEMR#	B12	A12			SA19	IO	24/24	8K2	
	8K2	24/24	IO	LA22			C3	D3	IRQ10	I	-	8K2	
	1K	24/24	OT	SMEMW#	B11	A11			AEN	OT	24/24	-	
	8K2	24/24	IO	LA23			C2	D2	IOCS16#	IOC	-	1K	
	-	-	PWR	GND	B10	A10			IOCHRDY	IOC	-	4K7	
	4K7	24/24	IO	SBHE#			C1	D1	MEMCS16#	IOC	-	1K	
	-	-	PWR	+ 12Ve	B9	A9			SD0	IO	24/24	8K2	
	-	-	PWR	GND			C0	D0	GND	PWR	-	-	
	1K	-	IOC	OWS#	B8	A8			SD1	IO	24/24	8K2	
	-	-	PWR	- 12Ve	B7	A7			SD2	IO	24/24	8K2	
	/8K2	-	I	DRQ2	B6	A6			SD3	IO	24/24	8K2	
	-	-	PWR	- 5V	B5	A5			SD4	IO	24/24	8K2	
	8K2	-	I	IRQ9	B4	A4			SD5	IO	24/24	8K2	
	-	-	PWR	5V	B3	A3			SD6	IO	24/24	8K2	
	-	24/24	O	RESETDRV	B2	A2			SD7	IO	24/24	8K2	
	-	-	PWR	GND	B1	A1			IOCHCHK#	IOC	-	4K7	

5.16.2 PC-AT Edge Connector

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN C	PIN S	Signal	Type	Ioh/Iol	Pull U/D	Note
	4K7	-	IOC	IOCHCHK#	A1	B1	GND	PWR	-	-	
	8K2	24/24	IO	SD7	A2	B2	RESETDRV		24/24	-	
	8K2	24/24	IO	SD6	A3	B3	5V	PWR	-	-	
	8K2	24/24	IO	SD5	A4	B4	IRQ9	I	-	8K2	
	8K2	24/24	IO	SD4	A5	B5	- 5V	PWR	-	-	
	8K2	24/24	IO	SD3	A6	B6	DRQ2	I	-	/8K2	
	8K2	24/24	IO	SD2	A7	B7	- 12Ve	PWR	-	-	
	8K2	24/24	IO	SD1	A8	B8	OWS#	IOC	-	1K	
	8K2	24/24	IO	SD0	A9	B9	+ 12Ve	PWR	-	-	
	1K	-	IOC	IOCHRDY	A10	B10	GND	PWR	-	-	
	-	24/24	OT	AEN	A11	B11	SMEMW#	OT	24/24	1K	
	8K2	24/24	IO	SA19	A12	B12	SMEMR#	OT	24/24	1K	
	8K2	24/24	IO	SA18	A13	B13	IOW#	IO	24/24	8K2	
	8K2	24/24	IO	SA17	A14	B14	IOR#	IO	24/24	8K2	
	8K2	24/24	IO	SA16	A15	B15	DACK3#	O	24/24	-	
	8K2	24/24	IO	SA15	A16	B16	DRQ3	I	-	/8K2	
	8K2	24/24	IO	SA14	A17	B17	DACK1#	O	24/24	-	
	8K2	24/24	IO	SA13	A18	B18	DRQ1	I	-	/8K2	
	8K2	24/24	IO	SA12	A19	B19	REFRESH#	IO	24/24	1K	2
	8K2	24/24	IO	SA11	A20	B20	SYSCLK	O	24/24	-	
	8K2	24/24	IO	SA10	A21	B21	IRQ7	I	-	8K2	
	8K2	24/24	IO	SA9	A22	B22	IRQ6	I	-	8K2	
	8K2	24/24	IO	SA8	A23	B23	IRQ5	I	-	8K2	
	8K2	24/24	IO	SA7	A24	B24	IRQ4	I	-	8K2	
	8K2	24/24	IO	SA6	A25	B25	IRQ3	I	-	8K2	
	8K2	24/24	IO	SA5	A26	B26	DACK2#	O	24/24	-	
	8K2	24/24	IO	SA4	A27	B27	TC	OT	24/24	-	
	8K2	24/24	IO	SA3	A28	B28	BALE	OT	24/24	4K7	
	8K2	24/24	IO	SA2	A29	B29	5V	PWR	-	-	
	8K2	24/24	IO	SA1	A30	B30	OSC	O	12/12	-	
	8K2	24/24	IO	SA0	A31	B31	GND	PWR	-	-	
		COMPONENT SIDE			**C**	**S**	**SOLDER SIDE**				
	4K7	24/24	IO	SBHE#	C1	D1	MEMCS16#	IOC	-	1K	
	8K2	24/24	IO	LA23	C2	D2	IOCS16#	IOC	-	1K	
	8K2	5/2	IO	LA22	C3	D3	IRQ10	I	-	8K2	
	8K2	24/24	IO	LA21	C4	D4	IRQ11	I	-	8K2	
	8K2	24/24	IO	LA20	C5	D5	IRQ12	I	-	8K2	
	8K2	24/24	IO	LA19	C6	D6	IRQ15	I	-	8K2	
	8K2	24/24	IO	LA18	C7	D7	IRQ14	I	-	8K2	
	8K2	24/24	IO	LA17	C8	D8	DACK0#	O	24/24	-	
	8K2	24/24	IO	MEMR#	C9	D9	DRQ0	I	-	/8K2	
	8K2	24/24	IO	MEMW#	C10	D10	DACK5#	O	24/24	-	
	8K2	24/24	IO	SD8	C11	D11	DRQ5	I	-	/8K2	
	8K2	24/24	IO	SD9	C12	D12	DACK6#	O	24/24	-	
	8K2	24/24	IO	SD10	C13	D13	DRQ6	I	-	/8K2	
	8K2	24/24	IO	SD11	C14	D14	DACK7#	O	24/24	-	
	8K2	24/24	IO	SD12	C15	D15	DRQ7	I	-	/8K2	
	8K2	24/24	IO	SD13	C16	D16	5V	PWR	-	-	
	8K2	24/24	IO	SD14	C17	D17	MASTER#	NC	-	1K	1
	8K2	24/24	IO	SD15	C18	D18	GND	PWR	-	-	

1. Master mode is not supported on the 786LCD boards.
2. While Master mode is not supported, the Refresh signal will only act as output.

5.16.3 ISA signal description

ADDRESS.

LA23..17	The address signals LA23..17 define the selection of a 128kB section of memory space within the 16MB address range of the 16 bit data bus. These signals are active high. The validity of the MEMCS16# depends on these signals only. These address lines are presented to the system with tri-state drivers. The permanent master drives these lines except when an alternate master cycle occurs; in this case the temporary master drives these lines. The LA signals are not defined for I/O accesses.
SA19..0	The address signals SA..0 define the selection with the granularity of one byte within the 1MB section of memory defined by the LA address lines. The address lines SA19..17 that are coincident with LA19..17 are defined to have the same value as LA19..17 for all memory cycles. These signals are active high. These address lines are presented to the system with tri-state drivers. The permanent master drives these lines except when an alternate master cycle occurs; in this case the temporary master drives these lines. SA7..0.
SBHE#	This signal is an active low signal, that indicates that a byte is being transferred on the upper byte (SD15..8) of the 16 bit bus. All bus masters will drive this line with a tri-state driver.

DATA.

SD15..8	These signals are defined for the high order byte of the 16 bit data bus. Memory or I/O transfers on this part of the bus are defined when SBHE# is active.
SD7..0	These signals are defined for the low order byte of the 16 bit data bus being the only bus for 8 bit PC-AT/PC104 adapter boards. Memory or I/O transfers on this part of the data bus are defined for 8 bit operations with even or odd addresses and for 16 bit operations for odd addresses only. The signals SA0 and SBHE# are used to define the data present on this bus as defined below:

SBHE#	SA0	SD15-SD8	SD7-SD0	Action
0	0	ODD	EVEN	Word transfer
0	1	ODD	ODD	Byte transfer on SD15-SD8
1	0	-	EVEN	Byte transfer on SD7-SD0
1	1	-	ODD	Byte transfer on SD7-SD0

COMMANDS.

BALE	This is an active high signal used to latch valid addresses from the current bus master on the falling edge of BALE. During DMA and alternate master cycles, BALE is forced high for the duration of the transfer. The permanent master drives BALE with a totem-pole driver.
IOR#	This is an active low signal driven by the current master to indicate an I/O read operation. I/O mapped devices using this strobe for selection should decode addresses SA15..0 and AEN. Additionally, DMA devices will use IOR# in conjunction with $DACK_n$# to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver.
IOW#	This is an active low signal driven by the current master to indicate an I/O write operation. I/O mapped devices using this strobe for selection should decode addresses SA15..0 and AEN. Additionally, DMA devices will use IOR# in conjunction with $DACK_n$# to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver.
SMEMR#	This is an active low signal driven by the permanent master to indicate a memory read operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA19..0 only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
SMEMW#	This is an active low signal driven by the permanent master to indicate a memory write operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA19..0 only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
MEMR#	This is an active low signal driven by the current master to indicate a memory read operation. Memory mapped devices using this strobe should decode addresses LA23..17 and SA19..0. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
MEMW#	This is an active low signal driven by the current master to indicate a memory write operation. Memory mapped devices using this strobe should decode addresses LA23..17 and SA19..0. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.

TRANSFER RESPONSE.

IOCS16#	This is an active low signal driven by an I/O-mapped PC-AT/PC104 adapter indicating that the I/O device located at the address is a 16 bit device. This open collector signal is driven, based on SA15..0 only (not IOR# and IOW#) when AEN is not asserted.
MEMCS16#	This is an active low signal driven by a memory mapped PC-AT/PC104 adapter indicating that the memory device located at the address is a 16 bit device. This open collector signal is driven, based on LA23..17 only.
0WS#	This signal is an active low open-collector signal asserted by a 16 bit memory mapped device causing an early termination of the current transfer. It should be gated with MEMR# or MEMW# and is not valid during DMA transfers. IOCHRDY precedes 0WS#.
IOCHRDY	This is an active high signal driven inactive by the target of either a memory or an I/O operation to extend the current cycle. This open collector signal is driven based on the system address and the appropriate control strobe. IOCHRDY precedes 0WS#.
IOCHCK#	This is an active low signal driven active by a PC-AT/PC104 adapter detecting a fatal error during bus operation. When this open collector signal is driven low it will typically cause a SMI.

CONTROLS.

SYSCLK	This clock oscillates at 8.33MHz.
OSC	This is a clock signal with a 14.31818 MHz ± 50 ppm frequency and a 50 ± 5% duty cycle. The signal is driven by the permanent master.
RESETDRV	This active high signal indicates that the adapter should be brought to an initial reset condition. This signal will be asserted by the permanent master on the bus for at least 100 ms at power-up or watchdog time-out to ensure that adapters in the system are properly reset. When active, all adapters should turn off or tri-state all drivers connected to the bus.

INTERRUPTS.

IRQ3..7, IRQ9..12, IRQ14..15	These signals are active high signals, which indicate the presence of an interrupting PC-AT/PC104 bus adapter. Unused interrupts should be masked.

BUS ARBITRATION.

DRQ0..3, DRQ5..7	These signals are active high signals driven by a DMA bus adapter to indicate a request for a DMA bus operation. DRQ0..3 request 8 bit DMA operations, while DRQ5..DRQ7 request 16 bit operations. All bus DMA adapters will drive these lines with a tri-state driver. The permanent master monitors these signals to determine which of the DMA devices, if any are requesting the bus.
DACK0#..3#, DACK5#..7#	These signals are active low signals driven by the permanent master to indicate that a DMA operation can begin. They are continuously driven by a totem pole driver for DMA channels attached.
AEN	This signal is an active high totem pole signal driven by the permanent master to indicate that the DMA controller drives the address lines. The assertion of AEN disables response to I/O port addresses when I/O command strobes are asserted. AEN being asserted, only the device with active $DACK_n$# should respond.
REFRESH#	This is an active low signal driven by the permanent master to indicate a memory refresh operation.
TC	This active high signal is asserted during a read or write command indicating that the DMA controller has reached a terminal count for the current transfer. $DACK_n$# must be presented by the bus adapter to validate the TC signal.
MASTER#	Master mode is not supported.

5.16.4 ISA Bus limitations

For the 786LCD/S and 786LCD/MG certain restrictions apply to the supported cycles on the ISA interface. The limitations are described below.

On the 786LCD series boards the ISA Bus is implemented by using a LPC to ISA Bus converter, because the chipset does not directly support ISA Bus interface. The LPC Bus only supports 8 Bit I/O and Memory cycles, the LPC interface automatically converts 16 Bit cycles into two 8 Bit cycles in succession.

For the 786LCD/S and 786LCD/MG boards no information regarding the original size of the cycle is transmitted through the LPC Bus, so the LPC to ISA Bus converter is not able to re-construct the original cycle size, but can only handle it as two separate 8 Bit cycles. Most 16 Bit I/O or Memory accessed ISA cards will work properly despite the cycle split, as they can also be accessed with 8 Bit cycles. The main impact is the reduced bandwidth that may affect ISA cards with heavy data transfer requirements. However many of those will use DMA cycles, where 16 Bit cycles are supported.

For the 786LCD/ST board the information regarding the original cycle is found by detecting the cycle size on the PCI bus and using this for handling the 2 byte I/O and Memory cycles. 16 Bit I/O and Memory transfers will still be handled as 2 x 8 Bit cycles.

Note: In order to allow room for connecting serial port C+D on 786LCD/S, 786LCD/MG, 786LCD/ST, PC104 connector spacers must be used for the PC104 devices.

The above is summarised in the table below:

Cycle Type	Sizes Supported	/S, /MG	/ST
Memory Read	1 byte	Supported	Supported
Memory Write	1 byte	Supported	Supported
I/O Read	1 byte	Supported	Supported
I/O Write	1 byte	Supported	Supported
Memory Read	2 byte	Not supported	Supported
Memory Write	2 byte	Not supported	Supported
I/O Read	2 byte	Not supported	Supported
I/O Write	2 byte	Not supported	Supported
DMA Read	1, 2 bytes	Supported	Supported
DMA Write	1, 2 bytes	Supported	Supported
Bus Master Cycles	1, 2 bytes	Not supported	Not supported

5.17 PC104+ PCI connector

5.17.1 PC104+ PCI Connector

The PC104+ connector provides a complete PCI interface with multiple copies of selected signals for up to 4 PC104+ boards to be used. Three of these boards may utilise the PCI bus mastering capability.
The 3.3V supply in the connector is only for low power boards. The total 3.3V current draw from the board should not exceed 1A at any time. This current draw includes current draw from the panel connector (JPLCD). External PCI component must be designed to work in a 3.3V signaling environment as defined in [2] and [5] (Universal board).
Pin A1 is located closest to the Processor.

Pin	A	B	C	D
1	GND	Reserved	5V	AD00
2	+5V	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	+5V	AD10	GND
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1#	AD15	+3.3V
9	SERR#	GND	SB0#	PAR
10	GND	PERR#	+3.3V	SDONE
11	STOP#	+3.3V	LOCK#	GND
12	+3.3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3V
14	GND	AD16	+3.3V	C/BE2#
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	+5V(I/O)	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	+5V(I/O)
24	GND	REQ2#	+5V	GNT0#
25	GNT1#	+5V(I/O)	GNT2#	GND
26	+5V	CLKA	GND	CLKB
27	CLKC	+5V	CLKD	GND
28	GND	INTD#	+5V	RST#
29	+12Ve	INTA#	INTB#	INTC#
30	-12Ve	Reserved	Reserved	GND

For a detailed description of PCI bus transactions, refer to [5].

5.17.2 PCI Edge Connector

Note	Type	Signal	PIN S	PIN C	Signal	Type	Note
	PWR	-12V	F01	E01	TRST#	O	2
2	O	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	O	2
2	I	TDO	F04	E04	TDI	O	2
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	I	
	I	INTB#	F07	E07	INTC#	I	
	I	INTD#	F08	E08	+5V	PWR	
	I	REQ2#	F09	E09	CLKC	O	
	I	REQ3#	F10	E10	+5V (I/O)	PWR	
	OT	GNT2#	F11	E11	CLKD	O	
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
	O	CLKA	F14	E14	GNT3#	OT	
	PWR	GND	F15	E15	RST#	O	
	O	CLKB	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0#	OT	
	I	REQ0#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	REQ1#	I	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	1
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
1	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3#	F26	E26	GNT1#	OT	
	IOT	AD23	F27	E27	+3.3V	PWR	1
	PWR	GND	F28	E28	AD22	IOT	
	IOT	AD21	F29	E29	AD20	IOT	
	IOT	AD19	F30	E30	GND	PWR	
1	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	1
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
1	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	1
	IOT	PERR#	F40	E40	SDONE	IO	3
1	PWR	+3.3V	F41	E41	SB0#	IO	3
	IOC	SERR#	F42	E42	GND	PWR	
1	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	1
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
SOLDER SIDE					**COMPONENT SIDE**		
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	1
1	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	
	IOT	ACK64#	F60	E60	REQ64#	IOT	
	PWR	+5V	F61	E61	+5V	PWR	
	PWR	+5V	F62	E62	+5V	PWR	

Note 1: The 3.3V supply pins in the edge connector are unconnected.
Note 2: The signalling interface is +5V tolerant.
Note 3: Signals used for JTAG testing to perform Boundary Scan are not supported.
Note 4: The system does not support PCI cacheable memory
Note 5: Some of the signals in the PCI interface is pulled up to +5V. Devices connected to the PCI interface must be +5V tolerant.

5.17.3 Signal Description – PC104+ Connector / PCI Edge Connector

SYSTEM PINS.

CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33 MHz.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.

ADDRESS AND DATA.

AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).

PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.

INTERFACE CONTROL PINS.

FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

ARBITRATION PINS (BUS MASTERS ONLY).

REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted.

While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.

ERROR REPORTING PINS.

The error reporting pins are required by all devices and maybe asserted when enabled:

PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.

INTERRUPT PINS (OPTIONAL).
Interrupts on PCI are optional and defined as "level sensitive," asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.

INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

Since most devices are single function and, therefore, can only use INTA# on the device, the interrupts are distributed evenly among the interrupt controller’s input pins.

PC104+ Interrupt and REQ/GNT routing.

For the device in the PCI slot to function, the routing in the slots has to follow the specifications as outlined in the PC/ 104+ Specification Version 1.0 February 1997.

The table below specifies the distribution for the four modules that can be plugged on the PC104+ Connector. Note that AD20-23 are used for IDSEL for the individual boards.

Module Slot	REQ*	GNT*	CLK	IDSEL	ID Address	INT0*	INT1*	INT2*	INT3*
1	REQ0*	GNT0*	CLKA	IDSEL0	AD20	INTA*	INTD*	INTC*	INTB*
2	REQ1*	GNT1*	CLKB	IDSEL1	AD21	INTB*	INTA*	INTD*	INTC*
3	REQ2*[1]	GNT2*[1]	CLKC	IDSEL2	AD22	INTC*	INTB*	INTA*	INTD*
4	REQ2*[1]	GNT2*[1]	CLKD	IDSEL3	AD23	INTD*	INTC*	INTB*	INTA*

Note 1: Because module slots 3 and 4 share REQ2/GNT2, they cannot both be bus master devices.

PCI Edge Connector Interrupt and REQ/GNT routing.

For the device in the PCI slot to function, the routing in the passive backplane has to follow the specifications as outlined in the PCI-ISA Card Edge Connector proposal for Single Board Computer, Revision Number 2.0, October 10, 1994.
The table below specify the connection from Kontron's PCI Card Edge Connector to the PCI expansion connectors.

PCI Connector 1		PCI-ISA Connector	
Signal	Pin	Signal	Pin
REQ#	F18	REQ0#	F18
GNT#	E17	GNT0#	E17
INTA#	E06	INTB#	F07
INTB#	F07	INTC#	E07
INTC#	E07	INTD#	F08
INTD#	F08	INTA#	E06
IDSEL	E26	AD31	F20
PCI Connector 2		PCI-ISA Connector	
Signal	Pin	Signal	Pin
REQ#	F18	REQ1#	F10
GNT#	E17	GNT1#	E14
INTA#	E06	INTC#	E07
INTB#	F07	INTD#	F08
INTC#	E07	INTA#	E06
INTD#	F08	INTB#	F07
IDSEL	E26	AD30	E20
PCI Connector 3		PCI-ISA Connector	
Signal	Pin	Signal	Pin
REQ#	F18	REQ2#	E19
GNT#	E17	GNT2#	E26
INTA#	E06	INTD#	F08
INTB#	F07	INTA#	E06
INTC#	E07	INTB#	F07
INTD#	F08	INTC#	E07
IDSEL	E26	AD29	F21
PCI Connector 4		PCI-ISA Connector	
Signal	Pin	Signal	Pin
REQ#	F18	REQ3#	F09
GNT#	E17	GNT3#	F11
INTA#	E06	INTA#	E06
INTB#	F07	INTB#	F07
INTC#	E07	INTC#	E07
INTD#	F08	INTD#	F08
IDSEL	E26	AD28	E22

The 3-slotted PICMG backplane from Advantec PCA-6106P3 Rev.A1.01 supports this configuration.

5.18 Mating Connectors List

Below is a list of the internal mounted and the mating connectors for the 786LCD/S and /MG board.

Connector (Reference)	**Connector Vendor / Part-number**	**Mating Connector Vendor / Part-number**
PWR Connector (PWRCON)	Molex / 39-29-0103	Molex / 39-01-2100 10 x Molex / 39-00-0056
Keyboard / PS/2 Pinrows (JPKBD, JPMSE)	Molex / 22-29-2051	Molex 6471 / 22-01-2055 Molex 4809 / 08-55-0110
Flat Panel Connector (PANEL)	Molex / 70246- 5021	Leoco / 2540S 50UB1 Leoco / 2540S 50SRB1
Floppy (FLOPPY)	Molex / 70246- 3421	Leoco / 2540S 34UB1 Leoco / 2540S 34SRB1
IDE Harddisk (IDE1)	Molex / 70246- 4021	Leoco / 2540S 40UB1 Leoco / 2540S 40SRB1
IDE Harddisk (IDE2)	Molex / 87331-4420	AMP / 1-111623-0
Printer Port (PRINTER)	Molex / 70246- 2621	Leoco / 2540S 26UB1 Leoco / 2540S 26SRB1
Serial Port 2 Header (COM2)	Molex / 70246- 1021	Leoco / 2540S 10UB1 Leoco / 2540S 10SRB1
Serial Port 3/4 Header (COM3/4)	Molex / 70246- 2021	Leoco / 2540S 20UB1 Leoco / 2540S 20SRB1
USB Connector (USB)	Molex / 10- 96- 7085	Leoco / 2655S 8 0000 Leoco / 2653TPBU002
Fan Connector (FAN)	Molex / 22- 29- 2031	Leoco / 2530S030013 Leoco / 2533TCBU000
Feature Port (FEATURE)	Molex / 70246- 2021	Leoco / 2540S 20UB1 Leoco / 2540S 20SRB1
PC104 (PC104XT, PC104AT)	Samtec / ESW-132-12-G-D Samtec / ESW-120-12-G-D	Samtec / ESW-132-44-G-D* Samtec / ESW-120-44-G-D*
PC104+ PCI Connector	Samtec / ESQT-130-03-M-Q-368	*
Bracket spacer (BRACK1, BRACK2)	Molex / 87331-3020	Samtec / SQT-115-02-L-D*

* Exact Part-number will depend on the specific application.

Below is a list of the internal mounted and the mating connectors for the 786LCD/3.5" board.

Connector (Reference)	**Connector Vendor / Part-number**	**Mating Connector Vendor / Part-number**
PWR Connector (PWRCON)	Molex / 43045-1201	Molex / 43025-1200 12 x Molex / 43030-0002
Keyboard / PS/2 Pinrows (JPKBD, JPMSE)	Molex / 22-29-2051	Molex 6471 / 22-01-2055 Molex 4809 / 08-55-0110
Flat Panel Connector (PANEL)	Molex / 70246- 5021	Leoco / 2540S 50UB1 Leoco / 2540S 50SRB1
Floppy (FLOPPY)	Molex / 87331-3420	Leoco / 2066S-34-0000 34 x Leoco / 2065TPB0000
IDE Harddisk (IDE1)	Molex / 70246- 4021	Leoco / 2540S 40UB1 Leoco / 2540S 40SRB1
IDE Harddisk (IDE2)	Molex / 87331-4420	AMP / 1-111623-0
Printer Port (PRINTER)	Molex / 87331-2620	Molex / 51110-2651 26 x Molex / 50394-8052
Serial Port 2 Header (COM2)	Molex / 87331-1020	Molex / 51110-1060 10 x Molex / 50394-8052
Fan Connector (FAN)	Molex / 22- 29- 2031	Leoco / 2530S030013 Leoco / 2533TCBU000
Feature Port (FEATURE)	Molex / 87331-2020	Molex / 51110-2051 20 x Molex / 50394-8052
PC104+ PCI Connector	Samtec / ESQT-130-03-M-Q-368	*
Bracket spacer (BRACK1, BRACK2)	Molex / 87331-3020	Samtec / SQT-115-02-L-D*

* Exact Part-number will depend on the specific application.

6. Warranty

Kontron Technology warrants its products to be free from defects in material and workmanship during the warranty period. If a product proves to be defective in material or workmanship during the warranty period, Kontron Technology will, at its sole option, repair or replace the product with a similar product.
Replacement Product or parts may include remanufactured or refurbished parts or components.

The warranty does not cover:

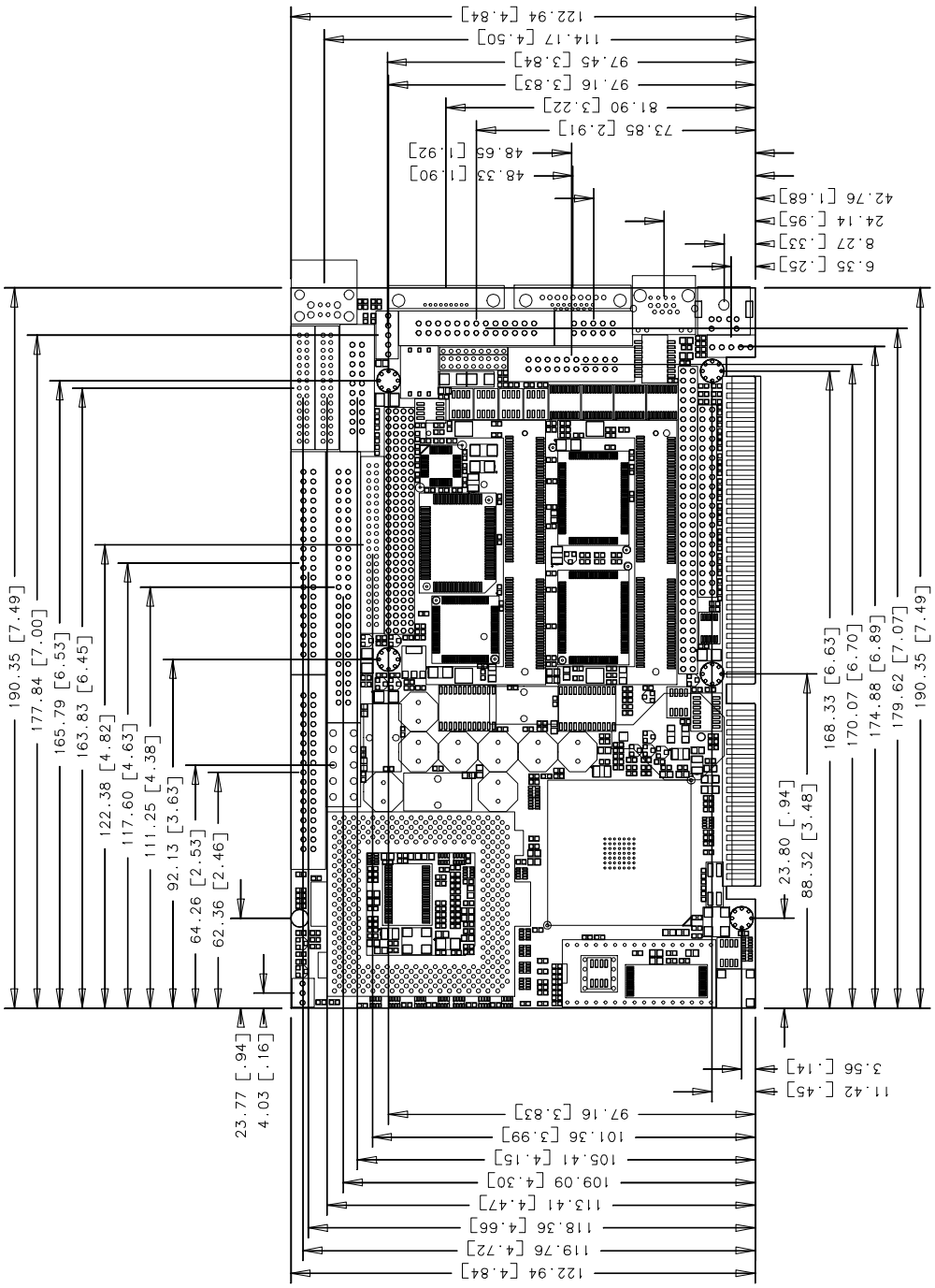
1. Damage, deterioration or malfunction resulting from:
   A. Accident, misuse, neglect, fire, water, lightning, or other acts of nature, unauthorised product modification, or failure to follow instructions supplied with the product.
   B. Repair or attempted repair by anyone not authorised by Kontron Technology.
   C. Causes external to the product, such as electric power fluctuations or failure.
   D. Normal wear and tear.
   E. Any other causes which does not relate to a product defect.
2. Removal, installation, and set-up service charges.

Exclusion of damages:

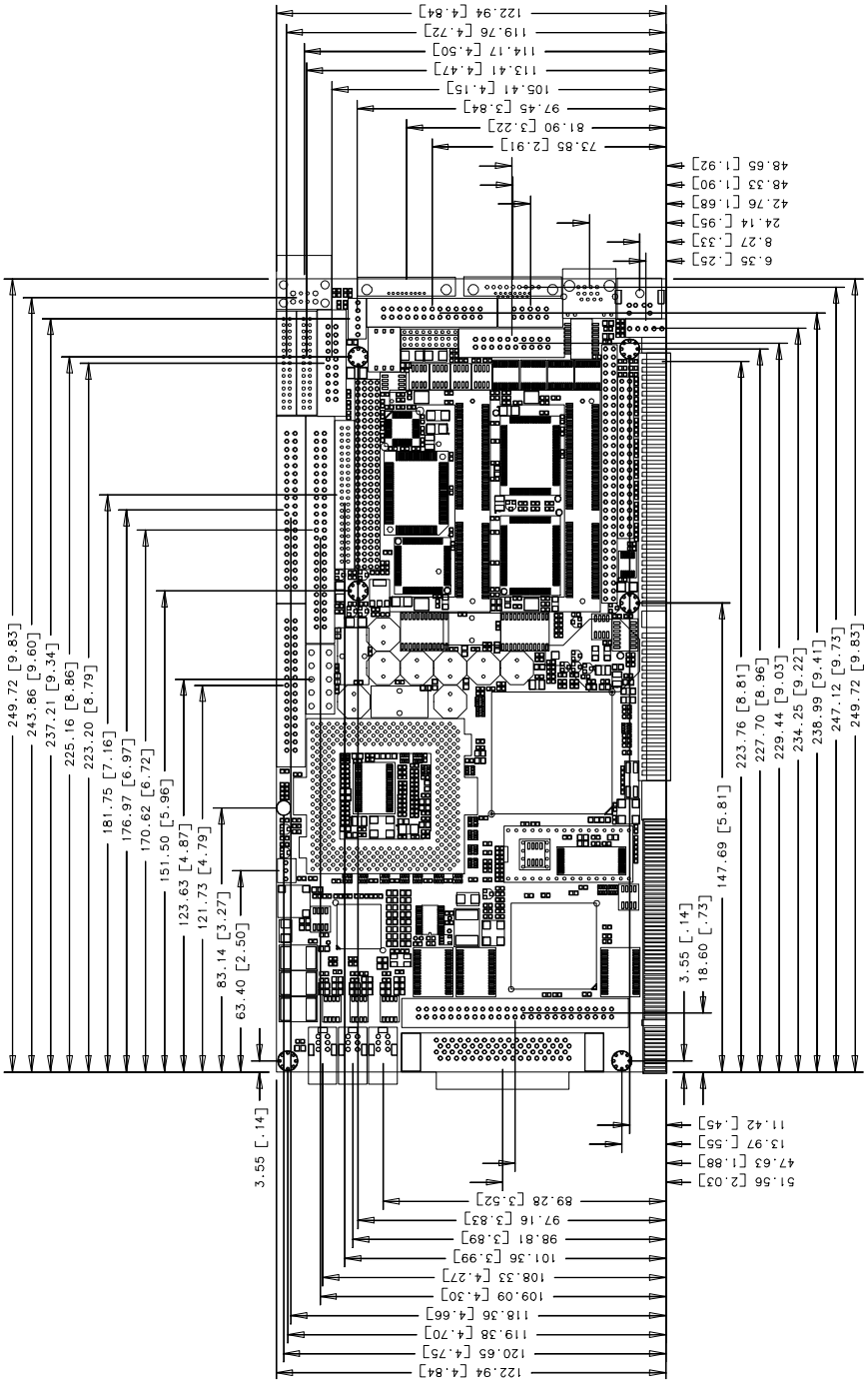
KONTRON TECHNOLOGY LIABILITY IS LIMITED TO THE COST OF REPAIR OR REPLACEMENT OF THE PRODUCT. KONTRON TECHNOLOGY SHALL NOT BE LIABLE FOR:
1. DAMAGE TO OTHER PROPERTY CAUSED BY ANY DEFECTS IN THE PRODUCT, DAMAGES BASED UPON INCONVENIENCE, LOSS OF USE OF THE PRODUCT, LOSS OF TIME, LOSS OF PROFITS, LOSS OF BUSINESS OPPORTUNITY, LOSS OF GOODWILL, INTERFERENCE WITH BUSINESS RELATIONSHIPS, OR OTHER COMMERCIAL LOSS, EVEN IF ADVISED OF THEIR POSSIBILITY OF SUCH DAMAGES.
2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.
3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.

7. Measurement Drawings

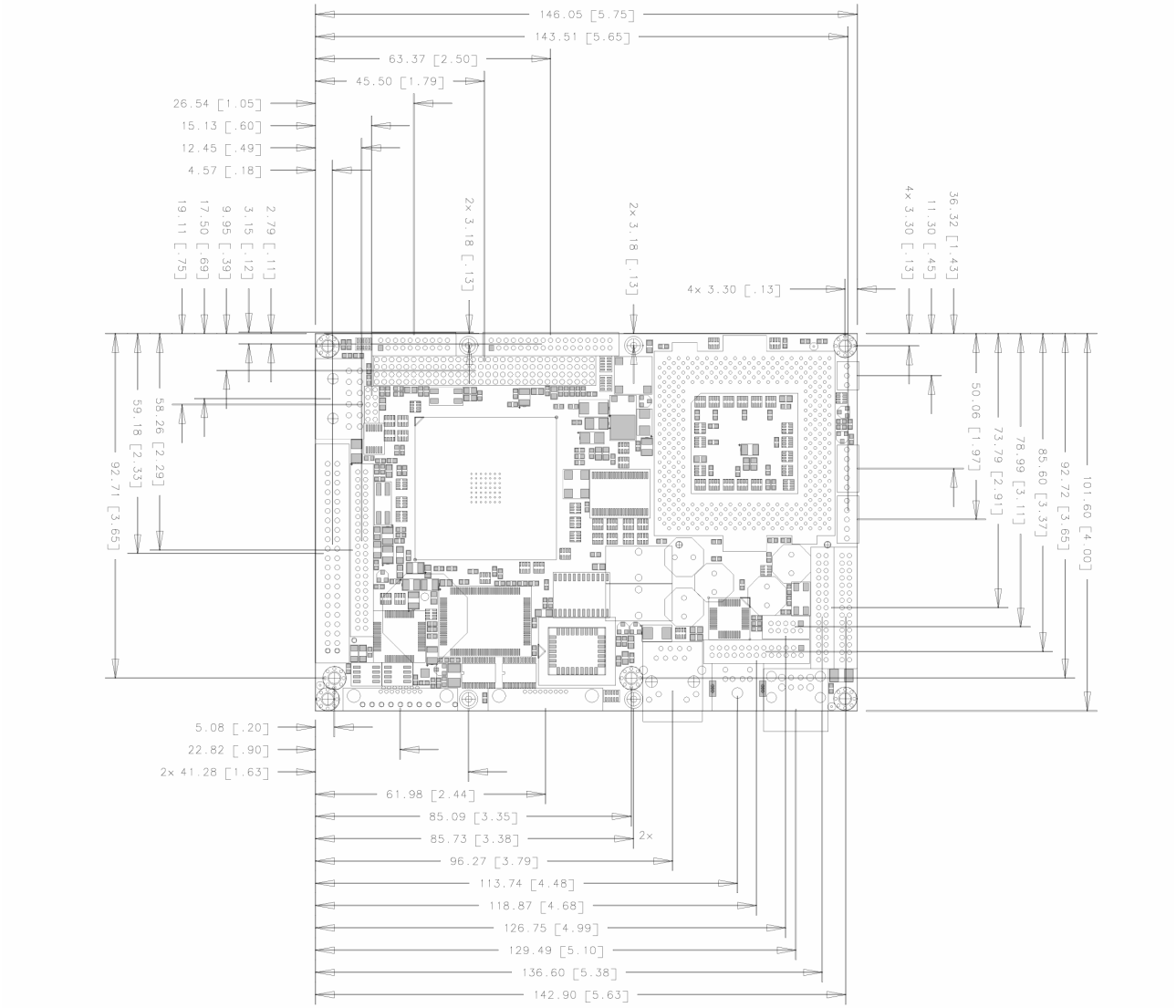
7.1 786LCD/s



7.2 786LCD/MG


122.94 [4.84]
119.76 [4.72]
114.17 [4.50]
113.41 [4.47]
105.41 [4.15]
97.45 [3.84]
81.90 [3.22]
73.85 [2.91]
48.65 [1.92]
48.33 [1.90]
42.76 [1.68]
24.14 [.95]
8.27 [.33]
6.35 [.25]
249.72 [9.83]
243.86 [9.60]
237.21 [9.34]
225.16 [8.86]
223.20 [8.79]
181.75 [7.16]
176.97 [6.97]
170.62 [6.72]
151.50 [5.96]
123.63 [4.87]
121.73 [4.79]
83.14 [3.27]
63.40 [2.50]
3.55 [.14]
223.76 [8.81]
227.70 [8.96]
229.44 [9.03]
234.25 [9.22]
238.99 [9.41]
247.12 [9.73]
249.72 [9.83]
147.69 [5.81]
18.60 [.73]
3.55 [.14]
11.42 [.45]
13.97 [.55]
47.63 [1.88]
51.56 [2.03]
89.28 [3.52]
97.16 [3.83]
98.81 [3.89]
101.36 [3.99]
108.33 [4.27]
109.09 [4.30]
118.36 [4.66]
119.38 [4.70]
120.65 [4.75]
122.94 [4.84]

7.3 786LCD/3.5”


146.05 [5.75]
143.51 [5.65]
63.37 [2.50]
45.50 [1.79]
26.54 [1.05]
15.13 [.60]
12.45 [.49]
4.57 [.18]
19.11 [.75]
17.50 [.69]
9.95 [.39]
3.15 [.12]
2.79 [.11]
2× 3.18 [.13]
2× 3.18 [.13]
4× 3.30 [.13]
4× 3.30 [.13]
11.30 [.45]
36.32 [1.43]
92.71 [3.65]
59.18 [2.33]
58.26 [2.29]
50.06 [1.97]
73.79 [2.91]
78.99 [3.11]
85.60 [3.37]
92.72 [3.65]
101.60 [4.00]
5.08 [.20]
22.82 [.90]
2× 41.28 [1.63]
61.98 [2.44]
85.09 [3.35]
85.73 [3.38]
2×
96.27 [3.79]
113.74 [4.48]
118.87 [4.68]
126.75 [4.99]
129.49 [5.10]
136.60 [5.38]
142.90 [5.63]

References

[1] IEEE Personal Computer BUS Standard P996. Draft D2.02 13. July 1990. This standard is an attempt to standardise the ISA bus introduced by IBM. The draft has not been approved, but is however the *official* ISA bus specification.

[2] PC/104-*Plus* Specification version 1.0 February 1997

[3] IEEE std. 1284-1996: Standard signalling method for a Bidirectional Parallel Peripheral Interface for Personal Computers. December 2. 1994.

[4] ATA-4 specification.

[5] PCI Local Bus Specification. Revision 2.1 June 1. 1995. PCI Special interests group.
[6] IEEE std. 802.3, 1998 Edition.

Additional details about specific functions or components of the board refer to the components datasheet or contact Kontron Technology support line.