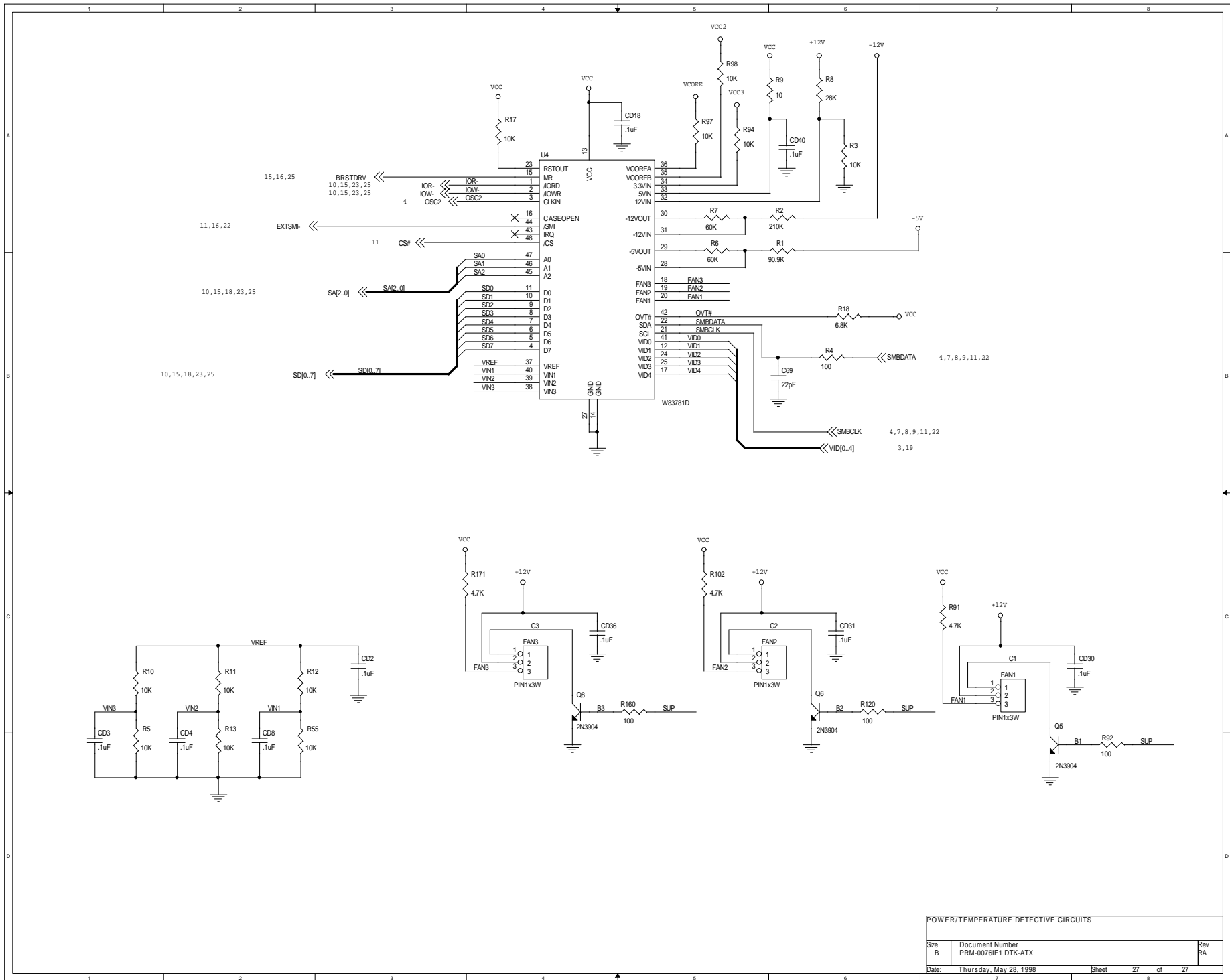


SINGLE CPU 440LX(3 DIMMS) CUSTOMER REFERENCE DESIGN

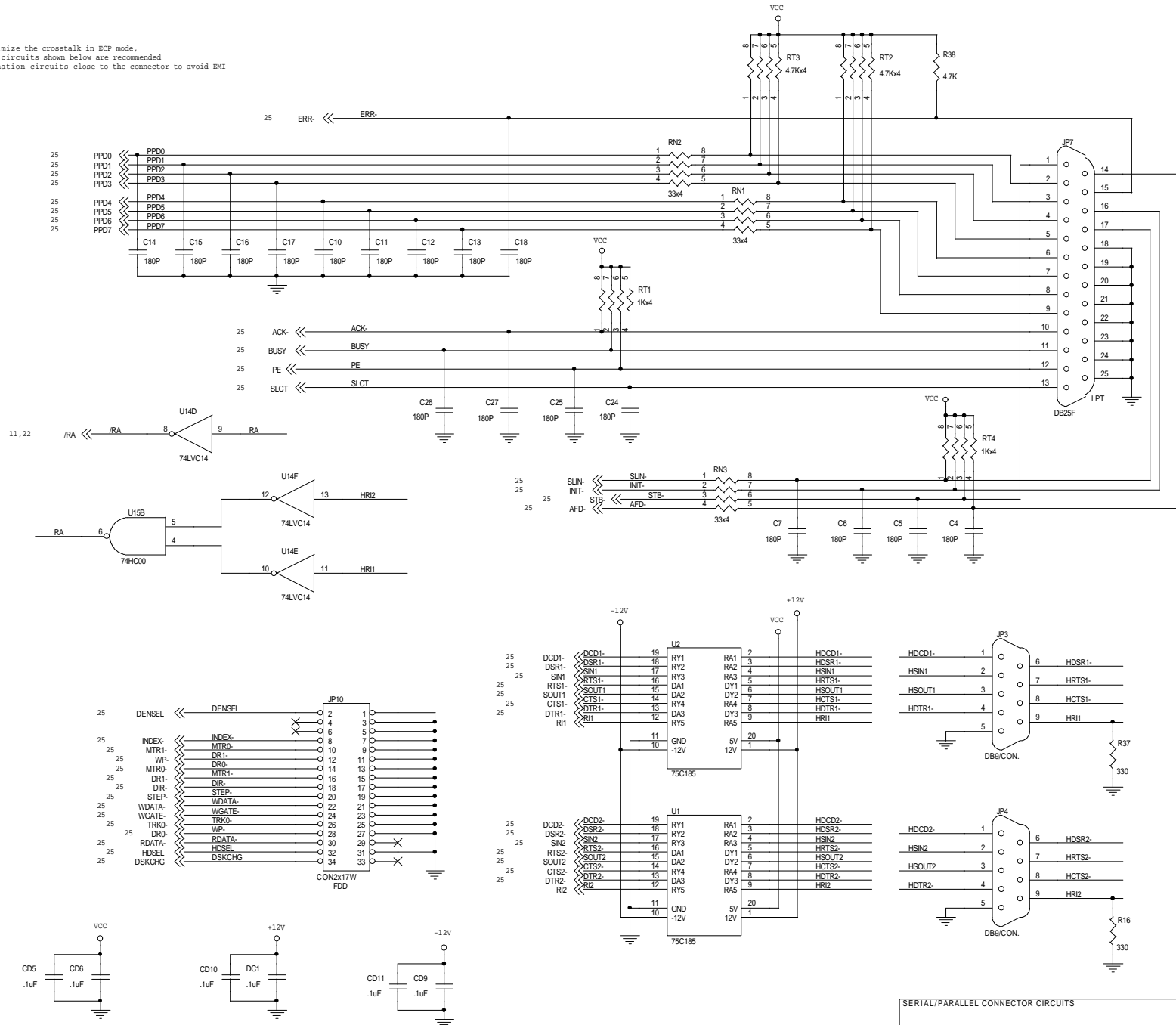
TITLE	PAGE	COMPONENT	PLACEMENT	PAGE
COVER SHEET	1	CPU SLOT1	JP9	2 , 3
KLAMATH	2 - 3	Clock Generator	U8	4
CLK SYNTHESIZER	4	74HC74	U7	16
PAC(82443LX)	5, 6	82443LX	U7	5, 6
DIMM1, 2, 3	7, 8, 9	PIIX4	U11	10, 11
PIIX4	10, 11	74LVC14	U14	16
AGP CONN.	12	74HCT14	U12	16, 20
PCI CONN.	13, 14	7407	U16	16
ISA CONN.	15	74HC00	U15	16, 26
PALEL	16	74F08	U10	17
IDE CONN.	17	FLASH BIOS	U6	18
USB / FLASH BIOS	18	SC1182CS	U5	19
DC TO DC COVERTER	19	74ALS244	U9	20
KEYB / MOUSE	20	W83977TF	U3	25
CPU FREQUENCE RATE	20	75C185	U1 , U2	26
CHIP GTL TERM.	21	W83781D	U4	27
PCI/AGP PULLUPS	22			
ISA/PAC DECOUP	23			
VREF PAGE	24			
WINBOND I/O CHIP	25			
SERIAL/FLOPPY	26			
TEMPERATE SENOR	27			

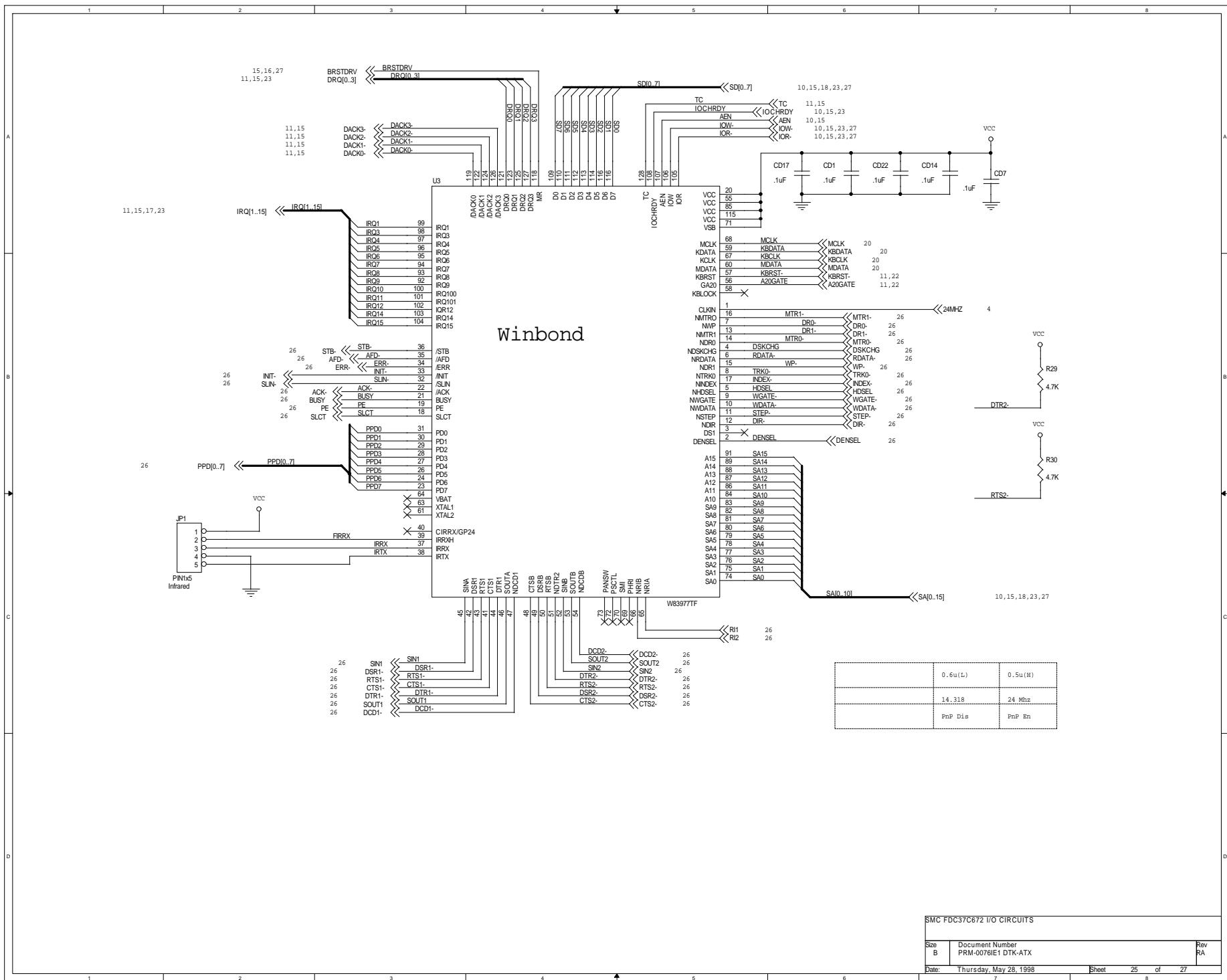
LINK
 2.SCH
 3.SCH
 4.SCH
 5.SCH
 6.SCH
 7.SCH
 8.SCH
 9.SCH
 10.SCH
 11.SCH
 12.SCH
 13.SCH
 14.SCH
 15.SCH
 16.SCH
 17.SCH
 18.SCH
 19.SCH
 20.SCH
 21.SCH
 22.SCH
 23.SCH
 24.SCH
 25.SCH
 26.SCH
 27.SCH

COMPONENTS PAGE EXAMPLATION		
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Date: Thursday, May 28, 1998	Sheet 1	of 27



In order to minimize the crosstalk in ECP mode,
the termination circuits shown below are recommended
Place all termination circuits close to the connector to avoid EMI

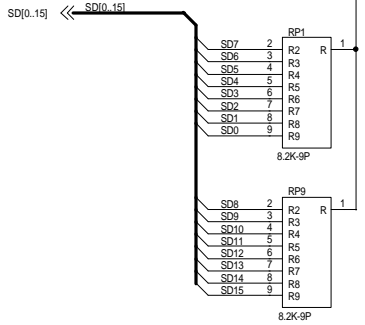




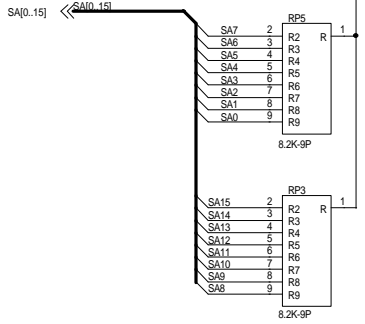
	0.6u(L)	0.5u(H)
	14.318	24 Mhz
	PnP Dis	PnP Sn

ISA BUS RESISTORS

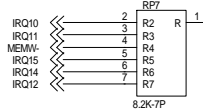
10, 15, 18, 25, 27



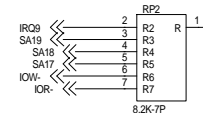
10, 15, 18, 25, 27



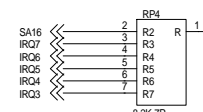
11, 15, 25
11, 15, 25
10, 15, 18
11, 15, 17, 25
11, 15, 27



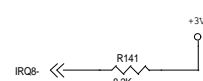
11, 15, 25
10, 15
10, 15
10, 15, 18
10, 15, 25, 27
10, 15, 25, 27



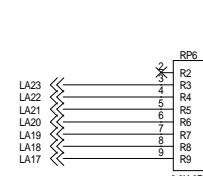
10, 15, 18
11, 15, 25
11, 15, 25
11, 15, 25
11, 15, 25
11, 15, 25



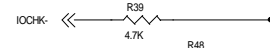
11



10, 15
10, 15
10, 15
10, 15
10, 15
10, 15
10, 15



10, 15



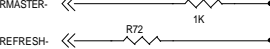
10, 15



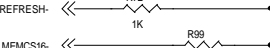
10, 15, 25



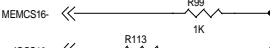
15



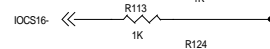
10, 15



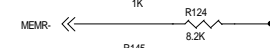
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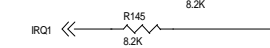
10, 15



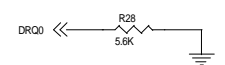
10, 15, 18



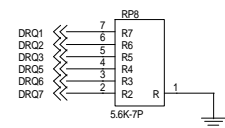
11, 25



11, 15, 25



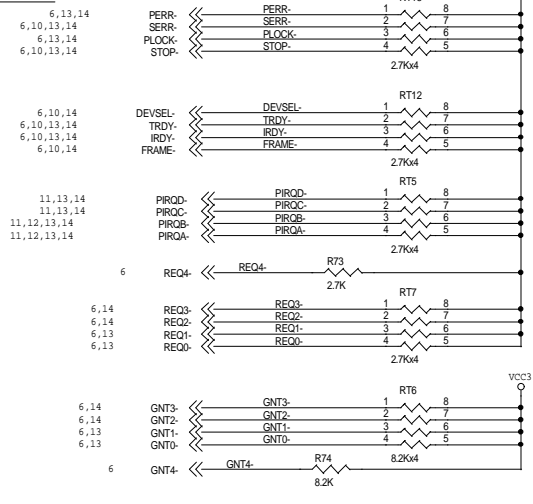
11, 15, 25
11, 15, 25
11, 15, 25
11, 15
11, 15
11, 15



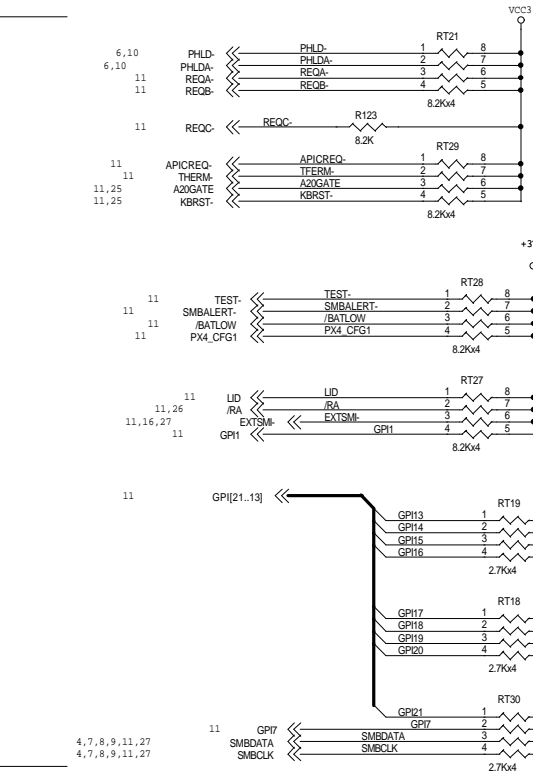
PULL UPS & PULL DOWNS

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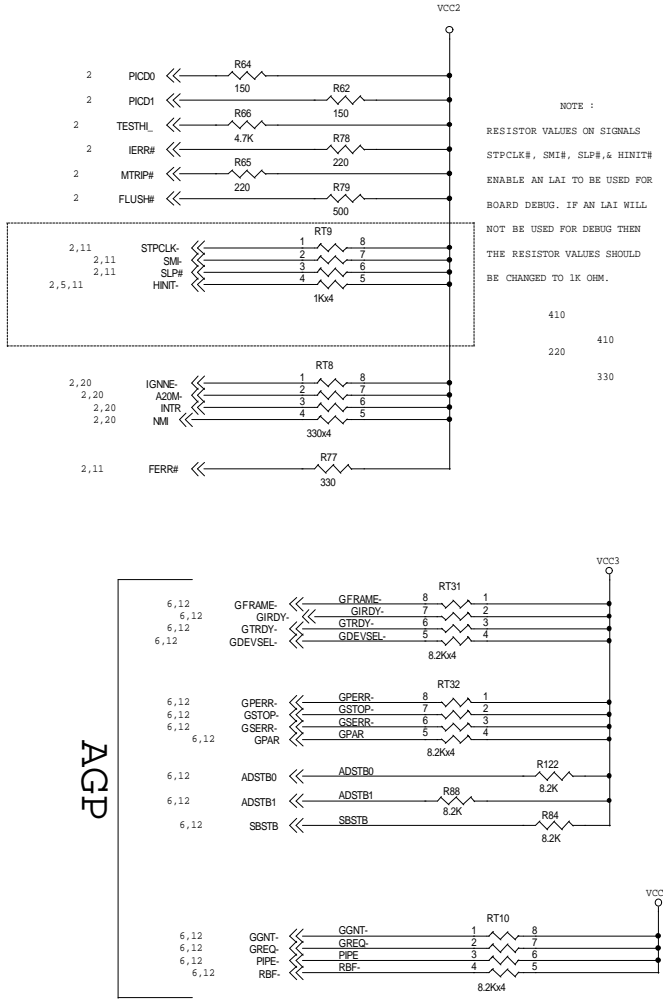
PCI BUS



PIIX4



AGP



NOTE :
RESISTOR VALUES ON SIGNALS
STPCLK#, SMI#, SLP#,& HINT#
ENABLE AN LAI TO BE USED FOR
BOARD DEBUG. IF AN LAI WILL
NOT BE USED FOR DEBUG THEN
THE RESISTOR VALUES SHOULD
BE CHANGED TO 1K OHM.

BUS RESISTORS

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3, 5, 21 /HA[3..31] << /HA[3..31]

2, 6 /HD[0..63] << /HD[0..63]

3, 5 HLOCK <<

3, 5 BREQ0 <<

3, 5 HRESET# <<

2 PRDY#0 <<

3, 5 /DEFER- <<
3, 5 /HREQ0 <<
3, 5 BPR- <<
3, 5 /HREQ4 <<

3, 5 HTM- <<
3, 5 HJT <<
3, 5 DBSY- <<
3, 5 RS1# <<

3, 5 HTRDY- <<
3, 5 BWP- <<
3, 5 /HREQ0 <<
3, 5 ADS- <<

3, 5 DRDY- <<
3, 5 /HREQ2 <<
3, 5 RSO# <<
3, 5 /HREQ3 <<

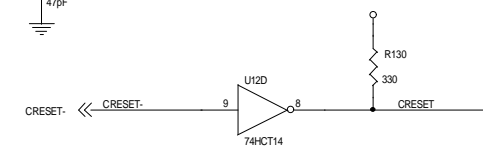
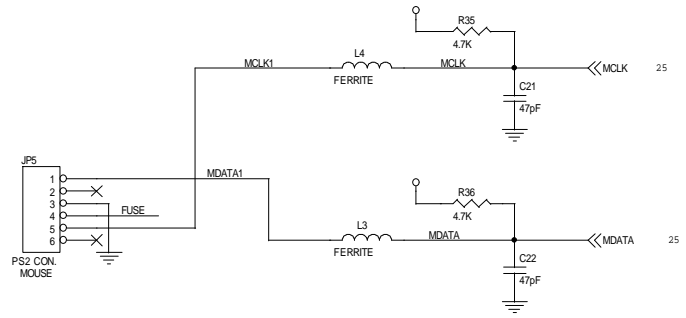
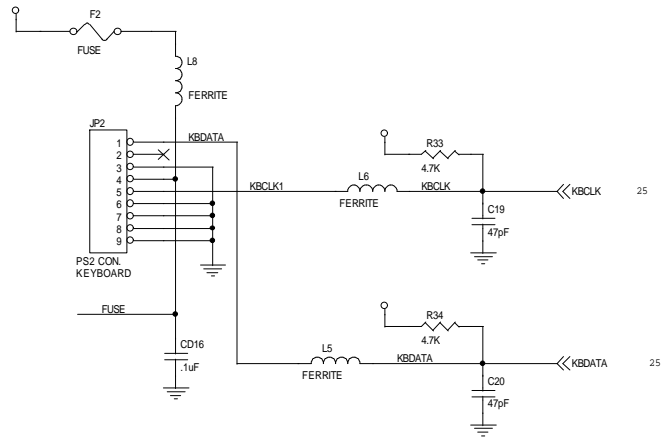
3, 5 RS2# <<

NOTE : VTT = TERMINATION VOLTAGE

STL TERMINATION FOR 440LX

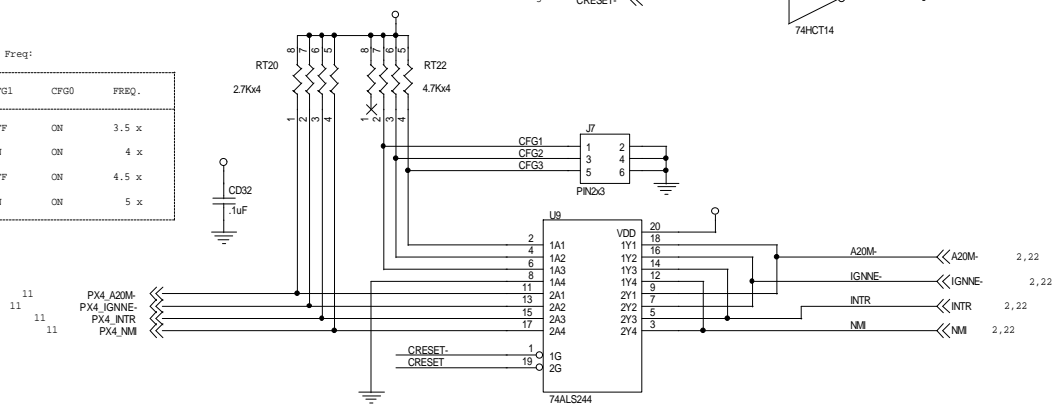
Size B	Document Number PRM-00761E1 DTK-ATX	Rev RA
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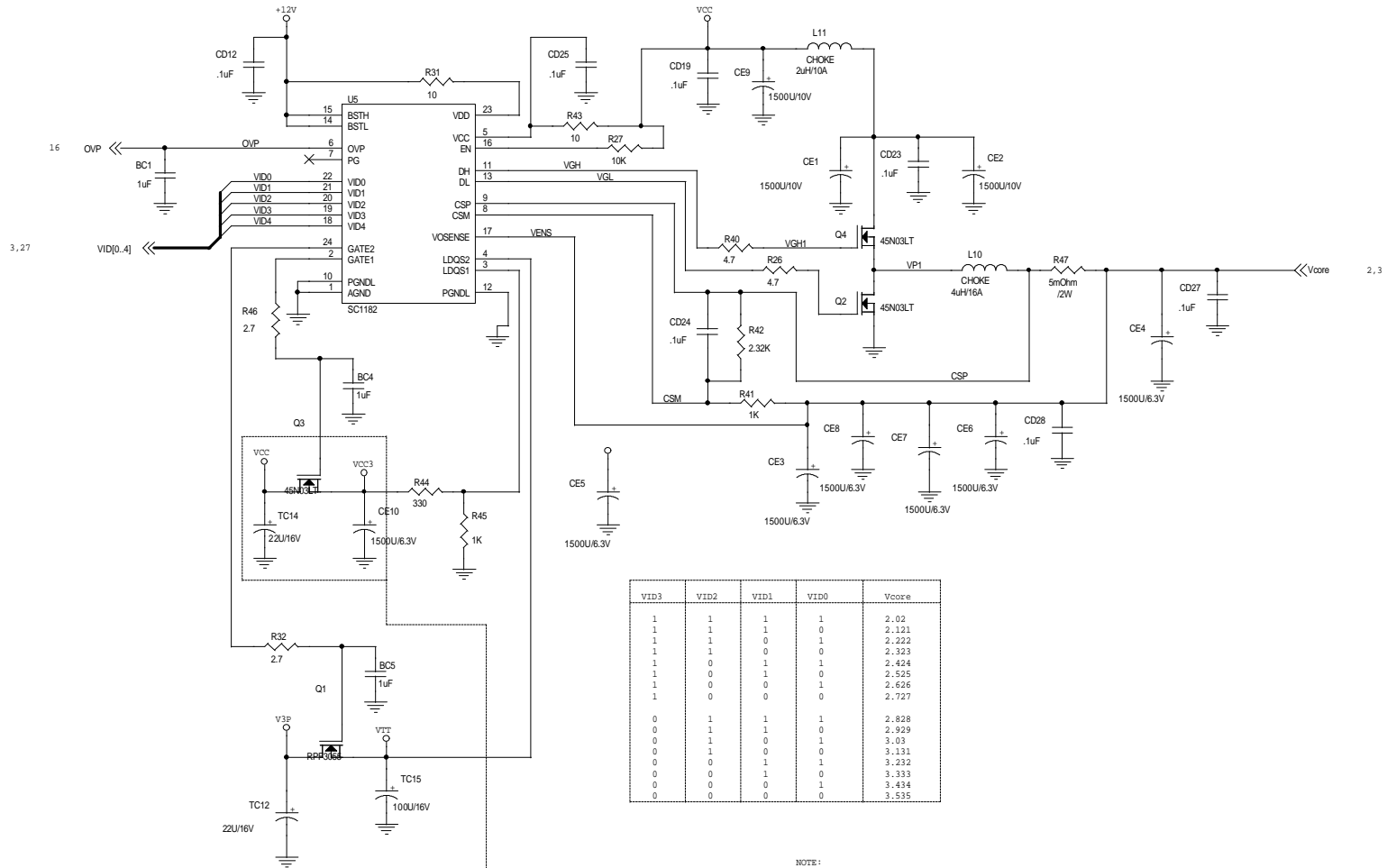
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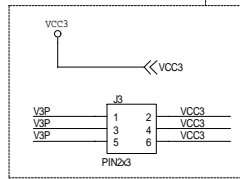
Processor Core Freq:

CFG3	CFG2	CFG1	CFG0	FREQ.
ON	OFF	OFF	ON	3.5 x
OFF	ON	ON	ON	4 x
OFF	ON	OFF	ON	4.5 x
OFF	OFF	ON	ON	5 x

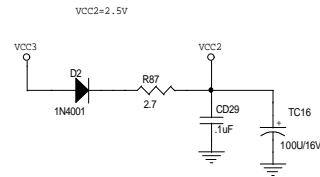




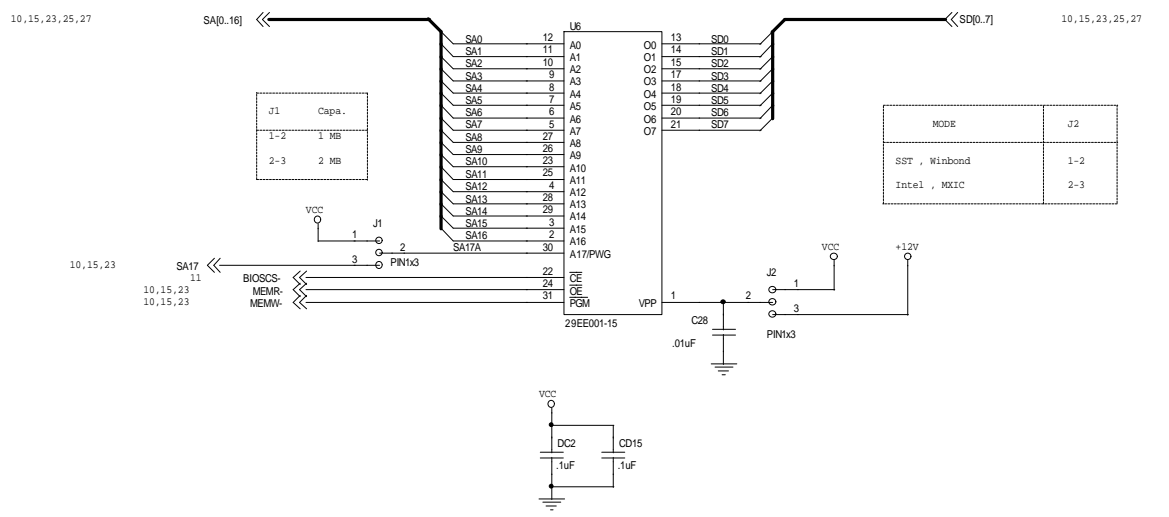
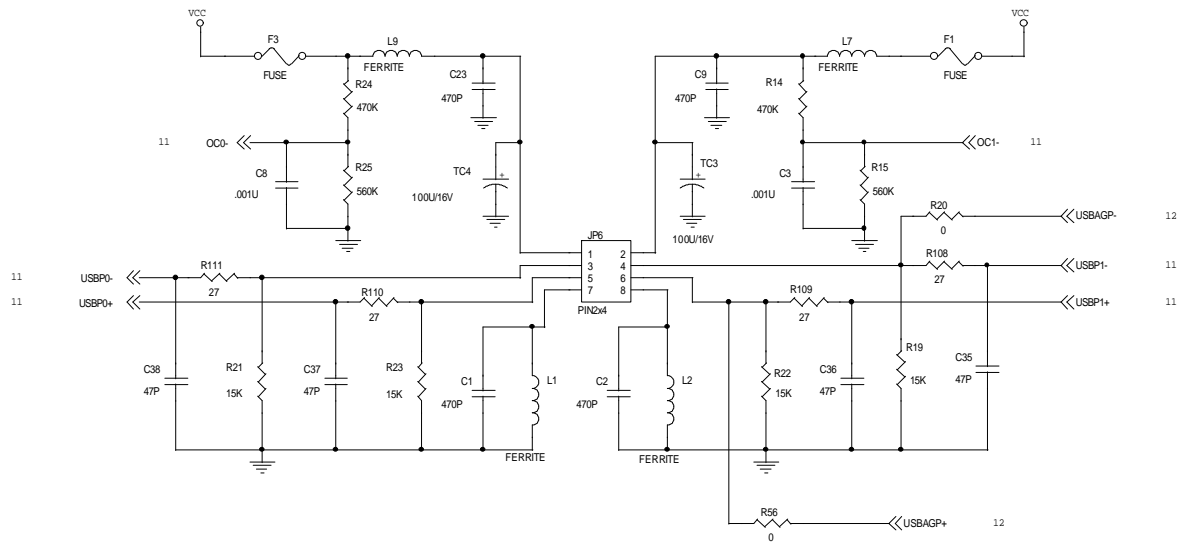
DASH BOX can change to each other

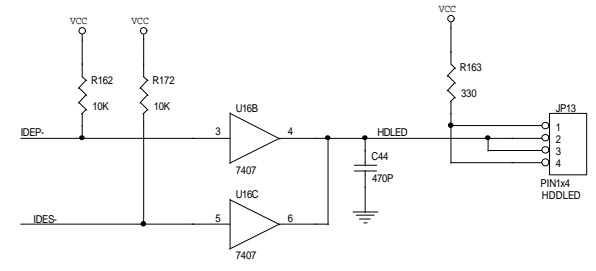
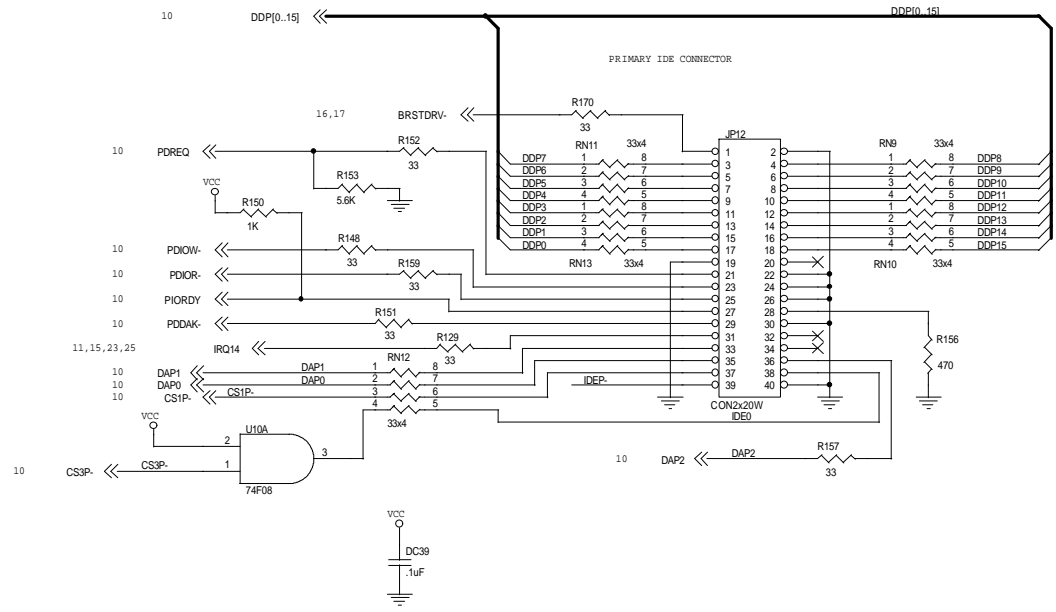


NOTE:
VOLTAGE REGULATOR SHOULD
BE LOCATED NEAR THE FAC

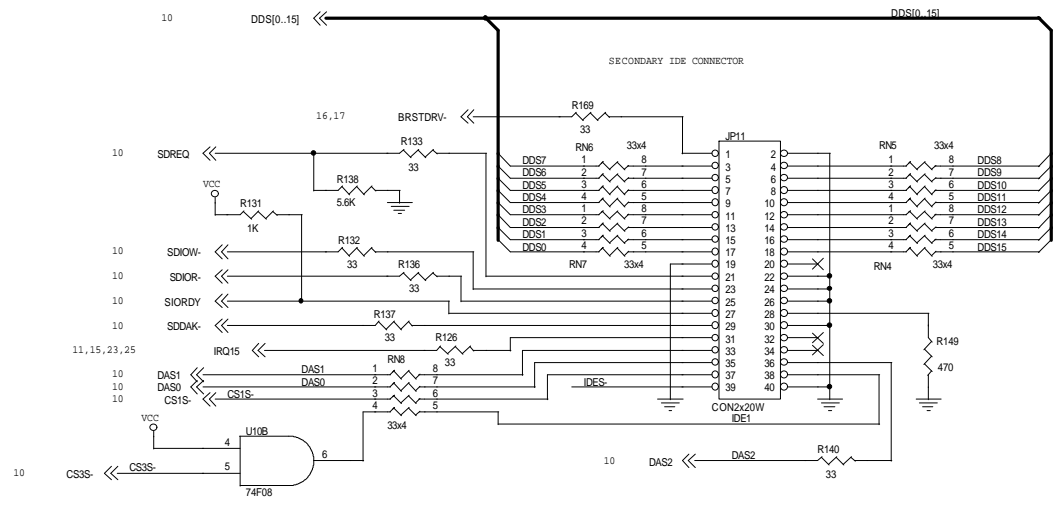


DC to DC CONVERTER CIRCUITS

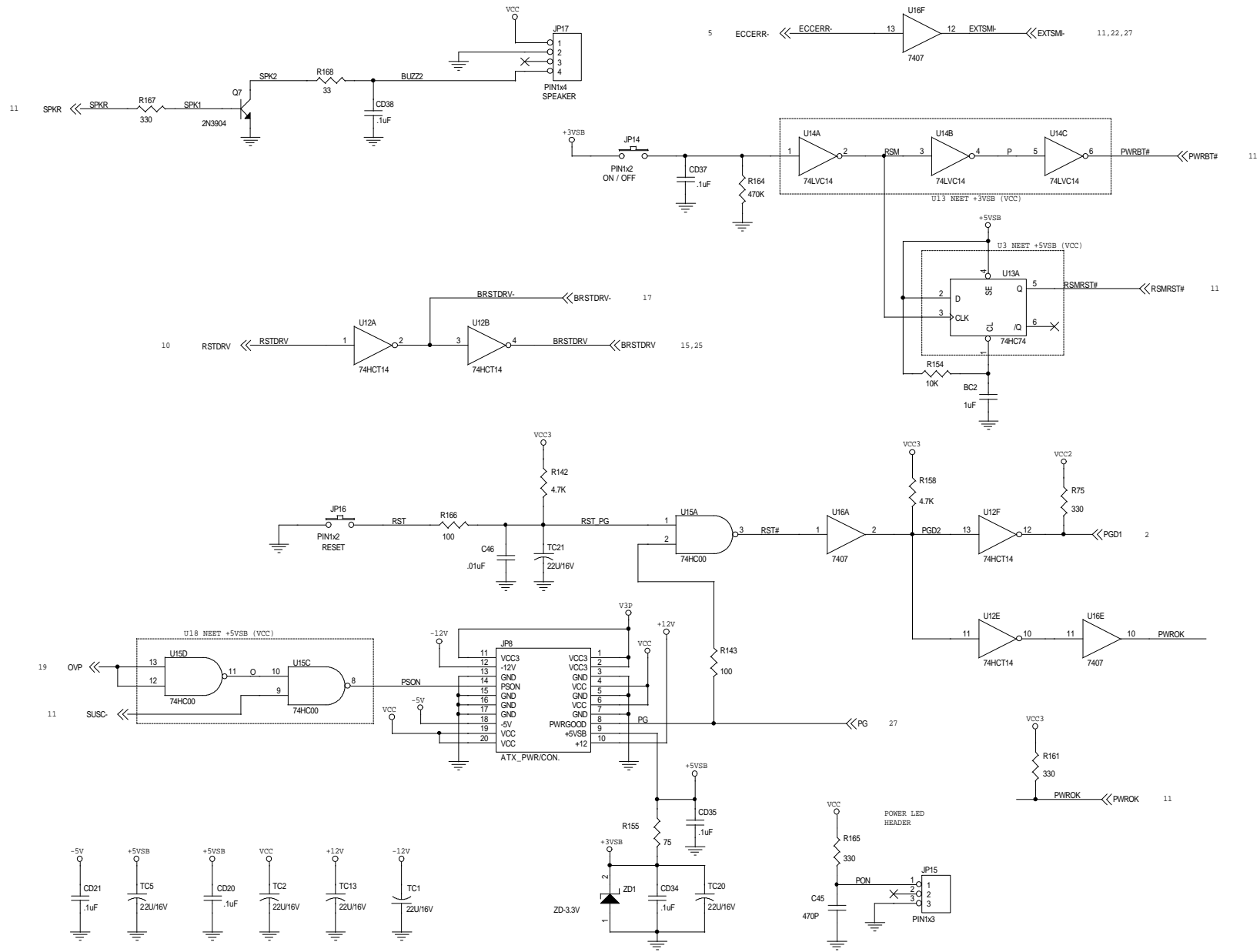




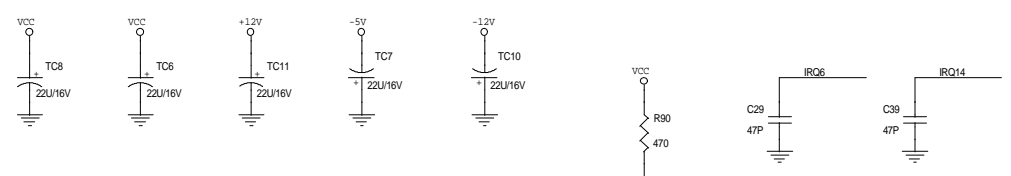
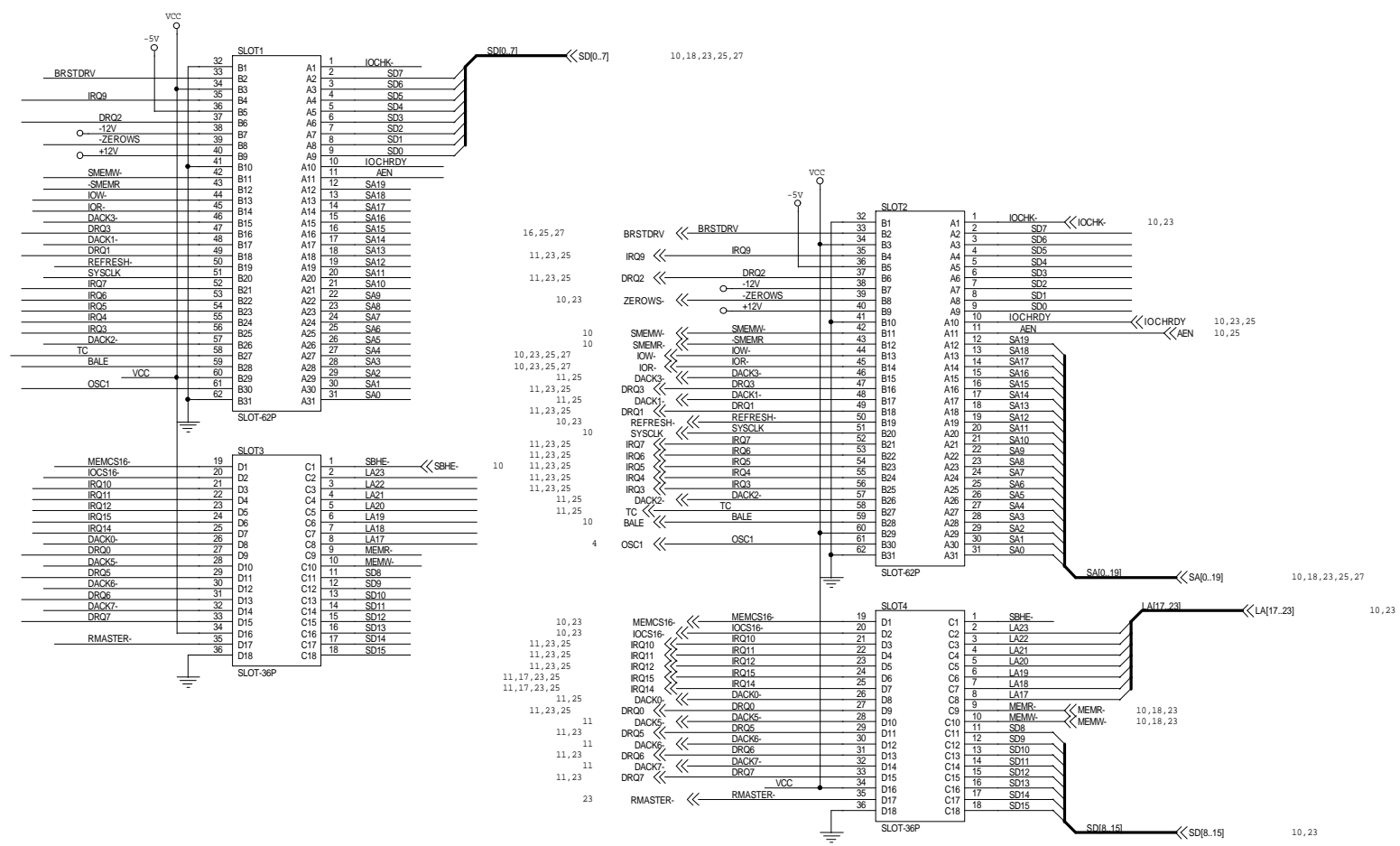
IDE CONNECTORS



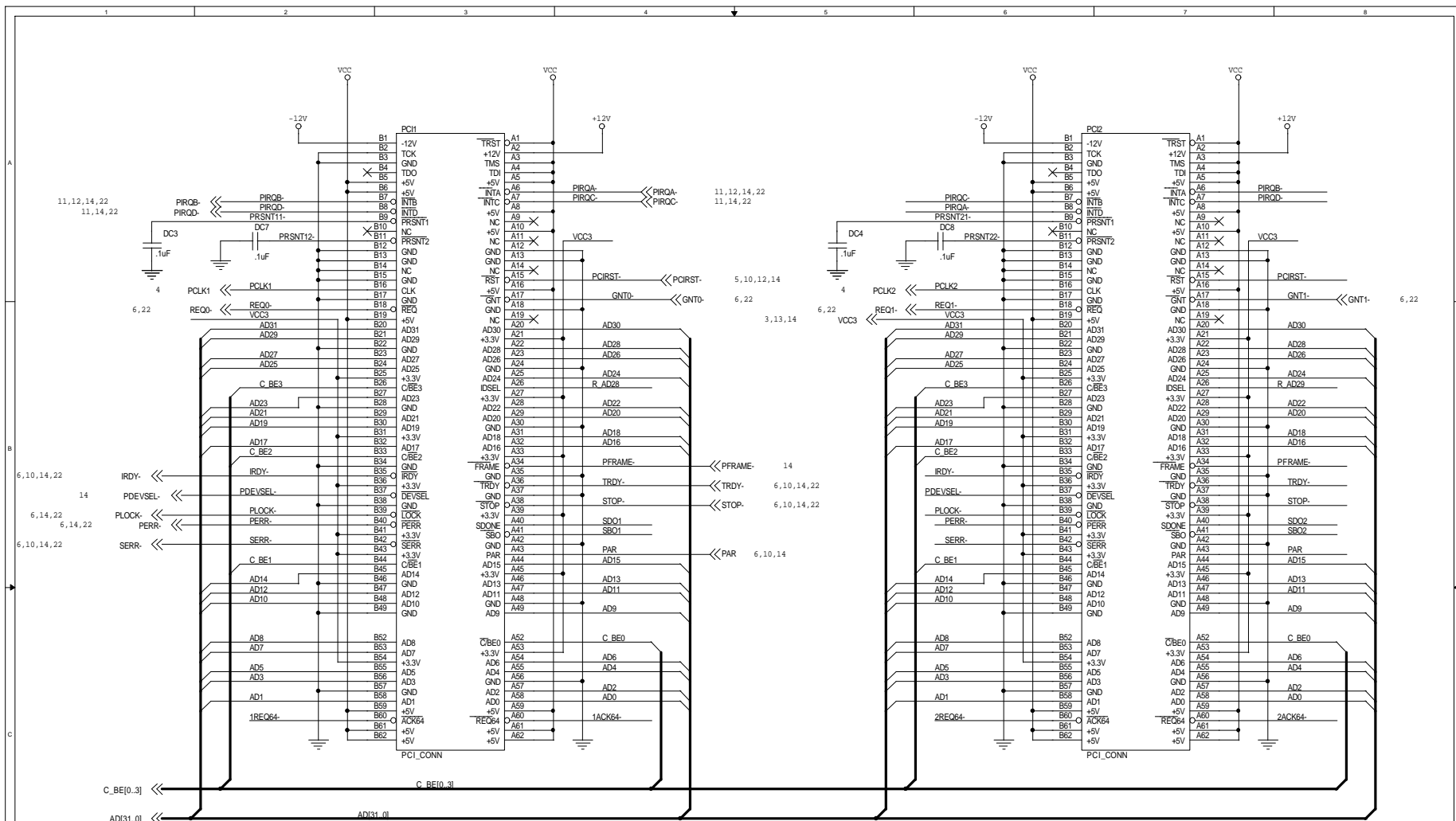
PCI IDE CONNECTORS		
Size B	Document Number PRM-0076IE1 DTK-ATX	Rev RA
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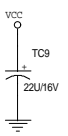
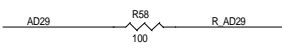
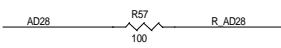
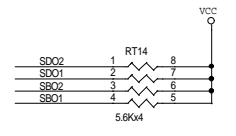
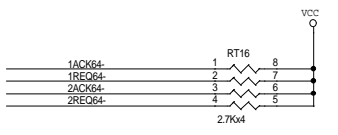
FRONT PANEL		
Size B	Document Number PRM-00761E1 DTK-ATX	Rev RA
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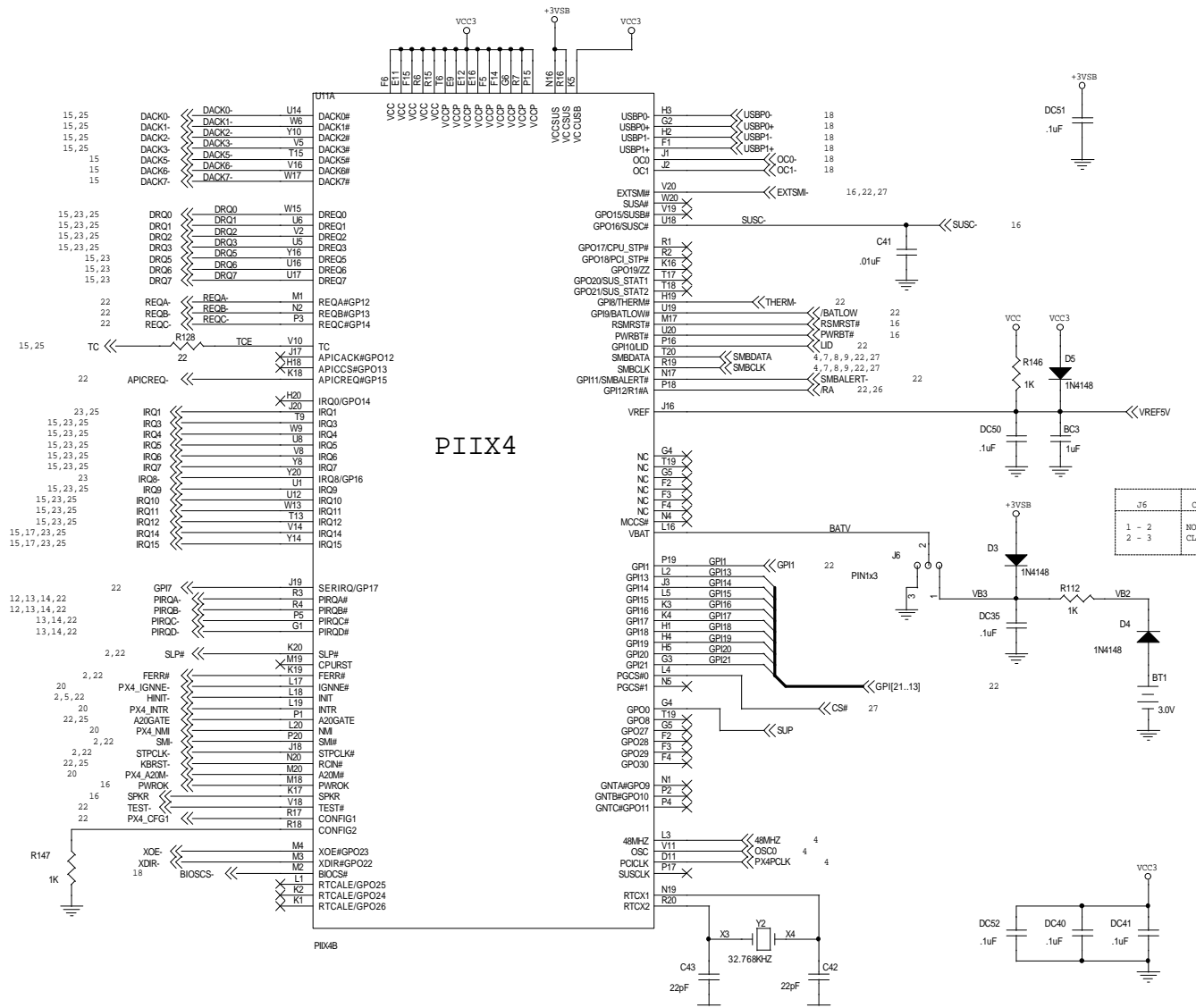
AT-BUS SLOTS		
Size B	Document Number PRM-0076IE1 DTK-ATX	Rev RA
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C_BE[0..3] <<< AD[31..0]

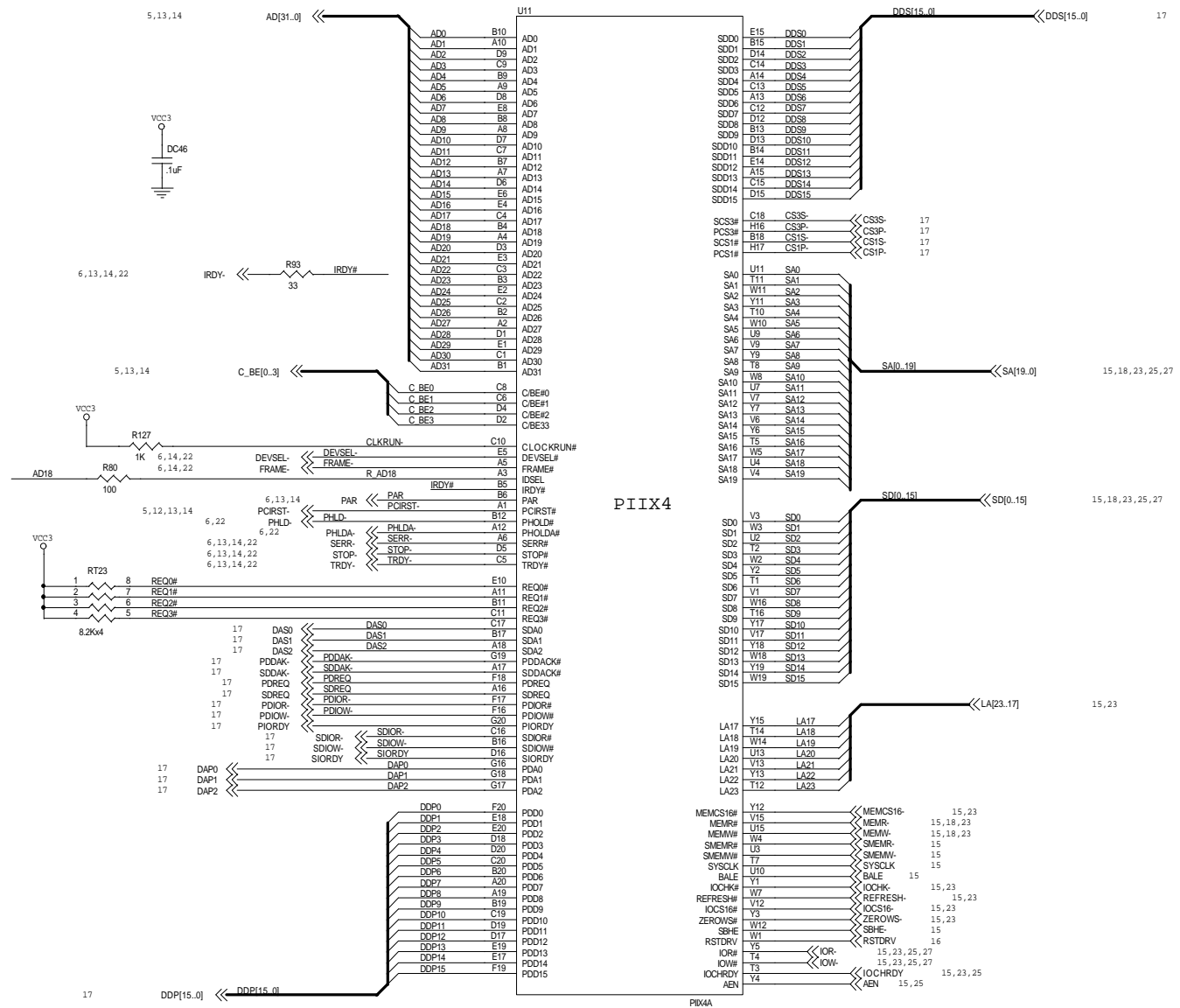


PCI SLOTS (1 & 2)



PIIX4

J6	CMOS
1 - 2	NORMAL
2 - 3	CLEAR

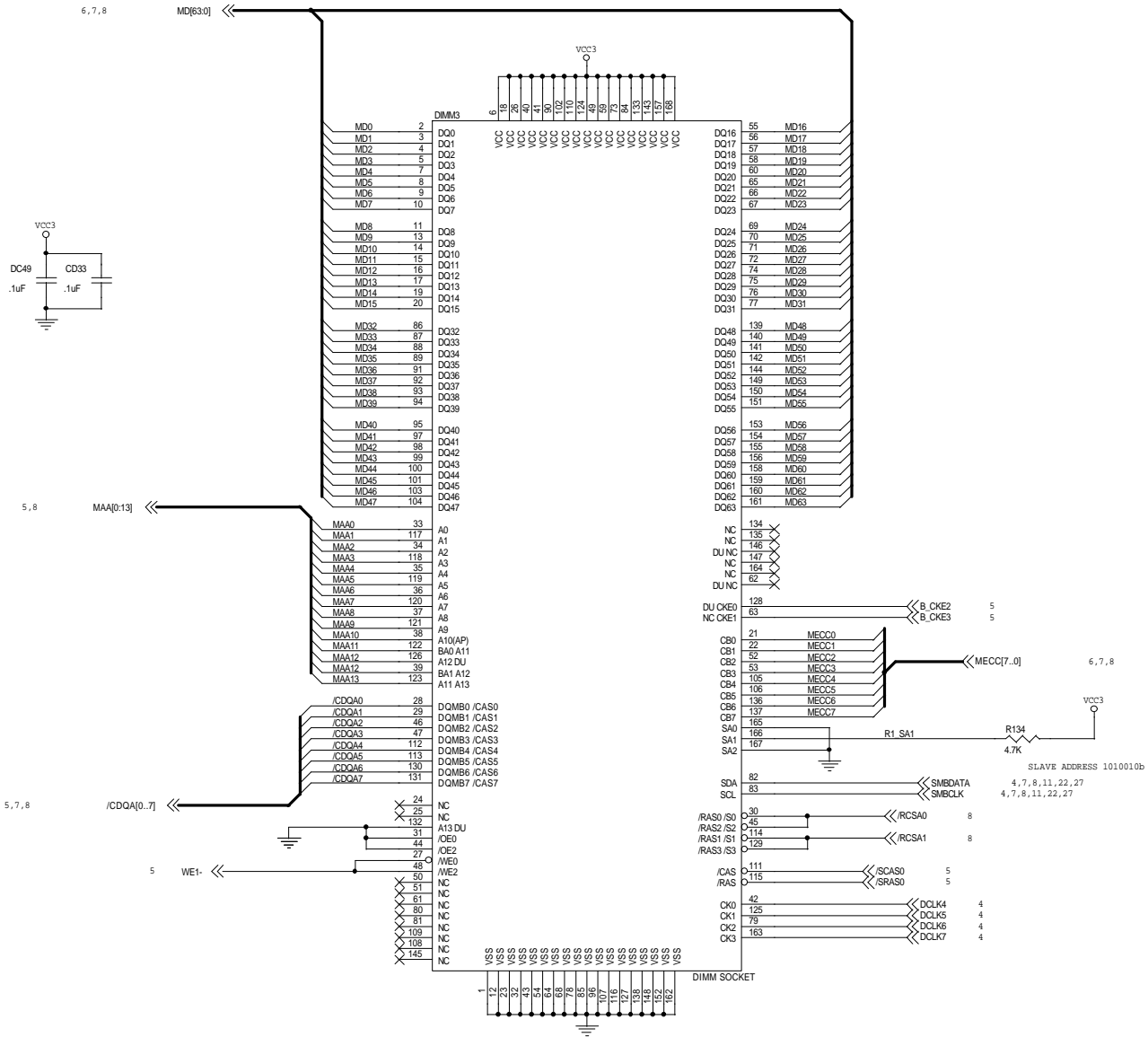


PIX4

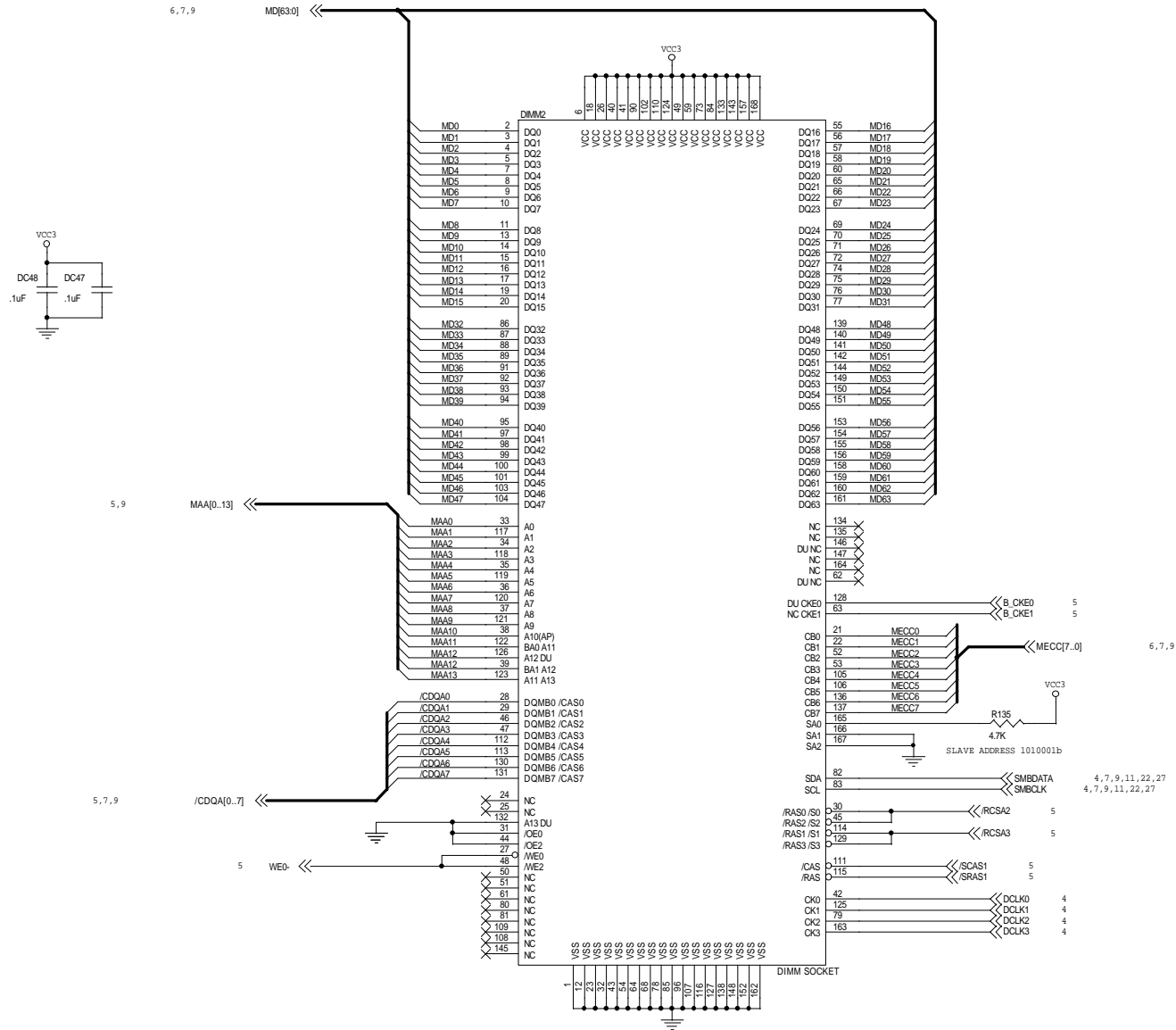
PIX4A

PIX4_A		
Size	Document Number	Rev
B	PRM-00761E1 DTK-ATK	RA
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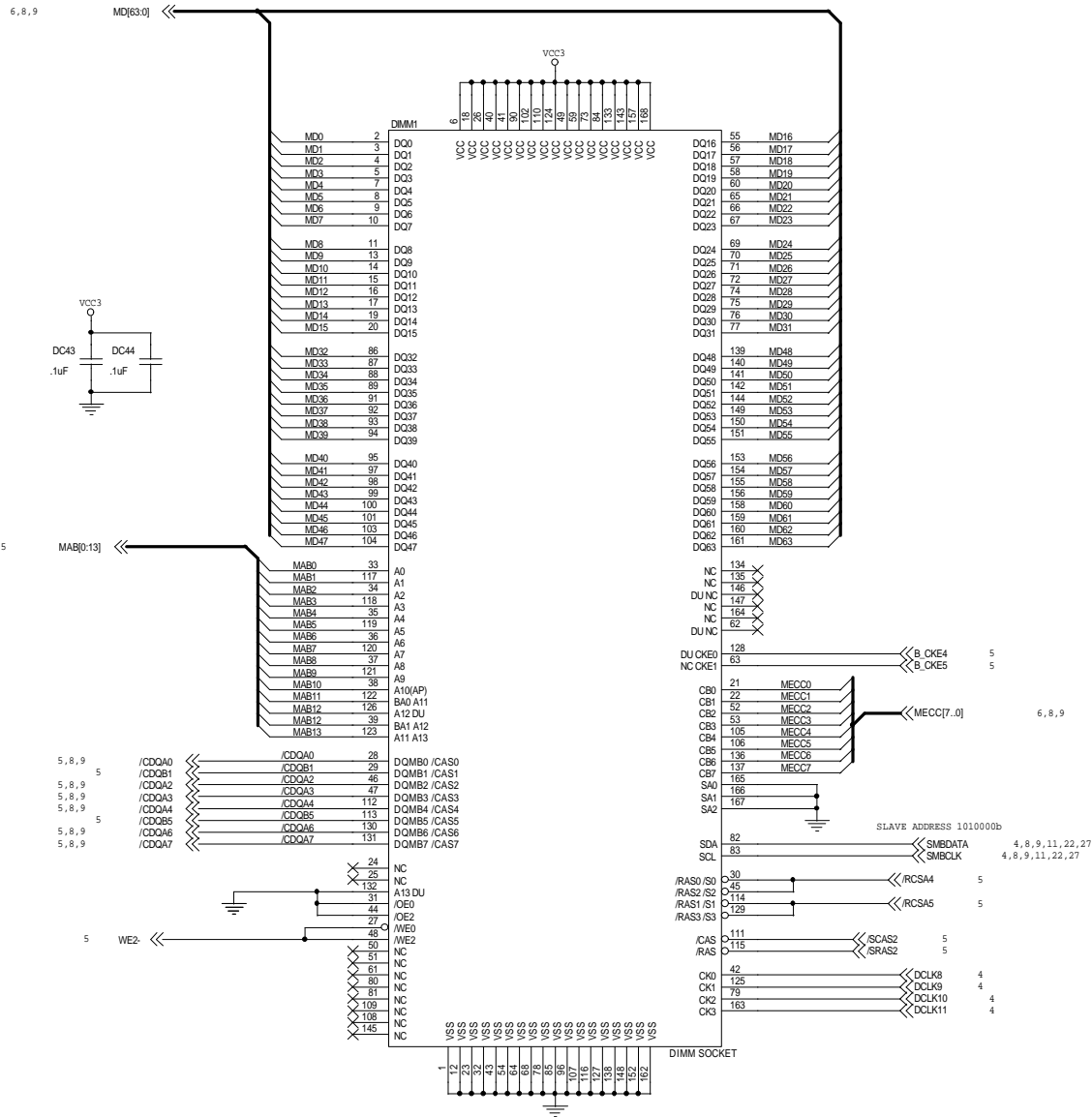
DIMM CONNECTOR 3

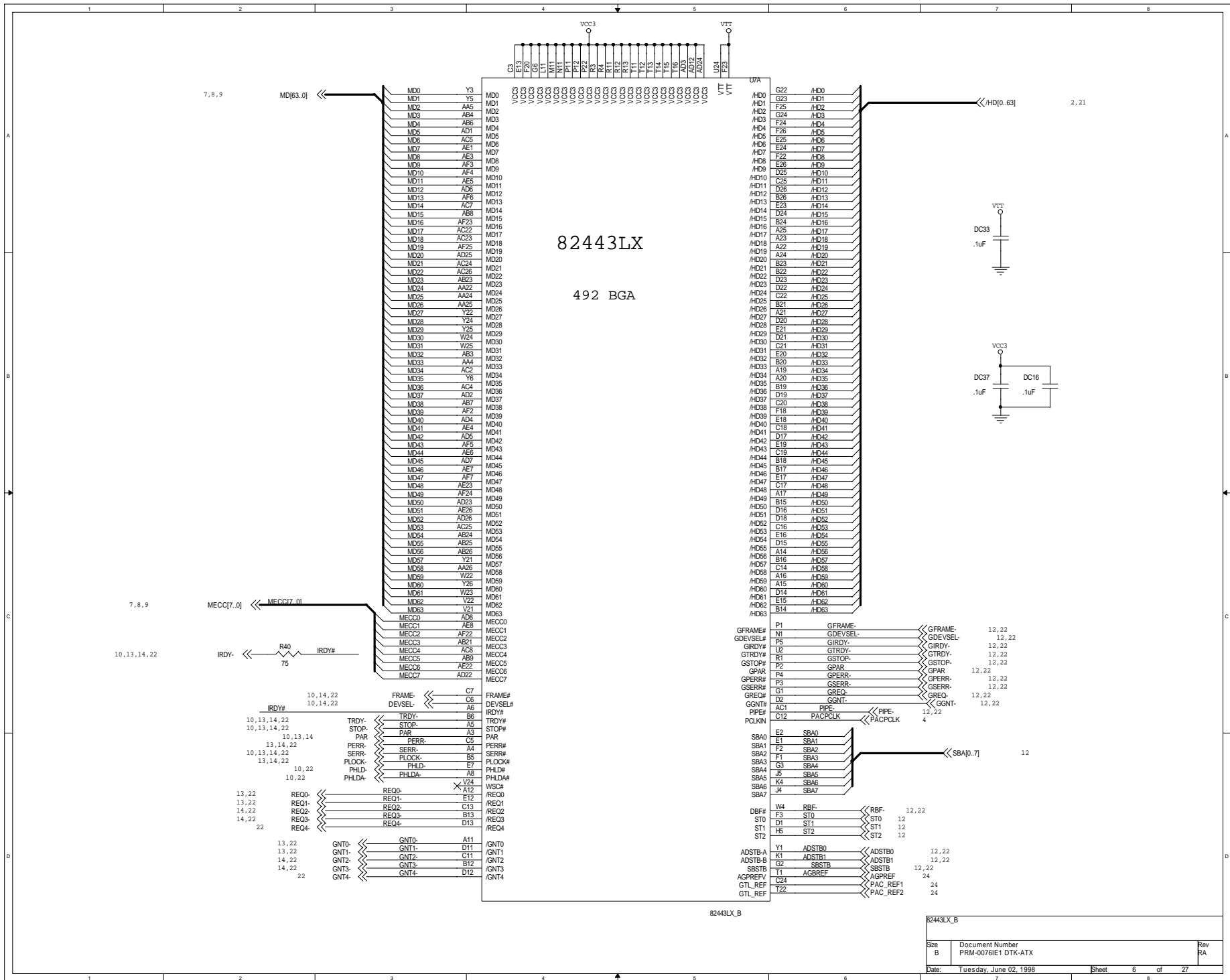


DIMM CONNECTOR 2



DIMM CONNECTOR 1





82443LX
492 BGA

82443LX_B		
Size	Document Number	Rev
B	PRM-00761E1 DTK-ATX	RA
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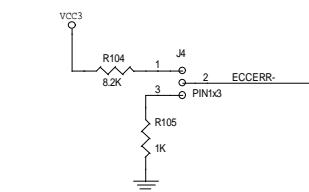
3, 21

/HA[3..31]

/HA3	M26	HA3
/HA4	N26	HA4
/HA5	N23	HA5
/HA6	N24	HA6
/HA7	N25	HA7
/HA8	M24	HA8
/HA9	N25	HA9
/HA10	M23	HA9
/HA10	M23	HA9
/HA11	L24	HA11
/HA12	L25	HA12
/HA13	L23	HA13
/HA14	M22	HA14
/HA15	K22	HA14
/HA16	K25	HA15
/HA17	K24	HA16
/HA18	L22	HA17
/HA19	J26	HA19
/HA20	J24	HA20
/HA21	J25	HA21
/HA22	H25	HA21
/HA23	J23	HA22
/HA24	H23	HA24
/HA25	K21	HA25
/HA26	G26	HA26
/HA27	H24	HA26
/HA28	J21	HA27
/HA29	G25	HA28
/HA30	H21	HA29
/HA31	H22	HA30
		HA31

3, 21	HRESET#	K26	CPU_RST#
3, 21	ADG#	P26	ADG#
3, 21	BNR#	F24	BNR#
2, 11, 22	HNIT#	A13	HNIT#
3, 21	BREQ0#	L26	BREQ0#
3, 21	BPR#	R24	BPR#
3, 21	DBSY#	V25	DBSY#
3, 21	DEFER#	R22	DEFER#
3, 21	DRDY#	R26	DRDY#
3, 21	HT#	U26	HT#
3, 21	HTM#	U25	HTM#
3, 21	HLOCK#	S26	HLOCK#
3, 21	HTRDY#	P23	HTRDY#
3, 21	RS0#	T24	HTRDY#
3, 21	RS1#	W26	RS0#
3, 21	RS2#	U22	RS1#
3, 21	/HREQ0	P25	RS2#
3, 21	/HREQ1	R23	/HREQ0
3, 21	/HREQ2	T23	/HREQ1
3, 21	/HREQ3	V26	/HREQ2
3, 21	/HREQ4	R25	/HREQ3

4	PACHCLK	T2	HCLKN
20	PCIRST#	AE2	RSTIN#
11	VREFSV	U23	REFSV
16	ECCERR#	B2	TESTIN#
		U23	ECC_ERR



J3	IOQD	DEPTH
1-2	1	Default
2-3	MAX	

10, 13, 14

AD[0..31]

10, 13, 14

C_BE[0..3]

AD0	H4	AD0
AD1	G4	AD1
AD2	G5	AD2
AD3	F4	AD3
AD4	E3	AD4
AD5	F5	AD5
AD6	E4	AD6
AD7	D4	AD7
AD8	E5	AD8
AD9	D5	AD9
AD10	C2	AD9
AD10	F7	AD11
AD11	C1	AD10
AD12	B3	AD12
AD13	B1	AD13
AD14	B4	AD14
AD15	B4	AD15
AD16	C8	AD16
AD17	D7	AD17
AD18	B8	AD17
AD19	E8	AD18
AD19	N5	AD19
AD20	D8	AD20
AD21	C9	AD21
AD22	B8	AD22
AD23	E9	AD22
AD24	D9	AD23
AD25	D10	AD24
AD26	C10	AD25
AD27	F10	AD26
AD28	B10	AD27
AD29	E10	AD28
AD30	B11	AD29
AD31	E11	AD30
	C4	AD31
C_BE0	A2	C_BE0
C_BE1	A7	C_BE1
C_BE2	A7	C_BE2
C_BE3	A9	C_BE3

82443LX

492 BGA

82443LX_A

MAA0	AC13	MAA0
MAA1	AE13	MAA1
MAA2	AB12	MAA2
MAA3	AD13	MAA3
MAA4	AC14	MAA4
MAA5	AD15	MAA5
MAA6	AC15	MAA6
MAA7	AD16	MAA7
MAA8	AC17	MAA8
MAA9	AE17	MAA9
MAA10	AA18	MAA10
MAA11	AE18	MAA11
MAA12	AE19	MAA12
MAA13	AF19	MAA13

MAB0	AD14	MAB0
MAB1	AF14	MAB1
MAB2	AE14	MAB2
MAB3	AE15	MAB3
MAB4	AF15	MAB4
MAB5	AA19	MAB5
MAB6	AF16	MAB6
MAB7	AB19	MAB7
MAB8	AE16	MAB8
MAB9	AF18	MAB9
MAB10	AD18	MAB10
MAB11	AD18	MAB11
MAB12	AD17	MAB12
MAB13	AD17	MAB13

RCSA0	AB20	RCSA0
RCSA1	AE20	RCSA1
RCSA2	AF20	RCSA2
RCSA3	AC20	RCSA3
RCSA4	AC19	RCSA4
RCSA5	AB17	RCSA5
CDQA0	AD9	CDQA0
CDQA1	AF21	CDQA2
CDQA2	AD21	CDQA3
CDQA3	AD11	CDQA4
CDQA4	AE11	CDQA5
CDQA5	AE21	CDQA6
CDQA6	AC21	CDQA7
CDQA7		

CKE	AD20	CKE
CDQB1	AF12	CDQB1
CDQB5	AE12	CDQB5
/SRAS0	AC10	/SRAS0
/SRAS1	AF13	/SRAS1
/SRAS2	AD10	/SRAS2
/SCAS0	AE9	/SCAS0
/SCAS1	AF10	/SCAS1
/SCAS2	AF8	/SCAS2
/WE0	AE10	/WE0
/WE1	AF9	/WE1
/WE2	AC12	/WE2

GAD0	AB2	GAD0
GAD1	AB1	GAD1
GAD2	AA3	GAD2
GAD3	AA2	GAD3
GAD4	AA1	GAD4
GAD5	Y2	GAD5
GAD6	W5	GAD6
GAD7	W3	GAD7
GAD8	W1	GAD8
GAD9	V5	GAD9
GAD10	V3	GAD10
GAD11	V1	GAD11
GAD12	V2	GAD12
GAD13	U8	GAD13
GAD14	U4	GAD14
GAD15	T5	GAD15
GAD16	N5	GAD16
GAD17	N4	GAD17
GAD18	N3	GAD18
GAD19	N2	GAD19
GAD20	M4	GAD20
GAD21	L5	GAD21
GAD22	M2	GAD22
GAD23	L4	GAD23
GAD24	L1	GAD24
GAD25	K5	GAD25
GAD26	K2	GAD26
GAD27	J3	GAD27
GAD28	J1	GAD28
GAD29	J2	GAD29
GAD30	H2	GAD30
GAD31	H1	GAD31
GC_BE0	W2	GC_BE0
GC_BE1	U5	GC_BE1
GC_BE2	M1	GC_BE2
GC_BE3	L2	GC_BE3

MAA[0..13]

MAB[0..13]

RCSA[0..5]

CDQA[0..7]

VCC3

8.2k

7

7, 8, 9

7, 8, 9

8

9

7

8

9

8

7

8

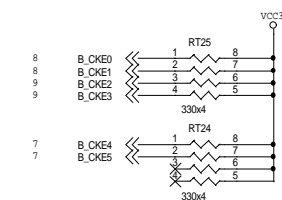
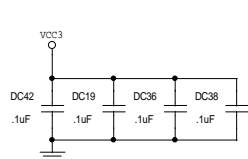
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12

12

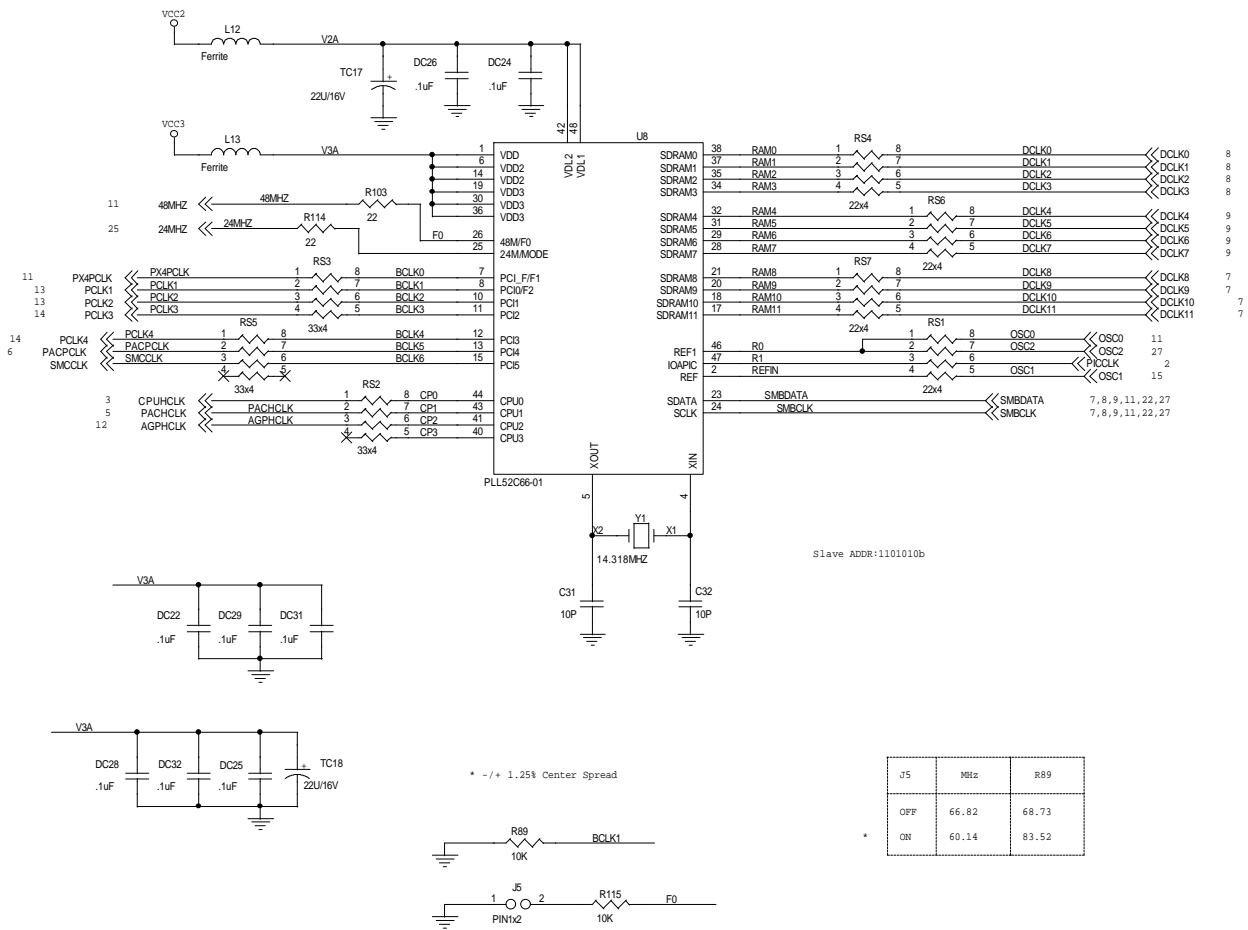
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R121 WON'T INSTALL

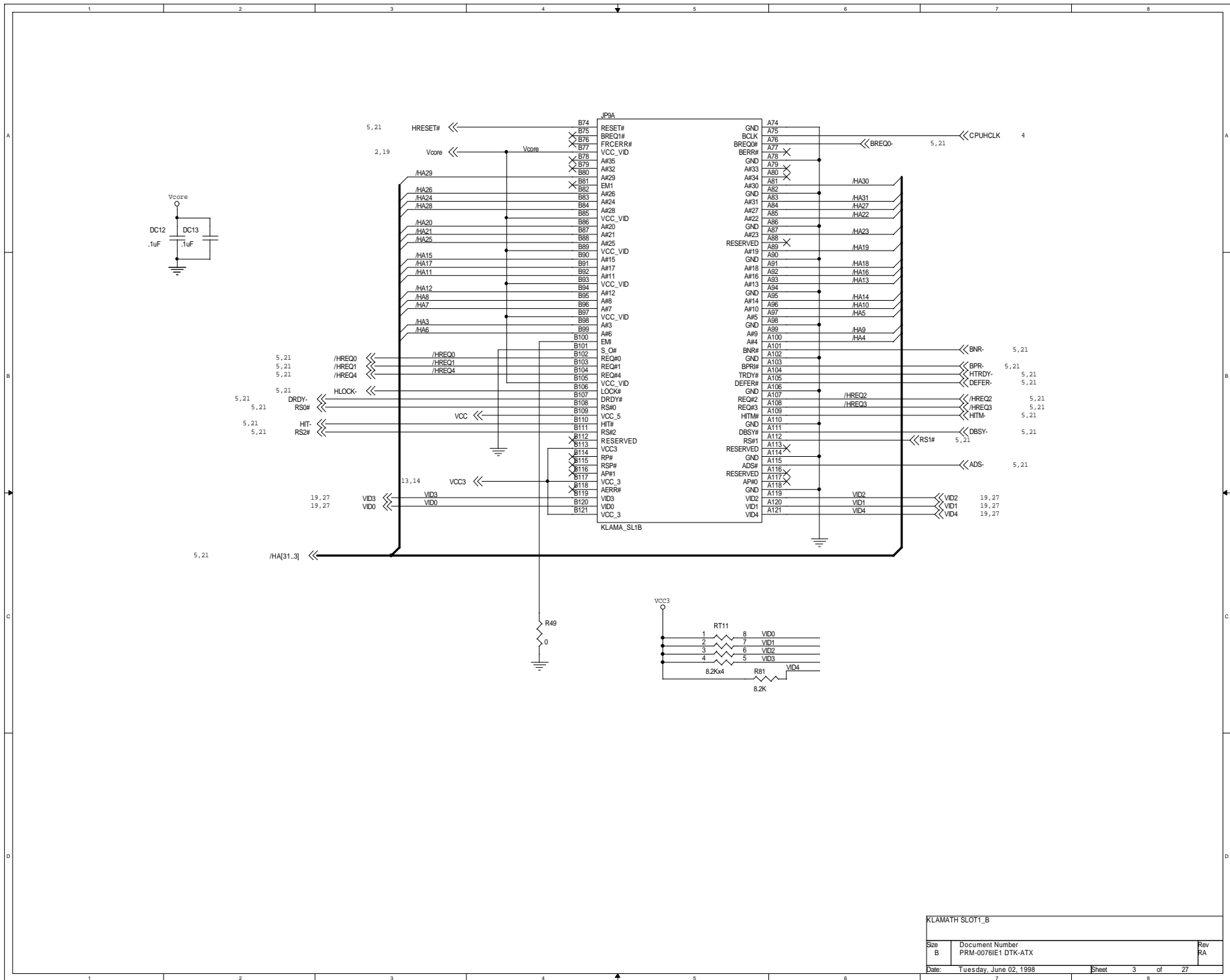


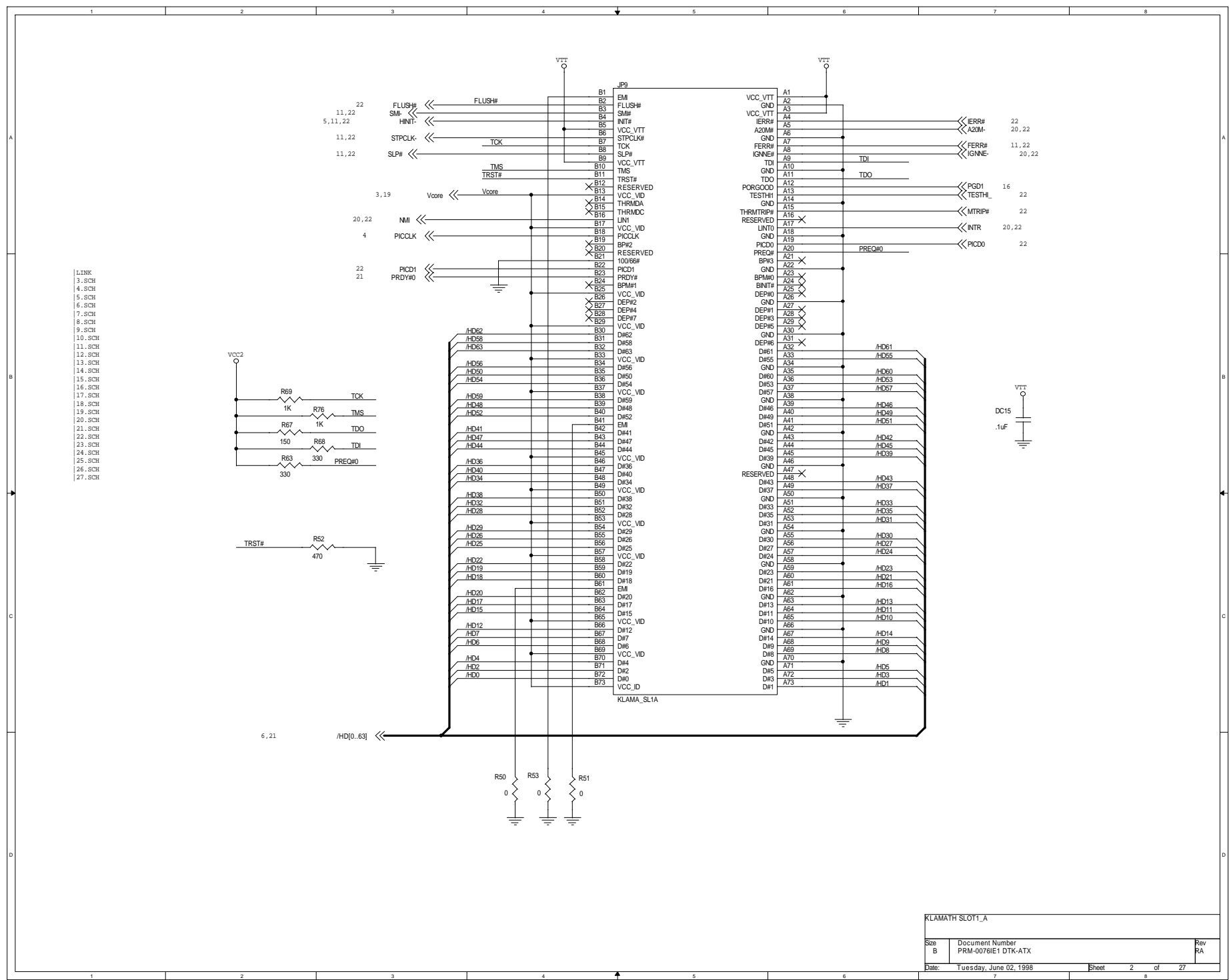
82443LX_A

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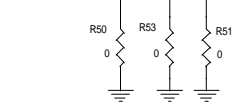
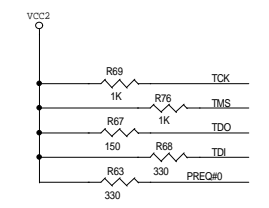


J5	MHz	R89
OFF	66.82	68.73
ON	60.14	83.52





- 1.INK
- 3.SCH
- 4.SCH
- 5.SCH
- 6.SCH
- 7.SCH
- 8.SCH
- 9.SCH
- 10.SCH
- 11.SCH
- 12.SCH
- 13.SCH
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- 26.SCH
- 27.SCH



KLAMATH SLOT1_A		
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