Technical Reference Manual Hardware and BIOS

HP Vectra XM 5/xx Series 4 PC

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PREFACE

This manual is a technical reference and BIOS document for engineers and technicians providing system level support. It is assumed that the reader possesses a detailed understanding of AT-compatible microprocessor functions and digital addressing techniques.

Technical information that is readily available from other sources, such as manufacturer's proprietary publications, has not been reproduced.

This manual contains summary information only. For additional reference material, refer to the bibliography.

CONVENTIONS

The following conventions are used throughout this manual to identify specific elements:

- Hexadecimal numbers are identified by a lower case h.
  For example, 0FFFFFFFh or 32F5h

- Binary numbers and bit patterns are identified by a lower case b.
  For example, 1101b or 10011011b

BIBLIOGRAPHY

- HP Vectra XM 5/xx series 4 PC *User's Guide* manual kit (D3960A).
- HP Vectra XM 5/xx series 4 PC *Familiarization Guide* (D3960-90901)
- HP *Network Administrator's Guide* (5964-1467).
- *HP Vectra Accessories Service Handbook - 5th edition* (5963-8034)
- *HP Vectra PC Service Handbook (Volume 1) - 9th edition* (5963-8033)
- HP *Support Assistant* CD-ROM

The following Intel® publication provides more detailed information:

- *Pentium Microprocessor Data Sheet* (241595-002)

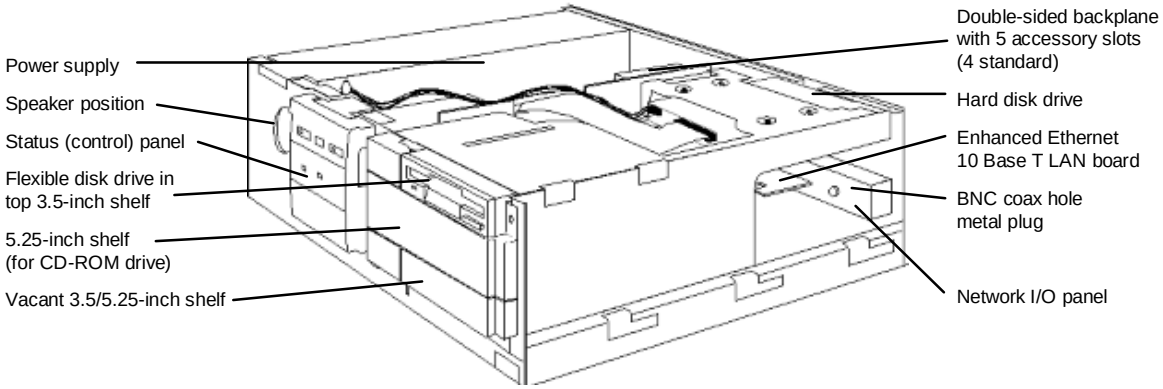
Table of Contents

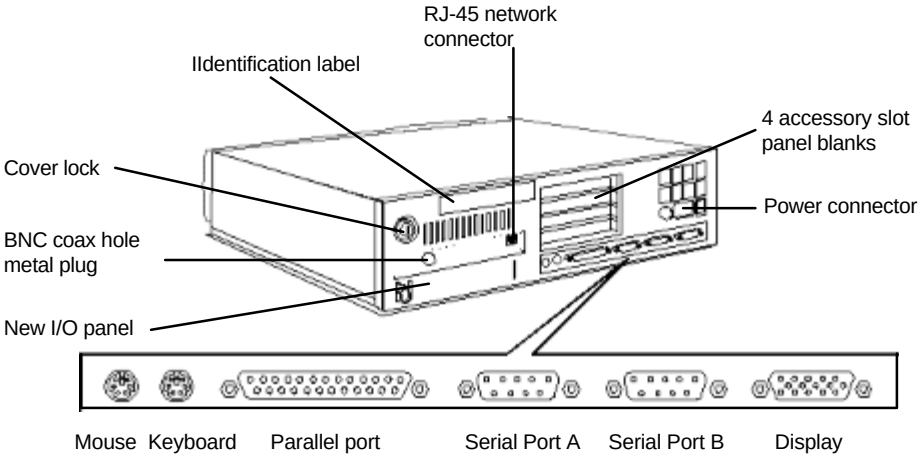
1 SYSTEM OVERVIEW

This manual describes the *HP Vectra XM 5/xx series 4 PC*, and provides detailed system specifications. The PC is constructed around the Peripheral Component Interconnect (PCI) bus and Industry Standard Architecture (ISA) bus. Its central feature is the Enhanced Ethernet Network board fitted as standard in a new PCI slot on the backplane, and the ability to be turned on remotely from another PC on the network.

EXTERNAL FEATURES

The following diagrams show the front and rear views of the *HP Vectra XM 5/xx series 4 PC*.





INTERNAL FEATURES

Diagrams of the double-sided back-plane and the system board can be found at the beginning of the next chapter. These show the locations of the PC's main field-serviceable components. The components of the system board are described in the same chapter. The characteristics of the PC's video, disk and networking devices are described in Chapter 3. The HP BIOS routines are described in Chapter 4; the Remote Power-On (RPO) facility and Desktop Management Interface (DMI) are described in Chapter 5; and the Power-On Self-Test routines are summarized in Chapter 6.

SPECIFICATIONS AND CHARACTERISTIC DATA

Physical Characteristics

Desktop Unit

Weight:	20 lbs (9 kg)
Dimensions:	15.3 inches (D) by 16.5 inches (W) by 4.9 inches (H) (39 cm by 42 cm by 12.5 cm)
Footprint:	1.8 sq ft (0.17 $m^{2)}$
Keyboard:	18 inches (W) by 7 inches (D) by 1.3 inches (H), when flat, or 18 inches (W) by 7 inches (D) by 2 inches (H), when standing (464mm by 178mm by 33mm when flat, or 464mm by 178mm by 51mm, when standing)

Electrical Specification

Parameter	**Limit for the Power Supply**	Limit per PCI Accessory Slot	Limit per ISA Accessory Slot
Input voltage	100-240 Vac (wide-ranging)	—	—
Input current (max)	3 A	—	—
Input power (max)	150 W	—	—
Input frequency	47 Hz to 63 Hz	—	—
Heat dissipation	150 W	—	—
Available power	100 W (continuous)	15 W (max)	15 W (max)
Max current at +12 V	4 A	0.5 A	1.5 A
Max current at -12 V	0.3 A	0.1 A	0.3 A
Max current at +5V	13.5 A	4.5 A	4.5 A
Max current at -5V	0.1 A		0.1 A
Input power (when turned Off)	Less than 5 W	When the PC is Off, but still plugged in, an independent mini power supply keeps the network board active enough to watch out for the “Remote Power-On” (RPO) signal	
Available power (when Off)	0.1 W		
Available current (when Off)	0.05 A		

An attempt to draw too much current (such as a short circuit across edge-connector pins, or an accessory board that is not suitable for the PC), will cause the overload protection in the power supply to be triggered, and the PC could fail to boot.

ENVIRONMENTAL SPECIFICATION

Environmental Specifications (System Processing Unit, with Hard Disk)

Operating Temperature	+ 40°F to 104° F (+5°C to +40°C)
Recommended Operating Temperature	+59°F to +158°F (+15°C to +30°C)
Storage Temperature	-40°F to +158°F (-40°C to +70°C)
Over Temperature Shutdown	+122°F (+50°C)
Operating Humidity	15% to 80% (relative)
Storage Humidity	8% to 80% (relative)
Acoustic noise emission	<40 dB in the workplace under normal conditions as defined by DIN 45635 T.19 and ISO 7779
Operating Altitude	10000 ft (3100m) max
Storage Altitude	15000ft (4600m) max

Operating temperature and humidity ranges may vary depending upon the mass storage devices installed. High humidity levels can cause improper operation of disk drives. Low humidity levels can aggravate static electricity problems and cause excessive wear of the disk surface.

CONTROL PANEL

The control (status) panel of the *HP Vectra XM 5/xx series 4 PC* has the following features:

- a power on/off button with integrated on/error status light (which flickers in power-saving mode)
- a *press-and-hold* RESET button
- a hard disk activity light (for IDE drives)
- a keyboard lock button with integral status light
- a LAN activity light (for the network board).

DOCUMENTATION

The table below summarizes the documentation that is available for the *HP Vectra XM 5/xx series 4 PC*.

Only selected publications are available in paper-based form. Most are available as printable files from the HP regional support servers, or from the *HP Support Assistant* CD-ROM.

Title	Regional Support Servers	Support Assistant CD-ROM	Paper-based
HP Vectra XM 5/xx series 4 PC User's Guide	printable PCL file	yes	D3960A
HP Vectra XM 5/xx series 4 PC Technical Reference Manual: Hardware and BIOS	printable PCL file	yes	no
HPVectra PC Service Handbook Volume 1 (9th Edition)	printable PCL file	yes	5963-8033
HPVectra Accessory Service Handbook (5th Edition)	printable PCL file	yes	5963-8034
Network Administrators Guide	WinHelp format	yes	5964-1467

WHERE TO FIND THE INFORMATION

The following table summarizes the availability of information within the *HP Vectra XM 5/xx series 4 PC* documentation set. In addition, documentation is available for each HP peripheral device. Notably, this includes the following:

	User's Guide or Installation Guide
Display User's Guide	Information on setting up and configuring
Disk drive User's Guide	Information on setting up and configuring
Audio User's Guide	Information on setting up and configuring
Network Administrator's Guide	Information on setting up and configuring

	User's Guide	User Online	Familiarization Guide	Service Handbook	Technical Reference Manual
Introducing the PC					
Product features	Key features	Exploring	New features Vectra PC comparison	Exploded view Parts list	Key features
Product model numbers			Product range	Product range CPL dates	
Using the PC					
Connecting cables and turning on	Keyboard, mouse, display, network, printer, power				
Finding on-line information	Finding READ.MEs and on-line documentation				
Preloaded software	Finding, initializing, starting	Using			
Environmental	Setting up the PC	Working in comfort			
Formal documents	License agreement Warranty information	License agreement			
Upgrading the PC					
Opening the PC	Full details				
Supported accessories	Part number details		Full PN details	Full PN details	
Installing accessories	How to install		New procedures		
Configuring devices	Installing drivers	Configuring peripherals			
Fields and their options within *Setup*	Complete list		New fields		Key fields
Repairing the PC					
Troubleshooting	Basic		Repair policy	Service notes	Advanced
Technical information	Basic		Basic		Advanced
System board	Switches and connectors		Switches and connectors How to replace	Switches and connectors	Switches and connectors Chip-set details
BIOS	Basic details		New features		Technical details Memory maps
Power-On Self-Test routines (POST)	Key error codes and suggestions for corrective action		New features		Error codes and suggestions for corrective action Order of tests

2 SYSTEM BOARD

The next chapter describes the video, disk and network devices which are supplied with the PC.

This chapter describes the components of the system board.

PRINCIPAL COMPONENTS AND FEATURES

The system board, as depicted on the next page, contains the following components:

Processor Socket

The microprocessor is packaged in a *pin-grid-array* (PGA), which is seated on the system board in a *zero-insertion-force* (ZIF) *socket*.

VRM Socket

P54C (75, 90 and 100 MHz) Pentium processors, and P54CS (133 and 150 MHz) Pentium processors require a 3.3 V supply. Since the power supply of the PC has a regulated 3.3 V output, a shorting block is used to connect this directly to the Pentium processor.

P54C (120 and 166 MHz) Pentium processors require slightly more than 3.3 V, and therefore need an active VRE *voltage regulator module* (VRM), in which the voltage is derived both from the 3.3 V and 5 V outlets of the power supply.

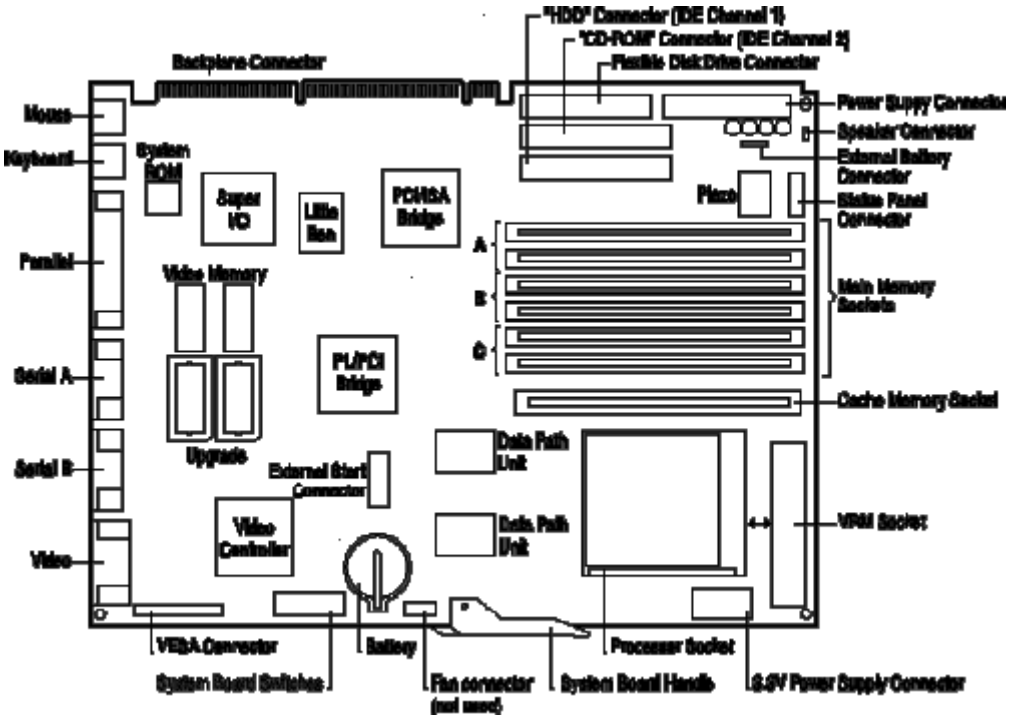
System Board Switches

The functions of the *system board switches*, used for configuring the PC, are summarized in the following table:

Switch		Function	Default
1-4	-	Processor frequency, see the table under "Bus Frequencies" later in this chapter	-
5	**Open**	**Enables User and Administrator passwords**	**Open**
	Closed	Clears User and Administrator passwords	
6	**Open**	**CMOS memory acts as non-volatile store for the *Setup* data**	**Open**
	Closed	Clears the *Setup* configuration data in the CMOS memory	
7	-	Processor frequency, see the table under "Bus Frequencies" later in this chapter	-
8	**Open**	**Disables secure mode**	**Open**
	Closed	Enables secure mode - prevents modification of the *Setup* data and flashing of the BIOS	
9	**Open**	**Disables keyboard power-on**	**Closed**
	Closed	Enables keyboard power-on	
10	**Open**	**Not used**	**Open**

Main Memory Sockets

There are six *main memory module sockets*, arranged in three banks (A to C), allowing installation up to 128 MB DRAM. One bank is already occupied by the pair of *memory modules* that contain the 8 or 16 MB of memory that is fitted as standard (depending on the model of the PC).



Video Controller and VESA Connector

There is an integrated 64-bit Ultra VGA controller (S3 Trio 64 PnP) on the PCI bus, with a VESA connector.

External Start Connector

This connector includes the VStandby power supply line that supplies the network board with its power whilst the rest of the PC is turned off. It also includes the control lines which the network board uses to turn on the main power supply, and to send or receive other control and status information.

Super I/O Chip

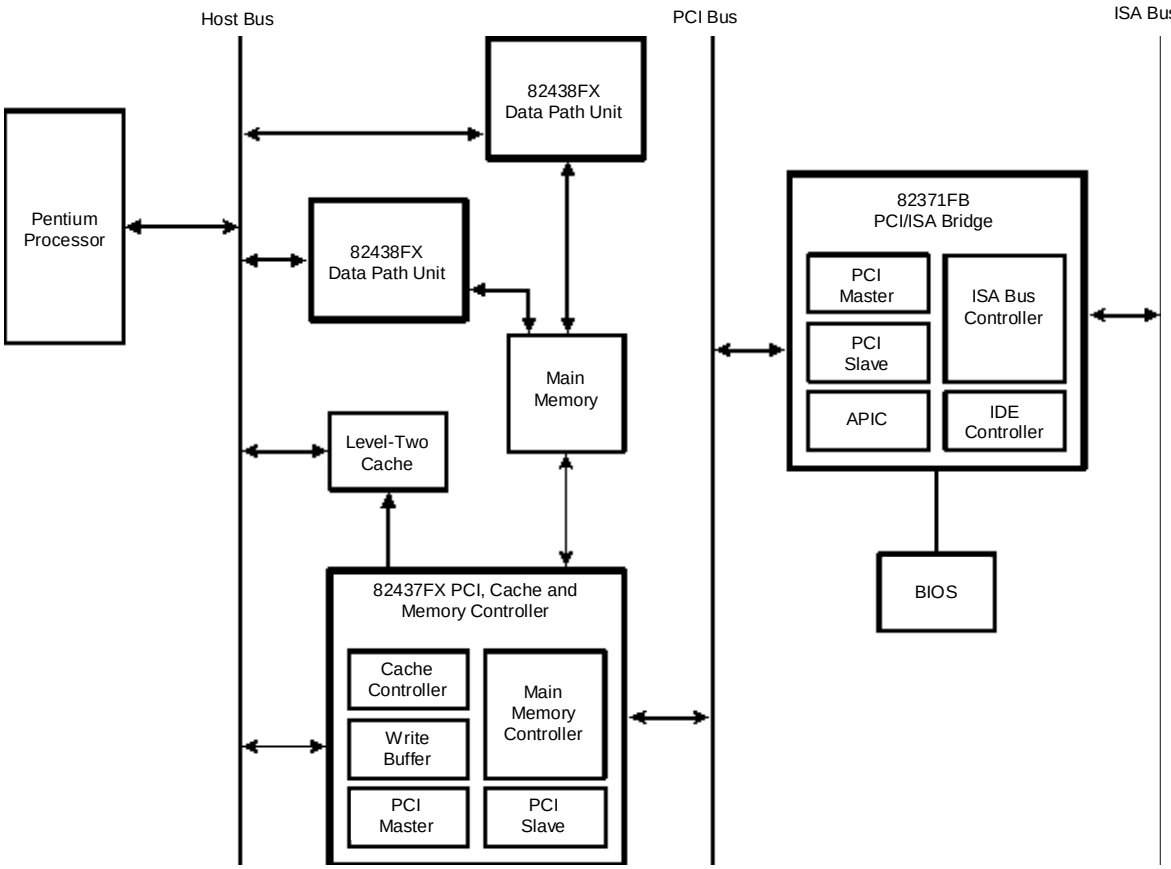
The *Super I/O* chip, driven from the ISA bus, provides the control for two slow mass-storage devices (any suitable combination of flexible disk and tape drives), one parallel and two serial communications ports.

Chip-Set

The *Intel Triton 82437/8 PCI chip-set* consists of four chips that interface between the three main buses (the Processor-Local bus, the PCI bus and the ISA bus).

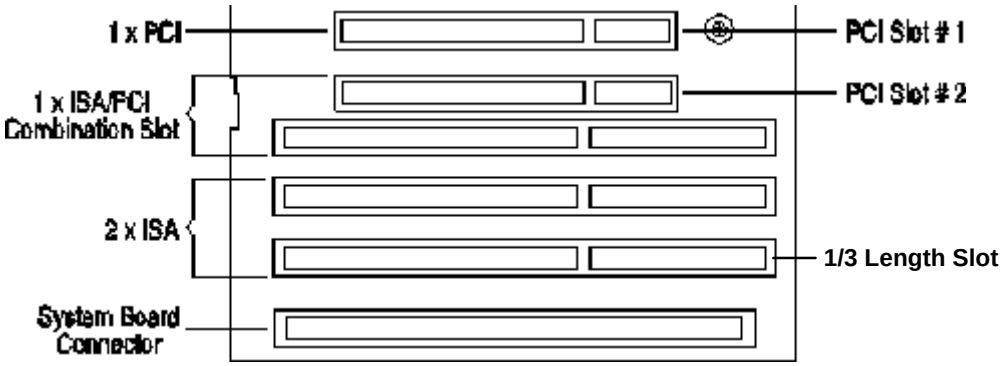
- The PL/PCI Bridge chip (82437FX) also provides the control for the PCI bus, L2 cache memory, and main memory.

- Two Data Path Unit chips (82438FX).
- The PCI/ISA Bridge chip (82371FB) also provides the control for the IDE.



THE BACKPLANE

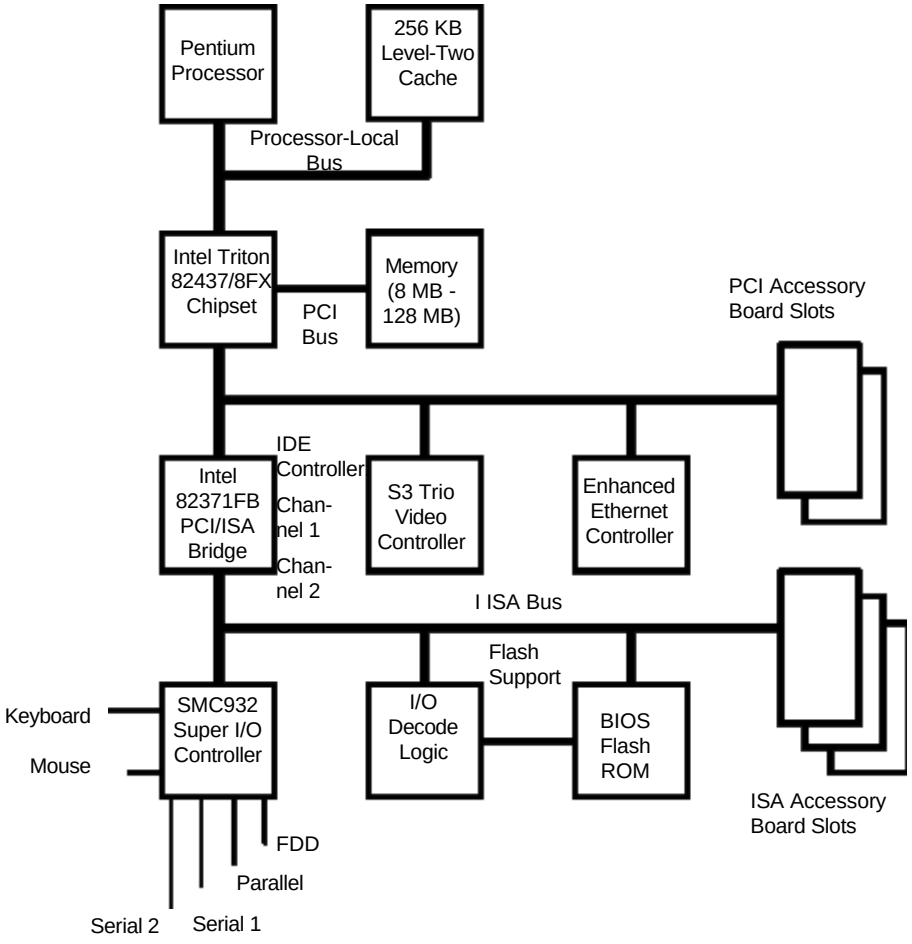
The left-hand side of the double-sided back-plane, as viewed from the front of the PC, is shown in the diagram below. It shows two *accessory slots* on the PCI bus, two on the ISA bus, and one that lies on either bus. Thus there are three PCI accessory sockets, and three ISA bus accessory sockets. The lowest ISA socket can only accommodate an HP proprietary ISA accessory board.



The other side of the back-plane bears a single PCI slot. This accommodates the Enhanced Ethernet 10 BaseT Network board.

ARCHITECTURAL VIEW

The block diagram on the next page gives an architectural view of the *HP Vectra XM 5/xx series 4 PC*. The next section in this chapter describes the devices on the system board which are associated with the Processor-Local (PL) bus. The section after describes the devices on the system board that are associated with the Peripheral Component Interconnect (PCI) bus. The final section describes the devices on the system board that are associated with the Industry Standard Architecture (ISA) bus.



DEVICES ON THE PROCESSOR-LOCAL BUS

The following subsystems are associated with the Processor-Local bus:

- The Intel Pentium microprocessor
- cache memory
- main memory.

THE INTEL PENTIUM MICROPROCESSOR

The Pentium is a 32-bit architecture processor on a 64-bit bus, and is 100% software compatible with Intel's family of x86 processors. All application software that has been written for Intel 80386 and Intel 80486 processors can run on the Pentium without modification. The Pentium processor contains all the features of the Intel 80486 processor, with the following added features which enhance performance:

Superscalar Architecture

The Pentium processor's *static superscalar architecture* has two instruction pipelines and a floating-point unit, each capable of independent operation. The two pipelines allow the Pentium to execute two integer instructions in parallel, in a single clock cycle. This is called instruction pairing. Each instruction must be simple. One pipeline will always receive the next sequential instruction of the one issued to the other pipeline. Using the pipelines in this way halves the instruction execution time and almost doubles the performance of the processor, compared with an Intel 80486 microprocessor of the same frequency.

FPU

The *floating point unit* (FPU) incorporates optimized algorithms and dedicated hardware for multiply, divide, and add functions. This increases the processing speed of common operations.

Dynamic Branch Prediction

To implement the Pentium's 4-state *dynamic branch prediction*, the processor uses two prefetch buffers. One buffer is used to prefetch instruction code in a linear way, and one to prefetch instruction code depending on the contents of the *branch target buffer* (BTB). The BTB is a small cache which keeps a record of the way that the instruction branched the last time it was used. When this information leads to a correct prediction on the subsequent branch, the branch is executed without delay, thereby enhancing performance.

Bus Frequencies

Like the 80486 DX2 processor, the Pentium uses internal clock multiplication. For example, the Pentium 150 MHz processor multiplies the 60 MHz system clock by 2.5. Switches 1 and 2, on the system board switch bank, set the frequency of the Processor-Local bus. Switches 3, 4 and 7 set the clock multiplier ratio. The relationship of the switch settings to Processor-Local bus and processor frequencies is summarized in the following table:

Switch		**Processor-Local Bus Frequency**	**Switch**			**Frequency Ratio Processor : Local Bus**	**Processor Frequency**
1	2		3	4	7		
Closed	Closed	50 MHz	Open	Open	Open	1.5 : 1	75 MHz
Closed	Open	60 MHz	Open	Open	Closed	1.5 : 1	90 MHz*
Open	Closed	66 MHz	Open	Open	Closed	1.5 : 1	100 MHz
Closed	Open	60 MHz	Closed	Open	Closed	2 : 1	120 MHz
Open	Closed	66 MHz	Closed	Open	Closed	2 : 1	133 MHz
Closed	Open	60 MHz	Closed	Closed	Closed	2.5 : 1	150 MHz
Open	Closed	66 MHz	Closed	Closed	Closed	2.5 : 1	166 MHz

*The 90 MHz model is not available for the HP Vectra XM 5/xx series 4 PCs at the time of printing. This information is provided for completeness only.

The computer will execute erratically, if at all, if the configuration switches are set to operate at a higher processor speed than the processor is capable of supporting. This can cause damage to the PC.

Setting the switches to operate at a slower speed, than the processor is capable of supporting, would not cause any failure of operation, but would not execute instructions as fast as might otherwise have been possible.

CACHE MEMORY

The PC allows for the provision of two levels of cache memory: Level-1 (L1), cache memory which is fabricated by Intel within the Pentium processor chip; Level-2 (L2), cache memory is optionally installed as a memory module on the system board. Each acts as temporary storage for data and instructions from the main memory; since the system is likely to use the same data several times, it is faster to get it from the on-chip cache than from the main memory.

The L1 cache memory is divided into two separate banks: an L1 I-cache for instruction words, and an L1 D-cache for data words. Each has a capacity of 8 KB, organized on a 32-byte (256-bit) line width. The I-cache is two-way set-associative. The D-cache four-way set-associative, and is configured for Write-Back on a line-by-line basis.

The cache memory line width is four times that of the Pentium's Processor-Local data bus. Since reads and writes involve a full cache line, they require four back-to-back cycles on the bus. The first cycle in each burst of four always requires more time to complete than the three subsequent cycles. This is because the first cycle includes the addressing phase and pre-charge timing (for memory). The read and write access timing has the pattern 3-1-1-1.

The L2 cache memory, when fitted, also has a 32-byte line size. It is controlled by the PL/PCI bridge chip (see page 10) in the system board chip-set. A single HP cache memory module consists of 256 KB of direct mapped, synchronous or asynchronous, static random access memory (SRAM). The synchronous cache memory module produces 10% better performance than the asynchronous module.

MAIN MEMORY

Fast memory access, with the timing pattern 7-2-2-2, is achieved by installing EDO DRAM. The PC can use 60 ns *extended data-out* (EDO) or 70 ns *fast page-mode* (FPM) *dynamic random-access memory* (DRAM).

The PL/PCI bridge chip provides the dedicated DRAM memory address and data buses. It implements a page mode of operation, allowing one or two pages to be open simultaneously. It supports pipelined accesses, and full RAS/CAS programmability. It allows for RAS only refresh. The two data path unit chips, controlled by the PL/PCI bridge chip, implement a 64-bit data path (not interleaved) between the Processor-Local bus and main memory modules. They also provide a buffer, four 64-bit words in depth, which is used for: writes from processor to main memory; L2 cache write back cycles; and transfers from PCI to main memory. It also provides a one-level posted write buffer for all processor writes to the PCI bus memory.

There is no parity detecting logic for the main memory on this PC.

Upgrades

The *Setup* program automatically detects which memory module capacity, and speed is installed in each bank. Individual pages of memory can be configured as cacheable or non-cacheable by software or hardware. They can also be enabled and disabled by hardware or software.

The PL/PCI Bridge chip also allows for the flexible support for bank configurations (different module sizes, bank widths and combinations of single or double-density modules), and for self configuring bank start addresses. It also provides support for shadow RAM (for the memory regions 640 KB to 1 MB, in 16 KB segments), and for system management. It will only support single density modules in Bank C (4 KB or 16 KB modules), and limits the maximum memory capacity to 128 KB. It requires, also, that memory be installed in pairs of modules of identical size, width, density and technology (both EDO or both FPM).

Extending the capacity of main memory, and upgrading it with faster chips, can never have a detrimental effect on the performance. However, it *can* experience a law of diminishing returns, so that upgrading the memory does not have a cost-effective impact on the performance. Finding the correct combination is an empirical process, whether it be through simulation, or by trial and error on the real hardware.

DEVICES ON THE PCI BUS

The PL/PCI bridge is implemented within the Intel 82437FX chip. It is responsible for transferring data between the Processor-Local bus and the PCI bus.

As a PCI bus slave, this chip becomes the PL bus master, to generate DRAM requests, on behalf of other PCI bus masters. It supports PCI bus burst cycles, posted writes to DRAM for PCI burst writes, and read-ahead from DRAM for PCI burst reads.

As a PCI bus master, this chip provides for programmable PCI bus memory regions in the memory address map, and supports PCI bus burst cycles for 64-bit and 32-bit misaligned Pentium reads and writes. It provides optional posting of PCI memory and I/O writes, optional buffering of PCI memory writes, and optional read-ahead for processor to PCI accesses.

As the PCI bus arbiter, it can handle up to four masters, using a rotating priority scheme.

The PCI bus handles the following peripheral devices:

- video controller
- IDE controller
- other devices in the PCI accessory slots, including the Enhanced Ethernet 10 BaseT Network controller.

VIDEO CONTROLLER

The S3 Trio 64 PnP video controller offers full compatibility with VGA. In addition, the features are enhanced beyond Super VGA by hardware which accelerates graphical user interface operation in environments such as Microsoft Windows or OS/2. It is directly connected to the PCI bus.

1 MB of video memory is fitted as standard. An additional 1 MB video memory accessory can be installed, to give a total of 2 MB video memory. The upgrade consists of two 512 KB video memory chips.

Further details, and the tables of supported video resolutions, can be found in the next chapter.

INTEGRATED DRIVE ELECTRONICS (IDE)

The IDE controller is implemented as part of the PCI/ISA bridge chip. It supports Enhanced IDE (EIDE) and Standard IDE (Bus Master IDE). To use the Enhanced IDE features, though, hard disk drives must be compliant with Enhanced IDE.

Up to four IDE devices can be supported: two connected to the primary channel cable, and two to the secondary channel cable. The primary channel is fitted with an IDE cable with two grey connectors; the secondary channel, though capable of supporting two devices, is fitted with an IDE cable bearing only one red connector.

With EIDE, it is possible to have a fast device, such as a hard disk drive, and a slow device, such as a CD-ROM, on the same channel without affecting the performance of the fast device. The BIOS sends a command to each drive, and to determine, automatically, the fastest configuration that it supports. However, in general, the primary channel cable (the grey one) is recommended for hard disk drives, and the secondary channel cable (the red one) for CD-ROM drives. Indeed, if a CD-ROM is placed on the same channel as a hard disk drive, problems could be experienced activating the 32-bit access drivers.

Transfer Rates Versus Modes of Operation

There is an eight by 32-bit buffer for Bus Master IDE PCI burst transfers. The controller supports 32-bit Windows and DOS I/O transfers (many IDE controllers use Windows integral IDE driver which only supports 16-bit I/O transfers). It has PCI master capability, with a cycle time of 90 ns, and a maximum transfer rate of 22 MB per second. It supports programmed I/O (PIO) modes up to, and beyond, mode 4, and direct memory access (DMA) modes up to, and beyond, mode 2. The PIO modes allow the following transfer rates:

Mode	0	1	2	3	4
Cycle time (ns)	600	383	240	180	120
Transfer rate (MBytes/s)	3.33	5.22	8.33	11.1	16.7

The DMA modes allow the following transfer rates:

Mode	0	1	2
Cycle time (ns)	480	150	120
Transfer rate (MBytes/s)	4.2	13.3	16.7

Disk Capacity Versus Modes of Addressing

The amount of addressable space on a hard disk drive is limited by three factors: the physical size of the hard disk, the addressing limit of the IDE hardware, and the addressing limit of the BIOS. The Extended-CHS addressing scheme allows larger disk capacities to be addressed than under CHS, by performing a translation (for example regrouping the sectors so that there are twice as many logical tracks as is possible under the CHS addressing scheme).

	Cylinders per Device	**Heads per Cylinder**	**Sectors per Track**	**Bytes per Sector**	**Bytes per Device**
CHS	64	16	1024	512	528 M
ECHS	64	256	1024	512	8.4 G
LBA	-	-	256 M (=2^{28})	512	137 G

If the *Setup* field has been set to **automatic**, the logical block addressing (LBA) mode will be selected for each device that supports it.

Operated in SLAVE mode, the IDE controller saturates the PCI bus with transfers, thus limiting the actual achieved transfer rate to around 7 MBytes per second. Operated in MASTER mode, though, the IDE controller is allowed to work autonomously of the CPU, and the full 22 MBytes per second transfer rate can be achieved, with less than 33% occupancy of the PCI bus (so allowing the CPU to get on with other work for more than 67% of the cycle times, whilst the IDE transfers are going on in parallel).

OTHER PCI ACCESSORY DEVICES

PCI accessory boards are used for high-speed peripheral accessories. There are three slots on the PCI bus for accessory boards. One of these is already occupied by the Enhanced Ethernet 10 BaseT Network board (which is described in the next chapter), and another is a combination slot with the ISA bus.

Plug and Play

Plug and Play is an industry standard for automatically configuring the PC's hardware. When you start the PC, the Plug and Play system BIOS can detect automatically which hardware resources (IRQs, DMAs, memory ranges, and I/O addresses) are used by the system-based components.

The *HP Vectra XM 5/xx series 4 PC* has a "PnP level 1.0A" BIOS and meets the "Windows 95 Required" level for Plug and Play. Accessory boards which are Plug and Play are automatically configured by the BIOS (Windows 3.11) or by the operating system (Windows 95).

DEVICES ON THE ISA BUS

The PCI/ISA Bridge chip (otherwise known as PIIX, or as the system I/O chip, SIO-A) is an Intel 82371FB. It is responsible for transferring data between the PCI bus and the ISA expansion bus.

As the ISA bus controller, the chip supports asynchronous ISA bus operation up to 16 MHz. It integrates: two 82C37A DMA controllers, two 82C59A interrupt controllers, an 82C54 timer, a hidden ISA refresh controller, support for the BIOS, data buffers to isolate the PCI and ISA buses, and NMI control logic. It also contains the two-channel PCI IDE controller.

When transferring data to or from the PCI bus (either as PCI master or PCI slave), fast positive decode is achieve through the use of programmable memory regions. For unclaimed PCI cycles, subtractive decoding is used. The chip supports PCI-to-ISA posted memory writes, and implements PCI address/data parity generation and checking. The chip translates DMA transfers for PCI slaves.

The ISA bus handles the following devices:

- Super I/O controller, containing the following:
  - serial / parallel communications ports
  - flexible drive controller (FDC)
  - real time clock (RTC) and CMOS memory
  - keyboard and mouse controller
- serial EEPROM
- System ROM
- other ISA accessory devices.

SUPER I/O CONTROLLER

Serial / parallel communications ports

The Super I/O chip (SMC FDC37C932) supports two serial ports and one bidirectional multi-mode parallel port. The two 9-pin serial ports (on the rear panel, and whose pin layouts are depicted on page 37) support RS-232-C and are buffered by 16550 UARTs, with 16 Byte FIFOs. They can be programmed as COM1, COM2, COM3, COM4, or disabled.

The 25-pin parallel port (also on the rear panel) is Centronics compatible, supporting IEEE 1284. It can be programmed as LPT1, LPT2, or disabled. It can operate in the four modes listed on the next page.

- Standard mode (PC/XT, PC/AT, and PS/2 compatible).
- Bidirectional mode (PC/XT, PC/AT, and PS/2 compatible).
- Enhanced mode (enhanced parallel port, EPP, compatible).
- High speed mode (MS/HP extended capabilities port, ECP, compatible).

FDC

The integrated *flexible drive controller* (FDC) supports 3.5-inch and 5.25-inch flexible disk drives, and tape drives. It is software and register compatible with the 82077AA, and 100% IBM compatible. It has an A and B drive-swapping capability and a non-burst DMA option.

It has a 16-byte FIFO, though this is disabled by default. It supports burst and non-burst modes. It provides perpendicular recording drive support. It has a high-performance internal digital data separator (no external filter components are required). It provides automatic media-sense support.

Keyboard and Mouse Controller

The PC has an 8042-based keyboard and mouse controller (the socket pin layouts are as shown in a diagram on page 37). The C3758A keyboard is supplied for use with the Windows 95 operating system (though it will also work with other operating systems). It has the following capabilities:

- Space bar power on, to start the computer from the *Off* state (if **power on from keyboard** is enabled in the *Setup* program).

- Windows key (next to the [ALT] keys), which has the same effect as clicking the “Start” button on the Windows 95 task bar.

- Pull-down key (next to the right [CTRL] key), which has the same effect as clicking the right mouse button.

RTC

The real-time clock (RTC) is 146818A-compatible. The configuration RAM is implemented as 256 bytes of CMOS memory.

Serial EEPROM

This is the non-volatile memory which holds the default values for the CMOS memory (in the event of battery failure, or the user pressing [F9] in *Setup*).

SYSTEM ROM

The PC uses 256 KB of 200ns, Flash EEPROM implemented within a single 256 K 5 8-bit ROM chip. This is a ROM that can be returned to its unprogrammed state by the application of appropriate electrical signals to its pins, and hence can then be reprogrammed with the latest upgrade firmware.

The System ROM contains the system BIOS (including the boot code, the ISA and PCI initialization, RPO, DMI, the *Setup* program and the Power-On Self-Test routines, plus their error messages). These are summarized in Chapters 4 to 6.

Updating the System ROM

The System ROM can be updated with the latest BIOS firmware. This can be ordered from HP or downloaded from one of HP's online services. (For more information on HP's online services, refer to the Hewlett-Packard Support and Information Services chapter in the User's Guide that was supplied with the computer.)

The System ROM is updated by running the PHLASH utility, **PHLASH.EXE**, which is supplied with the BIOS upgrade file, **GW07xx.FUL**, and the system definition file, **platform.bin**. You must specify the *model number* of the PC since the utility which is supplied for a different model cannot be used with this one. It must be run from diskette.

Before flashing, it is necessary to disable the "Secure Mode" switch on the system switches, and to type in the System Administrator's Password when starting up the computer. The PCI and PnP information is erased in the process. The procedure for performing the update, using a command of the form "**PHLASH GW07xx.FUL**", is given in the *User's Guide* that is supplied with the computer.

Do not switch off the computer until the system BIOS update procedure has completed, successfully or not, since irrecoverable damage to the ROM may be caused. While updating the flash ROM, the power supply switch and the reset button are disabled to prevent accidental interruption of the flash programming process.

When installing a new system board, the ROM will have a blank serial number field. This will be detected automatically by the BIOS, which will then prompt the user to enter the serial number which is printed on the identification label on the back of the PC (see the diagram in Chapter 1).

Error Diagnostics and Suggested Corrective Actions

The programs and data in the system ROM are accompanied by a check-sum code. If any of the programs or data ever become corrupted, the check-sum will not correspond with the contents of the ROM, and the appropriate part of the POST routine will attempt to report the error:

```
Cannot display error messages
Flash ROM may be defective
```

The suggested corrective action is to reprogram the system ROM by running the same utility as is normally used for upgrading it.

OTHER ISA ACCESSORY DEVICES

ISA accessory boards are for slow peripheral accessories. There are three slots on the ISA bus for accessory boards. One of these is a combination slot with the PCI bus.

Plug and Play

All PCI accessory boards are Plug and Play, although not all ISA boards are. Check the accessory board's documentation if you are unsure.

In general, in a Plug and Play configuration, resources for an ISA board have to be reserved first (using a utility under Windows 95 or ICU for DOS/Windows) and then you can plug in your board. When you run a non Plug-and-Play operating system, such as Windows for Workgroups, if you want to install an ISA board, you have to reserve the resources for the board using the ICU (for Windows). Failure to do so may lead to resource conflicts.

The procedure for installing an ISA accessory board that is not Plug and Play in Windows 3.11 or Windows 95 is described in the *User's Guide* that is supplied with the PC.

3 INTERFACE BOARDS AND MASS-STORAGE DRIVES

This chapter describes the Enhanced Ethernet Network board, and the disk drives that are supplied with the PC.

THE INTEGRATED ULTRA VGA VIDEO CONTROLLER

A 64-bit PCI Ultra VGA video controller, S3 Trio 64 PnP, is integrated on the system board on all models. It can be characterized as follows:

- 100% compatible with IBM® VGA display standard
- integrated 24-bit RAMDAC
- fully programmable Pixel Clock Generator up to 135 MHz
- 60 MHz clock for video memory
- fast linear addressing with full software relocation
- Green PC power saving features
- DDC 1 compliant.

Video Memory

1 MB is fitted as standard. Two sockets are provided for installation of an additional 1 MB (two modules, each with a 512 KB, 60 ns surface mount chip). The installed video memory capacity is detected automatically by the BIOS.

Normally, the controller gives 32-bit video memory access, with 1 MB of video RAM fitted. This is increased to 64-bit access when the additional 1 MB upgrade is installed.

There is no orientation key to determine the polarity of the upgrade chips, so care must be exercised to align the point on the chips with the white dot on the system board (place the cut edge of the chips towards the left side of the PC). A special extraction tool (5041-2553) is needed when removing them again.

Video Modes

Standard and Enhanced Video Graphics Array (VGA) modes are available, as detailed in the tables on the following pages. Hardware acceleration of graphical user interface (GUI) operations is provided, and acceleration for 8, 16 and 32-bit pixel depths.

The following table details the standard VGA modes which are currently implemented in the video BIOS. These modes are supported by standard BIOS functions. The video BIOS (which is mapped contiguously in the address range C0000h to C7FFFh) contains all the routines required to configure and access the video subsystem.

Standard VGA Modes

Mode No.	Stan-dard	Interface Type	Resolu-tion	No. of Colors	Vertical Refresh (Hz)	Horizontal Refresh (kHz)	Dot Clock (MHz)
00h	VGA	text	40 x 25 chars	b/w	70	31.5	25.175
00h*	VGA	text	40 x 25 chars	b/w	70	31.5	25.175
00h+	VGA	text	40 x 25 chars	b/w	70	31.5	28.322
01h	VGA	text	40 x 25 chars	16	70	31.5	25.175
01h*	VGA	text	40 x 25 chars	16	70	31.5	25.175
01h+	VGA	text	40 x 25 chars	16	70	31.5	28.322
02h	VGA	text	80 x 25 chars	b/w	70	31.5	25.175
02h*	VGA	text	80 x 25 chars	b/w	70	31.5	25.175
02h+	VGA	text	80 x 25 chars	b/w	70	31.5	28.322
03h	VGA	text	80 x 25 chars	16	70	31.5	25.175
03h*	VGA	text	80 x 25 chars	16	70	31.5	25.175
03h+	VGA	text	80 x 25 chars	16	70	31.5	28.322
04h	VGA	graph	320 x 200	4	70	31.5	25.175
05h	VGA	graph	320 x 200	4	70	31.5	25.175
06h	VGA	graph	640 x 200	2	70	31.5	25.175
07h	VGA	text	80 x 25 chars	b/w	70	31.5	28.322
07h+	VGA	text	80 x 25 chars	b/w	70	31.5	28.322
0Dh	VGA	graph	320 x 200	16	70	31.5	25.175
0Eh	VGA	graph	640 x 200	16	70	31.5	25.175
0Fh	VGA	graph	640 x 350	b/w	70	31.5	25.175
10h	VGA	graph	640 x 350	16	70	31.5	25.175
11h	VGA	graph	640 x 480	2	60	31.5	25.175
12h	VGA	graph	640 x 480	16	60	31.5	25.175
13h	VGA	graph	320 x 200	256	70	31.5	25.175

The extended modes supported by the video BIOS are:

Extended Video Modes with 1 MB DRAM

Extended Mode No.	VESA Mode No.	Inter-face Type	Resolution	No. of Colors	Vertical Refresh (Hz)	Horizontal Refresh (kHz)	Dot Clock (MHz)
4Eh	207h	graph	1152 x 864	256	60	55	80.000
4Fh	208h	graph	1280 x 1024	8	43i	47.7	80.000
4Fh	208h	graph	1280 x 1024	8	60	63.7	110.000
51h	212h	graph	640 x 480	16.7 M	60	31.5	25.000
52h	213h	graph	640 x 400	16.7 M	70	31.5	25.000
54h	10Ah	text	132 x 43 chars	16	70	31.5	40.000
55h	109h	text	132 x 25 chars	16	70	31.5	40.000
65h	10Dh	graph	320 x 200	32,768	70		12.540
66h	10Eh	graph	320 x 200	65,536	70		12.540
67h	10Fh	graph	320 x 200	16.7 M	70		12.540
68h	100h	graph	640 x 400	256	70	31.5	25.175
69h	101h	graph	640 x 480	256	60	31.5	25.175
69h	101h	graph	640 x 480	256	72	37.9	31.500
69h	101h	graph	640 x 480	256	75	37.5	31.500
69h	101h	graph	640 x 480	256	85	45	36.000
6Ah	102h	graph	800 x 600	16	60	37.9	40.000
6Ah	102h	graph	800 x 600	16	72	48.1	50.000
6Ah	102h	graph	800 x 600	16	75	47.5	49.500
6Ah	102h	graph	800 x 600	16	85	53.6	56.000
6Bh	103h	graph	800 x 600	256	60	37.9	40.000
6Bh	103h	graph	800 x 600	256	72	48.1	50.000
6Bh	103h	graph	800 x 600	256	75	46.8	49.500
6Bh	103h	graph	800 x 600	256	85	53.6	56.000
6Ch	104h	graph	1024 x 768	16	43i	35.5	44.900
6Ch	104h	graph	1024 x 768	16	60	48.4	65.000
6Ch	104h	graph	1024 x 768	16	70	56.5	75.000
6Ch	104h	graph	1024 x 768	16	75	60.2	80.000
6Ch	104h	graph	1024 x 768	16	85	68.7	95.000
6Dh	105h	graph	1024 x 768	256	43i	35.5	44.900
6Dh	105h	graph	1024 x 768	256	60	48.4	65.000
6Dh	105h	graph	1024 x 768	256	70	56.5	75.000
6Dh	105h	graph	1024 x 768	256	75	60.0	80.000
6Dh	105h	graph	1024 x 768	256	85	68.7	95.000
6Eh	106h	graph	1280 x 1024	16	45i	46	80.000
6Eh	106h	graph	1280 x 1024	16	60		110.000
70h	110h	graph	640 x 480	32,768	60	31.5	25.175
70h	110h	graph	640 x 480	32,768	72	37.5	31.500
70h	110h	graph	640 x 480	32,768	75	37.5	31.500
70h	110h	graph	640 x 480	32,768	85	45	36.000

Extended Mode No.	VESA Mode No.	Inter-face Type	Resolution	No. of Colors	Vertical Refresh (Hz)	Horizontal Refresh (kHz)	Dot Clock (MHz)
71h	111h	graph	640 x 480	65,536	60	31.5	25.175
71h	111h	graph	640 x 480	65,536	72	37.5	31.500
71h	111h	graph	640 x 480	65,536	75	37.5	31.500
71h	111h	graph	640 x 480	65,536	85	45	36.000
72h	112h	graph	640 x 480	16.7 M	60	31.5	25.175
72h	112h	graph	640 x 480	16.7 M	72	37.9	31.500
72h	112h	graph	640 x 480	16.7 M	75	37.5	31.500
72h	112h	graph	640 x 480	16.7 M	85	45	36.000
73h	113h	graph	800 x 600	32,768	60	37.9	40.000
73h	113h	graph	800 x 600	32,768	72	48.1	50.000
73h	113h	graph	800 x 600	32,768	75	46.8	49.500
73h	113h	graph	800 x 600	32,768	85	53.6	57.000
74h	114h	graph	800 x 600	65,536	60	37.9	40.000
74h	114h	graph	800 x 600	65,536	72	48.1	50.000
74h	114h	graph	800 x 600	65,536	75	46.8	49.500
74h	114h	graph	800 x 600	65,536	85	53.6	57.000

Extended Video Modes with 2 MB DRAM

Extended Mode No.	VESA Mode No.	Inter-face Type	Resolution	No. of Colors	Vertical Refresh (Hz)	Horizontal Refresh (kHz)	Dot Clock (MHz)
6Fh	107h	graph	1280 x 1024	256	45i	46	40.000
6Fh	107h	graph	1280 x 1024	256	60	65	55.000
6Fh	107h	graph	1280 x 1024	256	72	77.7	65.000
6Fh	107h	graph	1280 x 1024	256	75	79.5	67.000
75h	115h	graph	800 x 600	16.7 M	60	37.9	40.000
75h	115h	graph	800 x 600	16.7 M	72	41.8	50.000
75h	115h	graph	800 x 600	16.7 M	75	46.8	49.500
75h	115h	graph	800 x 600	16.7 M	85	53.6	57.000
76h	116h	graph	1024 x 768	32,768	43i	35	44.900
76h	116h	graph	1024 x 768	32,768	60	48.9	65.000
76h	116h	graph	1024 x 768	32,768	70	56.5	75.000
76h	116h	graph	1024 x 768	32,768	75	60.2	80.000
76h	116h	graph	1024 x 768	32,768	85	68.7	95.000
77h	117h	graph	1024 x 768	65,536	43i	35	44.900
77h	117h	graph	1024 x 768	65,536	60	48.9	65.000
77h	117h	graph	1024 x 768	65,536	70	56.5	75.000
77h	117h	graph	1024 x 768	65,536	75	60.2	80.000
77h	117h	graph	1024 x 768	65,536	85	68.7	95.000
7Ch	120h	graph	1600 x 1200	256	48.5i	62.00	67.000

AVAILABLE BIOS VIDEO RESOLUTIONS

The video BIOS has a revision number of 1.5-04-H06, or later. Windows for Workgroups need the newly released (1.51_04) drivers. Windows 95 and Windows NT drivers are the same as those on the *HP Vectra VL 5/xx series 4 PC*.

Resolution	**Number of colors**	**Refresh Rate* (Hz)**	**Memory**
640 x 480	16, 16M (24 bpp**) 256, 32K, 64K	60 60, 72, 75	1 MB
800 x 600	16, 256, 32K, 64K	60, 72, 75	
1024 x 768	16, 256	i43***, 60, 70, 75	
1280 x 1024	16	i45***, 60	
640 x 480	16, 16M (24 bpp**) 256, 32K, 64K, 16M (32 bpp**)	60 60, 72, 75	2 MB
800 x 600	16, 256, 32K, 64K, 16M (32 bpp**)	60, 72, 75	
1024 x 768	16, 256, 32K, 64K	i43***, 60, 70, 75	
1280 x 1024	16 256	i45***, 60 i45***, 60, 72, 75	

*Your display might not support the maximum refresh rates that are shown here. Refer to the User's Guide supplied with the display for details of the refresh rates which it supports.
**bpp = bits per pixel
***Interlaced

The following table summarizes the video resolutions that can be supported, provided that suitable drivers are available for the chosen operating system. (SCO Unix only supports 15 BPP, instead of 16 BPP, and does not support 32 BPP.)

Number of Colors	16	256	32 K	64 K Hi-Color	16.7 M True-Color
Bits per Pixel	4	8	15	16	32
640 x 480		1 MB		1 MB	2 MB
800 x 600		1 MB		1 MB (2 MB for OS/2)	2 MB
1024 x 768		1 MB		2 MB	
1280 x 1024	1 MB	2 MB	Not supported		

The maximum 2D resolutions for any given video memory capacity and color scale can be found from the following table:

Number of Colors	16	256	32 K	64 K Hi-Color	16.7 M True-Color
Bits per Pixel	4	8	15	16	32
1 MB	1280 x 1024	1024 x 768	800 x 600	800 x 600	Not supported
2 MB	1280 x 1024	1280 x 1024	1024 x 768	1024 x 768	800 x 600

If Video Plug and Play is **enabled** in *Setup*, and a DDC monitor is detected, *Setup* will automatically configure the best refresh rate. For non DDC monitors, or when video Plug and Play is **disabled**, refresh rates can be changed in *Setup*.

If you attempt to set the resolution or number of colors higher than is supported by the installed video memory, the screen refresh rate is lowered automatically, and image flicker becomes more noticeable. If the resolution/refresh-rate combination is set higher than the display can support, you risk damaging the display.

The number of colors supported is limited by the graphics card and the video RAM. The resolution/refresh-rate combination is limited by a combination of the display, the graphics card, and the video RAM.

CONNECTORS

The layout of the pins for the DB15 VGA socket are depicted under "Socket Pin Layouts" later in this chapter.

The Video Electronics Standards Association (VESA) defines a standard video connector, variously known as the VESA *feature* connector, *auxiliary* connector, or *pass-through* connector. The video controller supports an output-only VESA *feature* connector in VGA mode. This connector (whose pin names are listed in a table under "Internal Connectors" later in this chapter) is integrated on the system board, and is connected directly to the pixel data bus and the synchronization signals.

This internal VESA pass-through connector is disabled by default. To use it in DOS, Windows 3.11 or Windows 95, the **FCON.EXE** utility, from “HP Utils”, must be executed. This utility configures the system.

Use of the VESA feature connector will disable the 1 MB video memory upgrade, if one is installed. Only the standard 1 MB of video memory will be used.

ENHANCED ETHERNET NETWORK BOARD

The Enhanced Ethernet Network board (AMD PCnet-PCI-II AM79C970A) is supplied on all models in a PCI accessory slot underneath the internal, hard disk drive, rear-shelf. It is plugged into the PCI accessory slot that is situated on the right-hand side of the double-sided backplane board.

It is fully compliant with the 10-BaseT, 10 Mbits per second, ISO 8802-3 (IEEE/ANSI 802.3) standard. There is a socket to support an Option ROM of up to 32 KB. On the rear panel there is one RJ-45 unshielded-twisted-pair (UTP) connector, as shown in the diagram under "Internal Connectors" later in this chapter.

There is a cable from the network board to the external start connector on the system board. This is used to implement the Remote Power-On feature (RPO) that is described in Chapter 5. This cable must be routed through the hole in the chassis. Not doing so, and allowing the cable to be routed with the flexible disk drive and IDE cables, will raise the risk of radio frequency interference (RFI) cross-talk.

When shutdown into its RPO state, the board draws 35 mA, well within the 50 mA capability of the special RPO power supply.

The board can be configured completely by software (no switches or jumpers need changing). An HP provided driver needs to be installed within the operating system (Version T.01.00).

Installing the D3979A Coax Adapter

To use a BNC coax connection, instead of the RJ-45 connection, a coax adapter (D3979A) is required. Its installation is described in the *HP Vectra Accessory Service Handbook* (5963-8034), and is indicated in the *HP Vectra PC Service Handbook* (Volume 1, 5963-8033).

Switching between the UTP and coax connections is achieved automatically. If both are connected, and are being used, the UTP connection is given priority, unless specifically configured by the user.

The adapter draws 200 mA from the main power supply. Consequently, the Remote Power-On (RPO) facility does not work when using the coax adapter.

The *Network Administrator's Guide* (5964-1467, or online) is a useful source of further information.

MASS-STORAGE DRIVES

The IDE controller is described in chapter 2. The flexible disk and tape drive controller is described in chapter 2.

HARD DISK DRIVES

One of the two 3.5-inch hard disk drive, which is characterized in the table below, is supplied on an internal rear shelf in some models. The lower 3.5-inch front access shelf can be used to accommodate an extra hard disk drive (such as D2918A, D2929A, D2925A or D2930A).

	1.2 GB IDE	**850 MB IDE**
HP product number	D2930A	D2908-60xxx
Manufacturer	Quantum	Western Digital
Product name	Fireball 1280AT	AC2850
Interface	AT	AT
Random average seek time (read)	11 ms	10 ms
Spindle speed	5400 rpm	4500 rpm
Cylinders	2484	1654
Heads (logical)	16	16
Sectors per track	63	63
Disks	2	2
Heads (physical)	4	4
Tracks per surface	4142	
Total tracks	16568	
Total user sectors	2 503 872	1 667 232
Bytes per sector	512	512
Formatted storage capacity	1281 MB	853.6 MB
Maximum linear density (fci)	115774	55300
Encoding technology	16/17 PRML	RLL 1.7
Track density (tpi)	4270	4255
Total buffer size	128 KB	128 KB

	1.2 GB IDE	**850 MB IDE**
Cache segment size	80 KB	32 KB (write cache) 48 KB (read cache)
Track to track seek time (average)	3.1 ms	4.0 ms
Full stroke seek time (average)	19 ms	23 ms
Average rotational latency	5.6 ms	6.67 ms
External burst rate (PIO mode)	6.7 MB/s	
External burst rate (PIO mode+ IORDY)	16.7 MB/s (mode 4)	11.1 MB/s (mode 3)
External burst rate (DMA)	16.7 MB/s	13.3
Sound pressure at 1m (idle)	32 dBA	36 dBA
Sound pressure at 1m (max/random seek)	35 dBA	
Power on to drive-ready (typical)	10 s	10 s
Power on to drive-ready (worst case)	30 s	16 s
Spin-down time (typical)	10 s	5 s
Spin-down time (worst case)	20 s	

FLEXIBLE DISK DRIVES

A 3.5-inch, 1.44 MB flexible disk drive (D2035B) is supplied on the top front-access shelf of all models.

CD-ROM DRIVES

A D2896B quadruple-speed (45) IDE CD-ROM drive may be supplied on some later models, if they are fitted with the D3567B multimedia kit.

(Information on multimedia models was not available at the time of printing. The components are liable to variation until the time of introduction).

TAPE DRIVES

A C4330CA (1.36 GB) tape drive can be installed in the middle 5.25-inch front access shelf.

A C4320CB (800 MB) tape drive can be installed in the lower 3.5-inch front access shelf. This drive is the T1000 from CMS. It uses the flexible disk drive I/O controller. It is not customized for HP Vectras, but has a “Y” shaped flexible disk cable to fit on the 3.5-inch flexible disk connector. It is necessary to order 5063-7922 or D3566A for the mounting rails for this accessory.

INTERNAL CONNECTORS

Hard Disk Drive Data Connector

Pin	Signal	Pin	Signal
1	Reset#	2	Ground
3	HD7	4	HD8
5	HD6	6	HD9
7	HD5	8	HD10
9	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14
17	HD0	18	HD15
19	Ground	20	orientation key
21	DMARQ	22	Ground
23	IOW#	24	Ground
25	IOR#	26	Ground
27	IORDY#	28	SPSYNC:CSEL
29	DMACK#	30	Ground
31	INTRQ	32	IO16#
33	HA1	34	PDIAG#
35	HA0	36	HA2
37	CS0#	38	CS1#
39	DASP#	40	Ground

Flexible Disk Drive Data Connector

Pin	Signal	Pin	Signal
1	Ground	2	LDENSEL#
3	Ground	4	Microfloppy
5	Ground	6	EDENSEL
7	Ground	8	INDX#
9	Ground	10	MTEN1#
11	Ground	12	DRSEL0#
13	Ground	14	DRSEL1#
15	Ground	16	DTEN0#
17	Ground	18	DIR#
19	Ground	20	STP#
21	Ground	22	WRDATA#
23	Ground	24	WREN#
25	Ground	26	TRK0#
27	Ground	28	WRPRDT#
29	Ground	30	RDDATA#
31	Ground	32	HDSEL1#
33	Ground	34	DSKCHG#

Control Panel Connector

Pin	Signal	Pin	Signal
1A	Error_LED#	1B	Keylock_LED#
2A	RstDis_Allow#	2B	HD_LEDG#
3A	Keylock_Button	3B	Off_Ask#
4A	PwrGood	4B	Remote_On1
5A	Remote_On2	5B	+5 Volt supply
6A	Reset_Ask#	6B	not connected
7A	FPanel4	7B	Ground

External Start Connector

Pin	Signal	Pin	Signal
1	Ring	2	Ground
3	WAKE1#	4	WAKE2#
5	EN_PRO	6	ExtStart#
7	PWG	8	LANLED#
9	VSTD		

System Board Power Supply Connector

Pin	Signal
1	PwrGood
2	orientation key
3	Remote_On1
4	Ground
5	Ground
6	Ground
7	+12 Volt supply
8	+5 V Vstby
9	+5 Volt supply
10	+5 Volt supply
11	+5 Volt supply
12	-12 Volt supply
13	-5 Volt supply

Battery Pack Connector

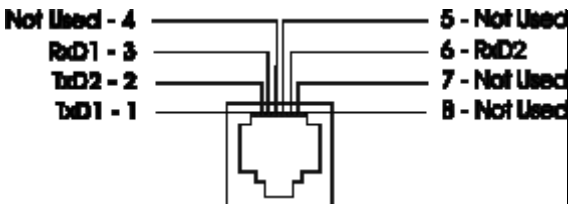
Pin	Signal
1	Ground
2	not connected
3	orientation key
4	VBATT

VESA Connector

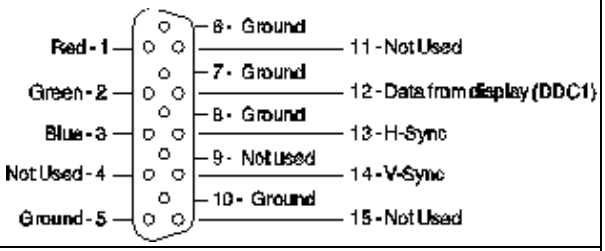
Pin	Signal	Pin	Signal
1	Ground	14	PA1
2	Ground	15	PA2
3	Ground	16	PA3
4	+5 V	17	PA4
5	+5 V	18	PA5
6	+5 V	19	PA6
7	not connected	20	PA7
8	not connected	21	PClk
9	Ground	22	BlankP#
10	Ground	23	HSyncB
11	Ground	24	VSyncB
12	not connected	25	Ground
13	PA0		

Socket Pin Layouts

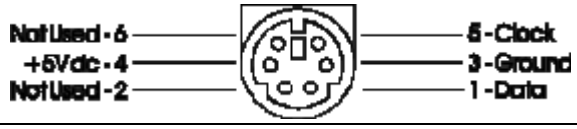
Ethernet UTP Connector



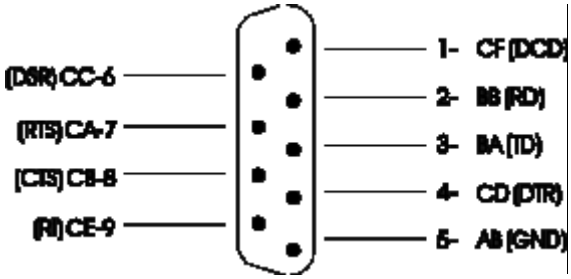
VGA Connector



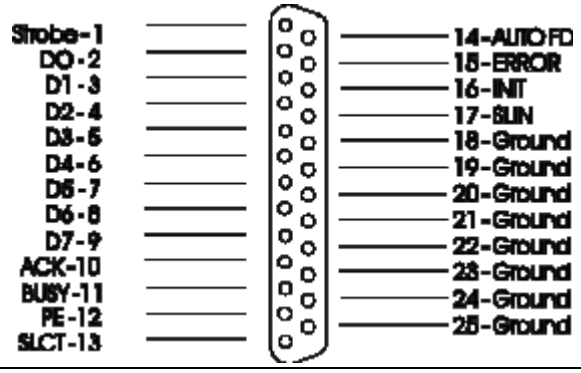
Keyboard and Mouse Connector



Serial Port Connector



Parallel Port Connector



4 SUMMARY OF THE HP/PHOENIX BIOS

This chapter and the following two chapters give an overview of the features of the HP/Phoenix BIOS.

SETUP PROGRAM

You can interrupt the POST to run the *Setup* program by pressing [F2] once the **F2=Setup** message appears on the initial "Vectra" logo screen.

The band along the top of the screen offers five menus: Main, Configuration, Security, Power, and Exit. To select one of these, simply move to the appropriate name, using the left and right arrow keys. Each menu is discussed in the following sub-sections.

MAIN MENU

The Main Menu presents the user with a list of fields, such as "System Time" and "Key auto-repeat speed". These can be selected using the up and down arrow keys, and can have their values changed using the [F7] and [F8] keys.

The "Item-Specific Help" field changes automatically as the user moves the cursor between the fields. It tells the user what the presently highlighted field is for, and what the options are.

Some fields are not changeable. Examples include fields that are for information only, and fields whose contents become "frozen" by the setting of a value in some other field. Such fields are displayed in a different color, without the "[" and "]" brackets. When the user moves the cursor with the up and down arrow keys, such fields are skipped.

Some fields disappear completely when a choice in another field makes their appearance inappropriate (for example, the "Key auto-repeat speed" and "Delay before auto-repeat" fields disappear when the user selects **Yes** in the "Running Windows 95" field, since these parameters can then be set within the operating system).

CONFIGURATION MENU

The Configuration Menu does not have the same structure as the Main Menu and Power Menu. Instead of presenting a list of fields, it offers the user a list of sub-menus. Again, the user steps between the options using the up and down arrow keys, but presses the [ENTER] key to enter the chosen sub-menu (and the [ESC] key to go back again when finished).

If access to devices has been disabled in the Security Menu, then the configuration of those devices on the Configuration Menu becomes frozen, as shown in the diagram below for Serial port A. The field becomes starred, appears in a different color and cannot be changed.

Phoenix BIOS Setup Copyright 1985-95 Phoenix Technologies Ltd. Copyright 1995 Hewlett-Packard Rev. GW.07.xx			
	Configuration		
Integrated I/O Ports			**Item-Specific Help**
Parallel port		[378h IRQ7]	Enables or disables the on-board parallel port at the specific address. 'Disabled' frees resources used by the port.
Parallel port mode		[Centronix™]	
Serial port A		* 3F8h IRQ4	
Serial port B		[Disabled]	
[*] = The device is disabled for security reasons. To enable it, use the Security/Hardware Protection menu			
F1 Help	**Select Item**	**F7/F8 Change Values**	**F9 Setup Defaults**
ESC Exit	↔ **Select Menu**	**Enter Select >Sub-Menu**	**F10 Previous Values**

Disabling a device in the Configuration Menu (for example, Serial port B in the diagram above) has the advantage of freeing the resources (such as IRQs and peripheral addresses). Disabling a device in the Security Menu disables the access, not the device. It does not have the advantage of freeing the resources, but has the advantage of temporarily disabling the device without losing the configuration settings.

Under the "Memory and Cache" sub-menu, memory caching can be set to **internal only** or **disabled**; the memory hole can be **enabled** between 15 MB and 16 MB; the graphic POST can be **disabled** if there is a Display Option ROM installed; the shadow/cache ISA option ROMs can be made accessible if detected as being fitted.

Under the "IDE" sub-menu, multi-sector transfers can be **disabled**, or set to **2**, **4**, **8**, or **16**; the translation method can be set to **extended** or **standard**; the integrated bus adapters can be set to **none, primary=IRQ15**, **secondary=IRQ14**, or **both**.

SECURITY MENU

Sub-menus are presented for changing the characteristics and values of the User Password, the System Administrator Password, the amount of protection against use of the system's drives and network connections (using the Hardware Protection sub-menu), and the amount of protection against being able to boot from the system's drives and network connections (using the Start-Up Centre sub-menu).

The minimum lengths of either type of password can be set to a specific number of characters, or to **none**. The maximum length of each is 32 characters. A limit can be set for the maximum number of retries that are permitted if the password is mistyped, and whether a delay should be imposed (of successively increasing lengths: 4 seconds, 8 seconds, 16 seconds, and finally 32 seconds) before successive retries are accepted (using the **exponential** setting for the "Lock Time Between Attempts" field).

The "User Password" sub-menu grants access to the keyboard lock timer option. Once this password has been set, the menu gives access to the main sub-menu of user preferences. Under the "Hardware Protection" sub-menu, the following devices can have their access **enabled/disabled**: flexible disk controller, IDE controllers, serial and parallel ports, network controller. Writes to the flexible disk can be **disabled**, so as to prevent the exporting of data.

Writes to the hard disk drive boot sector can be **disabled**, for instance as a protection against viruses.

Under the “Start-Up Center” sub-menu, the *Setup* program not only allows the user to select which devices are **enabled** or **disabled** for booting up the system, but also indicates their order of precedence when more than one is enabled: network, flexible disk drive, CD-ROM drive, or hard disk drive.

POWER MENU

The “Power” menu allows the user to set the standby delay. It also allows the system administrator to decide whether the network, serial ports, mouse, or space bar are enabled as a means of reactivating the system from *Standby* or *Suspend*. It is also possible to specify whether the network is enabled as a means of reactivating the system from *Off*, using the remote power-on (RPO) facility (as described in the next Chapter).

HP/PHOENIX BIOS DESCRIPTION

The System ROM contains the BIOS (System BIOS, video BIOS and low option ROM), an the power-on self-test routines that allows you to view the results of the diagnostics as well as a corrective action message (error message utility).

This chapter and the following two chapters give an overview of the HP/Phoenix BIOS. The information is divided into three main sections:

- The Remote Power-On (RPO), which is the mechanism for turning on the PC remotely from the network; and the Desktop Management Interface (DMI), which is the new method for storing and accessing information about the PC, described in Chapter 5.
- The Power-On-Self-Test or POST, which is the sequence of tests the PC performs to ensure that the system is functioning correctly, described in Chapter 6.
- menu-driven *Setup* with context-sensitive help (in US English only), described earlier in this chapter.
- The address space, with details of the interrupts used, described next.

The system BIOS is identified by the version number **GW.07.xx**. The procedure for updating the System ROM firmware is described in Chapter 2.

Summary configuration screen

You can press [F2] while the initial “Vectra” logo screen is being displayed to run the *Setup* program (as described in the previous sub-sections). Alternatively, you can press [ESC] to view the summary configuration screen, an example of which is depicted on the next page. By default, this remains on the screen for 20 seconds, but by pressing [F5] once, it can be held on the screen until [F5] is pressed again, or until [F1] is pressed. Pressing [F10] will cause the PC to be turned off.

XM/100 series 4 Copyright 1995 Hewlett-Packard — QA.xx.xx			
Any line of text can be entered here as a 'tatoo' for the PC			
BIOS version	GW.07.xx	PC Serial Number	FR54011111
CPU Date Code	N/A	LAN MAC address	0B.00.0C.13.44.45
System RAM	: 16 MB	COM1	: 3F8H (Serial A)
Bank A	: None	COM2	: 2F8H (Serial B)
Bank B	: 8 MB (EDO)	COM3	: None
Bank C	: 8 MB (FPM)	COM4	: None
Video RAM	: 1 MB	LPT1	: 378H
System Cache	: None	LPT2	: None
Video Device	: S3	LPT3	: None
1st IDE Device	: HDD 848 MB	Flexible Disk A	: 1.44 MB
2nd IDE Device	: None	Flexible Disk B	: None
3rd IDE Device	: None	Display type	: Not Available
4th IDE Device	: None		
ISA PnP	: Not Installed	PCI Slot #1	: Not Installed
ISA PnP	: Not Installed	PCI Slot #2	: Not Installed
ISA PnP	: Not Installed		
<F1> to continue, <F2> to run Setup, <F10> to power off, <F5> to retain			

I/O ADDRESSES USED BY THE SYSTEM*

Peripheral devices, accessory devices and system controllers are accessed via the system I/O space. The 64 KB of addressable I/O space comprises 8-bit and 16-bit I/O ports (these are registers that are located in the various system components). When installing an accessory board, ensure that theI/O address space selected is in the free area of the space reserved for accessory boards (100h to 3FFh).

*If configured.

170h-177h, 376h	IDE controller secondary channel
1F0h-1F7h, 3F6h	IDE controller primary channel
278h-27Fh, 378h-37Fh	Parallel port
2E8h-2EFh, 2F8h-2FFh, 3E8h-3EFh, 3F8h-3FFh	Serial port
370h-371h	Integrated I/O Controller
3B0h-3DFh	Integrated video graphics controller
3F0h-3F5h, 3F7h	Integrated flexible disk drive controller
496h-497h	HP reserved
678h-67Bh	Parallel port if ECP mode is selected
778h-77Bh	Parallel port if ECP mode is selected

Refer to the “HP BIOS I/O Port Map” in this chapter for more detailed information.

System Memory Map

00000h - 9FFFFh	640 KB–Base Memory Area
A0000h - BFFFFh	128 KB–Video Memory
C0000h - C7FFFh	32 KB–Video BIOS
C8000h - DFFFFh	96 KB–Accessory Boards Memory
E0000h - E7FFFh	32 KB–Available
E8000h - EFFFFh	Reserved
F0000h - FFFFFh	64 KB–System BIOS
100000h - FFFFFFFFh	1 MB plus–Extended Memory

Reserved memory used by accessory boards must be located in the area from C8000h to EFFFFh.

BIOS I/O PORT MAP

This section describes the HP BIOS port map. The next section provides more details about how the BIOS uses the system board components mentioned in the I/O port list.

I/O Address Ports	Function	Bits
0000-000F	DMA controller 1	8
0020-0021	Interrupt controller 1	8
0040-0043	Interval timer 1	8
0060, 0064	Keyboard controller	8
0061	NMI status and control	8
0070	NMI mask register, RTC address	8
0071	RTC data	8
0081-0083, 008F	DMA low page register	8
0092	Alternate reset and A20 Function	8
0096-009F	Internal ports	8
00A0-00A1	Interrupt controller 2	8
00C0-00DF	DMA controller 2	8
00F0-00FF	Co-processor error	
0170-0177	IDE controller secondary channel	
01F0-01F7	IDE controller primary channel	
0278-027F	Parallel port 3	
02E8-02EF	Serial port 4	
02F8-02FF	Serial port 2	
0370-0375	Secondary flexible disk controller	
0376	IDE controller secondary channel	
0377	Secondary flexible disk controller	
0378-037F	Parallel port 2	
03B0-03BB	Integrated video graphics controller	
03BC-03BF	Parallel port 1	
03C0-03DF	Integrated video graphics controller	
03E8-03EF	Serial port 3	
03F0-03F5	Flexible disk controller	
03F6	IDE controller primary channel	
03F7	Flexible disk controller	
03F8-03FF	Serial port 1	
0CF8-0CFF	Used for PCI configuration*	

*These addresses are dedicated to configuration registers for PCI devices.

ADDRESSING SYSTEM BOARD COMPONENTS

This section provides more details of how the BIOS uses the system board components mentioned in the I/O port list.

DMA Channel Controllers

Only “I/O-to-memory” and “memory-to-I/O” transfers are allowed.“I/O-to-I/O” and “memory-to-memory” transfers are disallowed by the hardware configuration.

The system controller supports seven DMA channels, each with a pageregister used to extend the addressing range of the channel to 16 MB. The following table summarizes how the DMA channels are allocated.

First DMA controller (used for 8-bit transfers)	
Channel	**Function**
0	Available
1	Available or ECP mode for parallel port
2	Flexible disk I/O
3	Available or ECP mode for parallel port
Second DMA controller (used for 16-bit transfers)	
Channel	**Function**
4	Cascade from first DMA controller
5-6	Available
6-7	Available

Interrupt Controllers

The system has two 8259A compatible interrupt controllers. They are arranged as a master interrupt controller and a slave that is cascaded through the master.

The following table shows how the master and slave controllers are connected. The Interrupt Requests (IRQ) are numbered sequentially, starting with the master controller, and followed by the slave.

IRQ (Interrupt Vector)		Interrupt Request Description
IRQ0(08h)		System timer
IRQ1(09h)		Keyboard controller
IRQ2(0Ah)	Slave IRQ	Cascade connection from INTC2 (Interrupt Controller 2)
	IRQ8(70h)	Real time clock
	IRQ9(71h)	Available for PCI accessory boards, if not used by ISA boards
	IRQ10(72h)	Available for PCI accessory boards, if not used by ISA boards
	IRQ11(73h)	Available for PCI accessory boards, if not used by ISA boards
	IRQ12(74h)	Mouse
	IRQ13(75h)	Pentium
	IRQ14(76h)	Primary channel of IDE controller
	IRQ15(77h)	Free, if not used by secondary channel of IDE controller
IRQ3(0Bh)		Free, if not used for serial port
IRQ4(0Ch)		Free, if not used for serial port

IRQ5(0Dh)		Free, if not used for parallel port
IRQ6(0Eh)		Flexible disk drive controller
IRQ7(0Fh)		Free, if not used for parallel port

Using the *Setup* program:

- IRQ3 can be made available by disabling serial ports 2 and 4.
- IRQ4 can be made available by disabling serial ports 1 and 3.
- IRQ5 can be made available by disabling the parallel port 2.
- IRQ7 can be made available by disabling parallel ports 1 and 2.
- IRQ12 can be made available by disabling the mouse interrupt.

PCI Interrupt Request Lines

PCI devices generate interrupt requests using up to four PCI interrupt request lines (INTA#, INTB#, INTC#, and INTD#).

When a PCI device makes an interrupt request, the request is re-directed to the system interrupt controller. The interrupt request will be re-directed to one of the IRQ lines made available for PCI devices.

All PCI devices with interrupt transfer support will use and share INTA#. A multiple-function PCI device may use several INT lines. These devices will require more than one system interrupt request line.

5 FACILITIES OF THE BIOS

This chapter describes a number of important features of the BIOS, such as the Remote Power-On (RPO) and Desktop Management Interface (DMI).

REMOTE POWER-ON (RPO)

The *HP Vectra XM 5/xx series 4 PC* is explicitly designed with networking in mind. All models are supplied with a tailor-made Enhanced Ethernet 10 BaseT network board fitted in a dedicated PCI bus slot.

Remote power-on (RPO) is a way to turn on the PC from a communication channel, such as a Network or Modem, using facilities that have been incorporated in the Little Ben chip and the ExtStart connector.

Switching off a networked PC normally makes it invisible to the network. As a result, many system administrators either ask users to tolerate interruptions during the day for crucial tasks like backups and software updates, or else ask them to leave their machines on all night. While *Standby*, or *Suspend* save some energy (typically 25% and 50% of the full power budget, respectively), turning the PC *Off* would save even more.

Remote power-on (RPO) is a facility that lets system administrators and authorized users switch on the PC from anywhere over an Ethernet network, perform remote administration or other tasks, and return it to *Off* or *Suspend* mode afterwards.

With RPO, HP offers wake-up at all times, whether the machine is in *Suspend* mode, *Standby* mode, or fully switched *Off*. RPO Vectra PCs are network-accessible 24 hours a day, thereby facilitating the current trend toward central PC administration.

Besides the standard suite of network-ready features, the *HP Vectra XM5/xx series 4 PC* includes all the hardware and firmware modifications necessary to implement remote wake-up from any state. These include special BIOS, a Magic Packet compatible integrated LAN chip, an external start connector, an HP-exclusive network RPO chip for controlling the start-up process, and a separate miniature power supply to keep the start-up hardware active when the machine is *Off*.

Magic Packet

Magic packet is a standard for remote wake-up developed by HP and Advanced Micro Devices (AMD). It defines a standard signal for awakening a dormant computer. The standard defines a Magic Packet frame as the PC's unique Ethernet *Media Access Control* (MAC) address, repeated 16 times and encoded in a valid network packet.

Any Magic Packet-compatible management application (such as HP OpenView Workgroup Node Manager) can send a Magic Packet frame. An administrator can do this manually, or can incorporate it into a management script.

The packet travels over any type of Ethernet LAN to the switched off the target *HP Vectra XM 5/xx series 4 PC*.

The only component not completely off in the PC is the network chip, which rests in a special low power mode. Power is supplied by a line called *VStandby* (VSTD), on the ExtStart connector (whose pin layout is shown in the table under "Internal Connectors" in chapter 3), as long as the power cord is plugged in. The independent mini power supply provides the power

necessary to keep the network chip half awake (see "Electrical Specification" in chapter 1 for more details), and ready to receive a wake-up signal. This is the only signal it can respond to in this state.

The network chip sends a signal over the HP external start connector, where it is received by the special network remote power chip. This in turn switches on the main power supply.

The *HP Vectra XM 5/xx series 4 PC* boots normally from whatever operating system is installed, just as if the power supply had been switched on from the external power switch. The console does not itself need to have RPO. If a password has been set, the **Start with keyboard locked** option must be enabled, to allow the operating system to boot.

At the end of the session, the *HP Vectra XM 5/xx series 4 PC* needs to be shut down again. This can be achieved remotely if it is running Windows 95. If, on the other hand, it is running Windows for Workgroups, using remote DMI, it can be configured to go back to *Suspend* mode.

Activity within Setup

Since the user is not physically present, the level of security must be tighter. There must be a distinction between the user-boot process, and the RPO-boot process. HP provides all the necessary *Setup* options to keep users from interfering with the PC during the remote session. Administrators can easily set the management package to toggle on options like:

- Keyboard lock mode: This offers the same suite of security features as the keyboard lock button on the front of every Vectra PC (keyboard, mouse, reset and power button disabled).

- Floppy disable: this makes sure the PC cannot be disrupted by re-booting from a diskette.

Some RPO hardware are extensions from existing designs that have not been designed for functioning under RPO. This implies that hardware has to be initialized by software before RPO is enabled. RPO is available when the POST routines have finished executing. It is initialized by an SMI which is triggered from the mains power button. A power failure when the PC is in RPO mode will deactivate the RPO feature.

RPO is intended for resource management (such as virus cleaners, nightly backups, etc.), not for crisis management (thunderstorm recovery, etc.).

Advanced Power Management (APM)

APM is incorporated in Windows for Workgroups 3.11, Windows 95 andOS/2. A file called **power.exe** is needed for APM under DOS.

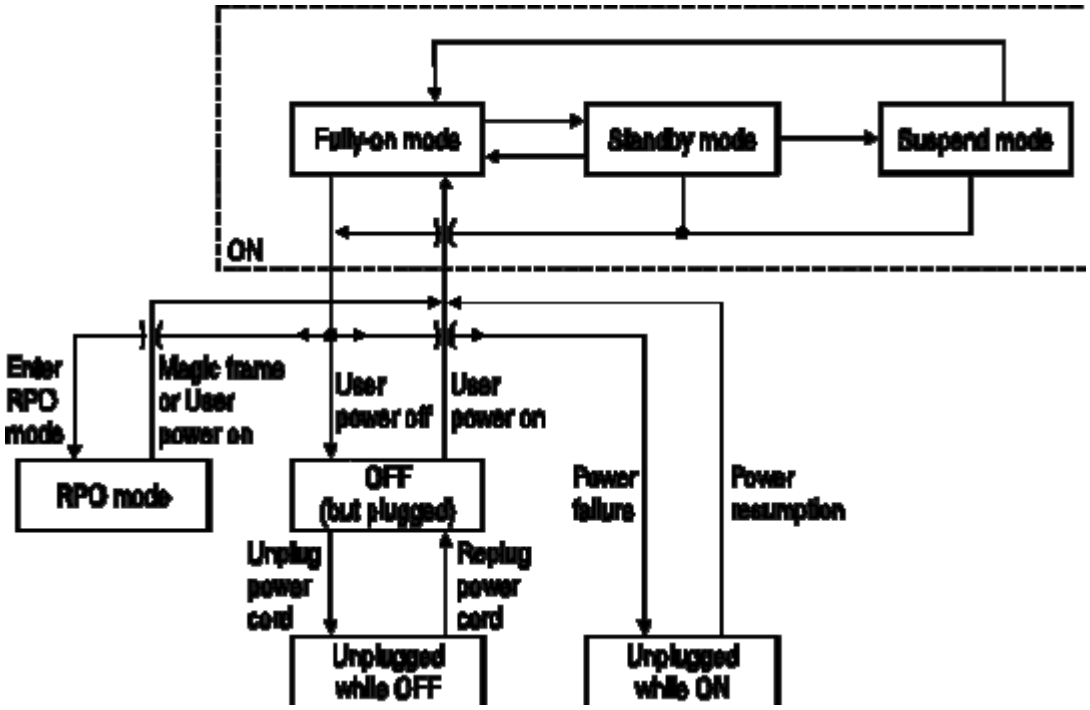
APM is a standard, defined by Intel and Microsoft, for a power-saving mode that is applicable under a wide range of operating systems. It consists of the following modes: *Fully-on*, *Standby*, *Suspend*, *Hibernation*, *Off*. Of these, APM 1.1 supports: *Fully-on*, *Standby*, *Suspend*, *Off*.

The *Suspend* mode, which used also to be known as *Sleep*, is now managed at the operating system level only, and by pressing the “sleep” icon. There is no longer the inter-activity between BIOS *Setup* and operating systems, and no longer a “sleep at” item in the desktop configuration menus, to avoid the BIOS from shutting down the system at the wrong moment.

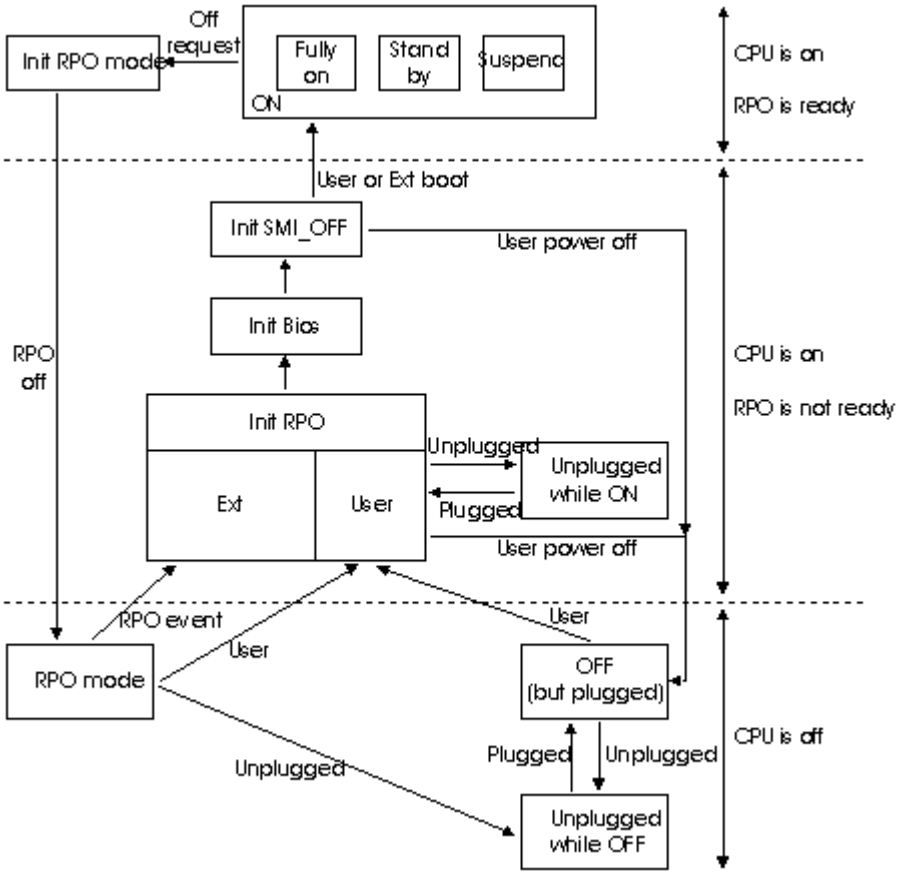
RPO defines a variation from the standard *Off* state. In *RPO* mode, the main CPU hardware is off while a RPO function is powered by a power supply called VStandby. VStandby is active as

soon as the PC is plugged in. RPO hardware can produce a triggering signal which turns on the PC.

The following diagram gives a simplified view of the useful states that the PC can be in: the three *On* states (*Fully-On*, *Standby* and *Suspend*), the *RPO* state (when the CPU is *Off*, and the RPO hardware is powered by VStandby), the *Off* state (when everything is powered off), and the state that is caused by power failure or unplugging the PC.



The following diagram gives a more accurate, more detailed account of the valid state changes. It highlights two limitations of the RPO system: power-off before the operating system boot procedure has initialized the RPO function, or a power failure whilst the system in RPO mode, will each de-activate the RPO function.



Little Ben

Little Ben is an HP application specific integrated circuit (ASIC) that is connected between the chipset and the processor. It has been designed to act as a companion to the Super I/O chip. It contains the following:

- hard and soft control for the power supply
- BIOS timer
  - hardware wired 50 ms long 880 Hz beep module
  - automatic blinker that feeds the LEDs module with a 1 Hz oscillator signal
- flash access and protection (supporting 128, 256 or 512 KB ROMs)
- Super I/O protection
- glue logic
  - support for SMIs (for Intel's SMM mode): enhanced keyboard lock, external wake-up
  - IRQ generator controlled by software
  - SMI generator controlled by software
  - programmable chip selects

Little Ben is powered by battery, so its consumption has to be as low as possible. When *VccState* and *PowerGood* pins are both low, all output pins are in tri-state mode, except for *RemoteOnBen* which continues to be driven. This allows the PC to be restarted even after a power loss has occurred.

If the BIOS needs to turn off the PC, it must ensure that the PC is not locked by Little Ben's lock bit. If it is, the power remains on, a red light is illuminated, and a buzzer is activated.

SMI_OFF is asserted if the Hard Soft Power Down Mode (HSPD) is enabled when Little Ben wants to turn off the computer (via the control panel or soft power down). The BIOS first performs some RPO initialization, and then proceeds to power down the computer. If the watch-dog timer detects that the BIOS is inactive (and not reloading the timer once every 6 seconds), the PC is turned off without further BIOS acknowledgment.

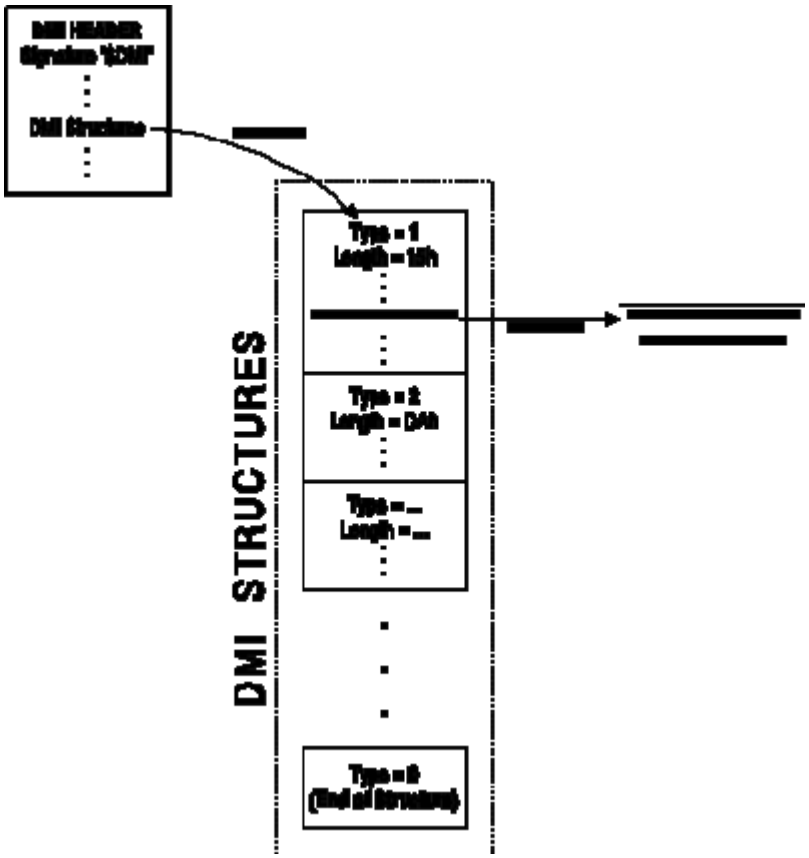
DESKTOP MANAGEMENT INTERFACE (DMI)

This BIOS presents a new method for storing and accessing information about the PC, called the Desktop Management Interface or DMI.

Administrators can use remote DMI to query and configure client *HP Vectra XM 5/xx series 4 PC*s, software, peripherals, manage passwords, and many other functions.

Overview of the DMI Information Structure

The system administrator uses the DMI to access information about the PC, such as the BIOS version number, the serial number, the processor type, and the size of the hard disk drive. This information is stored in the Management Information Format Database, or MIF.



Pointers are used to indicate the position of a table or a string value. The following rules apply to pointers:

- Pointers must never be zero. For empty strings, the pointer must point to a null (zero) value.
- Far pointers are in Intel (little-endian) format, with the segment in the high word and the offset in the low word.

All string values are terminated by a null (zero) value.

Accessing BIOS DMI Information

The BIOS information can be accessed as follows:

1 Locate the DMI header: Search for the “$DMI” signature in the segment E0000:0 or F0000:0.

2 Verify the check-sums: Refer to "Verifying the DMI Information Structure," in this chapter.

3 Locate the first sub-structure table using the far pointer given in the DMI header.

4 Walk through the tables to locate the desired table. Each table is identified by a unique type. The type is given by the first byte of the table. The length of the table is given by the second byte. The next table follows immediately after the current one.

5 Read off the required values. Each type of table has a pre-defined format. For a list of the major table types, refer to "DMI Sub-Structure Tables," in this chapter.

6 Use the pointer to retrieve string values: All string values are terminated by a null (zero) value.

Field	Offset	Length	Value
DMI Header Signature	0h	4 bytes	“$DMI”
Version	4h	1 byte	00010010 (Ver 1.2)
DMI Header Length	5h	1 byte	0Eh
Pointer to DMI structures	0Ah	4 bytes (DWORD)	Far pointer (variable)
Length of DMI structures	0Ch	2 bytes (WORD)	variable
Checksum of DMI structures	0Ch	1 byte	variable
Checksum of DMI header	0Dh	1 byte	variable

The DMI header is the starting point for all DMI information.

Verifying the DMI Information Structure

Before accessing the DMI tables, the check-sums must be verified to ensure the reliability of the information. The check-sum value of a structure can be calculated as follows:

1 Add together all the bytes of the structure.
2 Convert the value to negative.
3 Cast the value to a byte (take the low byte).

There are two check-sums, one for the DMI header and another for the remaining DMI structure. These two check-sums can be verified as follows:

1 Locate the DMI header.

2 Using the length value of the DMI header, calculate the check-sum value for the DMI header. (When adding together the bytes of the header, exclude the check-sum byte, offset 0Dh.)

3 Verify this value against the check-sum given for the DMI header.

4 Retrieve the position and length of the DMI structures.

5 Calculate the check-sum value for the DMI structures.

6 Verify this value against the check-sum given for the DMI structures.

DMI Sub-Structure Tables

Each type of table has a pre-defined format. Although the structure can evolve over time, new fields are always added to the end of the table and the length value reflects this new size.

To parse several tables in order to find a specific table, simply use the table length. Using this method will ensure that the parser can function even when the tables evolve over time.

To locate specific BIOS information, use the DMI sub-structure tables which are listed on the following pages.

Type 1 : BIOS Information

Field	Offset	Length	Value	Description
Type	0h	1 byte	1	BIOS information table
Length	1h	1 byte	15h	Table length (in bytes)
Vendor	2h	4 bytes (DWORD)	variable	Far pointer to string containing BIOS vendor name.
BIOS Version	6h	4 bytes (DWORD)	variable	Far pointer to string containing BIOS version number.
BIOS Starting Address	Ah	2 bytes (WORD)	variable	Segment location of BIOS starting address, i.e. E800h.
BIOS Release Date	Ch	4 bytes (DWORD)	variable	Far pointer to string containing BIOS release date.
BIOS Characteristics	10h	4 bytes (DWORD)	variable bit field	Bit field value indicating which functions the BIOS supports.
BIOS ROM Size	14h	1 byte	variable	Value indicating the size of the BIOS ROM: 0 → 64K, 1 → 128K, 2 → 256K, 3 → 512K, etc.

Type 2: Component ID

Field	Offset	Length	Value	Description
Type	0h	1 byte	2	Component ID table
Length	1h	1 byte	0Ah	Table length
Manufacturer	2h	2 bytes (WORD)	variable	Near pointer to string containing manufacturer's name.
Product	4h	2 bytes (WORD)	variable	Near pointer to string containing product name.
Version (Board Revision)	6h	2 bytes (WORD)	variable	Near pointer to string containing date code.
Serial Number	8h	2 bytes (WORD)	variable	Near pointer to string containing serial number.

Type 3: Processor Information

Field	Offset	Length	Value	Description
Type	0h	1 byte	3	Processor information table
Length	1h	1 byte	0Bh	Table length
Processor Type	2h	1 byte	ENUM	Value indicating processor type: 1 → Other 2 → Unknown 3 → Central Processor 4 → Math Processor 5 → DSP Processor 6 → Video Processor
Processor Family	3h	1 byte	ENUM	Value indicating processor family: 1 → Other 2 →Unknown 6 → 80486 A → 80487 B → Pentium 20 → Power PC
Processor Manufacturer	4h	2 bytes (WORD)	variable	Near pointer to string containing processor manufacturer's name.
Processor Version	6h	2 bytes (WORD)	variable	Near pointer to string describing the processor.
Max Speed	8h	2 bytes (WORD)	variable	Decimal value of maximum processor speed. Example: 166d for a 166 MHz processor.
Processor Upgrade	Ah	1 byte	ENUM	Value indicating processor upgrade type: 1 → Other 2 → Unknown 3 → Daughter Board 4 → ZIF Socket 5 → Replaceable Piggy Back 6 → None

HP-Specific DMI Sub-Structure Structures

Type 80h: HP ID

Field	Offset	Length	Value	Description
Type	0h	1 byte	80h	HP ID information table
Length	1h	1 byte	6	Table length
Signature	02h	2	"HP"	Hewlett-Packard signature
PC ID	04h	1 byte	variable	PC Identification
Capabilities	05h	1 byte	BITMAP	Bit 7=1 → Tatooing supported Bit 6=1 → PCMCIA device is present Bit 5=1 → Infrared is present Bit 4=1 → Two embedded serial ports present Bit 3=1 → Mini-Tower (1) or Desktop (0) Bit 2=1 → Embedded LAN present Bit 1=1 → Using integrated video Bit 0=1 → Supports HP LAN boot ROM

Type 81h: HP Configuration ID

Field	Offset	Length	Value	Description
Type	0h	1 byte	81h	HP Configuration table
Length	1h	1 byte	3	Table length
Serial/ Parallel Count	02h	1 byte	variable	Bits 7-4 → Number of integrated parallel ports Bits 3-0 → Number of integrated serial ports

Type 84h: HP System Information

Field	Offset	Length	Value	Description
Type	0h	1 byte	84h	HP system information table
Length	1h	1 byte	Eh	Table length
System Power-on Time	02h	2 bytes	variable	Short pointer to string containing date and time of last boot. Format: "ccyymmddHHMM" The value "**********" indicates RTC has failed.
Base Memory Size	04h	2 bytes	variable	Size of base memory in kilobytes
Extended Memory Size	06h	2 bytes	variable	Extended Memory size in 64 KB blocks
HP BIOS Version	08h	4 bytes	variable	Long pointer to string describing HP BIOS version
CPU Name	0Ch	2 bytes	variable	Short pointer to string describing CPU name

6 POWER-ON SELF-TESTS AND ERROR MESSAGES

This chapter describes the Power-On Self-Test (POST) routines, which are contained in the PC's ROM BIOS, the error messages which can result, and the suggestions for corrective action.

OVERVIEW

Each time the system is powered on, or a reset is performed, the POST is executed. The POST process verifies the basic functionality of the system components and initializes certain system parameters. The POST performs the tests in the order described in the following table.

The POST starts by displaying a graphic screen with the initial HP "Vectra" logo. If the POST detects an error, the error message is displayed inside a *view system errors* screen, in which the *error message utility* (EMU) not only displays the error diagnosis, but the suggestions for corrective action. Error codes are no longer displayed.

To see the tests performed during the POST, press [ESC] when the initial HP "Vectra" logo appears, and the display will switch to text mode. In this mode, a summary configuration screen will be displayed at the end of the POST. Pressing the PAUSE/BREAK key at any time will allow you to inspect the screen contents. Press any key to resume.

Devices, such as memory and hard disks, are configured automatically. The user is not requested to confirm the change. However, the user is prompted if a device is found to have gone missing since the previous boot. The user can simply accept the new configuration by pressing [F4]. Note, though, that the POST does not detect when a *slave hard disk drive* ("HDD 1" or "HDD 3" in the *Setup*) has been installed or changed.

During the POST, the BIOS and other ROM data is copied into high-speed shadow RAM. The shadow RAM is addressed at the same physical location as the original ROM in a manner which is completely transparent to applications. It therefore appears to behave as very fast ROM. This technique provides faster access to the system BIOS firmware.

The table on the following page lists the POST routines in the order in which they are executed (from the shadow RAM). If the POST is initiated by a soft reset [CTRL] [ALT] and [DELETE], the RAM tests are not executed and shadow RAM is not cleared. In all other respects, the POST executes in the same way following power-on or a soft reset.

Test	Description
System BIOS Tests	
LED Test	Tests the LEDs on the control panel.
Processor Test	Tests the processor's registers. Test failure causes the boot process to abort.
System (BIOS) ROM Test	Calculates an 8-bit checksum. Test failure causes the boot process to abort.
RAM Refresh Timer Test	Tests the RAM refresh timer circuitry. Test failure causes the boot process to abort.
Interrupt RAM Test	Checks the first 64 KB of system RAM used to store data corresponding to various system interrupt vector addresses. Test failures cause the boot process to abort.
Shadow the System ROM BIOS	Tests the system ROM BIOS and shadows it. Failure to shadow the ROM BIOS will cause an error code to display. The boot process will continue, but the system will execute from ROM. This test is not performed after a soft reset (using [CTRL] [ALT] and [DELETE]).
Load CMOS Memory	Checks the serial EEPROM and returns an error code if it has been corrupted. Copies the contents of the EEPROM into CMOS RAM.
CMOS RAM Test	Checks the CMOS RAM for start-up power loss, verifies the CMOS RAM checksum(s). Test failure causes error codes to display.
Internal Cache Memory Test	Tests the processor's internal level-one cache RAM. Test failure causes an error code to display and the boot process to abort.
Video Tests	
Initialize the Video	Initializes the video subsystem, tests the video shadow RAM, and, if required, shadows the video BIOS. A failure causes an error code to display, but the boot process continues.
System Board Tests	
Test External Cache	Tests the level-two cache. A failure causes an error code to display and disables the external cache.
Shadow SCSI ROM	Tests for the presence of HP SCSI ROMs. If SCSI ROMs are detected, their contents are copied into the shadow RAM area. A failure will cause an error code to display.
8042 Self-Test	Downloads the 8042 and invokes the 8042 internal self-test. A failure causes an error code to display.
Timer 0/Timer 2 Test	Tests Timer 0 and Timer 2. Test failure causes an error code to display.
DMA Subsystem Test	Checks the DMA controller registers. Test failure causes an error code to display.
Interrupt Controller Test	Tests the Interrupt masks, the master controller interrupt path (by forcing an IRQ0), and the industry-standard slave controller (by forcing an IRQ8). Test failure causes an error code to display.
Real-Time Clock Test	Checks the real-time clock registers and performs a test that ensures that the clock is running. Test failure causes an error code to display.

Memory Tests	
RAM Address Line Independence Test	Verifies the address independence of real-mode RAM (no address lines stuck together). Test failure causes an error code to display.
Size Extended Memory	Sizes and clears the protected mode (extended) memory and writes the value into CMOS bytes 30h and 31h. If the system fails to switch to protected mode, an error code is displayed.
Real-Mode Memory Test (First 640KB)	Read/write test on real-mode RAM. (This test is *not* done during a reset using [CTRL] [ALT] and [DELETE]). The test checks each block of system RAM to determine how much is present. Test failure of a 64 KB block of memory causes an error code to display, and the test is aborted.
Shadow RAM Test	Tests shadow RAM in 64 KB segments (except for segments beginning at A000h, B000h, and F000h). If they are *not* being used, segments C000h, D000h and E000h are tested. Test failure causes an error code to display.
Protected Mode RAM Test (Extended RAM)	Tests protected RAM in 64 KB segments above 1 MB. (This test is *not* done during a reset using [CTRL] [ALT] and [DELETE]). Test failure causes an error code to display.
Keyboard / Mouse Tests	
Keyboard Test	Invokes a built-in keyboard self-test of the keyboard's microprocessor and tests for the presence of a keyboard and for stuck keyboard keys. Test failure causes an error code to display.
Mouse Test	If a mouse is present, invokes a built-in mouse self-test of the mouse's microprocessor and for stuck mouse buttons. Test failure causes an error code to display.
Tests of Flexible Disk Drive A	
Flexible Disk Controller Subsystem Test	Tests for proper operation of the flexible disk controller. Test failure causes an error code to display.
Coprocessor Tests	
Internal Numeric Coprocessor Test	Checks for proper operation of the numeric coprocessor part of the processor. Test failure causes an error code to display.
Parallel Port Tests	
Parallel Port Test	Tests the integrated parallel port registers, as well as any other parallel ports. Test failure causes an error code to display.
Serial Port Tests	
Serial Port Test	Tests the integrated serial port registers, as well as any other serial ports. Test failure causes an error code to display.
Hard Disk Drive Tests	
Hard Disk Controller Subsystem Test	Tests for proper operation of the hard disk controller. Test failure causes an error code to display. The test does not detect hard disk replacement or changes in the size of the hard disk.

System Configuration Tests	
System Generation	Initiation of the system generation (SYSGEN) process, which compares the configuration information stored in the CMOS memory with the actual system. If a discrepancy is found, an error code will be displayed.
Plug and PlayConfiguration	Configures any Plug and Play device detected (either PCI or ISA): • All PCI devices, and any ISA device necessary for loading the operating system will be configured for use. • Any ISA device that is not required for loading the operating system, will be initialized (prepared for loading of a device driver), but not fully configured for use.

BEEP CODES

If a terminal error occurs during POST, the system issues a beep code before attempting to display the error. Beep codes are useful for identifying the error when the system is unable to display the error message.

Beep Code*	Numeric Code	Description
1-2-2-3	16h	BIOS ROM checksum failure
1-3-1-1	20h	DRAM refresh test failure
1-3-1-3	22h	8742 Keyboard controller test failure
1-3-4-1	2C	RAM failure
1-3-4-3	2E	RAM failure on data bits in low byte of memory bus
1-4-1-1	30	RAM failure on data bits in high byte of memory bus
2-1-2-3	46	ROM copyright notice check failure
2-2-3-1	58	Unexpected interrupts test failure
1-2	98	Video configuration failure or Option ROMs checksum failure
1	B4	This does not indicate an error. There is one short beep before system startup.

*Values indicate number and relative length of beep signals. For example, 1-2-2-3 is one long beep, followed by two short beeps, followed by another two short beeps, and finally three short beeps.

ERROR MESSAGES

When the PC is switched on or reset, a power-on hardware test is performed. If an error occurs, an error message is displayed.

HP's new style BIOS does not display POST error codes (such as 910B) which existed in the BIOS of previous HP Vectra PCs.

Message	**Corrective Action and/or Explanation**
Operating system not found	Check whether the disk, HDD, FDD or CD-ROM disk drive is connected. If it is connected, check that it is detected by *Setup.*Check that your boot device is enabled on the *Setup* Security menu. If the problem persists, check that the boot device contains the operating system.
Missing operating system	If you have configured HDD user parameters, check that they are correct. Otherwise, use HDD type "Auto" parameters.
Failure fixed disk (preceded by a 30" time-out)	Check that HDD is connected. Check that HDD is detected in *Setup.*Check that boot on hard disk drive is enabled in *Setup*.
Diskette Drive A (or B) error	Check whether the diskette drive is connected. Check *Setup* for the configuration.
System battery is dead	You may get this message if the PC is disconnected for a few days. When you Power-on the PC, run *Setup* to update the configuration information. The message should no longer be displayed. Should the problem persist, replace the battery.
Keyboard error	Check that the keyboard is connected.
Resource Allocation Conflict -PCI device 0079 on motherboard	Clear CMOS.
Video Plug and Play interrupted or failed. Re-enable in Setup and try again	You may have powered your PC Off/On too quickly and the PC turned off Video plug and play as a protection.
System CMOS checksum bad - run Setup	CMOS contents have changed between 2 power-on sessions. Run *Setup* for configuration.
I/O device IRQ conflict	Serial ports A and B may have been assigned the same IRQ. Assign a different IRQ to each serial port and save the configuration.
No message, system "hangs" after POST	Check that cache memory and main memory are correctly set in their sockets.
Other	An error message may be displayed and the PC may "hang" for 20 seconds and then beep. The POST is probably checking for a mass storage device which it cannot find and the PC is in Timeout Mode. After Timeout, run *Setup* to check the configuration.