HEWLETT® PACKARD

Technical Reference Manual Hardware and BIOS

HP Net Vectra PC

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Preface

This manual is a technical reference and BIOS document for engineers and technicians providing system level support. It is assumed that the reader possesses a detailed understanding of AT-compatible microprocessor functions and digital addressing techniques.

Technical information that is readily available from other sources, such as manufacturer's proprietary publications, has not been reproduced.

This manual contains summary information only. For additional reference material, refer to the bibliography, on the next page.

Conventions

The following conventions are used throughout this manual to identify specific numeric elements:

- Hexadecimal numbers are identified by a lower case h.
  For example, 0FFFFFFFh or 32F5h
- Binary numbers and bit patterns are identified by a lower case b.
  For example, 1101b or 10011011b

Bibliography

- ❒ HP Net Vectra *User's Guide* (D5470-90001).
- ❒ HP Net Vectra *Upgrading and Maintaining the PC* (available on WWW).
- ❒ HP Net Vectra *Recovery Guide* (available on WWW).
- ❒ HP Net Vectra *Familiarization Guide* (D5470-90901).
- ❒ HP Net Vectra *Online User's Guide* (online).
- ❒ *Exploring your* HP Net Vectra *PC* (online).
- ❒ HP *Network Administrator's Guide* (online).
- ❒ HP Vectra *Accessories Service Handbook - 7th edition* (5965-4074).
- ❒ HP Vectra *PC Service Handbook (Volume 1) - 12th edition* (to be announced).
- ❒ HP *Support Assistant* CD-ROM (by subscription).

The following Intel® publication provides more detailed information:

- ❒ *Pentium Microprocessor Data Sheet* (241595-002)

Contents

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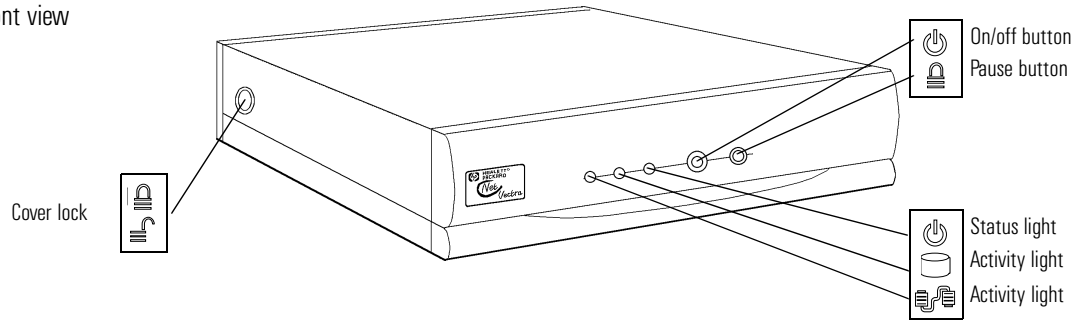
System Overview

This manual describes the *HP Net Vectra PC*, and provides detailed system specifications.

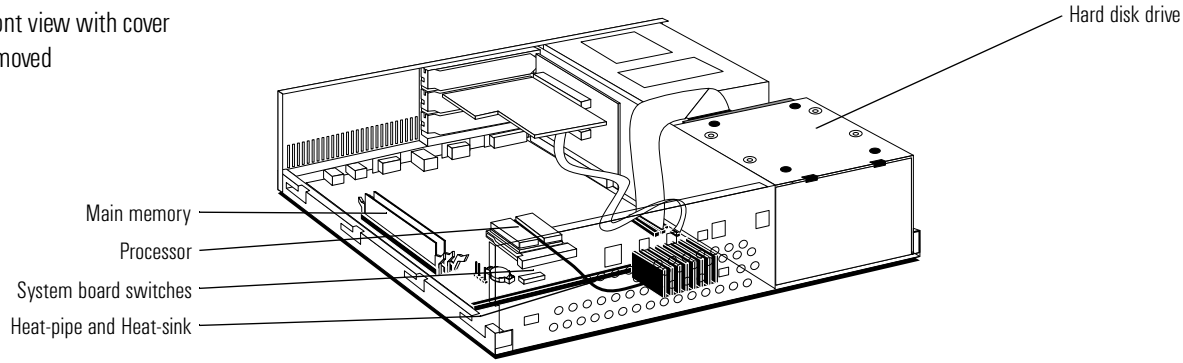
This chapter introduces the external features, and summarizes the documentation which is available.

Package

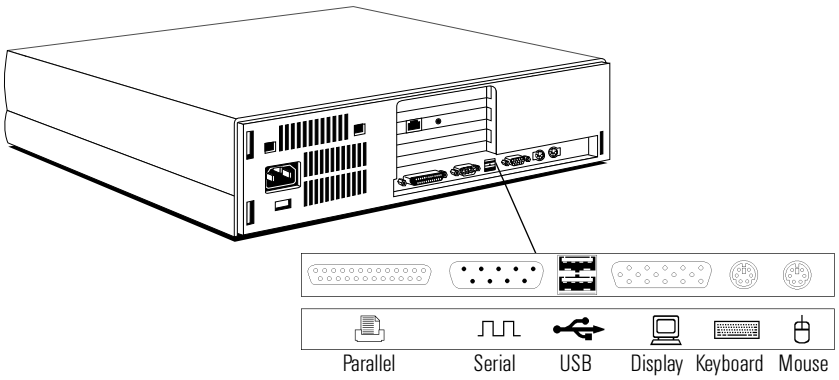
Front view



Front view with cover removed



Rear view



(All icons shown here are for information, and do not necessarily appear on the PC).

Documentation

The table below summarizes the availability of documentation that is appropriate to the *HP Net Vectra PC*. Most are available as viewable files (which can also be printed) from the HP division support servers, and on the *HP Support Assistant* CD-ROM.

	Preloaded on Hard Disk	Division Support Server	Support Assistant CD-ROM	Paper-based
HP Net Vectra User's Guide	no	PDF file	PDF file	D5470-90901
HP Net Vectra: Upgrading and Maintaining the PC	no	PDF file	PDF file	no
HP Net Vectra Recovery Guide	no	PDF file	PDF file	no
HP Net Vectra Familiarization Guide	no	PDF file	PDF file	D5470-90901
HP Net Vectra Technical Reference Manual	no	PDF file	PDF file	no
HP Vectra PC Service Handbook (Vol 1, 12th Edition)	no	PDF file	PDF file	To be announced
HP Vectra Accessory Service Handbook (7th Edition)	no	PDF file	PDF file	5965-4074
HP Net Vectra Online User's Guide	HTML file	PDF file	PDF file	no
Exploring your HP Net Vectra PC	no	PDF file	PDF file	no
Network Administrators Guide	no	PDF file	PDF file	no

Each PDF file (portable document format) can be viewed on the screen by opening it with Acrobat Reader. To print the document, press Ctrl+P whilst you have the document on the screen. You can use the page-up, page-down, goto page, search string functions to read the document on the screen. (Note, though, that for some documents there is difference between the page number that is printed on the page, and the page number that Acrobat Reader indicates, because of the presence of the front matter pages).

Where to Find the Information

The following table summarizes the availability of information within the *HP Net Vectra PC* documentation set. The user is supplied with the online documentation preloaded on the PC, and the User's Guide (in paper form). The remaining documents are available as an *MIS kit*, and can be downloaded from the HP WWW site.

	User Documentation			Online Documentation			Support Documentation		
	User's Guide	Upgrade Guide	Recovery Guide	User Online	Exploring Your PC	Network Admin. Guide	Familiar-ization Guide	Service Hand-book	Tech Ref Manual
Introducing the computer									
Product features									
Key features	x			x					x
Exploring				x	x				
New features							x		
Exploded view								x	
Parts list								x	
Product model numbers									
Product range								x	
CPL dates								x	
Using the computer									
Setting Up the PC									
Connecting cables	x								
Turning on	x								
Finding information									
READ.MEs									
On-line documentation									
Environmental									
System overview									x
Working in comfort				x	x				
Formal documents									
Sw license agreement	x			x	x				
Warranty information	x								
Upgrading the computer									
Opening the computer		x							
Supported accessories									
Full PN details								x	
Selected PN details									
Replacing accessories									
Complete procedures									
Selected procedures		x					x		

	User Documentation			Online Documentation			Support Documentation		
	User's Guide	Upgrade Guide	Recovery Guide	User Online	Exploring Your PC	Network Admin. Guide	Familiar-ization Guide	Service Hand-book	Tech Ref Manual
Configuring devices									
Peripherals				x	x				
Network						x			
Problem fixes									x
The *Setup* program									
Key fields									x
Repairing the computer									
Troubleshooting									
Basic	x	x							
Advanced									x
New symptoms							x		
Service notes								x	
Technical information									
Basic		x							
Detailed				x	x				
Advanced									x
System board									
Jumpers & Switches		x					x	x	x
Connectors		x					x	x	x
Replacement							x		
Chip-set									x
BIOS									
Basic details		x							
Technical details									x
Memory maps									x
Upgrading							x		x
Power-On Self-Test									
Key error conditions		x							x
Order of tests									x

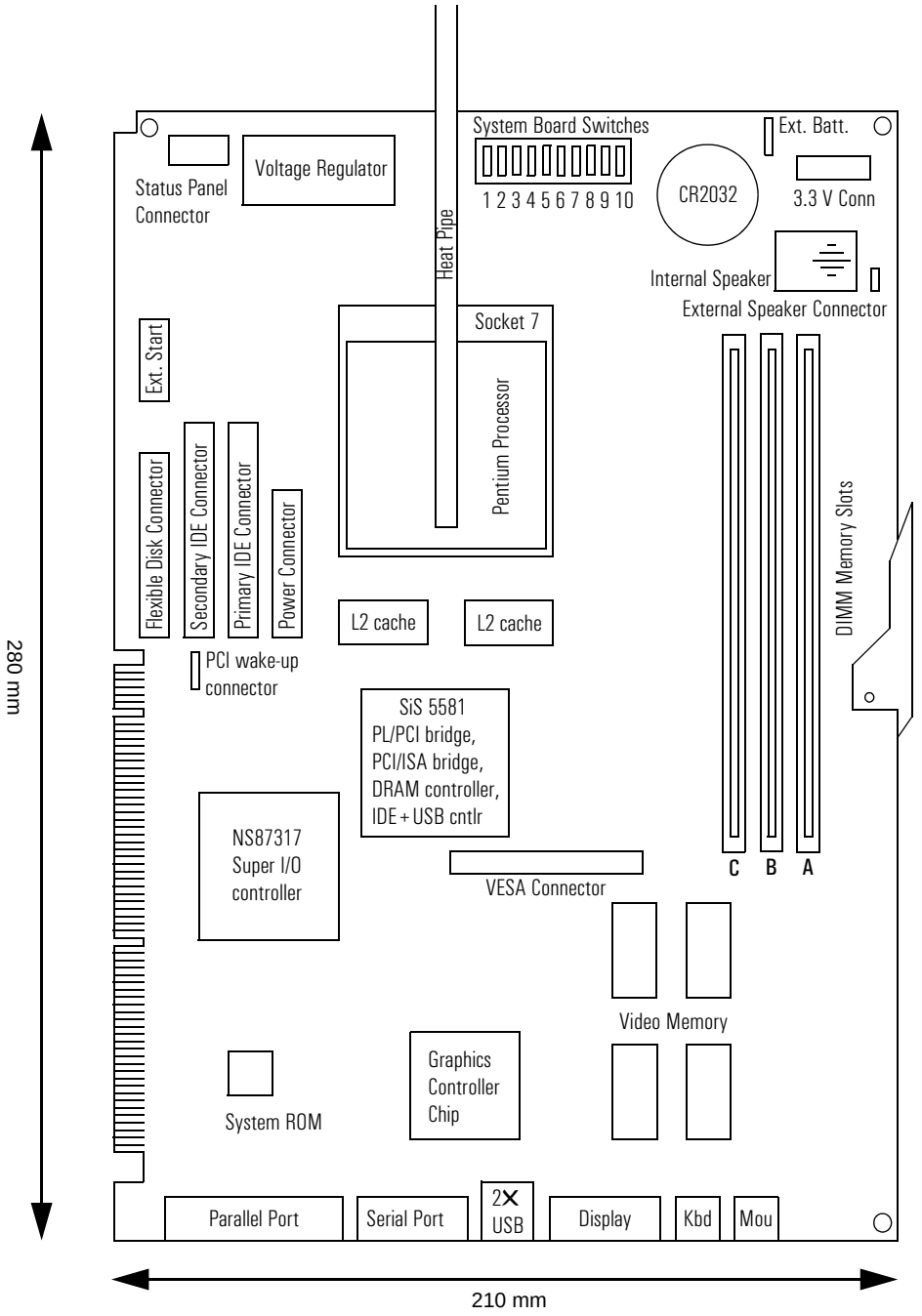
2

System Board

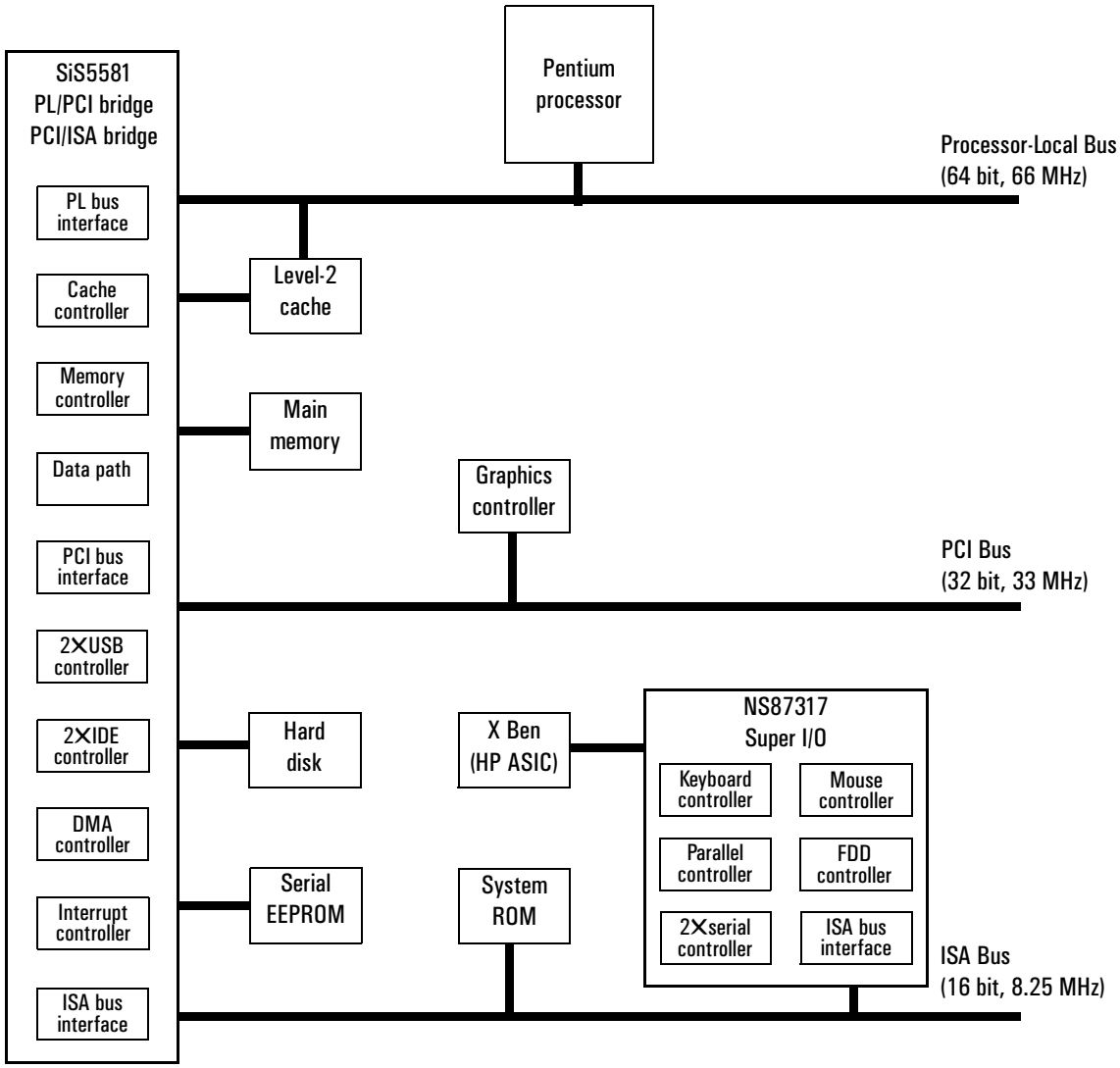
The next chapter describes the graphics, disk and network devices which are supplied with the computer.

This chapter describes the components of the system board, taking in turn the components of the Processor-Local Bus, the Peripheral Component Interconnect (PCI) bus and the Industry Standard Architecture (ISA) bus.

System Board



Architectural View



Chip-Set

The chip-set comprises two chips. These interface between the three main buses (the Processor-Local bus, the PCI bus and the ISA bus).

- The Bridge chip (SiS5581) is a combined *PL/PCI bridge* and *cache controller* and *main memory controller* and *PCI/ISA bridge* and *IDE controller* and *USB controller*.
- The Super I/O chip (NS87317) is a combined *serial interface* and *parallel interface* and *keyboard controller* and *mouse controller* and *flexible disk drive controller*.

Bridge Chip (SiS5581)

The bridges between the Processor Local Bus (PL Bus) and the PCI Bus, and between the PCI Bus and the ISA Bus, are encapsulated in a 553-pin ball grid array (BGA) package.

PL Bus Interface

The chip monitors each cycle that is initiated by the processor, and forwards those to the PCI bus that are not targeted at the local memory. It translates PL bus cycles into PCI bus cycles.

The chip supports the SMM mode of the Pentium processor, the CPU stop clock hardware function, and the keyboard lock function. These are used by the X-Ben chip, as described on page 51.

PCI Bus Interface

The chip is PCI 2.1 compliant, and provides for *PCI Concurrency*. Concurrent data transfers that do not contest for the same resources (such as processor to memory concurrent with PCI peer to peer, or processor to ISA device concurrent with PCI device to memory) are allowed to interleave their transfers.

The PCI arbiter supports PCI bus arbitration for up to four masters using a rotating priority mechanism. Its hidden arbitration scheme minimizes arbitration overhead.

ISA Bus Interface

As well as accepting cycles from the PCI bus interface, and translating them for the ISA bus, the ISA bus interface also requests the PCI master bridge to generate PCI cycles on behalf of a DMA or ISA master. The ISA bus interface contains a standard ISA bus controller and data buffering logic, and can

support up to four ISA slots without any external buffering.

Data Path

Storage elements are provided for bidirectional data buffering among the 64-bit PL data bus, the 64-bit memory data bus, and the 32-bit PCI address/data bus. This buffering is used, partly, to smooth the differences in bandwidths between the three buses, thereby improving the overall system performance.

Level-2 Cache Memory Controller

The Level-2 cache memory controller supports either *write through* or *write back* direct mapped pipelined burst static RAM. On the *HP Net Vectra PC*, 256KB of *write back* cache memory is implemented as two 32K × 32-bit chips soldered on the system board. An 8-bit tag is implemented in a separate 32K × 8-bit, 15 ns static RAM, and allows the lowermost 64 MB of main memory to be cached (if more than 64 MB of main memory is installed, accesses to the uppermost regions will be made directly to the main memory modules, and not via the cache memory mechanism).

The cache memory line width is 32-bytes (256-bits), four times the width of the Processor-Local data bus. Reads and writes always involve a full cache line, and so require four back-to-back cycles on the bus. Since they involve accesses to related addresses, they do not need four independent accesses to main memory, but can be organized as a pipelined burst. The second, third and fourth cycles in each burst require less time to complete than the first, the first cycle having included the addressing phase and memory pre-charge timing. The read and write access timing has the pattern 3-1-1-1. However, the timing for 64-byte burst reads can be even better than this (3-1-1-1,1-1-1-1 for a back-to-back burst read) provided that the main memory banks have been filled contiguously.

There are two programmable non-cacheable regions, with an option to disable local memory in these regions. A 64 KB to 1 MB cache summary is provided.

Main Memory Controller

The main memory controller supports up to 384 MB of EDO, FPM or SDRAM double interline memory modules (DIMMs). The *HP Net Vectra PC* supports three modules of SDRAM (synchronous dynamic random access memory). With the 64 MB module from HP, this gives a maximum total capacity of 192 MB.

In the case of 66 MHz PL bus operation, memory accesses have a timing pattern of 5-2-2-2 for a page-hit. This degrades to 8-2-2-2 for a row-miss, and to 11-2-2-2 for a page-miss. When the banks have been filled in an

arbitrary order, back-to-back burst reads keep to the 5-2-2-2,5-2-2-2 timing pattern. When the banks have been filled contiguously (bank A, then bank B, then bank C), back-to-back burst reads are improved to a 5-2-2-2,3-2-2-2 timing pattern.

IDE Controller

The PCI master/slave IDE controller, supporting four devices, two on each of two channels, is described on page 26. As well as the traditional five PIO modes (0 to 4) and three DMA modes (0 to 2), this controller also supports three Ultra ATA/33, or Ultra DMA, modes (0 to 2), allowing peak transfer rates up to 33 MB per second.

USB Controller

The PCI USB controller, supporting two connectors, is described on page 28.

DMA Controller

The seven channel DMA controller incorporates the functionality of two 82C37 DMA controllers. Channels 0 to 3 are for 8-bit DMA devices, while channels 5 to 7 are for 16-bit devices (as described on page 57). The channels can be programmed for any of the four transfer modes: the three active modes (single, demand, block), can perform three different types of transfer: read, write and verify. The address generation circuitry can only support a 24-bit address for DMA devices.

Interrupt Controller

The sixteen channel interrupt controller incorporates the functionality of two 82C59 interrupt controllers. The two controllers are cascaded, giving 14 external and two internal interrupt sources (as described on page 58).

Counter / Timer

The chip contains a three-channel 82C54 counter/timer. The counters use a division of the 14.318 MHz OSC input as the clock source.

Super I/O Chip (NS87317)

The Super I/O chip is contained within a 160-pin PQFP package. It includes the following features:

- ACPI register set
- Five Power-On/SCI/SMI channels
- Two SMI channels
- Signal line to an external light
- Power-State bit for PIIX4-based designs.

The chip provides the control for the following devices.

Function	Logical device number
Keyboard controller	0
Mouse controller	1
RTC and Advance power supply controller (APC)	2
Flexible disk controller	3
Parallel port controller	4
UART2 and IR controller	5
UART1 controller	6
General purpose I/O (GPIO)	7
Power management	8

Serial / parallel communications ports

The 9-pin serial port (whose pin layout is depicted on page 42) supports RS-232-C and is buffered by a 16550 UART, with a 16 Byte FIFO. It can be programmed as COM1, COM2, COM3, COM4, or disabled.

The 25-pin parallel port (also depicted on page 42) is Centronics compatible, supporting IEEE 1284. It can be programmed as LPT1, LPT2, or disabled. It can operate the four modes:

❒ Standard mode (PC/XT, PC/AT, and PS/2 compatible).
❒ Bidirectional mode (PC/XT, PC/AT, and PS/2 compatible).
❒ Enhanced mode (enhanced parallel port, EPP, compatible).
❒ High speed mode (MS/HP extended capabilities port, ECP, compatible).

FDC

The integrated *flexible drive controller* (FDC) supports any combination of two from the following: tape drives, 3.5-inch flexible disk drives, 5.25-inch flexible disk drives. It is software and register compatible with the 82077AA, and 100% IBM compatible. It has an A and B drive-swapping capability and a non-burst DMA option.

Keyboard and Mouse Controller

The computer has an 8042-based keyboard and mouse controller. The connector pin layouts are shown on page 42. The Power-on keyboard is described on page 29.

RTC

The real-time clock (RTC) is 146818A-compatible. With an accuracy of 20 ppm (parts per million). The configuration RAM is implemented as 256 bytes of CMOS memory.

Serial EEPROM

This is the non-volatile memory which holds the values for the *Setup* program (they are no longer stored in the CMOS memory).

ACPI Support

The Advanced Configuration and Power Interface (ACPI) provides a system-wide approach to system and device power management that allows the PC to be turned off, and yet remain sufficiently active to respond immediately to user and network requests.

General Purpose I/O

There are several general purpose I/O pins. Some of these are used on the *HP Net Vectra* to sense the current settings of system board switches (as described on page 24 and page 31).

Description	GPIO number
Cache-sleep	GPIO0
Screen blank	GPIO1
Error light	GPIO2
MA12	GPIO3
MA13	GPIO4
not connected	GPIO5
Low power mode	GPIO6
Clear product ID (connected to SW-10, open = 1, closed = 0)	GPIO7
USB fuse	GPIO8
IOCHK#	GPIO9
Thermal input (OVERTEMP)	GPIO10
Fan control (not used)	GPIO11
Remote wake up (RWO)	GPIO12
Keyboard and mouse lock (keyboard OR mouse IRQ)	GPIO13
Pause light	GPIO14
Remote power on (RPO)	GPIO15
Start key (connected to SW-9, open = 1, closed = 0)	GPIO16

Description	GPIO number
Enable RPO	GPIO17
Flash page select	GPIO20
Bus core frequency BCF2 (connected to SW-5, always 1)	GPIO21
POR# (ExtSMI)	GPIO22
Flash program enable (FLASHLOCK)	GPIO23
Backplane ID0 (always 1)	GPIO24
Backplane ID1 (always 1)	GPIO25
Bus core frequency BCF0 (connected to SW-3, open = 1, closed = 0)	GPIO26
Bus core frequency BCF1 (connected to SW-4, open = 1, closed = 0)	GPIO27
Host bus request detect (60/66 MHz) (connected to SW-1, always 0)	GPIO30
Serial EEPROM data	GPIO31
FDD write protect (not used)	GPIO32
Password enable (connected to SW-7, open = 1, closed = 0)	GPIO33
Clear CMOS (connected to SW-8, open = 1, closed = 0)	GPIO34
Serial EEPROM chip select	GPIO35
Serial EEPROM clock	GPIO36

Devices on the Processor-Local Bus

The Intel Pentium Microprocessor

The Pentium processor is packaged in a *pin-grid-array* (PGA), and is seated on the system board in a *zero-insertion-force* (ZIF) *socket 7*. Only upgrades that are pin compatible with the original processor, manufactured by Intel, are supported.

P54CS chips working at 166 and 200 MHz require between 3.45 and 3.60 V. A VRE voltage regulator, integrated on the system board, actively derives the voltage from the 3.3 V, 5 V and 0 V outlets of the power supply.

Processor Cooling

The processor is cooled by two heat-sinks: one on the processor (as normal), the other beside the system board. Surplus heat is carried from the first to the second by a heat pipe.

Since it involves no moving mechanical parts, it is unlikely to fail, and so involves no new support strategy.

Any thermal contact material between the parts and the heat-sinks must not be removed or disturbed. The cooling needs of the processor are critical.

Bus Frequencies

The location of the system board switches is shown in the diagram on page 16. Five of these switches (SW-1,2,3,4 and 5) determine the working frequencies of the PC, as summarized in the table below. The uses of the other switches are summarized on page 31.

There is a 14.318 MHz crystal oscillator on the system board. This frequency is multiplied to 66 MHz by a phase locked loop. This is further scaled by an internal clock multiplier within the processor. For example, the 200 MHz processor multiplies the 66 MHz system clock by three. Switches 1 and 2, on the system board switch bank, set the frequency of the Processor-Local bus. Switches 3, 4 and 5 set the clock multiplier ratio. The PCI bus works, synchronously, at half the frequency of the PL bus. The ISA bus works, synchronously, at a quarter of the frequency of the PCI bus.

You will need to change these switches if you exchange or replace the system board during a repair, so as to match the speed to that of the processor. You will not need to change the switches if you upgrade the original processor using the correct Intel Overdrive. No other types of processor upgrade are supported by HP.

Processor Frequency	Switch		Local Bus Frequency	Switch			Frequency Ratio Processor : Local Bus
	1	2		3	4	5	
166 MHz	Closed	Open	66 MHz	Closed	Closed	Open	2.5 : 1
200 MHz	Closed	Open	66 MHz	Open	Closed	Open	3 : 1
233 MHz[1]	Closed	Open	66 MHz	Open	Open	Open	3.5 : 1
266 MHz[1]	Closed	Open	66 MHz	Closed	Open	Closed	4 : 1

1. Switch settings if these processor frequencies become available (MMX technology only).

Cache Memory

The computer supports two levels of cache memory, each with a 32-byte line width. The Level-1 (L1) cache memory is fabricated on the processor chip. The Level-2 (L2) cache memory is a slower module on the system board. Each acts as temporary storage for data and instructions from the main memory. Since the system is likely to use the same, or adjacent, data several times, it is faster to get it from the on-chip or on-board cache memory than from the main memory.

The L1 cache memory is divided into two separate banks: an L1 I-cache for instruction words, and an L1 D-cache for data words. Each has a capacity of 8 KB.

The L2 cache memory is controlled by the Bridge chip in the system board chip-set. On the *HP Net Vectra PC*, 256 KB of direct mapped, write-back, synchronous *pipelined burst*, 8.5 ns static random access memory (SRAM) is integrated on the system board.

Main Memory

There are three main memory module sockets, arranged in three banks (A to C). One bank is already occupied by the *double interline memory module* (DIMM) that contains the 16 MB or 32 MB of memory that is supplied with the computer.

Different banks can have different capacities (8, 16, 32 or 64 MB). The banks should be filled in the order A, B, C. By installing a 64 MB DIMM in every bank, the maximum capacity of 192 MB of main memory can be attained.

Devices on the PCI Bus

PCI Device	Device Name	Device Number	Function	AD[xx]	Chip-set Interrupt Connection			
					INTA	INTB	INTC	INTD
PL/PCI bridge	Chip-set	0 (00h)	0	11	—	—	—	—
PCI/ISA bridge		1 (01h)	0	26	—	—	—	—
IDE controller			1		—	—	—	—
USB controller			2		—	—	—	—
Integrated graphics controller	S3 Trio 64V2	13 (0Dh)	0	24	A	—	—	—
PCI slot #1	J6	7 (07h)	—	18	A	B	C	D
PCI slot #2	J11	10 (0Ah)	—	21	D	A	B	C

The distribution of the interrupt lines is described more fully on page 59.

Integrated Drive Electronics (IDE)

The IDE controller is implemented as part of the Bridge chip. It is driven from the PCI bus, and has PCI-Master capability. It supports Ultra ATA (also known as Ultra DMA), Enhanced IDE (EIDE) and Standard IDE. To use the Enhanced IDE features the drives must be compliant with Enhanced IDE.

Up to four IDE devices are supported: two (one master and one slave) connected to the primary channel, and two (one master and one slave) to the secondary channel. A cable is supplied that provides a single connector for one device to one channel.

Transfer Rates Versus Modes of Operation

The controller supports 32-bit Windows I/O transfers. Five PIO modes, three DMA modes, and three Ultra ATA/33 modes are supported. The five supported PIO modes allow the following transfer rates.

Mode	0	1	2	3	4
Cycle time (ns)	600	383	240	180	120
Transfer rate (MB/s)	3.33	5.22	8.33	11.1	16.7

The three DMA modes (for single or double word) allow the following transfer rates:

Mode	0	1	2
Cycle time (ns)	480	150	120
Transfer rate (MB/s)	4.2	13.3	16.7

The three Ultra ATA/33 modes (also know as Ultra DMA modes) allow the following peak transfer rates:

Mode	0	1	2
Cycle time (ns)	144	75	60
Transfer rate (MB/s)	13.9	26.7	33.3

Disk Capacity Versus Modes of Addressing

The amount of addressable space on a hard disk is limited by three factors: the physical size of the hard disk, the addressing limit of the IDE hardware, and the addressing limit of the BIOS. By performing a translation, the Extended-CHS addressing scheme allows larger disk capacities to be addressed than under CHS.

	Cylinders per Device	Heads per Cylinder	Sectors per Track	Bytes per Sector	Bytes per Device
CHS	64	16	1024	512	528 M
ECHS	64	256	1024	512	8.4 G
LBA	-	-	256 M ($=2^{28}$)	512	137 G

Universal Serial Bus (USB) Controller

The OpenHCI USB controller (USB release 1.0) is implemented as part of the Bridge chip. It is driven from the PCI bus, and provides support for the two stacked USB connectors on the back panel. Over-current detection and protection is provided, but shared between the two ports. The specification is as follows:

- 12 M bps (bits per second) transfer rate
- Supports up to 127 devices (maximum)
- Isochronous and asynchronous data transfer support
- Up to 5 m per cable segment
- Built in power distribution
- Supports daisy-chaining through a tiered-star, multi-drop topology (up to 6 tiers)

USB works only if the USB interface has been enabled within the HP *Setup* program. Currently, only the Microsoft Windows 95 operating system provides support for the USB.

The Microsoft Supplement 2.1 software, which provides support of the Universal Serial Bus, can be obtained from the Hewlett-Packard World Wide Web site: **`http://www.hp.com/go/vectrasupport/`**

Devices on the ISA Bus

ISA Device	Index	Data
Super I/O	2Eh	2Fh
X Ben (HP ASIC)	496h	497h

Super I/O Controller

The *Super I/O* chip (NS87317) is part of the chip set, and is described on page 20.

The computer is supplied with a Logitech 2-button mouse, and a keyboard with the following features:

- ❒ Space bar power on, to start the computer from the *Off* state (if **`power on from keyboard`** is enabled in the *Setup* program).
- ❒ Windows key (next to the Alt keys), which has the same effect as clicking the "Start" button on the Windows 95 task bar.
- ❒ Pull-down key (next to the right Ctrl key), which has the same effect as clicking the right mouse button.

Serial EEPROM

The computer uses 4 Kbit of Serial EEPROM implemented within a single 512 K × 8-bit ROM chip. Serial EEPROM is ROM in which one byte at a time can be returned to its unprogrammed state by the application of appropriate electrical signals. In effect, it can be made to behave like very slow, non-volatile RAM. It is used for storing the tatoo string, the serial number, and the parameter settings for the *Setup* program.

When installing a new system board, the Serial EEPROM will have a blank serial number field. This will be detected automatically by the BIOS, which will then prompt the user to enter the serial number which is printed on the identification label on the back of the computer.

Flash EEPROM (the System ROM)

The computer uses 256 KB of Flash EEPROM implemented within a single 256 K × 8-bit ROM chip (or in two 128 K × 8-bit chips). Flash EEPROM is ROM in which the whole memory can be returned to its unprogrammed state by the application of appropriate electrical signals to its pins. It can then be reprogrammed with the latest firmware.

The System ROM contains: 64 KB of system BIOS (including the boot code, the ISA and PCI initialization, RPO, DMI, the *Setup* program and the Power-On Self-Test routines, plus their error messages); 32 KB of video BIOS; 32 KB of Plug-and-Play code; and 32 KB of power management code. The functions of these are summarized in Chapters 4 and 5.

Updating the System ROM

The System ROM can be updated with the latest BIOS. This can be downloaded, as a compressed file, from the *HP Electronic Services* (http://www.hp.com/go/vectrasupport). You must specify the model of the computer since the utility which is supplied for a different model cannot be used with this one. (More information is given in the "Hewlett-Packard Support and Information Services" chapter in the *User's Guide* that was supplied with the computer).

Since the PC does not have a flexible disk drive, the file is downloaded to the system administrator's PC and then to the target PC. The compressed file can be executed, causing it to be expanded, creating a number of files, including:

- the Flash EEPROM reprogramming utility programs, **`phlash32.exe`** and **`phlash.exe`**
- the BIOS upgrade file, **`HE0700xx.FUL`**
- the binary file, **`PFMHE106.bin`**
- the batch file, **`flash.bat`**
- a number of **`*.txt`** files, giving information about the new version of the BIOS, and instructions on how to install it.

The **`PHLASH32.EXE`** file is then executed from within the Windows NT operating system on the target PC.

Do not switch off the computer until the system BIOS update procedure has completed, successfully or not. To do so could cause irrecoverable damage to the ROM, thereby requiring the replacement of the system board. The control panel switches are automatically disabled to prevent accidental interruption of the flash programming process, but this, of course, does not protect against deliberate or inadvertent removal of the power cord, or other types of power failure, however caused.

If the flashing process goes wrong, isolate the PC from external connections, remove the cover, and connect an external flexible disk drive to the FDD connector on the system board. Insert a system diskette containing the new BIOS and its associated files. Close the “clear password” and “clear CMOS” switches (SW-7 and SW-8) on the system board, reconnect the PC and turn it on. This forces the PC to re-boot from the flexible disk drive. Once the recovery program has completed, the BIOS can be flashed by running the **PHLASH.EXE** program. Once completed, return the system board switches to their original positions, and disconnect the flexible disk drive.

System Board Switches

Five of the *system board switches* (whose location is shown on page 16) set the working frequencies for the computer, as summarized on page 24. The others set the configuration for the computer, as summarized in the following table.

Switch		Function	Default
1-5	-	Bus frequencies (see the table on page 24)	-
6	**Open**	**Not used**	**Open**
7	**Open**	**Normal operation**	**Open**
	Closed	Clears User and Administrator passwords	
8	**Open**	**Normal operation**	**Open**
	Closed	Clears CMOS (to reload the *Setup* program defaults)	
9	Open	Disables keyboard power-on	**Closed**
	Closed	**Normal operation**	
10	**Open**	**Normal operation**	**Open**
	Closed	Clears product identification field	

By setting switch SW8 in the **Closed** position, not only is the configuration data cleared (in the CMOS memory and the Serial EEPROM), but also all the Plug-and-Play data that had been saved in the Serial EEPROM. However, the serial number, the tattooing string, the date and the time are each retained.

By setting switch SW9 in the **Closed** position, the Power-On Space-Bar function is enabled. Note, though, that it must *also* be enabled in the **Power-On Space-Bar** field of the Power Menu in the *Setup* program.

Turning the computer on, with switch SW10 in the **Closed** position, clears the product identification field in the BIOS, and causes the computer to prompt for the new information. By identifying the product correctly (after replacing a defective system board by a new one), the BIOS is able to tailor itself for the particular product, and to enable the appropriate features.

Updating the BIOS Before Considering Replacing the System Board

If the computer is faulty, but it starts up correctly, and the fault is not clearly due to the system board hardware, then it is advisable to check the BIOS version number. The BIOS version number can be found from the summary screen, or the *Setup* program, obtained by pressing Esc or F2, respectively, when the computer has just been restarted, as described in Chapter 4.

If it is not the current version of the BIOS, the System ROM should be flashed with the new version, as described on the previous page. The computer should then be re-run to see if this has cleared the problem.

X-Ben

X-Ben is an HP application specific integrated circuit (ASIC), designed to be a companion to the Super I/O chip. It is described on page 51.

3

Interface Devices and Mass-Storage Drives

This chapter describes the graphics, mass storage and network devices which are supplied with the computer. It also summarizes the pin connections on the internal and external connectors.

S3 Trio 64V2 Graphics Controller Chip

All models are supplied with a graphics controller chip integrated on the system board. This 64-bit PCI Ultra VGA graphics controller can be characterized as follows:

- 100% compatible with IBM® VGA display standard
- 64-bit video memory access with 2 MB, 50 ns, EDO, video DRAM (this is not upgradeable since it is already fitted to capacity).
- integrated 24-bit RAMDAC
- fully programmable Pixel Clock Generator up to 170 MHz
- 60 MHz clock for video memory
- fast linear addressing with full software relocation
- green power saving features
- playback acceleration, continuous interpolation on X, continuous interpolation on Y
- DDC 2B compliant.

Video Modes

Standard and Enhanced Video Graphics Array (VGA) modes are available. Hardware acceleration of graphical user interface (GUI) operations is provided, and acceleration for 8, 16 and 32-bit pixel depths.

The table, on the following page, details the standard VGA modes which are currently implemented in the video BIOS. These modes are supported by standard BIOS functions. The video BIOS (which is mapped contiguously in the address range C0000h to C7FFFh) contains all the routines required to configure and access the graphics subsystem.

Standard VGA Modes

Mode No.	Standard	Interface Type	Resolution	No. of Colors	Vertical Refresh (Hz)	Horizontal Refresh (kHz)	Dot Clock (MHz)
00h	VGA	text	40 x 25 chars	b/w	70	31.5	25.175
00h*	VGA	text	40 x 25 chars	b/w	70	31.5	25.175
00h+	VGA	text	40 x 25 chars	b/w	70	31.5	28.322
01h	VGA	text	40 x 25 chars	16	70	31.5	25.175
01h*	VGA	text	40 x 25 chars	16	70	31.5	25.175
01h+	VGA	text	40 x 25 chars	16	70	31.5	28.322
02h	VGA	text	80 x 25 chars	b/w	70	31.5	25.175
02h*	VGA	text	80 x 25 chars	b/w	70	31.5	25.175
02h+	VGA	text	80 x 25 chars	b/w	70	31.5	28.322
03h	VGA	text	80 x 25 chars	16	70	31.5	25.175
03h*	VGA	text	80 x 25 chars	16	70	31.5	25.175
03h+	VGA	text	80 x 25 chars	16	70	31.5	28.322
04h	VGA	graphics	320 x 200	4	70	31.5	25.175
05h	VGA	graphics	320 x 200	4	70	31.5	25.175
06h	VGA	graphics	640 x 200	2	70	31.5	25.175
07h	VGA	text	80 x 25 chars	b/w	70	31.5	28.322
07h+	VGA	text	80 x 25 chars	b/w	70	31.5	28.322
0Dh	VGA	graphics	320 x 200	16	70	31.5	25.175
0Eh	VGA	graphics	640 x 200	16	70	31.5	25.175
0Fh	VGA	graphics	640 x 350	b/w	70	31.5	25.175
10h	VGA	graphics	640 x 350	16	70	31.5	25.175
11h	VGA	graphics	640 x 480	2	60	31.5	25.175
12h	VGA	graphics	640 x 480	16	60	31.5	25.175
13h	VGA	graphics	320 x 200	256	70	31.5	25.175

The extended modes supported by the video BIOS are listed in the table on the following page.

Extended Video Modes

Extended Mode No.	VESA Mode No.	Interface Type	Resolution	No. of Colors	Vertical Refresh (Hz)	Horizontal Refresh (kHz)	Dot Clock (MHz)
4Eh	207h	graphics	1152 x 864	256	60	55	80.000
4Fh	208h	graphics	1280 x 1024	8	60	63.7	110.000
51h	212h	graphics	640 x 480	16.7 M	60	31.5	25.000
52h	213h	graphics	640 x 400	16.7 M	70	31.5	25.000
54h	10Ah	text	132 x 43 chars	16	70	31.5	40.000
55h	109h	text	132 x 25 chars	16	70	31.5	40.000
65h	10Dh	graphics	320 x 200	32,768	70		12.540
66h	10Eh	graphics	320 x 200	65,536	70		12.540
67h	10Fh	graphics	320 x 200	16.7 M	70		12.540
68h	100h	graphics	640 x 400	256	70	31.5	25.175
69h	101h	graphics	640 x 480	256	60	31.5	25.175
69h	101h	graphics	640 x 480	256	72	37.9	31.500
69h	101h	graphics	640 x 480	256	75	37.5	31.500
69h	101h	graphics	640 x 480	256	85	45	36.000
6Ah	102h	graphics	800 x 600	16	60	37.9	40.000
6Ah	102h	graphics	800 x 600	16	72	48.1	50.000
6Ah	102h	graphics	800 x 600	16	75	47.5	49.500
6Ah	102h	graphics	800 x 600	16	85	53.6	56.000
6Bh	103h	graphics	800 x 600	256	60	37.9	40.000
6Bh	103h	graphics	800 x 600	256	72	48.1	50.000
6Bh	103h	graphics	800 x 600	256	75	46.8	49.500
6Bh	103h	graphics	800 x 600	256	85	53.6	56.000
6Ch	104h	graphics	1024 x 768	16	60	48.4	65.000
6Ch	104h	graphics	1024 x 768	16	70	56.5	75.000
6Ch	104h	graphics	1024 x 768	16	75	60.2	80.000
6Ch	104h	graphics	1024 x 768	16	85	68.7	95.000
6Dh	105h	graphics	1024 x 768	256	60	48.4	65.000
6Dh	105h	graphics	1024 x 768	256	70	56.5	75.000
6Dh	105h	graphics	1024 x 768	256	75	60.0	80.000
6Dh	105h	graphics	1024 x 768	256	85	68.7	95.000
6Eh	106h	graphics	1280 x 1024	16	60		110.000
6Fh	107h	graphics	1280 x 1024	256	60	65	55.000
6Fh	107h	graphics	1280 x 1024	256	72	77.7	65.000
6Fh	107h	graphics	1280 x 1024	256	75	79.5	67.000
70h	110h	graphics	640 x 480	32,768	60	31.5	25.175
70h	110h	graphics	640 x 480	32,768	72	37.5	31.500
70h	110h	graphics	640 x 480	32,768	75	37.5	31.500
70h	110h	graphics	640 x 480	32,768	85	45	36.000

Extended Mode No.	VESA Mode No.	Interface Type	Resolution	No. of Colors	Vertical Refresh (Hz)	Horizontal Refresh (kHz)	Dot Clock (MHz)
71h	111h	graphics	640 x 480	65,536	60	31.5	25.175
71h	111h	graphics	640 x 480	65,536	72	37.5	31.500
71h	111h	graphics	640 x 480	65,536	75	37.5	31.500
71h	111h	graphics	640 x 480	65,536	85	45	36.000
72h	112h	graphics	640 x 480	16.7 M	60	31.5	25.175
72h	112h	graphics	640 x 480	16.7 M	72	37.9	31.500
72h	112h	graphics	640 x 480	16.7 M	75	37.5	31.500
72h	112h	graphics	640 x 480	16.7 M	85	45	36.000
73h	113h	graphics	800 x 600	32,768	60	37.9	40.000
73h	113h	graphics	800 x 600	32,768	72	48.1	50.000
73h	113h	graphics	800 x 600	32,768	75	46.8	49.500
73h	113h	graphics	800 x 600	32,768	85	53.6	57.000
74h	114h	graphics	800 x 600	65,536	60	37.9	40.000
74h	114h	graphics	800 x 600	65,536	72	48.1	50.000
74h	114h	graphics	800 x 600	65,536	75	46.8	49.500
74h	114h	graphics	800 x 600	65,536	85	53.6	57.000
75h	115h	graphics	800 x 600	16.7 M	60	37.9	40.000
75h	115h	graphics	800 x 600	16.7 M	72	41.8	50.000
75h	115h	graphics	800 x 600	16.7 M	75	46.8	49.500
75h	115h	graphics	800 x 600	16.7 M	85	53.6	57.000
76h	116h	graphics	1024 x 768	32,768	60	48.9	65.000
76h	116h	graphics	1024 x 768	32,768	70	56.5	75.000
76h	116h	graphics	1024 x 768	32,768	75	60.2	80.000
76h	116h	graphics	1024 x 768	32,768	85	68.7	95.000
77h	117h	graphics	1024 x 768	65,536	60	48.9	65.000
77h	117h	graphics	1024 x 768	65,536	70	56.5	75.000
77h	117h	graphics	1024 x 768	65,536	75	60.2	80.000
77h	117h	graphics	1024 x 768	65,536	85	68.7	95.000
7Ch	120h	graphics	1600 x 1200	256	48.5i	62.00	67.000

Available Video Resolutions

The following table lists the available video resolutions using the current drivers. The available resolutions may be different with later versions of driver.

	Resolution	Number of colors	Refresh Rate (Hz)
Windows NT	640 x 480	16 256, 64K, 16M	60 60, 72, 75, 85
	800 x 600	256, 64K, 16M	60, 72, 75, 85
	1024 x 768	256, 64K	i43[1], 60, 70, 75, 85
	1280 x 1024	256	i45[1], 60, 75, 85
	1600 x 1200	256	i48[1], 60

[1.] Interlaced.

If Video Plug and Play is **`enabled`** in *Setup*, and a DDC monitor is detected, *Setup* will automatically configure the best refresh rate. For non DDC monitors, or when video Plug and Play is **`disabled`**, refresh rates can be changed in *Setup*.

The number of colors supported is limited by the graphics board and the video RAM. The resolution/refresh-rate combination is limited by a combination of the display, the graphics board, and the video RAM.

Connectors

The layout of the pins for the DB15 VGA socket is depicted on page 42.

The Video Electronics Standards Association (VESA) defines a standard video connector, variously known as the VESA *feature* connector, *auxiliary* connector, or *pass-through* connector. This connector (whose pin names are listed in a table on page 40) is integrated on the system board, and is connected directly to the pixel data bus and the synchronization signals.

The graphics controller supports an output-only VESA *feature* connector in VGA mode. It is disabled by default and must be enabled in the *Setup* program. Use of the VESA feature connector will disable 1 MB of the video memory; with access only to the remaining 1 MB of video memory, some of the video resolutions will not be available.

Mass-Storage Drives

A 3.5-inch hard disk drive is supplied on an internal shelf in all models. The IDE controller is described on page 26.

	1.6 GB IDE	1 GB IDE
HP product number	D2679A	D5190A
Manufacturer	Quantum	Quantum

Connectors and Sockets

IDE Hard Disk Drive Data Connector			
Pin	Signal	Pin	Signal
1	Reset#	2	Ground
3	HD7	4	HD8
5	HD6	6	HD9
7	HD5	8	HD10
9	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14
17	HD0	18	HD15
19	Ground	20	orientation key
21	DMARQ	22	Ground
23	DIOW#	24	Ground
25	DIOR#	26	Ground
27	IORDY	28	SPSYNC:CSEL
29	DMACK#	30	Ground
31	INTRQ	32	IOCS16#
33	DA1	34	PDIAG#
35	DA0	36	DA2
37	CS0#	38	CS1#
39	DASP#	40	Ground

Flexible Disk Drive Data Connector			
Pin	Signal	Pin	Signal
1	Ground	2	LDENSEL#
3	Ground	4	Microfloppy
5	Ground	6	EDENSEL
7	Ground	8	INDX#
9	Ground	10	MTEN1#
11	Ground	12	DRSEL0#
13	Ground	14	DRSEL1#
15	Ground	16	DTEN0#
17	Ground	18	DIR#
19	Ground	20	STP#
21	Ground	22	WRDATA#
23	Ground	24	WREN#
25	Ground	26	TRK0#
27	Ground	28	WRPRDT#
29	Ground	30	RDDATA#
31	Ground	32	HDSEL1#
33	Ground	34	DSKCHG#

Status Panel Connector			
Pin	Signal	Pin	Signal
1	LCK_LED_K	2	LCK_LED_A
3	PWR_LED_K	4	PWR_LED_A
5	not connected	6	common
7	Push_On	8	RED_LED_A
9	HDD_LED_K	10	HDD_LED_A
11	_Reset	12	Ground
13	LCK_PUSH2	14	LCK_PUSH2

External Start and Remote Start Connectors			
Pin	Signal	Pin	Signal
1	ExternalStart	2	Ground
3	Wake1#	4	Wake2#
5	not connected	6	Wake3#
7	PowerGood	8	not connected
9	Vstandby	10	orientation key

PCI Connector							
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B1	-12 V	A1	TRST#	B47	AD[12]	A47	AD[11]
B2	TCK	A2	+12 V	B48	AD[10]	A48	Ground
B3	Ground	A3	TMS	B49	+3.3 V	A49	AD[09]
B4	TDO	A4	TDI	B50	AD[08]	A50	C/BE#[0]
B5	+5 V	A5	+5 V	B51	AD[07]	A51	+3.3 V
B6	+5 V	A6	INTA#	B52	Ground	A52	AD[06]
B7	INTB#	A7	INTC#	B53	AD[05]	A53	AD[04]
B8	INTD#	A8	+5 V	B54	AD[03]	A54	Ground
B9	Ground	A9	reserved	B55	Ground	A55	AD[02]
B10	reserved	A10	PRSNT#	B56	AD[01]	A56	AD[00]
B11	+3.3 V	A11	reserved	B57	+5 V	A57	+5 V
	orientation key		orientation key	B58	+5 V	A58	+5 V
B12	reserved	A12	reserved	B59	+5 V	A59	+5 V
B13	Ground	A13	RESET#	B60	ACK64#	A60	REQ64#
B14	CLK	A14	+3.3 V		orientation key		orientation key
B15	Ground	A15	GNT#	B61	reserved	A61	Ground
B16	REQ#	A16	Ground	B62	Ground	A62	C/BE#[7]
B17	+3.3 V	A17	reserved	B63	C/BE#[5]	A63	C/BE#[6]
B18	AD[31]	A18	AD[30]	B64	C/BE#[4]	A64	+3.3 V
B19	AD[29]	A19	Ground	B65	Ground	A65	PAR64
B20	Ground	A20	AD[28]	B66	AD[63]	A66	AD[62]
B21	AD[27]	A21	AD[26]	B67	AD[61]	A67	Ground
B22	AD[25]	A22	+3.3 V	B68	+3.3 V	A68	AD[60]
B23	Ground	A23	AD[24]	B69	AD[59]	A69	AD[58]
B24	C/BE#[3]	A24	IDSEL	B70	AD[57]	A70	Ground
B25	AD[23]	A25	Ground	B71	Ground	A71	AD[56]
B26	+3.3 V	A26	AD[22]	B72	AD[55]	A72	AD[54]
B27	AD[21]	A27	AD[20]	B73	AD[53]	A73	+3.3 V
B28	AD[19]	A28	Ground	B74	Ground	A74	AD[52]
B29	Ground	A29	AD[18]	B75	AD[51]	A75	AD[50]
B30	AD[17]	A30	AD[16]	B76	AD[49]	A76	Ground
B31	C/BE#[2]	A31	+3.3 V	B77	+3.3 V	A77	AD[48]
B32	Ground	A32	FRAME#	B78	AD[47]	A78	AD[46]
B33	IRDY#	A33	Ground	B79	AD[45]	A79	Ground
B34	+3.3 V	A34	TRDY#	B80	Ground	A80	AD[44]
B35	DEVSEL#	A35	Ground	B81	AD[43]	A81	AD[42]
B36	Ground	A36	STOP#	B82	AD[41]	A82	+3.3 V
B37	LOCK#	A37	+3.3 V	B83	Ground	A83	AD[40]
B38	PERR#	A38	SDONE	B84	AD[39]	A84	AD[38]
B39	Ground	A39	SBO#	B85	AD[37]	A85	Ground
B40	SERR#	A40	Ground	B86	+3.3 V	A86	AD[36]
B41	+3.3 V	A41	C/BE#[1]	B87	AD[35]	A87	AD[34]
B42	AD[15]	A42	PAR	B88	AD[33]	A88	Ground
B43	+3.3 V	A43	+3.3 V	B89	Ground	A89	AD[32]
B44	+3.3 V	A44	+3.3 V	B90	reserved	A90	reserved
B45	AD[14]	A45	+3.3 V	B91	reserved	A91	Ground
B46	Ground	A46	AD[13]	B92	Ground	A92	reserved

Power Supply Connector for System Board			
Pin	Signal	Pin	Signal
1	PwrGood	8	+5 Vstdby
2	orientation key	9	+5 V supply
3	Remote_On	10	+5 V supply
4	Ground	11	+5 V supply
5	Ground	12	-12 V supply
6	Ground	13	-5 V supply
7	+12 V supply		

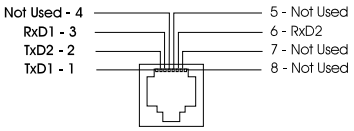
PS2 Connector for System Board			
Pin	Signal	Pin	Signal
1	Ground	4	+3.3 V supply
2	Ground	5	+3.3 V supply
3	Ground	6	+3.3 V supply

Battery Pack Connector			
Pin	Signal	Pin	Signal
1	VBATT	3	not connected
2	orientation key	4	Ground

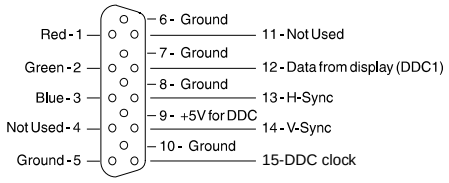
USB Connector	
Pin	Signal
1	Vcc
2	Data —
3	Data +
4	Ground

Socket Pin Layouts

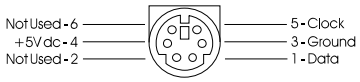
RJ-45 UTP Connector



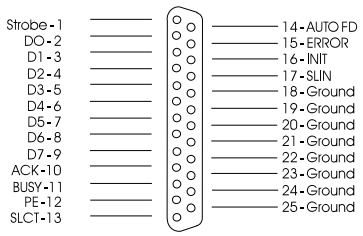
VGA Connector



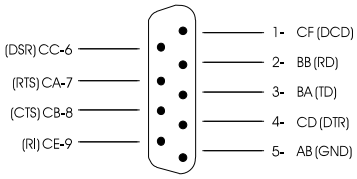
Keyboard and Mouse Connector



Parallel Port Connector



Serial Port Connector



4

Summary of the HP/Phoenix BIOS

The *Setup* program and HP/Phoenix BIOS are summarized in this chapter. The POST routines are described in the next chapter.

HP/Phoenix BIOS Summary

The System ROM contains the POST (power-on self-test) routines, and the BIOS: the System BIOS, video BIOS, network BIOS, and low option ROM. This chapter, and the following one, give an overview of the following aspects:

- menu-driven *Setup* with context-sensitive help (in US English only), described next in this chapter.
- The address space, with details of the interrupts used, described at the end of this chapter.
- The Remote Power-On (RPO), which is the mechanism for turning on the computer remotely from the network, described later in this chapter.
- The Power-On-Self-Test or POST, which is the sequence of tests the computer performs to ensure that the system is functioning correctly, described in the next chapter.

The system BIOS is identified by a version number of the form **HE.07.xx**. The procedure for updating the System ROM firmware is described on page 30.

Press F2, to run the *Setup* program, while the initial "Vectra" logo is being displayed immediately after restarting the PC. Alternatively, press Esc to view the summary configuration screen, an example of which is depicted on the next page. By default, this remains on the screen for 20 seconds, but by pressing F5 once, it can be held on the screen indefinitely until F1 is pressed. Pressing F10 will cause the computer to be turned off.

Net Vectra/200 – Copyright 1997 Hewlett-Packard – HE.07.xx			
Any line of text can be entered here as a 'tatoo' for the computer			
BIOS version	HE.07.xx	PC Serial Number	FR54011111
CPU Date Code	N/A	LAN MAC address	08-0009-85-03-00
System RAM	: 32 MB	Processor type	: Pentium
Bank A	: 32 MB (SDRAM)	COM1	: 3F8H (Serial)
Bank B	: None	COM2	: None
Bank C	: None	COM3	: None
Video RAM	: 2 MB	COM4	: None
System Cache	: 256KB (Synchronous)	LPT1	: 378H
Video Device	: S3 Trio 64V2	LPT2	: None
1st IDE Device	: HDD 1600 MB	LPT3	: None
2nd IDE Device	: None	Flexible Disk A	: None
3rd IDE Device	: None	Flexible Disk B	: None
4th IDE Device	: None	Display type	: Not Available
ISA PnP	: Not Installed	PCI Slot #1	: Not Installed
		PCI Slot #2	: Not Installed
<F1> to continue, <F2> to run Setup, <F10> to power off, <F5> to retain			

Setup Program

To run the *Setup* program, interrupt the POST by pressing F2 when the initial "Vectra" logo screen is being displayed, just after restarting the PC.

The band along the top of the screen offers five menus: Main, Configuration, Security, Power, and Exit. These are selected using the left and right arrow keys. Each menu is discussed in the following sub-sections.

Main Menu

The Main Menu presents the user with a list of fields, such as "System Time" and "Key auto-repeat speed". These can be selected using the up and down arrow keys, and can have their values changed using the F7 and F8 keys.

The "Item-Specific Help" field changes automatically as the user moves the cursor between the fields. It tells the user what the presently highlighted field is for, and what the options are.

Some fields are not changeable. Examples include fields that are for information only, and fields whose contents become "frozen" by the setting of a value in some other field. Such fields are displayed in a different color, without the "[" and "]" brackets. When the user moves the cursor with the up and down arrow keys, these fields are skipped.

Some fields disappear completely when a choice in another field makes their appearance inappropriate.

Advanced Menu

The Configuration Menu does not have the same structure as the Main Menu and Power Menu. Instead of presenting a list of fields, it offers the user with a list of sub-menus. Again, the user steps between the options using the up and down arrow keys, but presses the Enter key to enter the chosen sub-menu (and the Esc key to go back again when finished).

If access to devices has been disabled in the Security Menu, then the configuration of those devices on the Configuration Menu becomes frozen: the field becomes starred, appears in a different color, and cannot be changed.

Security Menu

Sub-menus are presented for changing the characteristics and values of the User Password, the System Administrator Password, the amount of protection against use of the system's drives and network connections (using the Hardware Protection sub-menu), and the amount of protection against being able to boot from the system's drives and network connections (using the Start-Up Center sub-menu).

Locking a device in the Security Menu frees the resources (such as IRQs and peripheral addresses).

Power Menu

The "Power" menu allows the user to set the standby delay. It also allows the system administrator to decide whether the network, serial port, mouse, or space bar are enabled as a means of reactivating the system from *Standby* or *Suspend*. It is also possible to specify whether the network is enabled as a means of reactivating the system from *Off*, using the remote power-on (RPO) facility (as described in the next section of this chapter).

Power Saving and Ergonometry

	Fully-On	Standby	Suspend	Off (but plugged in)
Processor	Normal speed	Clock throttled (divided by 8)	Halted	Halted
Display	Normal operation	Blanked (< 30 W)	Blanked (< 5 W typical)	Blanked (< 5 W typical)
Hard disk drive	Normal speed	Normal speed	Halted	Halted
Power consumption	24 W to 41 W depending on configuration & activity	< 30 W (230V, 50 Hz) < 27 W (115V, 60 Hz)	< 26 W (230V, 50 Hz) < 22 W (115V, 60 Hz)	< 1.6 W (230V, 50 Hz) < 0.5 W (115V, 60 Hz)
Resume events		Keyboard, mouse	Keyboard Network (RWU)	Space-bar Network (RPO)
Resume delay		Instantaneous	A few seconds	Boot delay

Desktop Management Interface (DMI)

HP TopTOOLS 2 is an integrated, easy-to-use desktop management application for efficient inventory, configuration, fault and security management. It is fully DMI compliant. It provides facilities for real-time monitoring and management of over 300 attributes of the PC (both the local PC, and remote ones over the network).

HP Lock

HP Lock provides a convenient and dynamic access to the security features of the PC. Facilities are provided for:

- Passwords
- Lock options (such as screen hiding and screen saving)
- Start-up protection
- Disk drive access (enabled or disabled)
- Communications port access (enabled or disabled)

HP Lock uses the dynamic link library **`gina.dll`**, which is the standard entry point to the Windows NT security engine. If you use another software application that also makes use of, or replaces this file (another security application for example) then it is not recommended to install *HP Lock*. The **`gina.dll`** file is not designed to be shared by multiple client applications.

Power-On from Space-Bar

The *power-on from the space-bar* function is enabled, provided that:

- The computer is connected to a Power-On keyboard (recognizable by the Power-On icon on the space bar).
- The function has not been disabled by setting SW-9 to **`open`** on the system board switches.
- The function has not been disabled in the "Power" menu of the *Setup* program.

Soft Power Down

When the user requests the operating system to shutdown, the environment is cleared, and the computer is powered off.

The hardware to do this, and the complementary function, *HP Off* (as described in the next section), is contained within the HP ASIC chip, X-Ben. This chip is described on page 51.

HP Off

If the user attempts to turn the PC off at the status panel, the PC logic will delay the shutting down of the power supply until it is safe to do so. *HP Off* protects the user from some types of unintentional data loss, providing a safe shutdown of running applications and unsaved files.

1 In the control panel, double-click on the Power icon.
2 Click on the **`HP Off`** tab to select *HP Off*, or on **`Immediate Power Off`** to cancel it.
3 Select the time-out period, between one and five seconds.

The time-out period is the delay during which the power-down command can be cancelled (whilst the **`About to shut down Windows`** message is displayed on the screen). If the user cancels, the computer is returned to normal operation; otherwise, the computer goes on to check if there are any

unsaved files. If there are, it offers three choices: **yes** (to saving the unsaved changes, followed by shutdown), **no** (thereby shutting down without saving the changes), and **cancel** (to return to normal operation).

Remote Power-On (RPO)

Remote power-on (RPO) provides a way to turn on the computer from a communication channel, such as a Network or Modem, using facilities that have been incorporated in the X-Ben chip and the ExtStart connector. It allows system administrators, and authorized users, to switch on the computer from anywhere over an Ethernet network, to perform remote administration or other tasks, and to return it to *Off* or *Suspend* mode afterwards.

Magic Packet

Magic packet is a standard for remote power-on and remote wake-up. The standard defines a Magic Packet frame as the computer's unique Ethernet *Media Access Control* (MAC) address (which it has stored in an EEPROM on the network board), repeated 16 times and encoded in a valid network packet.

Any Magic Packet-compatible management application (such as *HP OpenView Workgroup Node Manager*) can send a Magic Packet frame. An administrator can do this manually, or can incorporate it into a management script. The packet travels over any type of Ethernet LAN to the target PC.

The only component not completely turned off in the computer is the network chip, which rests in a special low power mode. Power is supplied by a line called *VStandby*, on the External Start connector (see the pin layout in the table on page 40) as long as the power cord is plugged in. The independent mini power supply provides the power necessary to keep one part of the network chip ready to receive a wake-up signal. This is the only signal it can respond to in this state.

The network chip sends a signal over the External Start connector, where it is received by the special network remote power chip. This in turn switches on the main power supply.

The PC starts normally from whatever operating system is installed, just as if the power supply had been switched on from the external power switch. The display does not itself need to have an RPO function. If a password has been set, the **`Start with keyboard locked`** option must be enabled.

Activity within the Setup Program

Since the user is not physically present, the level of security must be tighter. There is a distinction between the user-boot process, and the RPO-boot process. HP provides all the necessary *Setup* options to keep users from interfering with the computer during the remote session.

RPO is available when the POST routines have finished executing. It is initialized by an SMI signal which is triggered from the mains power button.

A power failure when the computer is in RPO mode will deactivate the RPO feature. RPO is intended for resource management (such as virus cleaners, nightly backups, etc.), not for crisis management (thunderstorm recovery, power failure, etc.).

X-Ben

X-Ben is an HP application specific integrated circuit (ASIC), designed to be a companion to the Super I/O chip. It interfaces between the chip-set and the processor, and contains the following:

- BIOS timer
  - ❒ hardware wired 50 ms long 880 Hz beep module.
  - ❒ automatic blinker that feeds the LEDs module with a 1 Hz oscillator signal.
- security protection (access, flash and anti-virus protection)
  - ❒ For 128, 256 or 512 KB Flash EEPROMs.
  - ❒ For the Super I/O space: the Serial EEPROM, serial port, parallel port and mass storage drives (disable write to the Flexible Disk Controller, disable boot on any drive, disable use of any embedded drive)
- hard and soft control for the power supply (available with the Windows NT and Windows 95 operating systems, but not with the OS/2 operating system)
- Advanced power management (APM) version 1.2 (available with the Windows 95 and OS/2 operating systems, but not with the Windows NT operating system)

- glue logic (such as programmable chip selects)

The computer can be turned on by typing the space-bar on the keyboard, or when it receives an external signal from a network board. When *VccState* and *PowerGood* pins are both low, power consumption is reduced to a minimum, and all output pins are in tri-state mode, except for *RemoteOnBen* which continues to be driven.

When the user requests a ShutDown from the operating system, the environment is first cleared. Any request to turn off the computer, from the status panel, or from the operating system, can only be granted if the computer is not locked by X-Ben's lock bit (otherwise the power remains on, a red light is illuminated, and the buzzer is sounded).

The *SMI_OFF* signal is asserted if the Hard Soft Power Down mode (HSPD) is enabled when X-Ben is instructed to turn off the computer (via the status panel or soft power down). The BIOS first performs some RPO initialization, and then proceeds to power down the computer.

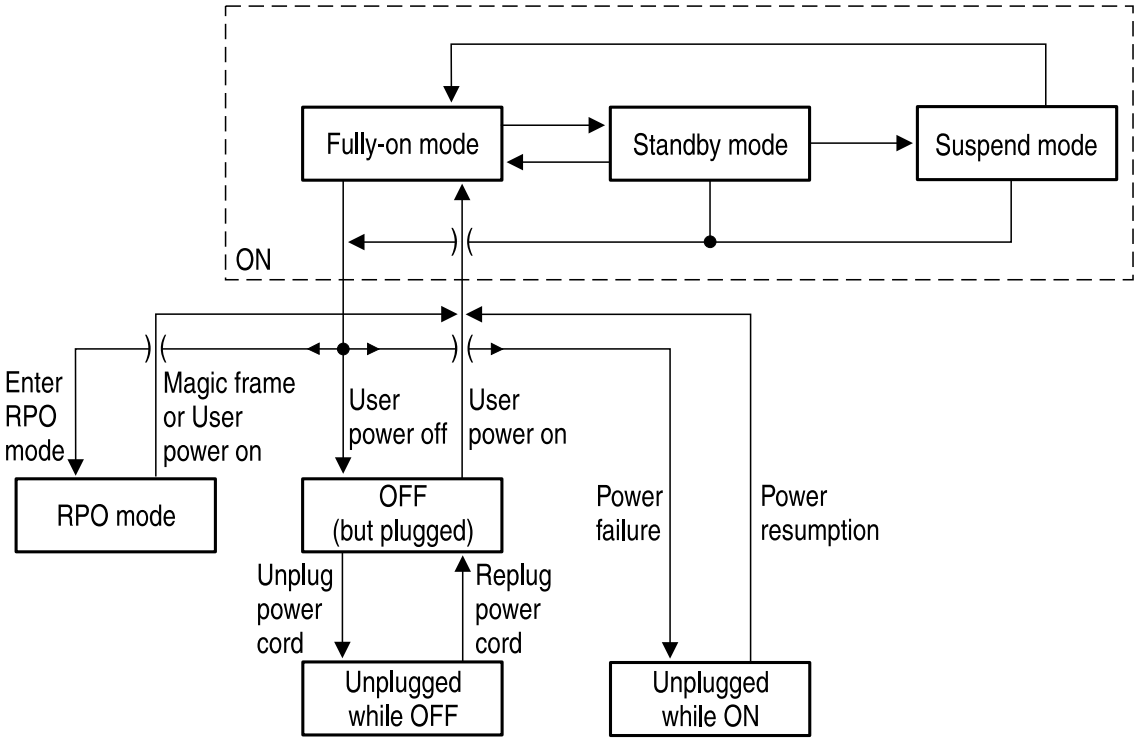
If the computer 'hangs', the power button on the status panel should be held 'pressed' for about 6 seconds. A watch-dog timer will detect that the BIOS is inactive, and not reloading the timer once every 6 seconds, thereby forcing the computer to turn itself off without further BIOS acknowledgment.

Advanced Power Management (APM)

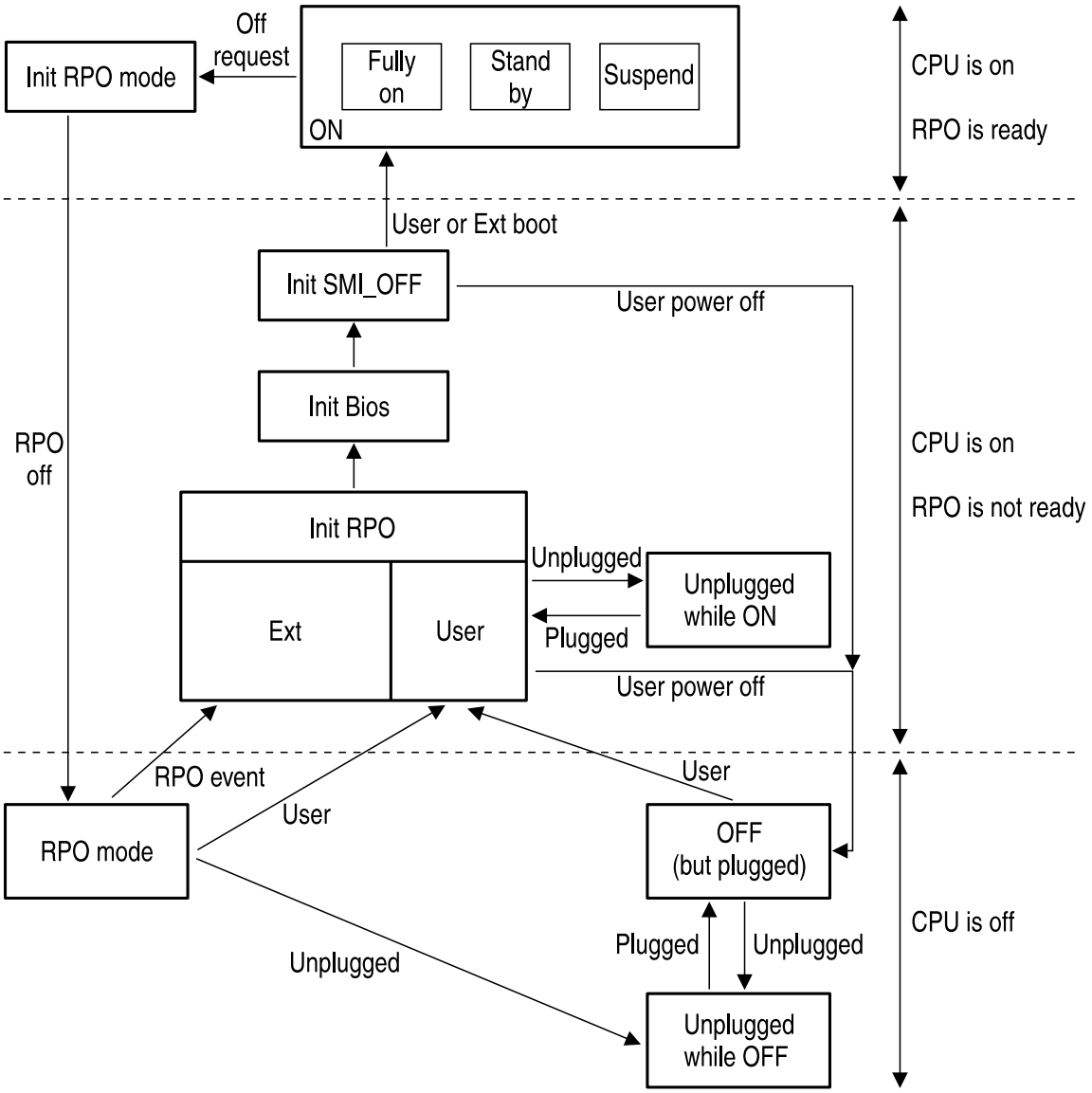
The BIOS is APM 1.2 compliant, providing it with facilities for *advanced power management* (APM). It supports the following modes: *Fully-on*, *Standby*, *Suspend*, *Hibernation* and *Off*. Of these, APM 1.2 supports *Fully-on*, *Standby*, *Suspend* and *Off*, as summarized in the table on page 48.

RPO defines a variation from the standard *Off* state. In *RPO* mode, the main CPU hardware is off while a RPO function is powered by a power supply called *VStandby*. *VStandby* is active as soon as the computer is plugged in. RPO hardware can produce a triggering signal which turns on the computer.

The following diagram gives a simplified view of the useful states that the computer can be in: the three *On* states (*Fully-On*, *Standby* and *Suspend*), the *RPO* state (when the CPU is *Off*, and the RPO hardware is powered by VStandby), the *Off* state (when everything is powered off), and the state that is caused by power failure or unplugging the computer.


Fully-on mode
Standby mode
Suspend mode
ON
Enter RPO mode
Magic frame or User power on
User power off
User power on
RPO mode
OFF (but plugged)
Power failure
Power resumption
Unplug power cord
Replug power cord
Unplugged while OFF
Unplugged while ON

The following diagram gives a more accurate, more detailed account of the valid state changes.



BIOS Addresses

This section provides a summary of the main features of the HP system BIOS. This is software that provides an interface between the computer hardware and the operating system.

System Memory Map

Any reserved memory that is used by accessory boards must be located in the area from C8000h to EFFFFh.

0 - 3FFh	Interrupt vector table	640 KB: The addresses 0-9FFFFh are collectively known as the Base memory area
400h - 4FFh	BIOS data area	
500h - 9EFFFh		
9F000h - 9FFFFh	Extended BIOS data area	
A0000h - BFFFFh	128 KB: Video memory area	
C0000h - C7FFFh	32 KB: Video BIOS area	
C8000h - D7FFFh	64 KB: available for accessory boards (used by the boot ROM, if configured in the *Setup* program)	
D8000h - EFFFFh	96 KB: available after the POST (for upper memory block, UMB, for example)	
F0000h - FFFFFh	64 KB: System BIOS area	
100000h - FFFFFFFFh	1 MB plus: Extended memory	

Product Identification

The reserved addresses in the 64 KB BIOS ROM data area, which contain various product identification and BIOS identification strings, are no longer accessed directly. Instead, the information is obtained from utilities in the Desk Management Interface (DMI).

HP I/O Port Map (I/O Addresses Used by the System[1])

Peripheral devices, accessory devices and system controllers are accessed via the system I/O space, which is not located in system memory space. The 64 KB of addressable I/O space comprises 8-bit and 16-bit registers (called I/O ports) located in the various system components. When installing an accessory board, ensure that the I/O address space selected is in the free area of the space reserved for accessory boards (100h to 3FFh).

Although the *Setup* program can be used to change some of the settings, the following address map is not completely BIOS dependent, but is determined partly by the operating system. Beware that some of the I/O addresses are allocated dynamically.

I/O Address Ports	Function
0000h - 000Fh	DMA controller 1
0020h - 0021h	Interrupt controller 1
0040h - 0043h	Interval timer 1
0060h, 0064h	Keyboard controller
0061h	System speaker, or NMI status and control
0070h	NMI mask register, RTC and CMOS address
0071h	RTC and CMOS data
0081h - 0083h, 008Fh	DMA low page register
0092h	Alternate reset and A20 Function
00A0h - 00A1h	Interrupt controller 2
00C0h - 00DFh	DMA controller 2
00EAh - 00EBh	Internal port
00F0h - 00FFh	Co-processor error
0102h	Graphics controller (S3 Trio 64V2)
0170h - 0177h	IDE hard disk drive controller secondary channel
01F0h - 01F7h	IDE hard disk drive controller primary channel

1. If configured (legacy resources only).

I/O Address Ports	Function
0278h - 027Fh	Parallel port 2
0279h	IO read data port for ISA Plug and Play enumerator
02E8h - 02EFh	Serial port 4 (available if not used)
02F8h - 02FFh	Serial port 2 (available if not used)
0370h - 0371h	Super I/O controller
0372h - 0375h	Secondary flexible disk drive controller
0376h	IDE hard disk drive controller secondary channel
0377h	Secondary flexible disk drive controller
0378h - 037Ah	Parallel port 1 (available if not used)
03B0h - 03DFh	Graphics controller (S3 Trio 64V2)
03E8h - 03EFh	Serial port 3
03F0h - 03F5h	Primary flexible disk drive controller
03F6h	IDE hard disk drive controller primary channel
03F7h	Primary flexible disk drive controller
03F8h - 03FFh	Serial port 1
0678h - 067Bh	Parallel port 2 if ECP mode is selected
0778h - 077Bh	Parallel port 1 if ECP mode is selected
0CF8h - 0CFFh	Configuration registers for PCI devices

DMA Channel Controllers

Only “I/O-to-memory” and “memory-to-I/O” transfers are allowed. “I/O-to-I/O” and “memory-to-memory” transfers are disallowed by the hardware configuration.

The system controller supports seven DMA channels, each with a page register used to extend the addressing range of the channel to 16 MB. The following table summarizes how the DMA channels are allocated.

First DMA controller (used for 8-bit transfers)	
Channel	Function
0	Available
1	ECP mode for parallel port (available if not used)
2	Flexible disk controller
3	ECP mode for parallel port (available if not used)
Second DMA controller (used for 16-bit transfers)	
Channel	Function
4	Cascade from first DMA controller
5	Available
6	Available
7	Available

Interrupt Controllers

The system has two 8259A compatible interrupt controllers. They are arranged as a master interrupt controller and a slave that is cascaded through the master.

The following table shows how the master and slave controllers are connected. The Interrupt Requests (IRQ) are numbered sequentially, starting with the master controller, and followed by the slave.

IRQ (Interrupt Vector)		Interrupt Request Description
IRQ0(08h)		System timer
IRQ1(09h)		Keyboard controller
IRQ2(0Ah)	Slave IRQ	Cascade connection from INTC2 (Interrupt Controller 2)
	IRQ8(70h)	Real Time Clock
	IRQ9(71h)	Available

	IRQ10(72h)	Available
	IRQ11(73h)	Reserved (used by the DHCP)
	IRQ12(74h)	Mouse
	IRQ13(75h)	Co-processor
	IRQ14(76h)	IDE controller
	IRQ15(77h)	Secondary IDE (available if not used)
IRQ3(0Bh)		Serial Port 2, Serial Port 4 (available if not used)
IRQ4(0Ch)		Serial Port 1, Serial Port 3 (available if not used)
IRQ5(0Dh)		Parallel Port 2 (available if not used)
IRQ6(0Eh)		Flexible Disk Controller
IRQ7(0Fh)		Parallel Port 1 (available if not used)

Using the *Setup* program:

- IRQ3 can be made available by disabling serial ports 2 and 4.
- IRQ4 can be made available by disabling serial ports 1 and 3.
- IRQ5 can be made available by disabling the parallel port 2.
- IRQ7 can be made available by disabling parallel ports 1 and 2.

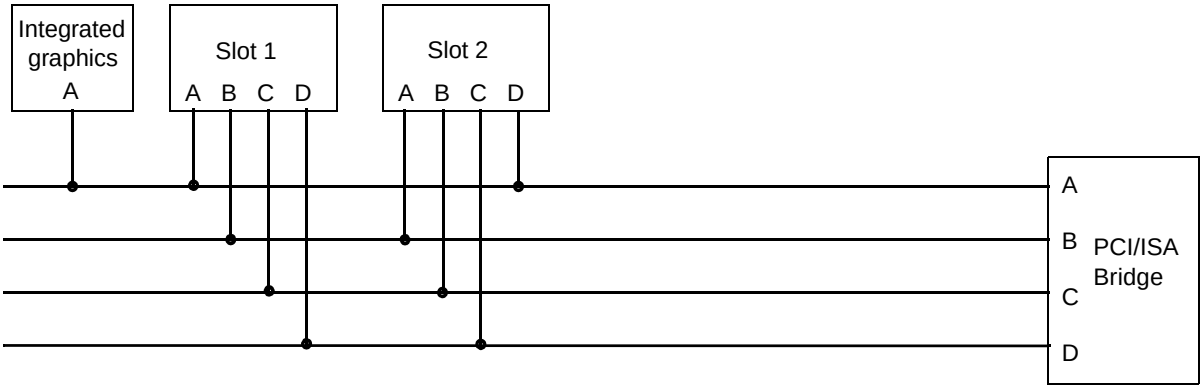
The IDE controller (device 04h, function 01h) is configured in *legacy mode*, and uses IRQ 14 (IRQ 15 for the secondary channel).

PCI Interrupt Request Lines

PCI devices generate interrupt requests using up to four PCI interrupt request lines (INTA#, INTB#, INTC#, and INTD#).

When a PCI device makes an interrupt request, the request is re-directed to the system interrupt controller. The interrupt request will be re-directed to one of the IRQ lines made available for PCI devices.

The PCI interrupt lines A, B, C and D are spread across the four inputs of the interrupt router (which is part of the PCI/ISA bridge, in the Bridge chip). Since most PCI devices are single-function, this allows for an even distribution of the lines. The distribution is shown in the following diagram.



PCI interrupts are then mapped into ISA interrupts inside the Bridge chip, by configuring registers 60h through 63h.

Bit	Description
7	Routing of interrupts: when enabled, this bit routes the PCI interrupt signal to the PC-compatible interrupt signal specified in bits[3:0]. At reset, this bit is disabled (set to 1)
6:4	Reserved: read as 000
3:0	IRQx# Routing Bits: these bits specify which IRQ signal to generate. Possible values are: 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15.

5

Power-On Self-Test and Error Messages

This chapter describes the Power-On Self-Test (POST) routines, which are contained in the System BIOS, the error messages that can result, and the suggestions for corrective action.

Order in Which the Tests are Performed

Each time the system is powered on, or a reset is performed, the POST is executed. The POST process verifies the basic functionality of the system components and initializes certain system parameters.

The POST starts by displaying a graphic screen with the initial "Vectra" logo when the PC is restarted. If the POST detects an error, the error message is displayed inside a *view system errors* screen, in which the *error message utility* (EMU) not only displays the error diagnosis, but the suggestions for corrective action (see page 65 for a brief summary). Error codes are no longer displayed.

Devices, such as memory and newly installed hard disks, are configured automatically. The user is not requested to confirm the change. Newly removed hard disks are detected, and the user is prompted to confirm the new configuration by pressing F4. Note, though, that the POST does not detect when a hard disk drive has been otherwise changed.

During the POST, the BIOS and other ROM data is copied into high-speed shadow RAM. The shadow RAM is addressed at the same physical location as the original ROM in a manner which is completely transparent to applications. It therefore appears to behave as very fast ROM. This technique provides faster access to the system BIOS firmware.

The following table lists the POST routines in the order in which they are executed (from the shadow RAM). If the POST is initiated by a soft reset Ctrl Alt and Delete, the RAM tests are not executed and shadow RAM is not cleared. In all other respects, the POST executes in the same way following power-on or a soft reset.

Test	Description
System BIOS Tests	
LED Test	Tests the LEDs on the status panel.
System ROM (BIOS) Test	Calculates an 8-bit checksum. Test failure causes the boot process to abort.
RAM Refresh Timer Test	Tests the RAM refresh timer circuitry. Test failure causes the boot process to abort.
Interrupt RAM Test	Checks the first 64 KB of system RAM used to store data corresponding to various system interrupt vector addresses. Test failures cause the boot process to abort.

Shadow the System ROM BIOS	Tests the system ROM BIOS and shadows it. Failure to shadow the ROM BIOS will cause an error code to display. The boot process will continue, but the system will execute from ROM. This test is not performed after a soft reset (using Ctrl Alt and Delete).
Load CMOS Memory	Checks the serial EEPROM and returns an error code if it has been corrupted. Copies the contents of the EEPROM into CMOS RAM.
CMOS RAM Test	Checks the CMOS RAM for start-up power loss, verifies the CMOS RAM checksums. Test failure causes error codes to display.
CPU Cache Memory Test	Tests the processor's internal level-one cache RAM. Test failure causes an error code to display and the boot process to abort.
Video Tests	
Initialize the Graphics Controller	Initializes the graphics subsystem, tests the video shadow RAM, and shadows the video BIOS. A failure causes an error code to display, but the boot process continues.
System Board Tests	
8042 Self-Test	Downloads the 8042 and invokes the 8042 internal self-test. A failure causes an error code to display.
Timer 0/Timer 2 Test	Tests Timer 0 and Timer 2. Test failure causes an error code to display.
DMA Subsystem Test	Checks the DMA controller registers. Test failure causes an error code to display.
Interrupt Controller Test	Tests the Interrupt masks, the master controller interrupt path (by forcing an IRQ0), and the industry-standard slave controller (by forcing an IRQ8). Test failure causes an error code to display.
Real-Time Clock Test	Checks the real-time clock registers and performs a test that ensures that the clock is running. Test failure causes an error code to display.
Memory Tests	
RAM Address Line Independence Test	Verifies the address independence of real-mode RAM (no address lines stuck together). Test failure causes an error code to display.
Size Extended Memory	Sizes and clears the protected mode (extended) memory and writes the value into CMOS bytes 30h and 31h. If the system fails to switch to protected mode, an error code is displayed.
Real-Mode Memory Test (First 640KB)	Read/write test on real-mode RAM. (This test is *not* done during a reset using Ctrl Alt and Delete). The test checks each block of system RAM to determine how much is present. Test failure of a 64 KB block of memory causes an error code to display, and the test is aborted.
Shadow RAM Test	Tests shadow RAM in 64 KB segments (except for segments beginning at A000h, B000h, and F000h). If they are *not* being used, segments C000h, D000h and E000h are tested. Test failure causes an error code to display.

Protected Mode RAM Test (Extended RAM)	Tests protected RAM in 64 KB segments above 1 MB. (This test is *not* done during a reset using Ctrl Alt and Delete). Test failure causes an error code to display.
Keyboard / Mouse Tests	
Keyboard Test	Invokes a built-in keyboard self-test of the keyboard's microprocessor and tests for the presence of a keyboard and for stuck keyboard keys. Test failure causes an error code to display.
Mouse Test	If a mouse is present, invokes a built-in mouse self-test of the mouse's microprocessor and for stuck mouse buttons. Test failure causes an error code to display.
Network Test	If the network board is present, invokes a built-in self-test. Test failure causes an error code to display.
Tests of Flexible Disk Controller	
Flexible Disk Controller Subsystem Test	Tests for proper operation of the flexible disk controller. Test failure causes an error code to display.
Coprocessor Tests	
Internal Numeric Coprocessor Test	Checks for proper operation of the numeric coprocessor part of the processor. Test failure causes an error code to display.
Communication Port Tests	
Parallel Port Test	Tests the integrated parallel port registers, as well as any other parallel ports. Test failure causes an error code to display.
Serial Port Test	Tests the integrated serial port registers, as well as any other serial ports. Test failure causes an error code to display.
Hard Disk Drive Tests	
Hard Disk Controller Subsystem Test	Tests for proper operation of the hard disk controller. Test failure causes an error code to display. The test does not detect hard disk replacement or changes in the size of the hard disk.
System Configuration Tests	
System Generation	Initiation of the system generation (SYSGEN) process, which compares the configuration information stored in the CMOS memory with the actual system. If a discrepancy is found, an error code will be displayed.
Plug and Play Configuration	Configures any Plug and Play device detected: ❒ All PCI devices will be configured for use.

Error Message Summary

The POST section of the HP BIOS no longer displays numeric error codes (such as 910B) but gives a self-explanatory, descriptive diagnosis, and a list of suggestions for corrective action. The following table summarizes the most significant of the problems that can be reported.

Message	**Explanation or Suggestions for Corrective Action**
Operating system not found	Check whether the disk drive is connected. If it is connected, check that it is detected by POST. Check that your boot device is enabled on the *Setup* Security menu. If the problem persists, check that the boot device contains the operating system.
Missing operating system	If you have configured the hard disk user parameters, check that they are correct. Otherwise, use the hard disk "Auto" parameters.
Failure fixed disk (preceded by a 30" time-out)	Check that the hard disk is connected. Check that the hard disk is detected in POST. Check that boot on the hard disk drive is enabled in *Setup*.
System battery is dead	You may get this message if the computer is disconnected for a few days. When you Power-on the computer, run *Setup* to update the configuration information. The message should no longer be displayed. Should the problem persist, replace the battery.
Keyboard error	Check that the keyboard is connected.
Resource Allocation Conflict -PCI device 0079 on system board	Clear CMOS.
Video Plug and Play interrupted or failed. Re-enable in Setup and try again	You may have powered your computer Off/On too quickly and the computer turned off Video plug and play as a protection.
System CMOS checksum bad - run Setup	CMOS contents have changed between 2 power-on sessions. Run *Setup* for configuration.
No message, system "hangs" after POST	Check that the main memory modules are correctly set in their sockets.
Other	An error message may be displayed and the computer may "hang" for 20 seconds and then beep. The POST is probably checking for a mass storage device which it cannot find and the computer is in Timeout Mode. After Timeout, run *Setup* to check the configuration.

Beep Codes

If a terminal error occurs during POST, the system issues a beep code before attempting to display the error. Beep codes are useful for identifying the error when the system is unable to display the error message.

Beep Pattern	Beep Code[1]	Numeric Code	Description
-	1	B4h	This does not indicate an error. There is one short beep before system startup.
— --	02	98h	Video configuration failure or option ROMs check-sum failure
— -- -- ---	0223	16h	BIOS ROM check-sum failure
— --- — —	0300	20h	DRAM refresh test failure
— --- — ---	0303	22h	8742 Keyboard controller test failure
— --- ---- —	0340	2Ch	RAM failure
— --- ---- ---	0343	2Eh	RAM failure on data bits in low byte of memory bus
— ---- — —	0400	30h	RAM failure on data bits in high byte of memory bus
-- — -- ---	2023	46h	ROM copyright notice check failure
-- -- --- —	2230	58h	Unexpected interrupts test failure
— -- — -- --	02022		Continuous beeps. Keyboard error

[1] Where digits 1, 2, 3, 4 represent the number of short beeps, and 0 represents the occurrence of a single long beep.

Lights on the Status Panel

When the computer is first powered on, the *power-on* light on the status panel illuminates yellow for about a second before changing to green. This change of color is caused by the execution of an instruction early in the System BIOS code.

If the light remains at yellow, therefore, it indicates a failure of the processor or the System ROM in the instruction-fetch process. Check that the processor is correctly seated in its socket.