MP440BX Motherboard
Technical Product Specification

April 1998

Order Number 694605-001

The MP440BX motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the MP440BX Motherboard Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the MP440BX Motherboard Technical Product Specification	April 1998

This product specification applies only to standard MP440BX motherboards with BIOS identifier 4M4PB0X1.86A.

Changes to this specification will be published in the MP440BX Motherboard Specification Update before being incorporated into a revision of this document.

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1 Motherboard Description

1.1 Overview

The features of the MP440BX motherboard are described below.

ATX form factor of 12 x 8 inches

Processor:

- Supports a single Pentium® II processor with a 66-MHz or 100-MHz front side bus (FSB)
- 512 KB or 1 MB second-level cache on the substrate in the Single Edge Contact (S.E.C.) cartridge
- Slot 1 connector

Main memory:

- Three 168-pin dual inline memory module (DIMM) sockets
- Supports up to 384 MB of synchronous DRAM (SDRAM)
- Supports error checking and correcting (ECC) memory or non-ECC memory

Intel 82440BX AGPset and PCI IDE Interface:

- Intel 82443BX PCI/A.G.P. controller (PAC)
  - Integrated PCI bus-mastering controller
  - Integrated Accelerated Graphics Port (A.G.P.) controller
- Intel 82371EB PCI ISA IDE Xcelerator (PIIX4E)
  - Supports up to four IDE drives or devices
  - Multifunction PCI-to-ISA bridge
  - USB and DMA controllers
  - Two fast IDE interfaces
  - Power management logic
  - Real-time clock

I/O features:

- SMC FDC37C777 I/O controller that integrates standard I/O functions, including an interface for one diskette drive, one multimode parallel port, two FIFO serial ports, a keyboard and mouse controller, and an IrDA†-compatible interface
- Two Universal Serial Bus (USB) ports

Six usable expansion slots:

- One ISA slot
- One shared PCI/ISA slot
- Three PCI slots
- A.G.P. slot

LAN subsystem:

- Integrates a complete onboard LAN interface using the Intel 82558 PCI LAN controller
- Includes Wake on LAN† technology

Manageability:

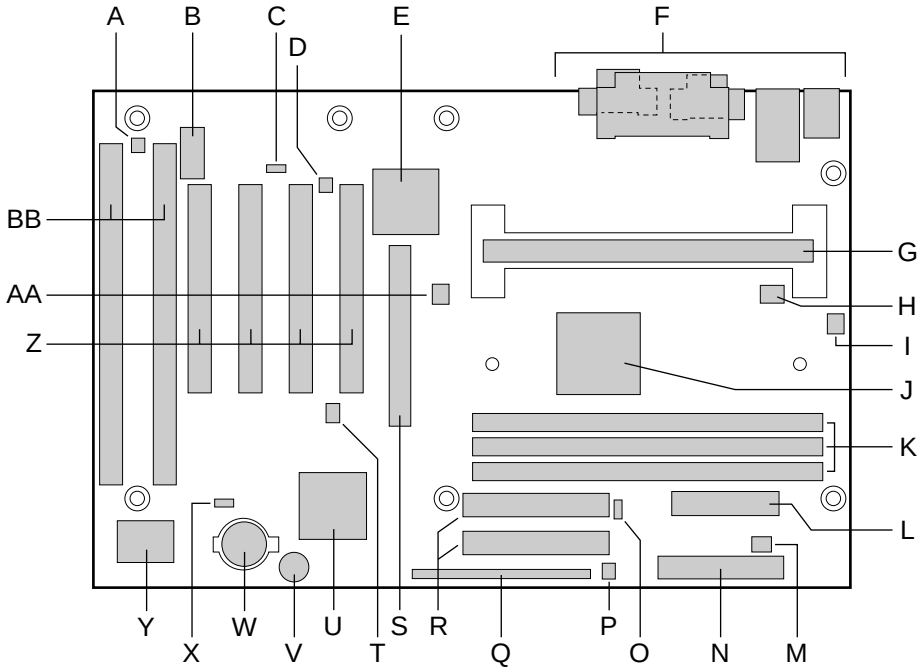
- Hardware monitor ASIC
- Wired for Manageability (WfM) 1.1 compliant
- Management level 4 support

Other features:

- Intel/Phoenix BIOS
- Plug and Play compatibility
- Single-jumper configuration
- Advanced Power Management (APM) 1.2 support
- Advanced Configuration and Power Interface (ACPI) 1.0 support

Software drivers and utilities are available from Intel.

1.2 Motherboard Components



A	Wake on ring connector	O	Sleep LED header
B	4 Mbit symmetrical flash memory	P	SCSI hard disk LED header
C	Wake on LAN technology header	Q	Front panel header
D	Chassis intrusion connector	R	IDE connectors
E	Intel 82558 PCI LAN controller	S	A.G.P. connector
F	Back panel I/O connectors	T	PC/PCI header
G	Slot 1 connector	U	Intel 82371EB (PIIX4E)
H	Hardware monitor ASIC	V	Speaker
I	Fan 2 header	W	Battery
J	Intel 82443BX (PAC)	X	Configuration header
K	DIMM sockets	Y	I/O controller
L	Power connector	Z	PCI connectors
M	Fan 1 header	AA	Fan 3 header (active heatsink fan)
N	Diskette drive connector	BB	ISA connectors

Figure 1. Motherboard Components

1.3 Form Factor

The motherboard is designed to fit into a standard ATX form-factor chassis. The outer dimensions are 12 x 8 inches. Figure 2 shows that the mechanical form factor, the I/O connector locations, and the mounting hole locations are in compliance with the ATX specification (see Section 6.2).

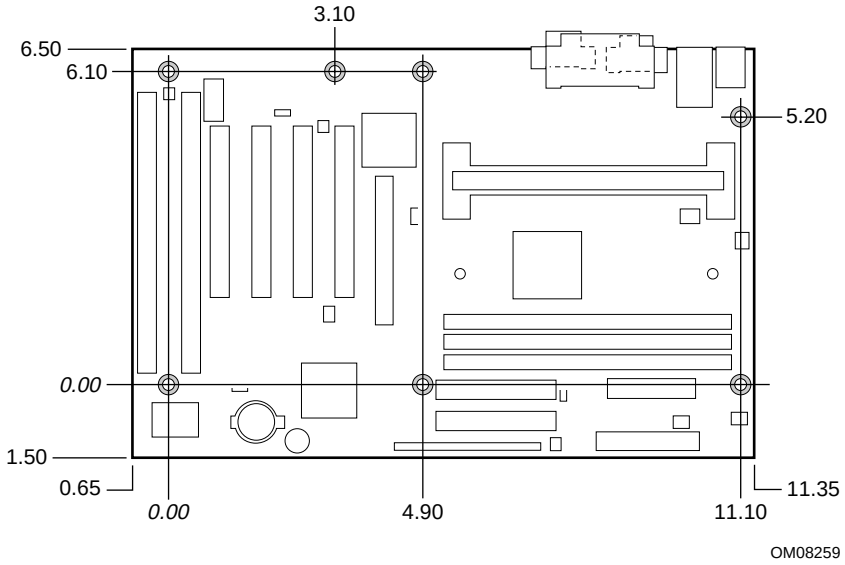


Figure 2. Motherboard Dimensions

1.4 I/O Shield

The back panel I/O shield for the motherboard must meet specific dimension and material requirements. Computers based on this motherboard need the back panel I/O shield to pass certification testing. Figure 3 shows the critical dimensions of the chassis-dependent I/O shield. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification. See Section 6.2 for information about the ATX specification.

NOTE

I/O shield specifications are available from Intel.

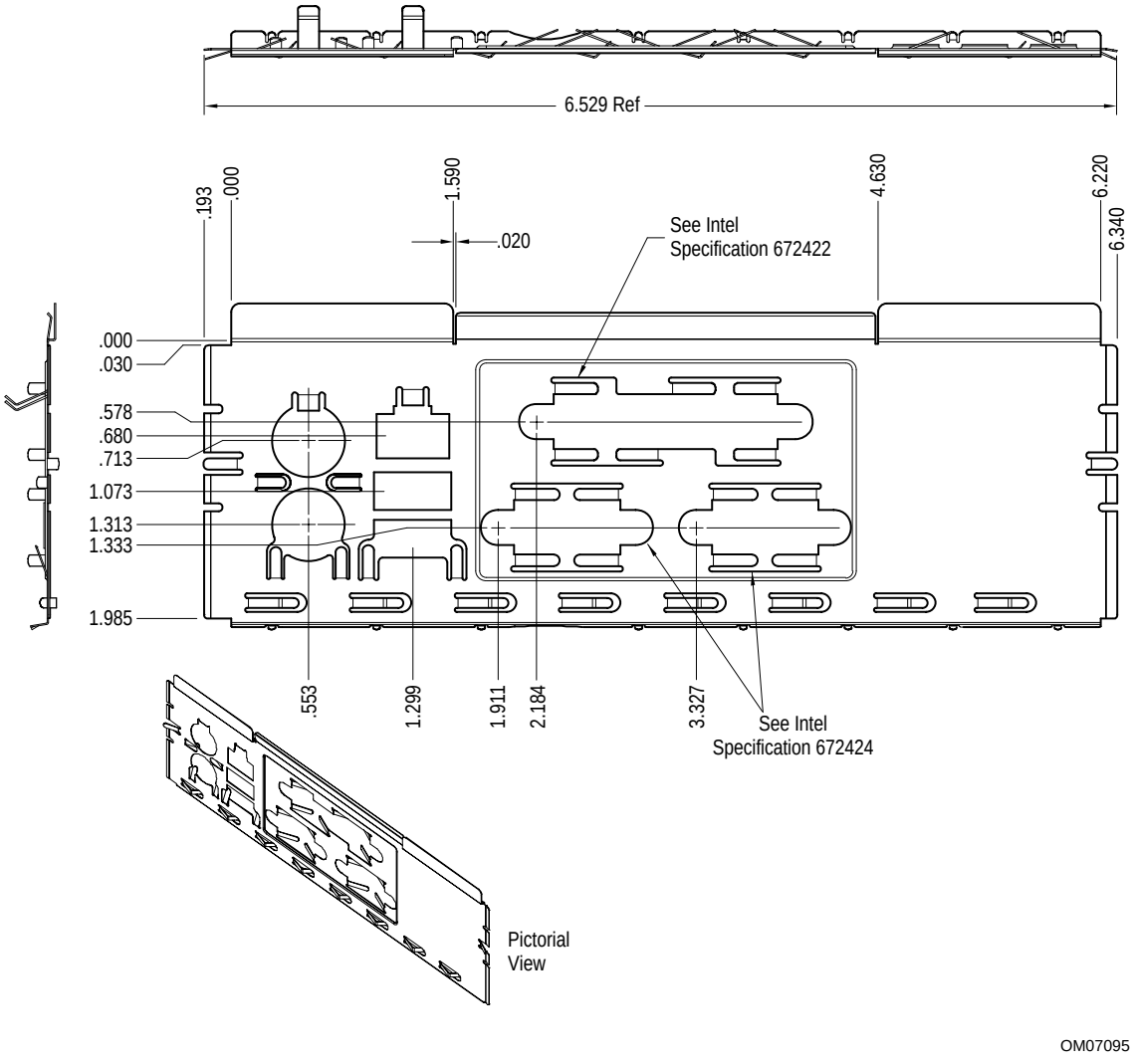


Figure 3. Back Panel I/O Shield Dimensions (ATX Chassis-Dependent)

1.5 Processor

The motherboard supports a single Pentium II processor. The processor's VID pins automatically program the voltage regulator on the motherboard for the required processor voltage. In addition, the front side bus speed (66 MHz and 100 MHz) is automatically selected. The motherboard supports all current Pentium II processor speeds, voltages, and bus frequencies.

⚠ CAUTION

The MP440BX motherboard supports Pentium II processors with a 100- or 66-MHz FSB. Processors with a 100-MHz FSB should be used only with 100-MHz SDRAM; the motherboard will not operate reliably if a processor with a 100-MHz FSB is paired with 66-MHz SDRAM. Processors with a 66-MHz FSB can be used with 66-MHz or 100-MHz SDRAM.

1.5.1 Processor Packaging

The processor is packaged in a Single Edge Contact (S.E.C.) cartridge. The cartridge includes the processor core, second-level cache, thermal plate, and back cover.

The processor connects to the motherboard through the Slot 1 connector, a 242-pin edge connector. When mounted in Slot 1, the processor is secured by a retention mechanism attached to the motherboard. Processors with passive heatsinks are stabilized by a heatsink support that is attached to the motherboard.

1.5.2 Second-Level Cache

The 512 KB or 1 MB second-level cache is located on the substrate of the S.E.C. cartridge. The cache includes pipelined burst static RAM (PBSRAM) and tag RAM. All supported onboard memory can be cached.

1.5.3 Processor Upgrades

The motherboard can be upgraded with Pentium II processors that run at higher speeds. When upgrading the processor, use the BIOS configure mode to change the processor speed (see Section 1.15).

1.6 Memory

1.6.1 Main Memory

The motherboard has three DIMM sockets. Minimum memory size is 8 MB; maximum memory size is 384 MB. The BIOS automatically detects memory type, size, and speed. Memory can be installed in one, two, or three sockets. Memory size and speed can vary between sockets.

The motherboard supports the following memory features:

- 168-pin DIMMs with gold-plated contacts
- 66- or 100-MHz SDRAM only
- Non-ECC (64-bit) and ECC (72-bit) memory
- 3.3 V memory only
- Single- or double-sided unbuffered DIMMs in the following sizes:

DIMM Size	Non-ECC Configuration	ECC Configuration
8 MB	1 Mbit x 64	1 Mbit x 72
16 MB	2 Mbit x 64	2 Mbit x 72
32 MB	4 Mbit x 64	4 Mbit x 72
64 MB	8 Mbit x 64	8 Mbit x 72
128 MB	16 Mbit x 64	16 Mbit x 72

NOTE

DIMMs used with this motherboard must comply with the following specifications: the PC Unbuffered DIMM Specification for either 64-bit or 72-bit SDRAM and the PC Serial Presence Detect Specification. See Section 6.2 for information about these specifications.

1.6.2 ECC Memory

ECC memory detects multiple-bit errors and corrects single-bit errors. When ECC memory is installed, the BIOS supports both ECC and non-ECC mode. ECC mode is enabled in the Setup program. The BIOS automatically detects if ECC memory is installed and provides the Setup option for selecting ECC mode. If any non-ECC memory is installed, the Setup option for ECC configuration does not appear and ECC operation is not available.

The following table describes the effect of using Setup to put each memory type in each supported mode. Whenever ECC mode is selected in Setup, some performance loss occurs.

	Memory Error Detection Mode Established in Setup Program	
	ECC Disabled	ECC Enabled
Non-ECC DIMM	No error detection	N/A
ECC DIMM	No error detection	Single-bit error correction, multiple-bit error detection

1.7 Chipset

The Intel 82440BX AGPset includes a host-PCI bridge integrated with both an optimized DRAM controller and an Accelerated Graphics Port (A.G.P.) interface. The I/O subsystem of the 82440BX is based on the PIIX4E, which is a highly integrated PCI ISA IDE Accelerator Bridge. This chipset consists of the Intel 82443BX PAC and the Intel 82371EB PCI ISA IDE Xcelerator (PIIX4E) bridge chip.

1.7.1 Intel 82443BX (PAC)

The PAC provides bus-control signals, address paths, and data paths for transfers between the processor's host bus, PCI bus, the A.G.P., and main memory. The PAC features:

- Processor interface control
  - Support for processor host bus frequencies of 100 MHz and 66 MHz
  - 32-bit addressing
  - Desktop Optimized GTL+ compliant host bus interface
- Integrated DRAM controller, with support for
  - +3.3 V only DIMM DRAM configurations
  - Up to three double-sided DIMMs
  - Synchronous 100-MHz or 66-MHz SDRAM
  - DIMM serial presence detect via SMBus interface
  - 16- and 64-Mbit devices with 2 KB, 4 KB, and 8 KB page sizes
  - x 4, x 8, x 16, and x 32 DRAM widths
  - SDRAM 64-bit data interface with ECC support
  - Symmetrical and asymmetrical DRAM addressing
- A.G.P. Interface
  - Complies with the A.G.P. specification (see Section 6.2 for specification information)
  - Support for +3.3 V A.G.P.-66/133 devices
  - Synchronous coupling to the host bus frequency
- PCI bus interface
  - Complies with the PCI specification Rev. 2.1, +5 V 33-MHz interface (see Section 6.2 for specification information)
  - Asynchronous coupling to the host-bus frequency
  - PCI parity generation support
  - Data streaming support from PCI-to-DRAM
  - Support for five PCI bus masters in addition to the host and PCI-to-ISA I/O bridge
  - Support for concurrent host, A.G.P., and PCI transactions to main memory
- Data buffering
  - DRAM write buffer with read-around-write capability
  - Dedicated host-to-DRAM, PCI0-to-DRAM, and PCI1/A.G.P.-to-DRAM read buffers
  - A.G.P. dedicated inbound/outbound FIFOs (133/66 MHz), used for temporary data storage

- Power management functions
  - Support for system suspend/resume (DRAM and power-on suspend)
  - Compliant with ACPI power management
- SMBus support for desktop management functions
- Support for system management mode (SMM)

1.7.2 Intel 82371EB (PIIX4E)

The PIIX4E is a multifunctional PCI device implementing the PCI-to-ISA bridge, PCI IDE functionality, Universal Serial Bus (USB) host/hub functionality, and enhanced power management. The PIIX4E features:

- Multifunctional PCI-to-ISA bridge
  - Support for the PCI bus at 33 MHz
  - PCI specification compliant (see Section 6.2 for specification information)
  - Full ISA bus support
- USB controller
  - Two USB ports (see Section 6.2 for specification information)
  - Support for legacy keyboard and mouse
  - Support for Universal Host Controller Interface (UHCI) Design Guide (see Section 6.2 for specification information)
- Integrated dual-channel enhanced IDE interface
  - Support for up to four IDE devices
  - PIO Mode 4 transfers at up to 16 MB/sec
  - Support for Ultra DMA/33 synchronous DMA mode transfers up to 33 MB/sec
  - Bus master mode with an 8 x 32-bit buffer for bus master PCI IDE burst transfers
- Enhanced DMA controller
  - Two 8237-based DMA controllers
  - Support for PCI DMA with three PC/PCI channels and distributed DMA protocols
  - Fast type-F DMA for reduced PCI bus usage
- Interrupt controller based on 82C59
  - Support for 15 interrupts
  - Programmable for edge/level sensitivity
- Power management logic
  - Sleep/resume logic
  - Support for wake on modem, Wake on LAN technology, and wake on power management event (PME)
  - Support for ACPI. See Section 6.2 for specification information
- Real-Time Clock
  - 256-byte battery-backed CMOS SRAM
  - Date alarm
- 16-bit counters/timers based on 82C54

1.7.3 A.G.P.

The A.G.P. is a high-performance bus for graphics-intensive applications, such as 3-D applications. A.G.P., while based on the *PCI Local Bus Specification*, Rev. 2.1, is independent of the PCI bus and is intended for exclusive use with graphical display devices. A.G.P. overcomes certain limitations of the PCI bus related to handling large amount of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent bus efficiency
- AC timing for 133-MHz data transfer rates, allowing real data throughput in excess of 500 MB/sec

For more information on the A.G.P., please refer to the *Accelerated Graphics Port Interface Specification* listed in Section 6.2.

1.7.4 USB

The motherboard has two USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The motherboard fully supports the UHCI and uses UHCI-compatible software drivers. See Section 6.2 for information about the USB specification. USB features include:

- Self-identifying peripherals that can be plugged in while the computer is running
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

NOTE

Computers that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

1.7.5 IDE Support

The motherboard has two independent bus-mastering PCI IDE interfaces. These interfaces support PIO Mode 3, PIO Mode 4, ATAPI device (CD-ROM, for example), and Ultra DMA/33 synchronous-DMA mode transfers. The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The BIOS automatically detects the IDE device transfer rate and translation mode.

The motherboard also supports laser servo (LS-120) drives. LS-120 technology allows the user to perform read/write operations to LS-120 (120 MB) and conventional 1.44 MB and 720 KB diskettes. An optical servo system is used to precisely position a dual-gap head to access the diskette's 2,490 tracks per inch (tpi) containing up to 120 MB of data storage. A conventional diskette uses 135 tpi for 1.44 MB of data storage.

LS-120 drives are ATAPI-compatible and connect to the motherboard's IDE interface. (LS-120 drives are also available with SCSI and parallel port interfaces.) Some versions of Windows† 95 and Windows NT† operating systems recognize the LS-120 drive as a bootable device in both 120 MB and 1.44 MB modes.

Connection of an LS-120 drive and a standard 3.5-inch diskette drive is allowed. The LS-120 drive can be configured as a boot device if selected in the Setup program.

NOTE

If you connect an LS-120 drive to an IDE connector and configure it as the boot drive and configure a standard 3.5-inch diskette drive as a B drive, the standard diskette drive is not seen by the operating system. If the LS-120 drive is configured as the boot device, the system will recognize it as both the A and B drive.

1.7.6 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multicentury calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

The time, date, and CMOS values can be specified in the Setup program. The CMOS values can be returned to their defaults by using the Setup program.

An external coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3.3 V standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 V applied.

1.8 I/O Controller

The motherboard uses the SMC FDC37C777 I/O controller which features:

- ISA Plug-and-Play compatible register set
- Two serial ports
- An interface for one floppy diskette drive
- FIFO support on both serial and diskette drive interfaces
- One parallel port with ECP and EPP support
- PS/2† style mouse and keyboard interfaces
- PCI PME interface
- Intelligent auto power management, including:
  - Shadowed write-only registers for ACPI compliance
  - Programmable wake-up event interface

The Setup program provides configuration options for the I/O controller.

1.8.1 Serial Ports

Two 9-pin D-Sub serial port connectors are located on the back panel and are compatible with 16450 and 16550A UARTs. The UARTs support data transfers at speeds up to 115.2 Kbits/sec with BIOS support.

1.8.2 Parallel Port

The connector for the multimode bi-directional parallel port is a 25-pin D-Sub connector located on the back panel. In the Setup program, the parallel port can be configured for the following:

- Compatible (standard mode)
- Bi-directional (PS/2 compatible)
- Extended Parallel Port (EPP)
- Enhanced Capabilities Port (ECP)

1.8.3 Diskette Drive Controller

The I/O controller supports a single diskette drive that is compatible with the 82077 diskette drive controller and supports both PC-AT† and PS/2 modes. In the Setup program, the diskette drive interface can be configured for the following diskette drive capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.2 MB, 3.5-inch (driver required)
- 1.25/1.44 MB, 3.5-inch
- 2.88 MB, 3.5-inch

1.8.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, re-establishes the connection after an over-current condition is removed.

NOTE

The mouse and keyboard can be plugged into either of the PS/2 connectors. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the keyboard and mouse controller code that provides the keyboard and mouse control functions and supports password protection for power on/reset. A power on/reset password can be specified in Setup.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del> for a software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power-On Self Test (POST).

1.8.5 Infrared Support

On the front panel I/O connector, there are six pins that support Hewlett-Packard HSDL-1000 compatible infrared (IR) transmitters and receivers. In the Setup program, Serial Port B can be directed to a connected IR device. The connection can be used to transfer files to or from portable devices like laptops, PDAs, and printers. The Infrared Data Association (IrDA) specification supports data transfers of 115 Kbits/sec at a distance of 1 meter. See Section 6.2 for information about the IrDA specification.

1.9 Intel EtherExpress™ PRO/100 WfM PCI LAN Subsystem

The Intel EtherExpress™ PRO/100 WfM PCI LAN subsystem is an Ethernet† LAN interface that provides both 10Base-T and 100Base-TX connectivity. Features include:

- 32-bit direct bus mastering on the PCI bus
- Shared memory structure in the host memory that copies data directly to/from the host memory
- 10Base-T and 100Base-TX capability using a single RJ-45 connector
- IEEE 802.3µ Auto-Negotiation for the fastest available connection
- Jumperless configuration; the LAN subsystem is completely software configurable

1.9.1 Intel 82558 LAN Controller

The Intel 82558 LAN controller provides the following functions:

- CSMA/CD Protocol Engine
- PCI bus interface (Rev 2.1 compliant)
- DMA engine for movement of commands, status, and network data across the PCI bus
- Integrated physical layer interface, including:
  - Complete functionality necessary for the 10Base-T and 100Base-TX interfaces; when in 10 Mbit/sec mode, the interface drives the cable directly
  - A complete set of MII management registers for control and status reporting
  - 802.3µ Auto-Negotiation for automatically establishing the best operating mode when connected to other 10Base-T or 100Base-TX devices
- Integrated power management features, including:
  - Support for ACPI
  - Support for Wake on LAN technology
- Digitally controlled adaptive equalizations and transmission

1.9.2 Alert on LAN Component

The Alert on LAN component is a companion device to the Intel 82558 LAN controller. Together, these devices provide a management interface between a remote management console (or management server) and client system monitoring instrumentation. When an alert input is asserted, the Alert on LAN component transmits Ethernet packets to the 82558 through an 8-bit dedicated data path. Examples of events that can trigger alert messages to a management server include:

- Chassis intrusion
- System BIOS hang (transmits a POST error code)
- LAN leash (transmits an alert that the LAN cable was disconnected)

For more information on the Alert on LAN component and its network management capabilities, contact your local Intel sales office.

1.9.3 LAN Subsystem Software

The EtherExpress PRO/100 WfM PCI LAN software provided includes setup/diagnostic software (SETUP.EXE), a readme file viewer (README.EXE) and the drivers listed in Table 1. The LAN software is available from Intel's World Wide Web site (see Section 6.1).

Table 1. EtherExpress PRO/100 WfM PCI Drivers

Driver	Description	Environment(s)
E100BODI.COM	Novell ODI	NetWare† DOS Client
E100BODI.SYS	Novell ODI	NetWare OS/2† Client
E100B.LAN	Novell ODI	NetWare 3.11 Server NetWare 3.12 Server NetWare 4.0x Server NetWare NT Requester NetWare for OS/2
E100B.DOS	NDIS 2.0.1	Windows for Workgroups 3.11 MS-DOS† LANMAN 2.1
E100B.OS2	NDIS 2.0.1	MS OS/2 1.3 IBM OS/2 2.11 IBM OS/2 Warp†
E100B.SYS	NDIS 3.X	Windows 95 Windows NT 3.5x
E100BNT.SYS	NDIS 4.0	Windows NT 4.0

1.10 Hardware Monitor Subsystem

The hardware monitor subsystem provides low-cost instrumentation capabilities. The features of the hardware monitor subsystem include:

- Management Level 4 functionality

- Hardware Monitor ASIC
  - Integrated temperature and voltage monitoring to detect levels above or below acceptable values (+12 V, -12 V, +5 V, +3.3 V, and +2.5 V). When the acceptable values for temperature, fan speed, or voltage are exceeded, an interrupt is activated.
  - Two fan speed sensors.
  - Access through the SMBus.
- Remote reset capabilities from a remote peer or server through Intel LANDesk® Client Manager 3.3 (or later) and service layers
- Chassis intrusion connector

The hardware monitor subsystem supports a chassis security feature: if the chassis cover is removed, a System Management Interrupt (SMI) is logged. For the chassis intrusion circuit to function, the chassis' power supply must be connected to AC power. The security feature uses a mechanical switch on the chassis that is attached to motherboard's 1 x 2-pin chassis intrusion connector (J2D2). Electrically, the mechanical switch is open for normal computer operation. See Section 1.14 for the location and pinouts of the chassis intrusion connector.

1.11 Wake on LAN Technology Connector

Wake on LAN technology enables remote wakeup of the computer through a network. If a PCI network interface card (NIC) with remote wakeup capability is installed, the remote wakeup header on the NIC must be connected to the onboard Wake on LAN technology connector. The NIC monitors network traffic at the MII interface; upon detecting a Magic Packet†, the NIC asserts a wakeup signal that powers up the computer. See Section 1.14 for the location and pinouts of the Wake on LAN technology connector.

⚠ CAUTION

For Wake on LAN technology, the 5 V standby line for the power supply must be capable of delivering +5 V ± 5 % at 720 mA. Failure to provide adequate standby current when implementing Wake on LAN can damage the power supply.

1.12 Wake on Ring

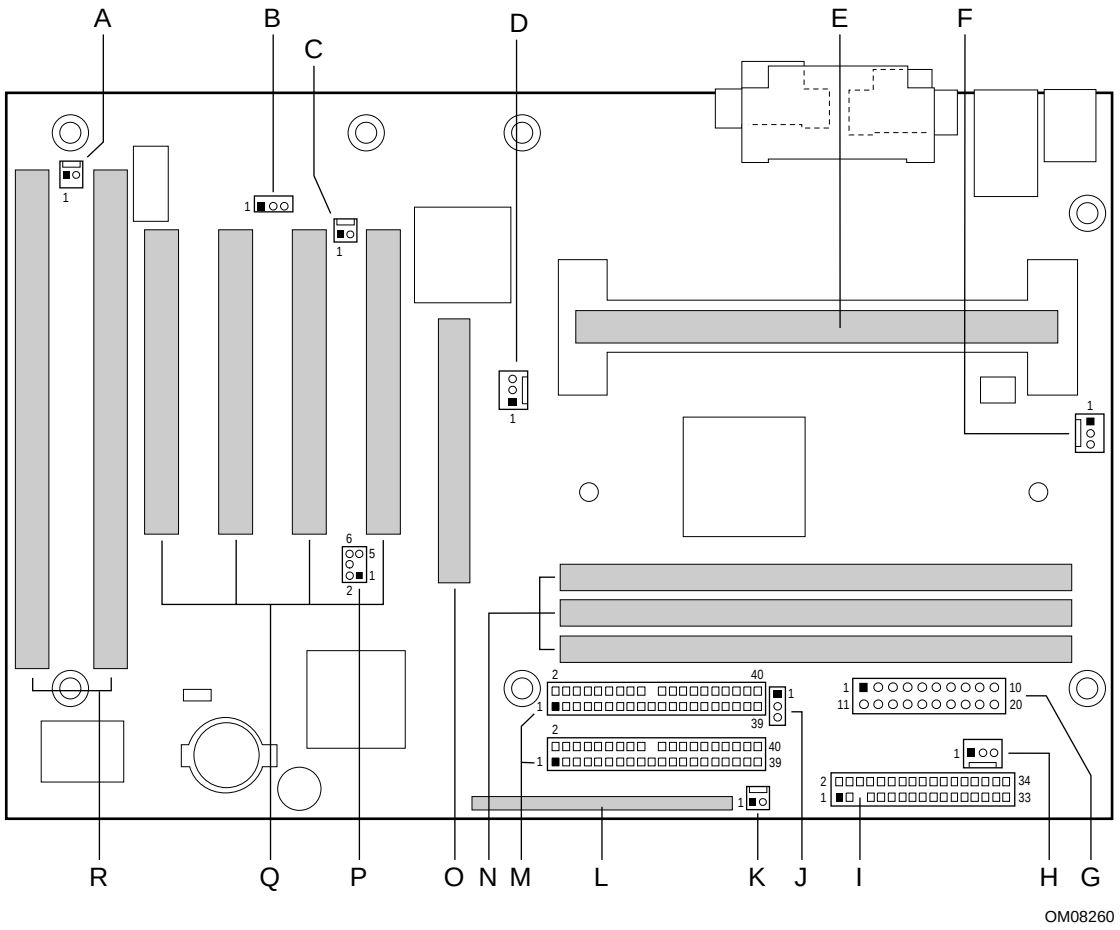
Wake on ring enables the computer to wake from sleep or soft-off mode when a call is received on a telephony device, such as a modem. If using an external modem, configure Serial Port A as COM1. If using an internal modem, insert the modem's wake on ring cable into the motherboard's wake on ring connector and configure the modem for operation on COM1. The first incoming call powers up the computer. A second call must be made to access the computer. See Section 1.14 for the location and pinouts of the motherboard's wake on ring connector.

1.13 PC/PCI Header

The PC/PCI header is a 2 x 3-pin header (J6D1) that may be used by some PCI add-in boards that require ISA DMA functionality. The most common example of this would be a PCI audio card. The ISA DMA functionality is required for true Sound Blaster† compatibility.

1.14 Motherboard Connectors

The following figure shows the location of the motherboard connectors.



A	Wake on ring connector	J	Sleep LED header
B	Wake on LAN technology header	K	SCSI hard disk LED header
C	Chassis intrusion connector	L	Front panel connectors
D	Fan 3 header (active heatsink fan)	M	IDE connectors
E	Slot 1 connector	N	DIMM sockets
F	Fan 2 header (chassis fan)	O	A.G.P. connector
G	Power connector	P	PC/PCI header
H	Fan 1 header (chassis fan)	Q	PCI connectors
I	Diskette drive connector	R	ISA connectors

Figure 4. Motherboard Connectors

Table 2. Wake on Ring Header (J1A1)

Pin	Signal Name
1	Ground
2	RINGA#

Table 3. Wake on LAN Technology Header (J2C1)

Pin	Signal Name
1	+5 VSB
2	Ground
3	WOL

Table 4. Chassis Intrusion Connector (J2D2)

Pin	Signal Name
1	Ground
2	CHS_SEC

Table 5. Fan 3 (Active Heatsink Fan) Header (J4F1)

Pin	Signal Name
1	Ground
2	+12 V
3	Ground

Table 6. Fan 2 (Chassis Fan) Header (J4M1)

Pin	Signal Name
1	Ground
2	Fan_Opamp (12 V, 300 mA max.)
3	Fan2_Tach (open collector, pulled up to 12 V)

Table 7. Fan 1 (Chassis Fan) Header (J8L1)

Pin	Signal Name
1	Ground
2	Fan_Opamp (12 V, 300 mA max.)
3	Fan1_Tach (open collector; pulled up to 12 V)

Table 8. SCSI Hard Disk LED Header (J8J1)

Pin	Signal Name
1	SCSI_ACT#
2	No connect

Table 9. PC/PCI Header (J6D1)

Pin	Signal Name	Pin	Signal Name
1	P_PCIGNTA#	2	Ground
3	No connect	4	P_PCIREQA#
5	Ground	6	SER_IRQ

Table 10. Diskette Drive Connector (J8K1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	+5 V
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	+5 V
17	No connect	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	No connect	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

Table 11. PCI IDE Connectors (J7G1, J8G1)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	P_ALE (Cable Select pullup)
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	Address 1	34	Reserved
35	Address 0	36	Address 2
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

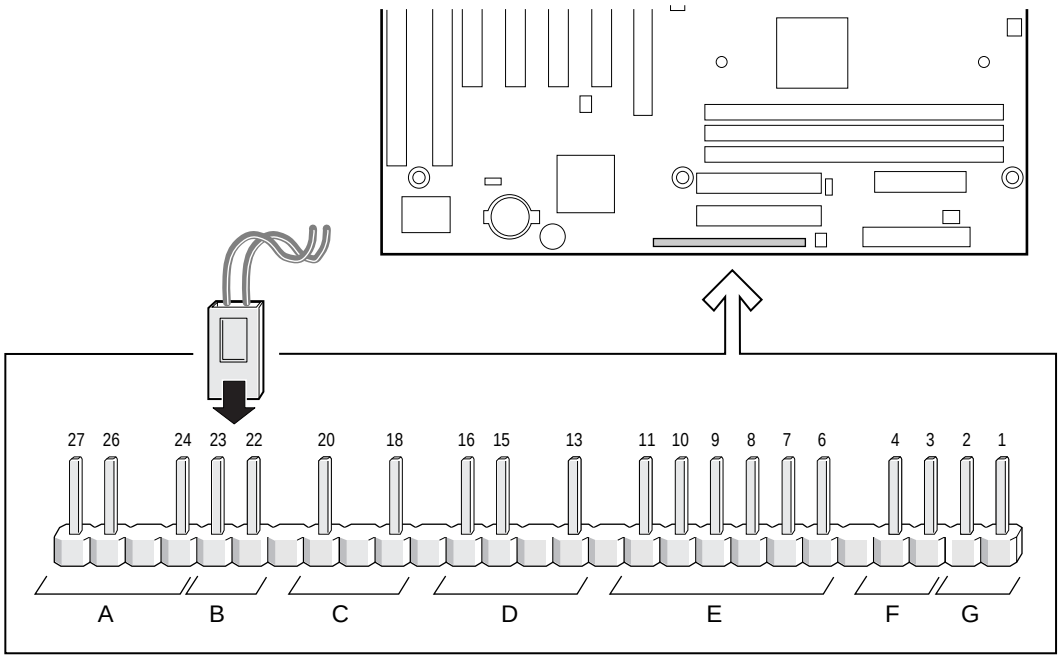
NOTE: Signal names in brackets ([ ]) are for the secondary IDE connector.

Table 12. A.G.P. Connector (J4E1)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	+12V	B1	No Connect	A34	Vcc3.3	B34	Vcc3.3
A2	No Connect	B2	Vcc	A35	AD22	B35	AD21
A3	Reserved	B3	Vcc	A36	AD20	B36	AD19
A4	No Connect	B4	No Connect	A37	Ground	B37	Ground
A5	Ground	B5	Ground	A38	AD18	B38	AD17
A6	INTA#	B6	INTB#	A39	AD16	B39	C/BE2#
A7	RST#	B7	CLK	A40	Vcc3.3	B40	Vcc3.3
A8	GNT1#	B8	REQ#	A41	FRAME#	B41	IRDY#
A9	Vcc3.3	B9	Vcc3.3	A42	Reserved	B42	3.3 V Auxiliary
A10	ST1	B10	ST0	A43	Ground	B43	Ground
A11	Reserved	B11	ST2	A44	Reserved	B44	Reserved
A12	PIPE#	B12	RBF#	A45	Vcc3.3	B45	Vcc3.3
A13	Ground	B13	Ground	A46	TRDY#	B46	DEVSEL#
A14	No Connect	B14	No Connect	A47	STOP#	B47	Vcc3.3
A15	SBA1	B15	SBA0	A48	PME#	B48	PERR#
A16	Vcc3.3	B16	Vcc3.3	A49	Ground	B49	Ground
A17	SBA3	B17	SBA2	A50	PAR	B50	SERR#
A18	Reserved	B18	SB_STB	A51	AD15	B51	C/BE1#
A19	PME#	B19	Ground	A52	Vcc3.3	B52	Vcc3.3
A20	SBA5	B20	SBA4	A53	AD13	B53	AD14
A21	SBA7	B21	SBA6	A54	AD11	B54	AD12
A22	Key	B22	Key	A55	Ground	B55	Ground
A23	Key	B23	Key	A56	AD9	B56	AD10
A24	Key	B24	Key	A57	C/BE0#	B57	AD8
A25	Key	B25	Key	A58	Vcc3.3	B58	Vcc3.3
A26	AD30	B26	AD31	A59	Reserved	B59	AD_STB0
A27	AD28	B27	AD29	A60	AD6	B60	AD7
A28	Vcc3.3	B28	Vcc3.3	A61	Ground	B61	Ground
A29	AD26	B29	AD27	A62	AD4	B62	AD5
A30	AD24	B30	AD25	A63	AD2	B63	AD3
A31	Ground	B31	Ground	A64	Vcc3.3	B64	Vcc3.3
A32	Reserved	B32	AD_STB1	A65	AD0	B65	AD1
A33	C/BE3#	B33	AD23	A66	SMB0	B66	SMB1

1.14.1 Front Panel Connectors

Figure 5 shows the locations of the front panel connectors and Table 13 lists the connectors' signals.



A	Speaker	E	Infrared (IrDA) port
B	Reset switch	F	Sleep/resume switch
C	Sleep/power/message waiting LED	G	Power switch
D	Hard drive activity LED		

Figure 5. Front Panel I/O Connectors

Table 13. Front Panel I/O Connectors

Connector	Pin	Signal Name	Connector	Pin	Signal Name
A. Speaker	27	SPKR_HDR	none	12	No connect
	26	PIEZO_IN	E. IrDA port	11	Reserved
	25	Key		10	IrTX
	24	Ground		9	Ground
B. Reset switch	23	SW_RST		8	IrRX
	22	Ground		7	Key
none	21	No connect/Key		6	+5 V
C. Sleep/power/message waiting LED	20	PWR_LED (5 V, 15 mA max.)	none	5	No connect
	19	Key	F. Sleep/resume switch	4	SLEEP_PU (pullup)
	18	Ground		3	SLEEP
none	17	No connect/Key	G. Power switch	2	Ground
D. Hard drive activity LED	16	HD_PWR (5 V, 15 mA max.)		1	SW_ON#
	15	HD Active#			
	14	Key			
	13	HD_PWR +5 V			

1.14.1.1 Speaker

A piezoelectric speaker is installed on the motherboard. The speaker provides error beep code information during the POST. An offboard speaker can be connected in parallel with the onboard speaker.

1.14.1.2 Reset Switch

This header can be connected to a momentary SPST-type switch that is normally open. When the switch is closed, the motherboard resets and runs the POST.

1.14.1.3 Sleep/Power/Message Waiting LED

This header can be connected to a single- or dual-colored LED. Table 14 shows the possible states for a single-colored LED. Table 15 shows the possible states for a dual-colored LED.

Table 14. States for a Single-colored Power LED (J7L1)

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting

Table 15. States for a Dual-colored Power LED (J7L1)

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting
Steady Yellow	Sleeping
Blinking Yellow	Sleeping/message waiting

1.14.1.4 Hard Drive Activity LED

This header can be connected to an LED to provide a visual indicator that data is being read from or written to an IDE hard drive. For the LED to function properly, the IDE drive must be connected to the onboard IDE controller. This LED will also show activity for devices connected to the SCSI hard drive LED header. See Section 1.14.3 for information about the SCSI hard drive LED header.

1.14.1.5 Infrared Port

Serial Port B can be configured to support an IrDA module connected to this 6-pin header. After the IrDA interface is configured, files can be transferred to or from portable devices such as laptops, PDAs, and printers using application software.

1.14.1.6 Sleep/Resume Switch

When APM is enabled in the system BIOS, and the operating system's APM driver is loaded, the system can enter sleep (standby) mode in one of the following ways:

- Optional front panel sleep/resume button
- Prolonged system inactivity using the BIOS inactivity timer feature (see Section 4.5)

The 2-pin header located on the front panel I/O connector supports a front panel sleep/resume switch, which must be a momentary SPST type that is normally open.

Closing the sleep/resume switch sends a System Management Interrupt (SMI) to the processor, which immediately goes into System Management Mode (SMM). While the system is in sleep mode it is fully capable of responding to and servicing external interrupts (such as an incoming fax) even though the monitor turns on only if a keyboard or mouse interrupt occurs. To reactivate or resume the system, the sleep/resume switch must be pressed again, or the keyboard or mouse must be used.

1.14.1.7 Power Switch

This header can be connected to a front panel power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the motherboard.) At least two seconds must pass before the power supply will recognize another on/off signal.

1.14.2 Power Connector

When used with an ATX-compliant power supply that supports remote power on/off, the motherboard can turn off the system power through software control. See Section 6.2 for information about the ATX specification.

To enable soft-off control in software, advanced power management must be enabled in the Setup program and in the operating system. When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

Table 16. Power Connector (J7L1)

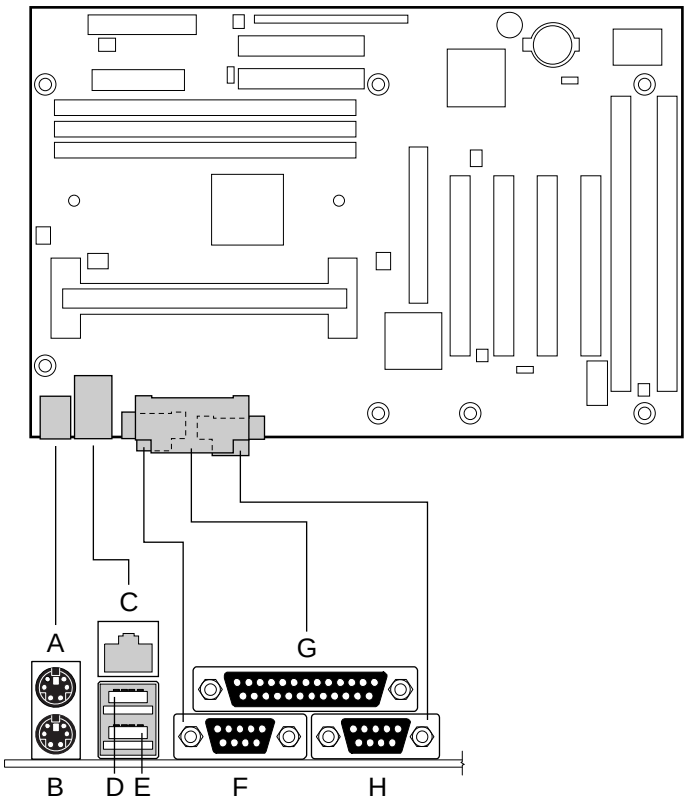
Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off control)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	-5 V
9	+5 VSB	19	+5 V
10	+12 V	20	+5 V

1.14.3 SCSI Hard Disk LED Header

The SCSI hard disk LED header is a 1 x 2-pin header (J8J1) that allows add-in SCSI controller applications to use the same LED as the IDE controller. This header can be connected to the LED output of the add-in controller card. The LED will indicate when data is being read or written using the add-in controller. See Section 1.14.1.4 for information about the onboard IDE hard drive LED header. See page 24 for the SCSI hard disk LED header pinouts.

1.14.4 Back Panel Connectors

Figure 6 shows the location of the back panel I/O connectors.



A	PS/2 keyboard/mouse	E	USB port 1
B	PS/2 keyboard/mouse	F	Serial port A
C	RJ-45 LAN	G	Parallel port
D	USB port 0	H	Serial port B

Figure 6. Back Panel I/O Connectors

Table 17. PS/2 Keyboard/Mouse Connectors

Pin	Signal Name
1	Data
2	No connect
3	Ground
4	+5 V (fused)
5	Clock
6	No connect

Table 18. RJ-45 LAN Connector

Pin	Signal Name
1	TX+
2	TX-
3	RX+
4	No connect
5	No connect
6	RX-
7	No connect
8	No connect

Table 19. USB Connectors

Pin	Signal Name
1	Power
2	USBP0# [USBP1#]
3	USBP0 [USBP1]
4	Ground

Signals names in brackets ([]) are for the USB port 1 connector.

Table 20. Parallel Port Connector

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data bit 0	15	Fault#
3	Data bit 1	16	INIT#
4	Data bit 2	17	SLCT IN#
5	Data bit 3	18	Ground
6	Data bit 4	19	Ground
7	Data bit 5	20	Ground
8	Data bit 6	21	Ground
9	Data bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Error	25	Ground
13	Select		

Table 21. Serial Port Connectors

Pin	Signal Name	Pin	Signal Name
1	DCD	6	DSR
2	Serial In #	7	RTS
3	Serial Out #	8	CTS
4	DTR#	9	RI
5	Ground		

1.14.5 Add-in Board Connectors

There are three PCI slots, one ISA slot, and one shared slot (for a PCI or ISA card). The PCI bus supports up to four bus masters through the four PCI connectors (see Section 6.2 for information about compliance with the PCI specification).

Table 22. PCI Bus Connectors

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground (TRST#)*	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK)*	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS)*	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI)*	B4	no connect (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	no connect (PRSNT1#)*	A40	+5 V (SDONE)*	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	+5 V (SBO#)*	B41	+3.3 V
A11	Reserved	B11	no connect (PRSNT2#)*	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	Reserved	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

* These signals (in parentheses) are optional in the PCI specification and are not currently implemented.

Table 23. ISA Bus Connectors

Pin	Signal Name	Pin	Signal Name
B1	Ground	A1	IOCHK# (IOCHCK#)
B2	RESET (RESDRV)	A2	SD7
B3	+5 V	A3	SD6
B4	IRQ9	A4	SD5
B5	-5 V	A5	SD4
B6	DRQ2	A6	SD3
B7	-12 V	A7	SD2
B8	SRDY# (NOWS#)	A8	SD1
B9	+12 V	A9	SD0
B10	Ground	A10	IOCHRDY (CHRDY)
B11	SMEMW# (SMWTC#)	A11	AEN
B12	SMEMR# (SMRDC#)	A12	SA19
B13	IOW# (IOWC#)	A13	SA18
B14	IOR# (IORC#)	A14	SA17
B15	DACK3#	A15	SA16
B16	DRQ3	A16	SA15
B17	DACK1#	A17	SA14
B18	DRQ1	A18	SA13
B19	REFRESH#	A19	SA12
B20	BCLK	A20	SA11
B21	IRQ7	A21	SA10
B22	IRQ6	A22	SA9
B23	IRQ5	A23	SA8
B24	IRQ4	A24	SA7
B25	IRQ3	A25	SA6
B26	DACK2#	A26	SA5
B27	TC	A27	SA4
B28	BALE	A28	SA3
B29	+5 V	A29	SA2
B30	OSC	A30	SA1
B31	Ground	A31	SA0
Key		Key	
D1	MEMCS16# (M16#)	C1	SBHE#
D2	IOCS16# (IO16#)	C2	LA23
D3	IRQ10	C3	LA22

Note: Items in parentheses are alternate versions of signal names.

continued

Table 23. ISA Bus Connectors (continued)

Pin	Signal Name	Pin	Signal Name
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19
D7	IRQ14	C7	LA18
D8	DACK0#	C8	LA17
D9	DRQ0	C9	MEMR# (MRDC#)
D10	DACK5#	C10	MEMW# (MWTC#)
D11	DRQ5	C11	SD8
D12	DACK6#	C12	SD9
D13	DRQ6	C13	SD10
D14	DACK7#	C14	SD11
D15	DRQ7	C15	SD12
D16	+5 V	C16	SD13
D17	Master16# (MASTER#)	C17	SD14
D18	Ground	C18	SD15

Note: Items in parentheses are alternate versions of signal names.

1.15 Jumper Settings

The configuration header (J7B1) requires a single jumper to set the configuration mode for the Setup program. This allows all motherboard configuration to be done in Setup. The following figure shows the location of the configuration header on the motherboard.

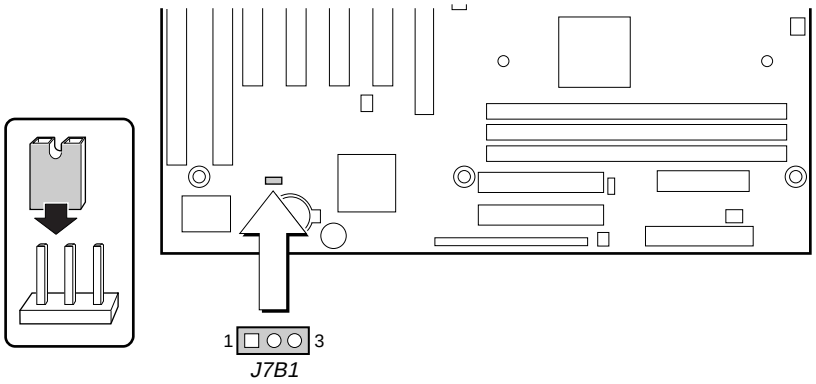


Figure 7. Configuration Header

Table 24. Jumper Settings for Configuration Header

Function / mode	Jumper setting	Configuration
Normal	1-2	The BIOS uses current configuration information and passwords for booting.
Configure	2-3	After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	none	The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

CAUTION

Moving the jumper with the power on may result in unreliable computer operation. Always turn off the power and unplug the power cord from the computer before changing the jumper.

NOTE

There is no jumper setting for configuring the processor speed. Set the processor speed in the Setup program using configure mode.

1.16 Reliability

The mean time between failures (MTBF) prediction is used for estimating repair rates and spare parts requirements. This prediction is calculated using component and subassembly random failure rates and is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. Data is predicted at 55 °C.

The MTBF prediction for the motherboard is 124,698 hours.

1.17 Environmental Specifications

Table 25. Environmental Specifications

Parameter	Specification		
Temperature			
Non-operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 G trapezoidal waveform		
	Velocity change of 170 inches/sec		
Packaged	Half sine 2 millisecond		
	Product Weight	**Free Fall (inches)**	**Velocity Change (inches/sec)**
	<20 lbs	36	167
	21-40 lbs	30	152
	41-80 lbs	24	136
	81-100 lbs	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz : 0.01g² Hz sloping up to 0.02 g² Hz		
	20 Hz to 500 Hz : 0.02g² Hz (flat)		
Packaged	10 Hz to 40 Hz : 0.015g² Hz (flat)		
	40 Hz to 500 Hz : 0.015g² Hz sloping down to 0.00015 g² Hz		
Humidity			
Non-operating	non-condensing		
Operating	non-condensing		

1.18 Power Consumption

Table 26 lists the power specifications for a computer that contains a motherboard with a 400-MHz Pentium II processor, 32 MB RAM, 512 KB cache, 1.44MB diskette drive, 1.6 GB IDE hard drive, 6X IDE CD-ROM drive, and A.G.P. graphics card. This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 95 desktop mode are measured at 640 x 480 x 256 colors and 60 Hz refresh rate. AC watts are measured with a Delta DPS-200PB-78A 145 W supply, nominal input voltage and frequency, with a true RMS wattmeter at the line input.

Table 26. Power Usage

Mode	AC (Watts) from 110 VAC Wall Outlet	3.3 V	5 V	12 V	-12 V
DOS prompt, APM disabled	46 W	1.64 A	3.16 A	178 mA	16.55 mA
Windows 95 desktop, APM disabled	47 W	1.59 A	3.17 A	190.5 mA	32.83 mA
Windows 95 desktop, APM enabled, in SMM	29 W	1.58 A	865 mA	156 mA	32.64 mA

For typical configurations, the motherboard is designed to operate with at least a 250 W ATX power supply (see Section 6.2 for the information on the ATX specification). A higher-wattage power supply should be used for heavily-loaded configurations. The power supply must comply with the following recommendations found in the indicated sections of the ATX specification:

- The potential relation between +3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

Table 27 lists the DC voltage tolerances for the motherboard.

Table 27. DC Voltage Tolerances

DC Voltage	Acceptable Tolerance
+3.3 V	± 5%
+5 V	± 5%
+5 VSB (standby)	± 5%
-5 V	± 10%
+12 V	± 5%
-12 V	± 10%

1.19 Thermal Considerations

The following table provides maximum component case temperatures for motherboard components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the motherboard.

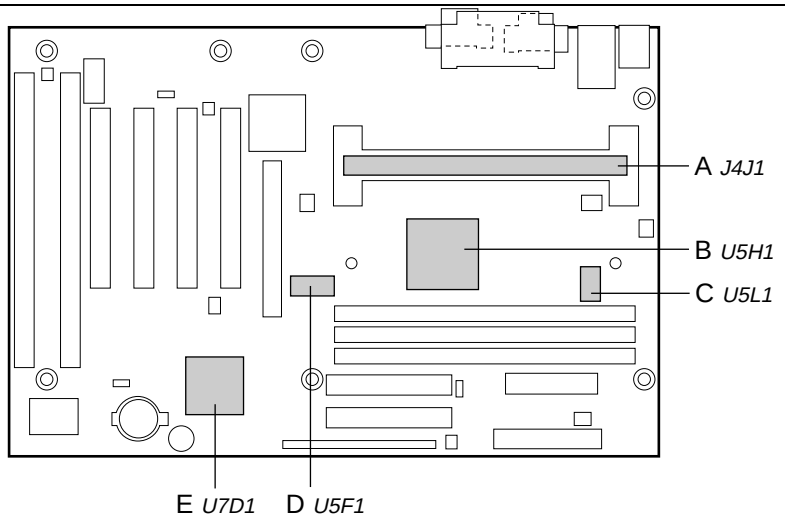
CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 5 °C to 10 °C could cause components to exceed their maximum case temperature. For information about the maximum operating temperature, see the environmental specifications in Section 1.17.

Table 28. Thermal Considerations for Components

Component	Maximum Case Temperature		Motherboard Location
Pentium II processor	233 MHz	75 °C (thermal plate)	J4J1 (Slot 1 connector)
	266 MHz	75 °C (thermal plate)	
	300 MHz	72 °C (thermal plate)	
	333 MHz	65 °C (thermal plate)	
	350 MHz	75 °C (thermal plate)	
Intel 82443BX (PAC)	105 °C		U5H1
Intel 82371EB (PIIX4E)	85 °C		U7D1
Clock generator	70 °C		U5F1
Clock generator	70 °C		U5L1

The following figure shows motherboard components that may be sensitive to thermal changes.



A Pentium II processor (in Slot 1 connector)
B Intel 82443BX
C Clock generator
D Clock generator
E Intel 82371EB

Figure 8. Thermally-Sensitive Components

1.20 Regulatory Compliance

This section describes the safety and Electromagnetic Compatibility (EMC) standards and regulations with which the MP440BX motherboard complies.

1.20.1 Safety

This printed circuit assembly complies with the following safety regulations when correctly installed in a compatible host system. Certification reports for this printed circuit assembly are maintained under File E139761, Vol. 11, Sec. 2.

1.20.1.1 UL 1950 - CSA 950-95, 3rd edition, Dated July 28, 1995

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment (USA and Canada).

1.20.1.2 UL Classified to IEC 950

See Section 1.20.1.3.

1.20.1.3 IEC 950, 2nd edition (with Amendments 1-4)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment (International).

1.20.2 Electromagnetic Compatibility (EMC)

This printed circuit assembly complies with the following EMC regulations when correctly installed in a compatible host system.

1.20.2.1 CFR 47, Parts 2 and 15

Title 47, Code of Federal Regulations; General Rules and Regulations, Radio Frequency Devices. Product compliance is verified using limits from CSIPR 22 (frequencies to 1 GHz), FCC Rules, Section 15.109(a) (frequencies above 1 GHz), and test criteria as defined in ANSI C63.4 and FCC Rules, Section 15.32(a).

1.20.2.2 CISPR 22 / EN 55 022, Dated 1993/1995, Class B

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment (International/Europe).

1.20.2.3 EN 50 082-1, Dated 1992

Generic Immunity Standard. Currently compliance is determined via testing to IEC 801-2, -3, and -4 (Europe).

1.20.3 Product Certification Markings

This printed circuit assembly has the following product certification markings:

- European CE Marking: Consists of a marking on the motherboard and shipping container.
- UL Recognition Mark: UL Safety certification is identified with the UL File No. E139761 on the component side of the motherboard and the PB number on the solder side of the motherboard. Motherboard material flammability is compliant with UL 94 and is rated V-1 or V-0.
- FCC Compliance: Consists of an FCC Declaration of Conformity on the motherboard.
- Canadian Compliance: Consists of small c followed by a stylized backward UR on the component side of the motherboard.

2 Motherboard Resources

2.1 DMA Channels

Table 29. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Open
1	8 or 16 bits	Parallel port
2	8 or 16 bits	Diskette drive
3	8 or 16 bits	Parallel port (for ECP)
4		Reserved - cascade channel
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

2.2 I/O Map

Table 30. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX4E- DMA 1
0020 - 0021	2 bytes	PIIX4E - interrupt controller 1
002E - 002F	2 bytes	I/O controller configuration registers
0040 - 0043	4 bytes	PIIX4E - Counter/Timer 1
0048 - 004B	4 bytes	PIIX4E- Counter/Timer 2
0060	1 byte	Keyboard Controller Byte - Reset IRQ
0061	1 byte	PIIX4E - NMI, Speaker Control
0064	1 byte	Keyboard controller, CMD/STAT Byte
0070, bit 7	1 bit	PIIX4E - enable NMI
0070, bits 6:0	7 bits	PIIX4E - real-time clock, address
0071	1 byte	PIIX4E - real-time clock, data
0078	1 byte	Reserved - motherboard configuration
0079	1 byte	Reserved - motherboard configuration
0080 - 008F	16 bytes	PIIX4E - DMA page registers
00A0 - 00A1	2 bytes	PIIX4E - interrupt controller 2
00B2 - 00B3	2 bytes	APM control
00C0 - 00DE	31 bytes	PIIX4E - DMA 2
00F0	1 byte	Reset numeric error

continued

Table 30. I/O Map (continued)

Address (hex)	Size	Description
0170 - 0177	8 bytes	Secondary IDE channel
01F0 - 01F7	8 bytes	Primary IDE channel
0228 - 022F	8 bytes	LPT3
0278 - 027F	8 bytes	LPT2
0290 - 0297	8 bytes	Management extension hardware
02E8 - 02EF	8 bytes	COM4/Video (8514A)
02F8 - 02FF	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0377, bits 6:0	7 bits	Secondary IDE channel status port
0378 - 037F	8 bytes	LPT1
03B4 - 03B5	2 bytes	Video (VGA†)
03BA	1 byte	Video (VGA)
03C0 - 03CA	11 bytes	Video (VGA)
03CC	1 byte	Video (VGA)
03CE - 03CF	2 bytes	Video (VGA)
03D4 - 03D5	2 bytes	Video (VGA)
03DA	1 byte	Video (VGA)
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Diskette drive Channel 1
03F6	1 byte	Primary IDE channel command port
03F7 (Write)	1 byte	Diskette drive channel 1 command
03F7, bit 7	1 bit	Diskette drive disk change channel 1
03F7, bits 6:0	7 bits	Primary IDE channel status port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
LPT*n* + 400h	8 bytes	ECP port, LPT*n* base address + 400h
0CF8 - 0CFB*	4 bytes	PCI configuration address register
0CF9**	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
FF00 - FF07	8 bytes	IDE bus master register
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers

* Doubleword access only

** Byte access only

NOTE

Table 30 does not list all I/O addresses that may be used by add-in cards in the system.

2.3 PCI Configuration Space Map

Table 31. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Intel 82443BX (PAC)
00	01	00	Intel 82443BX (PAC) A.G.P. bus
00	06	00	PCI LAN
00	07	00	Intel 82371EB (PIIX4E) PCI ISA bridge
00	07	01	Intel 82371EB (PIIX4E) IDE bus master
00	07	02	Intel 82371EB (PIIX4E) USB
00	07	03	Intel 82371EB (PIIX4E) power management
00	0D	00	PCI expansion slot 1 (J4D2)
00	0E	00	PCI expansion slot 2 (J4D1)
00	0F	00	PCI expansion slot 3 (J4C1)
00	10	00	PCI expansion slot 4 (J4B1)

2.4 Interrupts

Table 32. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2*
4	COM1*
5	LPT2 (Plug and Play option) / user available
6	Diskette drive
7	LPT1*
8	Real-time clock
9	Reserved
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

* Default, but can be changed to another IRQ

2.5 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI expansion slots and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The PIIX4E PCI-to-ISA bridge has four programmable interrupt request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the motherboard and therefore share the same interrupt. Table 33 lists the PIRQ signals and shows how the signals are connected to the onboard PCI interrupt sources.

Table 33. PCI Interrupt Routing Map

PIIX4E PIRQ Signal	PCI Slot 1: J4D2	PCI Slot 2: J4D1	PCI Slot 3: J4C1	PCI Slot 4: J4B1	A.G.P. Slot: J4E1	USB	LAN	Power Mgmt
PIRQA	INTA	INTD	INTC	INTB				INTA
PIRQB	INTB	INTA	INTD	INTC	INTA			
PIRQC	INTC	INTB	INTA	INTD	INTB		INTA	
PIRQD	INTD	INTC	INTB	INTA		INTA		

For example, assume an add-in card has one interrupt (group INTA) and is plugged into the fourth PCI slot. In this slot, an interrupt source from group INTA connects to the PIRQD signal, which is already connected to the onboard USB PCI source. Therefore, the add-in card shares an interrupt with this onboard interrupt source.

Now, however, plug an add-in card that has one interrupt (group INTA) into the first PCI slot. Plug a second add-in card that has two interrupts (groups INTA and INTB) into the second PCI slot. INTA in the first slot is connected to signal PIRQA. INTA in the second slot is connected to signal PIRQB, and INTB is connected to signal PIRQC. With no other cards added, the three interrupt sources on the first two cards each have a PIRQ signal to themselves. Typically, they will not share an interrupt.

NOTE

The PIIX4E can connect each PIRQ line internally to one IRQ signal (3, 4, 5, 7, 9, 11, 14, or 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

3 Overview of BIOS Features

The motherboard uses an Intel/Phoenix BIOS, which is stored in flash memory and can be upgraded using a disk-based program. In addition to the BIOS, the flash memory contains the Setup program, POST, APM, the PCI auto-configuration utility, and Windows 95-ready Plug and Play. See Section 6.2 for the supported versions of the APM, PCI, Phoenix BIOS, and Plug and Play specifications.

This motherboard supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the BIOS type and revision code. The initial production BIOS is identified as 4M4PB0X1.86A.

3.1 BIOS Upgrades

The BIOS can be upgraded from a diskette using the Intel Flash Memory Update utility that is available from Intel. This utility does BIOS upgrades as follows:

- Updates the flash BIOS from a file on a disk
- Updates the language section of the BIOS
- Makes sure that the upgrade BIOS matches the target system to prevent accidentally installing a BIOS for a different type of system

BIOS upgrades and the update utility are available from Intel through the Intel World Wide Web site. See Section 6.1 for information about this site.

NOTE

Please review the instructions distributed with the upgrade utility before attempting a BIOS upgrade.

3.2 4 Mbit E28F004S5 Symmetrical Flash Memory

The Intel E28F004S5 is a high performance 4 Mbit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable. Figure 9 shows the organization of the flash memory.

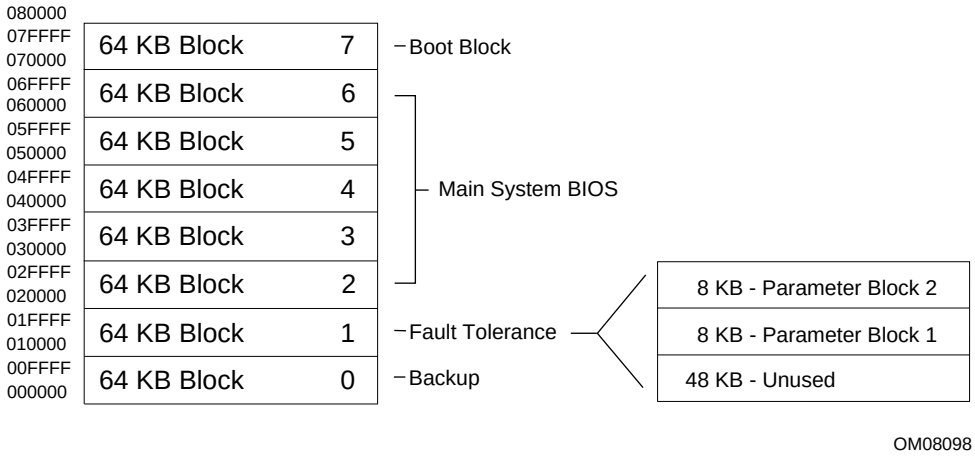


Figure 9. Memory Map of the Flash Memory Device

Symmetrical flash memory allows both the boot and the fault tolerance blocks to increase in size from 16 KB to 64 KB. This increase allows the addition of features such as Flash memory manager (FMM), dynamic memory detection, LS-120 recovery code, and extended security features.

The last two 8 KB blocks of the fault tolerance area are the parameter blocks. These blocks contain data such as microcode patches, vital product data (VPD), logo, System Management BIOS (SMBIOS) interface, and extended system configuration data (ESCD) information. The backup block contains a copy of the fault tolerance block.

3.3 Plug and Play: PCI Autoconfiguration

The BIOS automatically configures PCI devices and Plug and Play devices. PCI devices may be onboard or add-in cards. Plug and Play devices are ISA add-in cards built to meet the Plug and Play specification. Autoconfiguration lets a user insert or remove PCI or Plug and Play cards without having to configure the system. When a user turns on the system after adding a PCI or Plug and Play card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

PCI interrupts are distributed to available ISA interrupts that have not been assigned to an ISA card or to system resources. The assignment of PCI interrupts to ISA IRQs is nondeterministic. PCI devices can share an interrupt, but an ISA device cannot share an interrupt allocated to PCI or to another ISA device. Autoconfiguration information is stored in ESCD format.

For information about the versions of PCI and Plug and Play supported by this BIOS, see Section 6.2.

3.4 PCI IDE Support

If Auto is selected as a primary or secondary IDE device type (see Section 4.3.2.1) in Setup, the BIOS automatically sets up the two local-bus IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to PIO Mode 4 and recognizes any ATAPI devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 6.2 for the supported version of ATAPI). Add-in ISA IDE controllers are not supported. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for logical block addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. To override the autoconfiguration options, specify manual configuration in Setup. The ATAPI specification recommends that ATAPI devices be configured as shown in Table 34.

Table 34. Recommendations for Configuring an ATAPI Device

	Primary Cable		**Secondary Cable**	
Configuration	Drive 0	Drive 1	Drive 0	Drive 1
Normal, no ATAPI	ATA			
Disk and CD-ROM for enhanced IDE systems	ATA		ATAPI	
Legacy IDE system with only one cable	ATA	ATAPI		
Enhanced IDE with CD-ROM and a tape or two CD-ROMs	ATA		ATAPI	ATAPI

3.5 ISA Plug and Play

If Plug and Play O/S (see Section 4.3) is selected in Setup, the BIOS autoconfigures only ISA Plug and Play cards that are required for booting (IPL devices). If Plug and Play operating system is not selected in Setup, the BIOS autoconfigures all Plug and Play ISA cards.

3.6 ISA Legacy Devices

Since ISA legacy devices are not autoconfigurable, the resources for them must be reserved. Resources can be reserved in the Setup program or with an ISA configuration utility. The ISA configuration utility can be downloaded from the Intel World Wide Web site (see Section 6.1).

3.7 System Management BIOS (SMBIOS)

System Management BIOS (SMBIOS) is a Desktop Management Interface (DMI) compliant method of managing computers in an enterprise environment. SMBIOS' main component is the management information format (MIF) database, which contains information about the computing system and its components. The MIF database defines the data and provides the method for accessing this information. Using the SMBIOS interface, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The BIOS enables applications such as Intel LANDesk Client Manager to use the SMBIOS interface. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

OEMs can use a utility that programs flash memory so the BIOS can report on system and chassis information. This utility is available through Intel sales offices. See Section 6.1 for information about contacting a local Intel sales office.

Non-Plug and Play operating systems, such as Windows NT, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

See Section 6.2 for information about the latest SMBIOS specification.

3.8 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. ACPI requires an ACPI-aware operating system such as Windows NT 5.0 or Windows 98. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM functionality normally contained in the BIOS
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 30-watt system operation in the Power On Suspend sleeping state, and less than 5-watt system operation in the Suspend to Disk sleeping state
- A soft-off feature that enables the operating system to power off the computer
- Support for multiple wake up events (see Table 37)
- Support for a front panel power and sleep mode switch. Table 35 describes the system states based on how long the switch is pressed.

Table 35. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off	Less than four seconds	Power on
On	Less than four seconds	Soft off/suspend
On	More than four seconds	Fail safe power off
Sleep	Less than four seconds	Wake up

3.8.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state. Table 36 lists the power states supported by the motherboard along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 36. Power States and Targeted System Power

Global States	Sleeping States	CPU States	Device States	Targeted System Power*
G0 - working state	S0 - working	C0 - working	D0 - working state	Full power > 60 W
G1 - sleeping state	S1 - CPU stopped	C1 - stop grant	D1, D2, D3- device specification specific.	5 W < power < 30 W
G1 - sleeping state	S4BIOS - suspend to disk***. Context saved to disk.	No power	D3 - no power except for wake up logic.	power < 5 W **
G2/S5	S5 - Soft off. Context not saved. Cold boot is required.	No power	D3 - no power except for wake up logic.	power < 5 W **
G3 - mechanical off. The power supply switch is off.	No power to the system.	No power	D3 - no power for wake up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

* Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.

** Dependent on the standby power consumption of wake-up devices used in the system.

*** S3 and S4BIOS states are entered at the same time to preserve system context. In normal operation, the system restores context from RAM. In case of power failure, the system restores context from disk.

3.8.2 Wake Up Devices and Events

The table below describes which devices or specific events can wake the computer from specific states. Sleeping states S4BIOS and S5 are the same for the wake up events.

Table 37. Wake Up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S1, S4BIOS, S5
RTC alarm	S1, S4BIOS, S5
LAN	S1, S4BIOS, S5
Modem	S1, S4BIOS, S5
IR command	S1
USB	S1
PS/2 keyboard	S1
PS/2 mouse	S1

3.8.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure motherboard devices that do not have other hardware standards for enumeration and configuration. PCI devices on the motherboard, for example, are not enumerated by ACPI.

3.8.4 BIOS Support

The BIOS supports both APM and ACPI. If the board is used with an ACPI-aware operating system, the BIOS provides ACPI support. Otherwise, it defaults to APM support.

3.9 APM

The energy saving standby mode can be initiated in the following ways:

- Time-out period specified in Setup
- Suspend/resume switch connected to the front panel sleep connector
- From the operating system, such as the Suspend menu item in Windows 95

In standby mode, the motherboard reduces power consumption by spinning down hard drives and reducing power to or turning off VESA† DPMS-compliant monitors. Power-management mode can be enabled or disabled in Setup (see Section 4.5).

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default; but the operating system must support an APM driver for the power-management features to work. For example, Windows 95 supports the power-management features upon detecting that APM is enabled in the BIOS. See Section 6.2 for the version of the APM specification that is supported.

3.10 Language Support

The Setup program and help messages can be supported in 32 languages. Five languages are available: American English, German, Italian, French, and Spanish. The default language is American English, which is used unless another language is selected in the Setup program. See Section 3.1 for information about the BIOS update utility.

The BIOS includes extensions to support the Kanji character set and other non-ASCII character sets. Translations of other languages may become available at a later date.

3.11 Boot Options

In the Setup program, the user can choose to boot from a diskette drive, hard drive, CD-ROM, or the network. The default setting is for the diskette drive to be the primary boot device and the hard drive to be the secondary boot device. By default the third and fourth devices are disabled.

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. See Section 6.2 for information about the El Torito specification. Under the Boot menu in the Setup program, CD-ROM is listed as a boot device. Boot devices are defined in priority order. If the CD-ROM is selected as the boot device, it must be the first device.

The network can be selected as a boot device. This selection allows booting from a network add-in card with a remote boot ROM installed.

3.12 OEM Logo or Scan Area

A 4 KB flash-memory user area is available for displaying a custom OEM logo during POST. A utility is available from Intel to assist with installing a logo into the flash memory. Contact Intel customer support for further information. See Section 6.1 for information on contacting Intel customer support.

3.13 USB Legacy Support

USB legacy support enables USB keyboards and mice to be used even when no operating system USB drivers are in place. By default, USB legacy support is disabled. USB legacy support is only intended to be used in accessing BIOS Setup and installing an operating system that supports USB.

This sequence describes how USB legacy support operates in the default (disabled) mode.

1. When you power up the computer, USB legacy support is disabled.
2. POST begins.
3. USB legacy support is temporarily enabled by the BIOS. This allows you to use a USB keyboard to enter the Setup program or the maintenance mode.
4. POST completes and disables USB legacy support (unless it was set to Enabled while in Setup).
5. The operating system loads. While the operating system is loading, USB keyboards and mice are not detected. After the operating system loads the USB drivers, the USB devices are detected.

To install an operating system that supports USB, enable USB Legacy support in BIOS Setup and follow the operating system's installation instructions. After the operating system is installed and the USB drivers configured, USB legacy support is no longer used. USB Legacy Support can be left enabled in BIOS Setup if needed.

Notes on using USB legacy support:

- If USB legacy support is enabled, don't mix USB and PS/2 keyboards and mice. For example, do not use a PS/2 keyboard with a USB mouse, or a USB keyboard and a PS/2 mouse.
- Do not use USB devices with an operating system that does not support USB. USB legacy is not intended to support the use of USB devices in a non USB operating system.
- USB legacy support is for keyboards and mice only. Hubs and other USB devices are not supported.

3.14 BIOS Setup Program Access

The BIOS security features restrict who can access the BIOS Setup program and boot the computer. A administrator password and a user password can be set for the Setup program and for booting the computer, with the following restrictions:

- The administrator password gives unrestricted access to view and change all the Setup options in the Setup program. This is administrator mode.
- The user password gives restricted access to view and change Setup options in the Setup program. This is user mode.
- If only the administrator password is set, pressing the <Enter> key at the password prompt of the Setup program allows the user restricted access to Setup.
- If both the administrator and user passwords are set, users can enter either the administrator password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the administrator password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

3.15 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode (see Section 1.15).

To create a BIOS recovery diskette, a bootable diskette must be created and the recovery files copied to it. The recovery files are available from Intel, contact Intel customer support for further information. See Section 6.1 for information on contacting Intel customer support.

4 BIOS Setup Program

The Setup program is for viewing and changing the BIOS settings for a computer. Setup is accessed by pressing the <F2> key after the Power-On Self Test (POST) memory test begins and before the operating system boot begins.

Table 38 shows the menus available from the menu bar at the top of the Setup screen.

Table 38. Setup Menu Bar

Setup Menu Screen	Description
Maintenance	Specifies the processor speed and clears the Setup passwords. This is only available in configure mode. Refer to Section 1.15 for information about configure mode.
Main	Allocates resources for hardware components.
Advanced	Specifies advanced features available through the chipset.
Security	Specifies passwords and security features.
Power	Specifies power management features.
Boot	Specifies boot options and power supply controls.
Exit	Saves or discards changes to the Setup program options.

Table 39 shows the function keys available for menu screens.

Table 39. Setup Function Keys

Setup Key	Description
<F1> or <Alt-H>	Displays a help screen for the current item.
<Esc>	Exits the menu.
<←> or <→>	Selects a different menu screen.
<↑> or <↓>	Moves the cursor up or down.
<Home> or <End>	Moves the cursor to the top or bottom of the window.
<PgUp> or <PgDn>	Moves the cursor to the top or bottom of the window.
<F5> or <->	Selects the previous value for a field.
<F6> or <+> or <Space>	Selects the next value for a field.
<F9>	Load the default configuration values for the current menu.
<F10>	Save the current values and exit Setup.
<Enter>	Executes command or selects the submenu.

4.1 Maintenance Menu

This menu is for setting the processor speed and clearing the Setup passwords. Setup only displays this menu in configure mode. See Section 1.15 for information about setting configure mode.

Table 40. Maintenance Menu

Feature	Options	Description
Processor Speed	200 233 266 300 333 350 366 400 450	Specifies the processor speed in megahertz. This setup screen will only show speeds up to and including the maximum speed of the processor installed on the motherboard. With a host bus operating at 66 MHz, the board supports processors at the following speeds: 200, 233, 266, 300, 333, and 366 MHz. With a host bus operating at 100 MHz, the board supports processors at the following speeds: 300, 350, 400, and 450 MHz.
Clear Passwords	No options	Clears the user and administrator passwords.

4.2 Main Menu

This menu reports processor and memory information and is used for setting the system date and time.

Table 41. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed.
Cache RAM	No options	Displays size of second-level cache.
System Memory	No options	Displays the total amount of RAM on the motherboard.
Memory Bank 0 Memory Bank 1 Memory Bank 2	No options	Displays size and type of DIMM installed in each memory bank.
Language	**English (US) (default)** Italian Francais Deutch Espanol	Selects the default language used by the BIOS.
ECC Configuration	**Non-ECC (default)** ECC	Specifies ECC memory operation if ECC memory is detected.
L2 Cache ECC Support	**Disabled (default)** Enabled	Specifies L2 cache ECC operation.
System Time	Hour, minute, and second	Specifies the current time.
System Date	Month, day, and year	Specifies the current date.

4.3 Advanced Menu

This menu is for setting advanced features that are available through the chipset.

Table 42. Advanced Menu

Feature	Options	Description
Plug & Play O/S	**No (default)** Yes	Specifies if a Plug and Play operating system is being used. *No* lets the BIOS configure all devices. *Yes* lets the operating system configure Plug and Play devices. Not required with a Plug and Play operating system.
Reset Configuration Data	**No (default)** Yes	Clears the BIOS configuration data on the next boot.
Numlock	**Auto (default)** On Off	Specifies the power on state of the Num Lock feature on the numeric keypad of the keyboard.
Peripheral Configuration	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
IDE Configuration	No options	Specifies type of connected IDE device.
Floppy Configuration	No options	When selected, displays the Floppy Options submenu.
DMI Event Logging	No options	Configures DMI Events Logging. When selected, displays the DMI Events Logging submenu.
Video Configuration	No options	Configures video features. When selected, displays the Video Configuration submenu.
Resource Configuration	No options	Configures memory blocks and IRQs for legacy ISA devices. When selected, displays the Resource Configuration submenu.

4.3.1 Peripheral Configuration Submenu

This submenu is for configuring the computer peripherals.

Table 43. Peripheral Configuration Submenu

Feature	Options	Description
Serial port A	Disabled Enabled **Auto (default)**	Configures serial port A. *Auto* assigns the first free COM port, normally COM1, the address 3F8h and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address	**3F8 (default)** 2F8 3E8 2E8	Specifies the base I/O address for serial port A.
Interrupt	IRQ 3 **IRQ 4 (default)**	Specifies the interrupt for serial port A.
Serial port B	Disabled Enabled **Auto (default)**	Configures serial port B. *Auto* assigns the first free COM port, normally COM2, the address 2F8h and the interrupt IRQ3. An * (asterisk) displayed next to an address indicates a conflict with another device. If either serial port address is set, that address will not appear in the list of options for the other serial port. If an *ATI mach32*† or an *ATI mach64*† video controller is active as an add-in card, the COM4, 2E8h address will not appear in the list of options for either serial port.
Mode	**Normal (default)** IrDA ASK-IR	Specifies the mode for serial port B for normal (COM 2) or infrared applications.
Base I/O address	3F8 **2F8 (default)** 3E8 2E8	Specifies the base I/O address for serial port B.
Interrupt	**IRQ 3 (default)** IRQ 4	Specifies the interrupt for serial port B.

continued

Table 43. Peripheral Configuration Submenu (continued)

Feature	Options	Description
Parallel port	Disabled Enabled **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	Output Only **Bi-directional (default)** EPP ECP	Selects the mode for the parallel port. *Output Only* operates in AT†-compatible mode. *Bi-directional* operates in bi-directional PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bi-directional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode.
Base I/O address	**378 (default)** 278 228	Specifies the base I/O address for the parallel port.
Interrupt	IRQ 5 **IRQ 7 (default)**	Specifies the interrupt for the parallel port.
LAN	Disabled **Enabled (default)**	Enables or disables the LAN device.
Embedded PXE Support	Disabled **Enabled (default)**	Enables or disables embedded PXE support.
Legacy USB Support	**Disabled (default)** Enabled	Enables or disables USB legacy support. (See Section 3.13 for more information.)

4.3.2 IDE Configuration

This menu is for the configuring the IDE controller.

Table 44. IDE Configuration

Feature	Options	Description
IDE Controller	Disabled Primary Secondary **Both (default)**	Specifies the integrated IDE controller. *Primary* enables only the primary IDE controller. *Secondary* enables only the secondary IDE controller. *Both* enables both IDE controllers.
Hard Disk Pre-Delay	**Disabled (default)** 3 Seconds 6 Seconds 9 Seconds 12 Seconds 15 Seconds 21 Seconds 30 Seconds	Specifies the hard disk drive pre-delay.
Primary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Primary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu
Secondary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.3.2.1 IDE Configuration Submenus

This submenu is for configuring IDE devices, including:

- Primary IDE master
- Primary IDE slave
- Secondary IDE master
- Secondary IDE slave

Table 45. IDE Configuration Submenus

Feature	Options	Description
Type	None ATAPI Removable Other ATAPI CD-ROM User IDE Removable **Auto (default)**	Specifies the IDE configuration mode for IDE devices. *User* allows the cylinders, heads, and sectors fields to be changed. *Auto* automatically fills in the values for the cylinders, heads, and sectors fields.
Maximum Capacity	No options	Reports the maximum capacity for the hard disk.
Multi-Sector Transfers	**Disabled (default)** 2 Sectors 4 Sectors 8 Sectors 16 Sectors	Specifies number of sectors per block for transfers from the hard drive to memory. Check the hard drive's specifications for optimum setting.
LBA Mode Control	Disabled **Enabled (default)**	Enables or disables the LBA mode control.
Transfer Mode	**Standard (default)** Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2	Specifies the method for moving data to/from the drive.
Ultra DMA	**Disabled (default)** Mode 0 Mode 1 Mode 2	Specifies the Ultra DMA mode for the drive.

4.3.3 Floppy Options

This submenu is for configuring floppy drives.

Table 46. Floppy Options

Feature	Options	Description
Floppy Disk Controller	Disabled **Enabled (default)** Auto	Disables, enables, or automatically configures the integrated floppy disk controller.
Diskette A	Disabled 360 KB, 5¼″ 1.2 MB, 5¼″ 720 KB, 3½″ **1.44/1.25 MB, 3½″ (default)** 2.88 MB, 3½″	Specifies the capacity and physical size of diskette drive A.
Floppy Write Protect	**Disabled (default)** Enabled	Disables or enables write protect for the diskette drive(s).

4.3.4 DMI Event Logging

This submenu is for configuring the DMI event logging features.

Table 47. DMI Event Logging Submenu

Feature	Options	Description
Event log capacity	No options	Indicates if there is space available in the event log.
Event log validity	No options	Indicates if the contents of the event log are valid.
View DMI event log	No options	Enables viewing of DMI event log.
Clear all DMI event logs	**No (default)** Yes	Clears the DMI event log after rebooting.
Event Logging	Disabled **Enabled (default)**	Enables or disables logging of DMI events.
ECC Event Logging	Disabled (default) **Enabled (default)**	Enables or disables logging of ECC events.
Mark DMI events as read	No options	Marks all DMI events as read.

4.3.5 Video Configuration Submenu

This submenu is for configuring special video features.

Table 48. Video Configuration Submenu

Feature	Options	Description
Palette Snooping	**Disabled (default)** Enabled	Controls the ability of a primary PCI graphics controller to share a common palette with an ISA add-in video card.
AGP Aperture Size	**64 MB (default)** 256 MB	Specifies the aperture size for the A.G.P. video controller.

4.3.6 Resource Configuration Submenu

This submenu is for configuring the memory and interrupts.

Table 49. Resource Configuration Submenu

Feature	Options		Description
Memory Reservation	C800 - CBFF	**Available (default)** | Reserved	Reserves specific upper memory blocks for use by legacy ISA devices.
	CC00- CFFF	**Available (default)** | Reserved	
	D000 - D3FF	**Available (default)** | Reserved	
	D400 - D7FF	**Available (default)** | Reserved	
	D800 - DBFF	**Available (default)** | Reserved	
	DC00 - DFFF	**Available (default)** | Reserved	
IRQ Reservation	IRQ3	**Available (default)** | Reserved	Reserves specific IRQs for use by legacy ISA devices. An * (asterisk) displayed next to an IRQ indicates an IRQ conflict.
	IRQ4	**Available (default)** | Reserved	
	IRQ5	**Available (default)** | Reserved	
	IRQ7	**Available (default)** | Reserved	
	IRQ10	**Available (default)** | Reserved	
	IRQ11	**Available (default)** | Reserved	

4.4 Security Menu

This menu is for setting passwords and security features.

Table 50. Security Menu

Feature	Options	Description
User Password Is	No options	Reports if there is a user password set.
Administrator Password Is	No options	Reports if there is an administrator password set.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Set Administrative Password	Password can be up to seven alphanumeric characters.	Specifies the administrator password.
Clear User	No Options	Clears the user password.
User Setup Access	None **View Only (default)** Limited Access Full	*None* prevents the user from accessing Setup. *View Only* prevents the user from changing settings. *Limited Access* allows the user to change Date, Time, User Password, and Unattended Start. *Full* allows the user to change all settings.
Unattended Start	**Disabled (default)** Enabled	Enables the unattended start feature. When enabled, the computer boots, but the keyboard is locked. The user must enter a password to unlock the computer or boot from a floppy diskette.

4.5 Power Menu

This menu is for setting power management features.

Table 51. Power Menu

Feature	Options	Description
Power Management	Disabled **Enabled (default)**	Enables or disables the BIOS power management feature.
Fan Always On	**No (default)** Yes	*Yes* forces the fan to remain on when the system is in a power-managed state.
Inactivity Timer	**Off (default)** 1 Minute 5 Minutes 10 Minutes 20 Minutes 30 Minutes 60 Minutes 120 Minutes	Specifies the amount of time before the computer enters standby mode.
Hard Drive	Disabled **Enabled (default)**	Enables power management for hard disks during standby and suspend modes.
VESA Video Power Down	Disabled **Standby (default)** Suspend Sleep	Specifies power management for video during standby and suspend modes.

4.6 Boot Menu

This menu is for setting the boot features and the boot sequence.

Table 52. Boot Menu

Feature	Options	Description
Quick Boot Mode	Disabled **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	**Disabled (default)** Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
After Power Failure	Stay Off **Last State (default)** Power On	Specifies the mode of operation if an AC/Power loss occurs. *Stay Off* keeps the power off until the power button is pressed. *Last State* restores the previous power state before power loss occurred. *Power On* restores power to the computer.
On Modem Ring	Stay Off **Power On (default)**	Specifies how the computer responds to an incoming call on an installed modem when the power is off.
On LAN	Stay Off **Power On (default)**	Specifies how the computer responds to a LAN wakeup event when the power is off.
On PME	**Stay Off (default)** Power On	Specifies how the computer responds to a PME wakeup event when the power is off.
First Boot Device Second Boot Device Third Boot Device Fourth Boot Device Fifth Boot Device	Removable devices Hard Drive ATAPI CD-ROM Drive Network Boot LANDesk Service Agent	Specifies the boot sequence from the available devices. To specify boot sequence: Select the boot device with <↑> or <↓>. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering.
Hard Drive	No options	Lists available hard drives. When selected, displays the Hard Drive submenu.
Removable Devices	No options	Lists available removable devices. When selected, displays the Removable Devices submenu.

4.6.1 Hard Drive Submenu

This submenu is for configuring the boot sequence for hard drives.

Table 53. Hard Drive Submenu

Options	Description
Bootable Add-in Card	Specifies the boot sequence for the hard drives attached to the computer. To specify boot sequence: Select the boot device with <↑> or <↓>. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

4.6.2 Removable Devices Submenu

This submenu is for configuring the boot sequence for removable devices.

Table 54. Removable Devices Submenu

Options	Description
Legacy Floppy Drives	Specifies the boot sequence from the specified removable devices attached to the computer. To specify boot sequence: Select the boot device with <↑> or <↓>. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

4.7 Exit Menu

This menu is for exiting the Setup program, saving changes, and loading and saving defaults.

Table 55. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS RAM.
Exit Discarding Changes	Exits without saving any changes made in Setup.
Load Setup Defaults	Loads the default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

5.1 BIOS Error Messages

This table explains the BIOS error messages and in some cases suggests corrective action.

Table 56. BIOS Error Messages

Error Message	Explanation
Diskette drive A error	Drive A is present but fails the POST diskette tests. Check that the drive is defined with the proper diskette type in Setup and that the diskette drive is installed correctly.
Extended RAM Failed at offset: *nnnn*	Extended memory not working or not configured properly at offset *nnnn*.
Failing Bits: *nnnn*	The hexadecimal number *nnnn* is a map of the bits at the RAM address (System, Extended, or Shadow memory) that failed the memory test. Each 1 in the map indicates a failed bit.
Fixed Disk 0 Failure or Fixed Disk 1 Failure or Fixed Disk Controller Failure	Fixed disk is not working or not configured properly. Check to see if fixed disk is installed properly. Run Setup to be sure the fixed-disk type is correctly identified.
Incorrect Drive A type - run SETUP	Type of diskette drive for drive A not correctly identified in Setup.
Invalid NVRAM media type	Problem with NVRAM (CMOS) access.
Keyboard controller error	The keyboard controller failed test. Try replacing the keyboard.
Keyboard error	Keyboard not working.
Keyboard error nn	BIOS discovered a stuck key and displays the scan code nn for the stuck key.
Keyboard locked - Unlock key switch	Unlock the system to proceed.
Monitor type does not match CMOS - Run SETUP	Monitor type not correctly identified in Setup.
Operating system not found	Operating system cannot be located on either drive A or drive C. Enter Setup and see if fixed disk and drive A are properly identified.
Parity Check 1	Parity error found in the system bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.
Parity Check 2	Parity error found in the I/O bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.
Press <F1> to resume, <F2> to Setup	Displayed after any recoverable error message. Press <F1> to start the boot process or <F2> to enter Setup and change any settings.

continued

Table 56. BIOS Error Messages (continued)

Error Message	Explanation
Real-time clock error	Real-time clock fails BIOS test. May require motherboard repair.
Shadow RAM Failed at offset: *nnnn*	Shadow RAM failed at offset *nnnn* of the 64 KB block at which the error was detected.
System battery is dead - Replace and run SETUP	The CMOS clock battery indicator shows the battery is dead. Replace the battery and run Setup to reconfigure the system.
System cache error - Cache disabled	RAM cache failed the BIOS test. BIOS disabled the cache.
System CMOS checksum bad - run SETUP	System CMOS RAM has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. Run Setup and reconfigure the system either by getting the default values and/or making your own selections.
System RAM Failed at offset: *nnnn*	System RAM failed at offset *nnnn* of the 64 KB block at which the error was detected.
System timer error	The timer test failed. Requires repair of system motherboard.

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires an add-in card (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display. These cards can be purchased from JDR Microdevices or other sources.

The following table provides the POST codes that can be generated by the BIOS. Some codes are repeated in the table because that code applies to more than one operation.

Table 57. Port 80h Codes

Code	Description of POST Operation
02h	Verify real mode
03h	Disable non-maskable interrupt (NMI)
04h	Get processor type
06h	Initialize system hardware
08h	Initialize chipset with initial POST values
09h	Set IN POST flag
0Ah	Initialize CPU registers
0Bh	Enable CPU cache
0Ch	Initialize caches to initial POST values
0Eh	Initialize I/O component
0Fh	Initialize the local bus IDE
10h	Initialize power management
11h	Load alternate registers with initial POST valuesnew
12h	Restore CPU control word during warm boot
13h	Initialize PCI bus-mastering devices
14h	Initialize keyboard controller
16h	BIOS ROM checksum
17h	Initialize cache before memory autosize
18h	8254 timer initialization
1Ah	8237 DMA controller initialization
1Ch	Reset programmable interrupt controller
20h	Test DRAM refresh
22h	Test keyboard controller
24h	Set ES segment register to 4 GB
26h	Enable A20 line
28h	Autosize DRAM
29h	Initialize POST memory manager

continued

Table 57. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
2Ah	Clear 512 KB base RAM
2Ch	RAM failure on address line *xxxx* (See Note on page 79)
2Eh	RAM failure on data bits *xxxx* of low byte of memory bus (See Note on page 79)
2Fh	Enable cache before system BIOS shadow
30h	RAM failure on data bits *xxxx* of high byte of memory bus (See Note on page 79)
32h	Test CPU bus-clock frequency
33h	Initialize POST dispatch manager
34h	Test CMOS RAM
35h	Initialize alternate chipset registers
36h	Warm start shut down
37h	Reinitialize the chipset (MB only)
38h	Shadow system BIOS ROM
39h	Reinitialize the cache (MB only)
3Ah	Autosize cache
3Ch	Configure advanced chipset registers
3Dh	Load alternate registers with CMOS valuesnew
40h	Set Initial CPU speed new
42h	Initialize interrupt vectors
44h	Initialize BIOS interrupts
45h	POST device initialization
46h	Check ROM copyright notice
47h	Initialize manager for PCI option ROMs
48h	Check video configuration against CMOS RAM data
49h	Initialize PCI bus and devices
4Ah	Initialize all video adapters in system
4Bh	Display QuietBoot screen
4Ch	Shadow video BIOS ROM
4Eh	Display BIOS copyright notice
50h	Display CPU type and speed
51h	Initialize EISA motherboard
52h	Test keyboard
54h	Set key click if enabled
56h	Enable keyboard
58h	Test for unexpected interrupts
59h	Initialize POST display service
5Ah	Display prompt "Press F2 to enter SETUP"
5Bh	Disable CPU cache

continued

Table 57. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
5Ch	Test RAM between 512 and 640 KB
60h	Test extended memory
62h	Test extended memory address lines
64h	Jump to UserPatch1
66h	Configure advanced cache registers
67h	Initialize multiprocessor APIC
68h	Enable external and processor caches
69h	Setup System Management Mode (SMM) area
6Ah	Display external L2 cache size
6Ch	Display shadow-area message
6Eh	Display possible high address for UMB recovery
70h	Display error messages
72h	Check for configuration errors
74h	Test real-time clock
76h	Check for keyboard errors
7Ah	Test for key lock on
7Ch	Set up hardware interrupt vectors
7Eh	Initialize coprocessor if present
80h	Disable onboard Super I/O ports and IRQs
81h	Late POST device initialization
82h	Detect and install external RS232 ports
83h	Configure non-MCD IDE controllers
84h	Detect and install external parallel ports
85h	Initialize PC-compatible PnP ISA devices
86h	Re-initialize onboard I/O ports
87h	Configure motherboard configurable devices
88h	Initialize BIOS Data Area
89h	Enable Non-Maskable Interrupts (NMIs)
8Ah	Initialize extended BIOS data area
8Bh	Test and initialize PS/2 mouse
8Ch	Initialize diskette drive controller
8Fh	Determine number of ATA drives
90h	Initialize hard-disk controllers
91h	Initialize local-bus hard-disk controllers
92h	Jump to UserPatch2
93h	Build MPTABLE for multiprocessor boards
94h	Disable A20 address line (Rel. 5.1 and earlier)
95h	Install CD ROM for boot

continued

Table 57. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
96h	Clear huge ES segment register
97h	Fix up multiprocessor table
98h	Search for option ROMs
99h	Check for SMART Drive
9Ah	Shadow option ROMs
9Ch	Set up power management
9Eh	Enable hardware interrupts
9Fh	Determine number of ATA and SCSI drives
A0h	Set time of day
A2h	Check key lock
A4h	Initialize typematic rate
A8h	Erase F2 prompt
Aah	Scan for F2 key stroke
Ach	Enter SETUP
Aeh	Clear IN POST flag
B0h	Check for errors
B2h	POST done - prepare to boot operating system
B4h	One short beep before boot
B5h	Terminate QuietBoot
B6h	Check password (optional)
B8h	Clear global descriptor table
B9h	Clean up all graphics
Bah	Initialize DMI parameters
BBh	Initialize PnP Option ROMs
BCh	Clear parity checkers
BDh	Display MultiBoot menu
Beh	Clear screen (optional)
BFh	Check virus and backup reminders
C0h	Try to boot with INT 19
C1h	Initialize POST Error Manager (PEM)
C2h	Initialize error logging
C3h	Initialize error display function
C4h	Initialize system error handler

continued

Table 57. Port 80h Codes (continued)

Code	**Description of POST Operation** (The following are for the boot block in flash ROM)
E0h	Initialize the chipset
E1h	Initialize the bridge
E2h	Initialize the processor
E3h	Initialize system timer
E4h	Initialize system I/O
E5h	Check force recovery boot
E6h	Checksum BIOS ROM
E7h	Go to BIOS
E8h	Set huge segment
E9h	Initialize multiprocessor
Eah	Initialize OEM special code
Ebh	Initialize PIC and DMA
Ech	Initialize memory type
Edh	Initialize memory size
Eeh	Shadow boot block
Efh	System memory test
F0h	Initialize interrupt vectors
F1h	Initialize runtime clock
F2h	Initialize video
F3h	Initialize beeper
F4h	Initialize boot
F5h	Clear huge segment
F6h	Boot to mini-DOS
F7h	Boot to full DOS

NOTE

*If the BIOS detects error 2Ch, 2Eh, or 30h (base 512 KB RAM error), it displays an additional word-bitmap (*xxxx*) indicating the address line or bits that failed. For example, "2C 0002" means address line 1 (bit one set) has failed. "2E 1020" means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. The BIOS also sends the bitmap to the port-80h LED display. It first displays the check point code, followed by a delay, the high-order byte, another delay, and then the low-order byte of the error. It repeats this sequence continuously.*

5.3 BIOS Beep Codes

Whenever a recoverable error occurs during power-on self test (POST), the BIOS displays an error message describing the problem. The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (no card installed or faulty) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 58. Beep Codes

Beeps	80h Code	Description
1-2-2-3	16h	BIOS ROM checksum
1-3-1-1	20h	Test DRAM refresh
1-3-1-3	22h	Test keyboard controller
1-3-3-1	28h	Autosize DRAM
1-3-3-2	29h	Initialize POST memory manager
1-3-3-3	2Ah	Clear 512 KB base RAM
1-3-4-1	2Ch	RAM failure on address line *xxxx* (See Note on page 79)
1-3-4-3	2Eh	RAM failure on data bits *xxxx* of low byte of memory bus (See Note on page 79)
1-4-1-1	30h	RAM failure on data bits *xxxx* of high byte of memory bus (See Note on page 79)
2-1-2-2	45h	POST device initialization
2-1-2-3	46h	Check ROM copyright notice
2-2-3-1	58h	Test for unexpected interrupts
2-2-4-1	5Ch	Test RAM between 512 and 640 KB
1-2	98h	Search for option ROMs

6 Specifications and Customer Support

6.1 Online Support

Find information about Intel boards under “Product Info” or “Customer Support” at this World Wide Web site:

http://www.intel.com/

6.2 Specifications

The motherboard complies with the following specifications:

Table 59. Compliance with Specifications

Specification	Description	Revision Level
ACPI	Advanced Configuration and Power Interface Specification	Revision 1.0; December 22, 1996; Intel Corporation, Microsoft Corporation, Toshiba America Information Systems Inc.
A.G.P.	Accelerated Graphics Port Interface Specification	Revision 1.0, July 1996, Intel Corporation. The specification is available through the Accelerated Graphics Port Implementers Forum at: http://www.agpforum.org/
APM	Advanced Power Management BIOS interface specification	Revision 1.2; February 1996; Intel Corporation, Microsoft Corporation
ATA-3	Information Technology - AT Attachment-3 Interface	X3T10/2008D Revision 6, ATA Anonymous FTP Site: fission.dt.wdc.com
ATAPI	ATA Packet Interface for CD-ROMs	SFF-8020i Revision 2.5, (SFF) Fax Access: (408) 741-1600
ATX	ATX form factor specification	Revision 2.01, February 1997, Intel Corporation. The specification is available at: http://www.intel.com/
SMBIOS	System Management BIOS Reference Specification	Version 2.1; June 16, 1997; Award Software International Inc., Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Ltd., SystemSoft Corporation
El Torito	Bootable CD-ROM format specification	Version 1.0; January 25, 1995; Phoenix Technologies Ltd., IBM Corporation. The El Torito specification is available on the Phoenix Web site http://www.ptltd.com/techs/specs.html.
EPP	Enhanced Parallel Port	IEEE 1284 standard, Mode [1 or 2], v1.7

continued

Table 59. Compliance with Specifications (continued)

Specification	Description	Revision Level
IrDA	Serial Infrared Physical Layer Link specification	Version 1.1; October 17, 1995; Infrared Data Association
PCI	PCI Local Bus specification	Revision 2.1; June 1, 1995; PCI Special Interest Group
Phoenix BIOS	Phoenix BIOS	Revision 4.0; February 27, 1997; Phoenix Technologies Ltd.
Plug and Play	Plug and Play BIOS specification	Version 1.0a; May 5, 1994; Compaq Computer Corporation, Phoenix Technologies Ltd., Intel Corporation
SDRAM DIMMs (64- and 72-bit)	PC SDRAM Unbuffered DIMM specification	Revision 0.9, October 1997, Intel Corporation. The specification is available at: http://www.intel.com/design/pcisets/memory/
SDRAM Serial Presence Detect	PC SDRAM Serial Presence Detect specification	Revision 1.2A, December 1997, Intel Corporation. The specification is available at: http://www.intel.com/design/pcisets/memory/
UHCI	Universal Host Controller Interface (UHCI) Design Guide	Revision 1.1, March 1996; Intel Corporation. The specification is available at: http://www.usb.org
USB	Universal serial bus specification	Revision 1.0; January 15, 1996; Compaq Computer Corporation, Digital Equipment Corporation, IBM PC Company, Intel Corporation, Microsoft Corporation, NEC, Northern Telecom