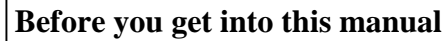# MAIN BOARD
USER'S MANUAL
VER. 5VPX2

User's Manual

Before you get into this manual

Important Notice

The information presented in this publication has been carefully designed for reliability. However, no responsibility is assumed for inaccuracies. Specifications are subject to modification without notice.

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Warning!!!

Shut down power before the computer is completely assembled. Check if everything is ready before you turn on the computer.

Table of Contents

Chapter 1 Introduction

This VT82C585VPX mainboard combines the advanced capabilities of the VIA Apollo VPX chipset with a high performance concurrent PCI local bus architecture. It provides the ideal platform to unleash the unsurpassed speed and the power of Intel Pentium® processor, Cyrix®6x86/6x86L/6X86 MX /MII and AMD® K5/K6/K6-2 processors, and can be easily upgraded for 321 pin ZIF socket.

The processor's advanced performance is complemented by a second level write-back PB-SRAM up to 512KB and main memory up to 512MB RAM. The main memory is initiated using the board's two 72-pin SIMM sockets and two 168-pin DIMM sockets that accept either the new high performance EDO, BEDO, or Fast Page mode DRAM. The VT82C585VPX integrates a full set of I/O features on board, including two 16550 UART compatible serial ports, one EPP/ECP capable port, one floppy disk controller, and one infrared communication controller.   On chip built in Enhanced IDE controller that provides convenient, high speed PCI bus Master connection with up to four IDE devices, including Hard disk and CD-ROM.

VIA builds all products to exacting standards with the best components available. We are proud to provide this system board and hope it brings you years of reliable service.

1-1 Main Features

Socket 7/ 321 Pins for CPU

1. Intel Pentium® P54C/ 55C CPU speed 75- 233 MHz processors
2. Cyrix® 6x86/6x86L/6X86 MX /MII
3. AMD® K5/K6/K6-2 processors

Memory

* Support synchronous DRAM using 168-pin DIMM modules of 8,16,32
* Take up to 256MB RAM in one bank using 72-pin SIMM modules of 1,2,4,8,
  16,32,64 or 128MB with supports for EDO,BEDO or Fast Page mode memory

PCI & ISA Slots

1. Three 16-bit ISA expansion slots and four 32-bit PCI expansion slots.

2. Integrated Enhanced PCI local bus IDE controller with two connectors support
   Up to four IDE devices such as Hard disk, CD-ROM.

3. Integrated ITE IT8661F/RF multi I/O chipset that offer two 16550 UART compatible
serial ports, one EPP/ECP capable port, one IR port, and one Floppy Disk Drive
connector.

COAST * Support 256K/512K synchronous PB SRAM


Flash ROM

*Supports 128KB Flash ROM

Other Features

1. A CPU interface controller
2. Avanced cache controller
3. Integrated DRAM controller
4. Asynchronous/synchronous PCI local bus interface
5. Integrated power management unit
6. Internal keyboard controller
7. Real-time Clock.

PCB SIZE

● * PCB size : 22 x 24 cm. ➡ See Chapter 2 Mother Board Specification

2-1 Motherboard Layout
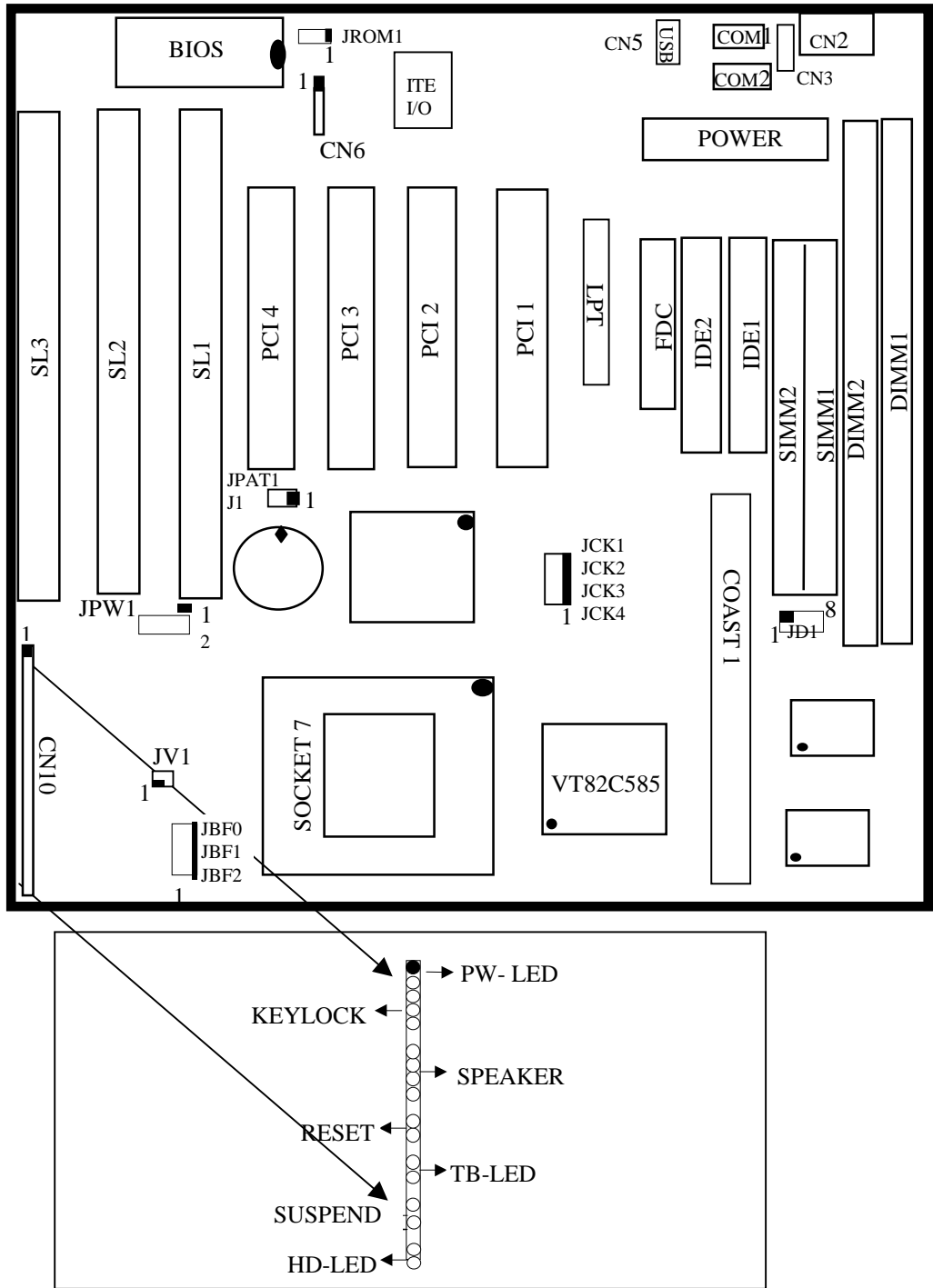
2-2 Jumper Setting

Make sure the jumpers are correctly set.

Intel Pentium® Processor Installation

CPU CLOCK	SYS. CLOCK	JCK1	JCK2	JCK3	JCK4	JBF0	JBF1	JPF2	JPW1	JV1	RATIO
P54C 90 MHZ 3.3V	60 MHZ	1-2	2-3	2-3	2-3	OPEN	OPEN	OPEN	1-2,5-6,7-8	OPEN	1.5X
P54C 100 MHZ 3.3V	66 MHZ	2-3	1-2	2-3	2-3	OPEN	OPEN	OPEN	1-2,5-6,7-8	OPEN	1.5X
P54C 120 MHZ 3.3V	60 MHZ	1-2	2-3	2-3	2-3	CLOSE	OPEN	OPEN	1-2,5-6,7-8	OPEN	2X
P54C 133 MHZ 3.3V	66 MHZ	2-3	1-2	2-3	2-3	CLOSE	OPEN	OPEN	1-2,5-6,7-8	OPEN	2X
P54C 150 MHZ 3.3V	60 MHZ	1-2	2-3	2-3	2-3	CLOSE	CLOSE	OPEN	1-2,5-6,7-8	OPEN	2.5X
P54C 166 MHZ 3.3V	66 MHZ	2-3	1-2	2-3	2-3	CLOSE	CLOSE	OPEN	1-2,5-6,7-8	OPEN	2.5X
P55C 166 MHZ 2.8/3.3V	66 MHZ	2-3	1-2	2-3	2-3	CLOSE	CLOSE	OPEN	7-8	1-2, 3-4	2.5X
P54C 200 MHZ 3.3V	66 MHZ	2-3	1-2	2-3	2-3	OPEN	CLOSE	OPEN	1-2,5-6,7-8	OPEN	3X
P55C 200 MHZ 2.8/3.3V	66 MHZ	2-3	1-2	2-3	2-3	OPEN	CLOSE	OPEN	7-8	1-2, 3-4	3X
P55C 233 MHZ 2.8/3.3V	66 MHZ	2-3	1-2	2-3	2-3	OPEN	OPEN	OPEN	7-8	1-2,3-4	3.5X

AMD® K5/K6/K6-2 Processor Installation

CPU CLOCK	SYS. CLOCK	JCK1	JCK2	JCK3	JCK4	JBF0	JBF1	JBF2	JPW1	JV1	RATIO
K5-PR90/PR120	60 MHZ	1-2	2-3	2-3	2-3	OPEN	OPEN	OPEN	1-2,3-4,5-6,7-8	1-2,3-4	1.5X
K5-PR100/PR133 3.52V	66 MHZ	2-3	1-2	2-3	2-3	OPEN	OPEN	OPEN	1-2,3-4,5-6,7-8	OPEN	1.5X
K5-PR166 3.52V	66 MHZ	2-3	1-2	2-3	2-3	CLOSE	CLOSE	OPEN	1-2,3-4,5-6,7-8	1-2,3-4	2.5X
K6-PR166 2.9/3.3V	66 MHZ	2-3	1-2	2-3	2-3	CLOSE	CLOSE	OPEN	1-2,7-8	OPEN	2.5X
K6-PR200 2.9/3.3V	66 MHZ	2-3	1-2	2-3	2-3	OPEN	CLOSE	OPEN	1-2,7-8	1-2, 3-4	3X
K6-PR233 3.2V/3.3V	66 MHZ	2-3	1-2	2-3	2-3	OPEN	OPEN	OPEN	5-6,7-8	1-2, 3-4	3.5X
K6-PR233 3.3V/3.3V	66 MHZ	2-3	1-2	2-3	2-3	OPEN	OPEN	OPEN	1-2, 5-6, 7-8	1-2, 3-4	3.5X
K6-PR266 3.2V/3.3V	66 MHZ	2-3	1-2	2-3	2-3	CLOSE	OPEN	CLOSE	3-4	1-2, 3-4	4X
K6-PR300 2.2/3.45V	66 MHZ	2-3	1-2	2-3	2-3	CLOSE	CLOSE	CLOSE	3-4	1-2, 3-4	4.5X
K6-2 266 3.2V/3.3V	66 MHZ	2-3	1-2	2-3	2-3	CLOSE	OPEN	CLOSE	3-4	1-2, 3-4	4X

Cyrix® 6x86 Processor Installation

CPU CLOCK	SYS. CLOCK	JCK1	JCK2	JCK3	JCK4	JBF0	JBF1	JPF2	JPW1	JV1	RATIO
P120+ M1 3.52V	50 MHZ	2-3	2-3	2-3	1-2	CLOSE	OPEN	OPEN	1-2,3-4,5-6,7-8	OPEN	2X
P133+ M1 3.52V	55 MHZ	2-3	2-3	1-2	2-3	CLOSE	OPEN	OPEN	1-2,3-4,5-6,7-8	OPEN	2X
P150+ 3.52V	60 MHZ	1-2	2-3	2-3	2-3	CLOSE	OPEN	OPEN	1-2,3-4,5-6,7-8	OPEN	2X
P166+ 3.52V	66 MHZ	2-3	1-2	2-3	2-3	CLOSE	OPEN	OPEN	1-2,3-4,5-6,7-8	OPEN	2X
P133+ 2.8\3.3V 6X68L	55 MHZ	2-3	2-3	1-2	2-3	CLOSE	OPEN	OPEN	7-8	1-2,3-4	2X
P150+ 2.8\3.3V 6X86L	60 MHZ	1-2	2-3	2-3	2-3	CLOSE	OPEN	OPEN	7-8	1-2,3-4	2X
P166+2.8\3.3V 6X86L	66 MHZ	2-3	1-2	2-3	2-3	CLOSE	OPEN	OPEN	7-8	1-2,3-4	2X
P200+ 2.8\3.3V 6X86L	75 MHZ	1-2	2-3	1-2	2-3	CLOSE	OPEN	OPEN	7-8	1-2,3-4	2X
MX PR200+ 2.9\3.3V	66 MHZ	2-3	1-2	2-3	2-3	CLOSE	CLOSE	OPEN	7-8	1-2,3-4	2.5X
MX PR166+2.9/3.3V	66 MHZ	2-3	1-2	2-3	2-3	CLOSE	OPEN	OPEN	1-2, 7-8	1-2,3-4	2X
MX PR200+ 2.9\3.3V	66 MHZ	2-3	1-2	2-3	2-3	CLOSE	CLOSE	OPEN	1-2, 7-8	1-2,3-4	2.5X
MX PR200+ 2.9\3.3V	75 MHZ	1-2	2-3	1-2	2-3	CLOSE	OPEN	OPEN	1-2,7-8	1-2,3-4	2X
MX PR233+ 2.9/3.3V	75 MHZ	1-2	2-3	1-2	2-3	CLOSE	CLOSE	OPEN	1-2, 7-8	1-2, 3-4	2.5X
MII 300 2.9/3.3V	66 MHZ	2-3	1-2	2-3	2-3	OPEN	OPEN	OPEN	1-2,7-8	1-2,3-4	3.5X

2-3 Connectors

CN2 - Keyboard Connector

Pin	Description
1	Keyboard Clock
2	Keyboard Data
3	N.C.
4	Ground
5	+5 V DC

CN3 - Mouse Connector

Pin	Description
1	Mouse Clock
2	Mouse Data
3	N.C.
4	Ground
5	+5 V DC

CN4, CN5 - USB Connector (Optional)

CN6 - Infrared Connector : IR

Pin	Signal Name
1	IRRX
2	Ground
3	IRTX
4	+5 V DC
5	IRRXH
6	+5 V DC
7	Ground

ATX1 - ATX Power Supply Connector (Optional)

Pin	Description	Pin	Description
1	+3.3V DC	11	+3.3V DC
2	+3.3V DC	12	-12V DC
3	Ground	13	Ground
4	+5V DC	14	Soft-Power
5	Ground	15	Ground
6	+5V DC	16	Ground
7	Ground	17	Ground
8	Power Good	18	-5V DC
9	+5V Standby	19	+5V DC
10	+12V DC	20	+5V DC

CN7 - AT Power Supply Connector

Pin	Description	Pin	Description
1	Power Good	7	Ground
2	+5 V DC	8	Ground
3	+12 V DC	9	- 5 V DC
4	- 12 V DC	10	+5 V DC
5	Ground	11	+5 V DC
6	Ground	12	+5 V DC

CN8 - Printer Port Connector

CN9 - Floppy Disk Connector

IDE1 - Primary IDE Connector

IDE2 - Secondary IDE Connector

COM1,COM2 - Serial Ports Connector

JCK1-4 - CPU Speed Selector

Jumper	50MHZ	55MHZ	60MHZ	66MHZ	75MHZ
JCK1	2-3	2-3	1-2	2-3	1-2
JCK2	2-3	2-3	2-3	1-2	2-3
JCK3	2-3	1-2	2-3	2-3	1-2
JCK4	1-2	1-2/2-3	1-2/2-3	1-2/2-3	1-2/2-3
PCICLK	25	27.5/32	30/32	33.3/32	37.5/32

Note: 1. JCK4 is PCI synchronous/asynchronous selection. Do not select "1-2" when using 75 MHz.

JPW1 - CPU Voltage Selector (FOR ONE REGULATOR)

Description	CPU Voltage	JPW1	JV1
3.3V	Core: 3.3V I/O: 3.3 V (P54C-STD,VR, AMD® K5-C,F, Cyrix 6X86-016)	1-2,5-6,7-8	OPEN
3.52V	Core: 3.4 ~ 3.6V I/O: 3.4 ~ 3.6V (P54C-VRE, AMD® K5-B, Cyrix® 6X86-028)	1-2,3-4,5-6,7-8	OPEN

(FOR TWO REGULATOR)

Description	CPU Voltage	JPW1	JV1

2.8V	Core: 2.8V I/O: 3.3V	7-8	1-2, 3-4
(INTEL P55C, AMD® K5-H,J, Cyrix® 6x86L)			
2.9V	Core: 2.9V I/O: 3.3V	1-2,7-8	1-2, 3-4
(AMD® K6, Cyrix® 6x86MX)			
3.2V	Core: 3.2V I/O: 3.3V	5-6,7-8	1-2, 3-4
(AMD® K6)			

***Note : INTEL P55C MMX, AMD® K6 AND CYRIX®
6X86L are "Dual Voltage CPUs" , "6X86L" is CYRIX® New
Low Power CPU.**

JBF0-JBF1 - CPU/BUS Ratio

Ratio	JBF0	JBF1
1.5X	OPEN	OPEN
2X	CLOSE	OPEN
2.5X	CLOSE	CLOSE
3X	OPEN	CLOSE
3.5X	OPEN	OPEN

JBF2: Reserved for 4/4.5/5X

JBAT1 - CMOS Selector

Description	JBAT1
Normal (default)	1-2
Clear CMOS (clear password)	2-3

JROM1 - Flash ROM Voltage Selector

Description	JROM1
5V (SST,Winbond)	1-2
12V (Intel,MXIC)	2-3

JD1 - DIMM Voltage Selector

Description	JD1
5V DIMM	1-3,2-4
3.3V DIMM	5-7,6-8

*Note: This cannot mix 3.3V Dimm with 5V simm

J1 - AT/ATX Power Select

Description	J1
AT Power	1-2
ATX Power (Optional)	2-3

2-4 DRAM Configuration

System memory RAM is comprised of industry standard 72-pin Single In-line. Memory Modules (SIMMs), Burst Extended Data Out (BEDO) and Extended Data Out (EDO) memory are the latest DRAM chip designs that perform a lot better than the Fast Page mode DRAM type. With BEDO and EDO memory, CPU access to memory is 10 to 15% faster. The VT82C580VPX97 is able to support standard FPM (Fast Page Mode), EDO (Extended Data Out), or BEDO (Burst Extended Data Out); memory can be installed in a variety of conf., as shown in the following table:

Total Memory	Bank 0/1 (DIMM1)	Bank 2/3 (DIMM2)	Bank4/5 (SIMM1, SIMM2)

8MB	8MB		
8MB			4MB & 4MB
12MB	8MB	4MB	
16MB	8MB	8MB	
16 MB	16MB		
16 MB			8MB & 8MB
24MB	16MB	8MB	
32MB	16MB	16MB	
32MB	32MB		
32MB			16MB & 16MB
40MB	32MB	8MB	
48MB	32MB	16MB	
64MB	32MB	32MB	
64MB	64MB		
64MB			32MB & 32MB
72MB	64MB	8MB	
80MB	64MB	16MB	
96MB	64MB	32MB	
128MB	64MB	64MB	
128MB			64MB & 64MB

* All SIMMs must be faster than 70ns.
* All Banks can use either 1-sided or 2-sided SIMMs.
* All Banks are auto bank.
* All memory banks use 72-pin memory modules.

2-5 Cache Memory Configuration

The VT82C580VPX comes with COAST 256KB/512KB synchronous 3.3V Pipeline Burst SRAMs. For 256K secondary cache, COAST should be mounted with 32Kx32 PB SRAM. Regardless of COAST, 64Kx32 PB SRAM can offer 512K secondary cache.

Chapter 3   BIOS setup

Award ROM BIOS provides a built-in Setup program which allows user to modify the basic system configuration and hardware parameters. The modified data will be stored in a battery-backed CMOS ram so data will be retained even when the power is turned off. In general, the information saved in the CMOS ram stays unchanged unless there is config. change in the system, such as hard drive replacement or new equipment change.

It is possible that CMOS has a battery failure which causes data loss in CMOS ram. If so, re-enter system config. parameters become necessary.

TO ENTER SETUP PROGRAM

Turn on the computer and press <Del> key immediately will bring you into BIOS CMOS SETUP UTILITY.

```
┌─────────────────────────────────────────────────────────────┐
│             ROM PCI/ISA BIOS (2A5LDL1C)                       │
│                 CMOS SETUP UTILITY                            │
│                AWARD SOFTWARE, INC.                           │
├──────────────────────────────┬──────────────────────────────┤
│ STANDARD CMOS SETUP          │ INTEGRATED PERIPHERALS        │
│ BIOS FEATURES SETUP          │ SUPERVISOR PASSWORD           │
│ CHIPSET FEATURES SETUP       │ USER PASSWORD                 │
│ POWER MANAGEMENT SETUP       │ IDE HDD AUTO DETECTION        │
│ PNP/PCI CONFIGURATION        │ HDD LOW LEVEL FORMAT          │
│ LOAD SETUP DEFAULTS          │ SAVE & EXIT SETUP             │
│                              │ EXIT WITHOUT SAVING           │
├──────────────────────────────┼──────────────────────────────┤
│ ESC : Quit                   │ ▢▢▢▢ : Select Item            │
│ F10 : Save & Exit Setup      │ (Shift)F2 : Change Color      │
└──────────────────────────────┴──────────────────────────────┘
```

The menu displays all the major selection items and allows user to select any one of shown

item. The selection is made by moving cursor (press any direction key) to the item and press "enter" key. An on line help message is displayed at the bottom of the screen as cursor is moving to various items which provide user better understanding of each function. When a selection is made, the menu of selected item will appear so the user can modify associated configuration parameters.

3-1 Standard CMOS setup

```
┌─────────────────────────────────────────────────────────────┐
│             ROM PCI/ISA BIOS (2A5LDL1C)                       │
│                STANDARD CMOS SETUP                            │
│                AWARD SOFTWARE, INC.                           │
└─────────────────────────────────────────────────────────────┘
```

```
Date (mm:dd:yy) : Wed, Jan,  1 1997
Time (hh:mm:ss) : 00:00:00
HARD DISKS        TYPE  SIZE  CYLS  HEAD  PRECOMP  LANDZ  SECTOR  MODE
Primary Master :   Auto    0     0     0        0       0       0     Auto
Primary Slave :    Auto    0     0     0        0       0       0     Auto
Secondary Master : Auto    0     0     0        0       0       0     Auto
Secondary Slave :  Auto    0     0     0        0       0       0     Auto


Driver A : 1.44M, 3.5 in
Driver B : None                          Base Memory      :      640K
Floppy 3 Mode Support : Disabled         Extended Memory  :     7168K
                                         Other Memory     :      384K
Video : EGA/VGA                          Total Memory     :     8192K
Halt On : All Errors
    ESC : Quit          □□□□ : Select Item        PU/PD/+/- : Modify
    F1 : Help          (shift)F2 : Change Color
```

The Standard CMOS setup screen is displayed above. System BIOS automatically detects memory size. Thus, no changes are necessary. It has a few items for setting.   Each item may have one or more option settings. It allows you to change the system Date and Time, IDE hard disk, floppy disk drive types for drive A: and B: boot up video display mode, and POST error handling selection. Use the arrow keys to highlights the item and then use the <Pgup> or <Pgdn> keys to select the value you want in each item.

Hard Disk Configurations

   TYPE :

            Select from "1" to "45" to fill remaining fields with redefined values of disk drives. Select "User" to fill the remaining fields. Select "Auto" to detect the HDD type automatically.

   SIZE :

            The hard disk size. The unit is Mega Byte.

   CYLS :

            The cylinder number of the hard disk.

   HEAD :

            The read/write head number of hard disk. The range is from "1" to "16".

   PRECOMP :

            The cylinder number at which the disk drive changes the write timing.

   LANDZ :

             The cylinder number that the disk drive heads (read/write) are seated when the disk drive is parked.

   SECTOR :

            The sector number of each track defined on the hard disk. The range is from "1" to "64".

   Mode :

            Select "AUTO" to detect the mode type automatically. If your hard disk supports the LBA mode, select "LBA" or "Large". However, if your hard disk cyclinder is more than 1024 and does not support the LBA function, you have to set at "Large". Select "Normal" if your hard disk supporting cylinder is below 1024.

3-2 BIOS Feature Setup

```
┌─────────────────────────────────────────────────────────────────────────┐
│                   ROM PCI/ISA BIOS (2A5LDL1C)                             │
│                      BIOS FEATURES SETUP                                  │
│                     AWARD SOFTWARE, INC.                                  │
├─────────────────────────────────────┬───────────────────────────────────┤
│ Virus warning          : Disabled   │ Video BIOS Shadow     : Enabled    │
│ CPU Internal Cache     : Enabled    │ C8000-CBFFF Shadow   : Disabled    │
│ External Cache         : Enabled    │ CC000-CFFFF Shadow   : Disabled    │
│ Quick Power On Self Test : Disabled │ D0000-D3FFF Shadow   : Disabled    │
│ Boot Sequence          : A,C,SCSI   │ D4000-D7FFF Shadow   : Disabled    │
│ Swap Floppy Drive      : Disabled   │ D8000-DBFFF Shadow   : Disabled    │
│ Boot Up Floppy Seek    : Enabled    │ DC000-DFFFF Shadow   : Disabled    │
│ Boot Up Numlock Status : On         │                                    │
│ Boot Up System Speed   : High       │                                    │
│ Gate A20 Option        : Normal     │                                    │
│ Typematic Rate Setting : Disabled   │                                    │
│ Typematic Rate (Chars/Sec) : 6      │                                    │
│ Typematic Delay (Msec)    : 250     │                                    │
│ Security Option        : Setup      │                                    │
│ IDE Second Channel Control : Enabled│                                    │
│ PCI/VGA Palette Snoop    : Disabled │ ESC : Quit      □□□□ : Select Item │
│ OS Select for DRAM>64MB : Non-OS2   │ F1 : Help        PU/PD/+/- : Modify│
│                                     │ F5 : Old Values  (Shift)F2 : Color │
│                                     │ F7 : Load Setup Defaults           │
└─────────────────────────────────────┴───────────────────────────────────┘
```

Selecting the "BIOS FEATURE SETUP" option in the CMOS setup utility menu allows user to change system related parameters in the display menu. This menu shows all of the manufacturer's default values of SV-P55V. Again, user can move the cursor by pressing direction keys and <PgDn> or <PgUp> key to modify the parameters. Pressing [F1] key to display help message of the selected item.

The setup program also provides 2 convenient ways to load the default parameter data from CMOS [F7] area if shown data is corrupted. This provides the system a capability to recover from any possible error.

Virus Warning:
When enabled, it assigns the BIOS to monitor the master boot sector and the DOS boot sector of the first hard disk drive.

The options are: Enabled, Disabled (Default).

CPU Internal Cache:
When enabled, it improves the system performance. Disable this item when testing or trouble-shooting.

The options are : Enabled (Default), Disabled

External Cache:
When enabled, it supports an optional cache SRAM.

The options are : Enabled (Default), Disabled

Quick Power On Self Test:

When enabled, it allows the BIOS to bypass the extensive memory test.

The options are : Enabled, Disabled (Default)

Boot Sequence:
Allows the system BIOS to first try to boot the operating system from the selected disk drive.

The options are : A,C,SCSI (Default); C,A,SCSI; C,CDROM,A; CDROM,C,A; D,A,SCSI; E,A,SCSI; F,A,SCSI; SCSI,A,C; SCSI,C,A; C only; LS/ZIP,C.

Swap Floppy Drive:
When enabled, it allows you to switch the order in which the operating system accesses the floppy drives during boot up.

The options are : Enabled, Disabled (Default)

Boot Up Floppy Seek:
When enabled, assigns the BIOS to perform floppy disk drive tests by issuing the time-consuming seek commands.

The options are : Enabled (Default), Disabled

Boot Up Numlock Status:
When set to On, it allows the BIOS to automatically enable the Num Lock function when the system boots up.

The options are : On (Default), Off

Port 92H Fast A20G:
When enabled, allows the A20G bus line signal generated from the chipset 82C586 PC/AT to directly pass to port 92H, instead of the keyboard controller. It will speed up the system performance.

The options are : Fast, Normal(Default)

Typematic Rate Setting:
The term "typematic" means that when a keyboard key is held down, the character is repeatedly entered until the key is released. When this item is enabled, you may change the typematic repeat rate.

The options are : Disabled (Default), Enabled

Typematic Rate (Chars/Sec):
Sets the rate of a character repeat when the key is held down.

The options are : 6 (Default), 8, 10, 12, 15, 20, 24, 30

Typematic Delay (Msec):
Sets the delay time before a character is repeated.

The options are : 250 (Default), 500, 750, 1000 millisecond

Security Option:
Allows you to set the security level of the system.

The options are : Setup (Default), System

PCI/VGA Paiette Snoop:
When enabled, it allows you to install an enhanced graphics adapter card. If your graphics adapter card does not support the Pallete Snoop function, please set at Disable to avoid system malfunctions.

The options are : Enabled, Disabled (Default)

Video BIOS Shadow:
When enabled, it allows the BIOS to copy the video ROM code of the add-on video cards to the system memory for faster access.

The options are : Enabled (Default), Disabled

C8000-CBFFF to DC000-DFFFF Shadow:
When enabled, it allows the BIOS to copy the BIOS ROM code of the add-on card to system memory for faster access. It may improve the performance of the add-on card. Some add-on cards will not function properly if it's BIOS ROM code is shadowed. To use these options correctly, you need to know the memory address range used by the BIOS ROM of each add-on card.

The options are : Enabled, Disabled (Default)

3-3 Chipset Features Setup

ROM PCI/ISA BIOS (2A5LDL1C)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

```
DRAM Auto Configuration    : Disabled        On Chip USB          : Disabled
DRAM Timing Control        : Normal
SDRAM Cycle Length         : 3
SDRAM Bank Interleave      : Disabled

Sustained 3T write         : Disabled
2 Bank PBSRAM              : 3-1-1-1
Read Pipeline              : Disabled
Write Pipeline             : Enabled
Cache Timing               : Fast
Linear Burst               : Disabled

Video BIOS Cacheable       :Disabled
System BIOS Cacheable      :Disabled
Memory Hole At 15MB Addr.  : Disabled
                                                ESC : Quit          □□□□ : Select item
                                                F1 : Help           PU/PD/+/- : Modify
                                                F5 : Old Values      (Shift)F2 : Color
                                                F7 : Load Setup Defaults
```

Video BIOS Cacheable:

When enabled, it allows the system to use the video BIOS codes C0000H-C7FFFH from cache, instead of the slower DRAMs or ROMs. Video BIOS must be shadowed first.

The options are : Enabled (Default), Disabled

System BIOS Cacheable:

When enabled, it allows the ROM area E0000H-FFFFFH to be cacheable when cache controller is activated.

The options are : Enabled (Default), Disabled

Memory Hold At 15MB Addr.:

When enabled, the memory hole at the 15MB address will be relocated to the 15~16MB address range of the ISA cycle when the processor accesses the 15~16MB address area.

When disabled, the memory hole at the 15MB address will be treated as a DRAM cycle when the processor accesses the 15~16MB address.

The options are : Enabled, Disabled (Default)

Sustained 3T Write:

The cache architecture adopts Write Through. When Write Through is enabled, the performance is better under most application environment because the 580VP FIFO queue is deep.

The options are : Enabled, Disabled (Default)

Read/Write Pipeline:

Turn on Read/Write Pipeline operation to increase performance.

DRAM Timing Control:
Allows you to speed up the data access of 82C585M.

For example:	DRAM type	Turbo	Fast
	FP-7		V
	EDO-6	V	
	EDO-7		V

The options are : Turbo, Fast, Medium, Normal

3-4 Power Management Setup

ROM PCI/ISA BIOS (2A5LDL1C)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.

```
Power Management       : User Defined
PM Controlled by APM : Yes
Video off Option       : Suspend->Off
Video off Method       : V/H SYNC+ Blank    IRQ5    (LPT2)        : Primary
Conserve Mode          : Disabled           IRQ6    (Floppy Disk) :  Primary
Moden Use IRQ          : 3                   IRQ7    (LPT1)        :  Primary
                                             IRQ8    (RTC Alarm)   :  Disabled
      **PM Timers**                          IRQ9    (IRQ2 Redir)  : Secondary
HDD Power Down         : Disabled            IRQ10   (Reserved)    :  Secondary
Doze Mode              : Disbaled            IRQ11   (Reserved)    :  Secondary
Suspend Mode           : Disabled            IRQ12   (PS/2 Mouse)  :  Primary
      **PM Events**                          IRQ13   (Coprocessor) :  Primary
VGA                    : OFF                 IRQ14   (Hard Disk)   :  Primary
LPT & COM              : LPT/COM             IRQ15   (Reserved)    :  Disabled
HDD & FDD              : ON
DMA/MASTER             : OFF                 ESC : Quit        □□□□ : Select Item
Primary INTR           :  ON                 F1 : Help         PU/PD/+/- : Modify
IRQ3 (COM2)            :  Primary            F5 : Old Values    (Shift) F2 : Color
IRQ4 (COM1)            :  Primary            F7 : Load Setup Defaults
```

Power Management:
When enable, it allows you to use Power Management features.

PM Control by APM:
The option "**No**" allows the BIOS to ignore the APM (Advanced Power Management) specification. Selecting "**Yes**" will allow the BIOS wait for APM's prompt before it enters Doze mode, Standby mode, or Suspend mode. If the APM is installed, it will prompt the BIOS to set the system into the power saving mode after all tasks are done.

Video off Option:
This feature provides the selections of the video display power saving mode. The option "**Suspend -> Off**" allows the display blanks if the system enters Suspend mode. The option "**All modes -> Off**" allows the video display blanks if the system enters Doze mode or Suspend mode. The option "**Always On**" allows the video display to stay in Standby mode even the system enters Doze or Suspend mode.

Video Off Method:
The option "**V/H SYNC+ Blank**" allows the BIOS to blank off screen display by turning off the V-Sync signals sent from add-on VGA card. "**DPMS Supported**" allows the BIOS to blank off screen display by your add-on VGA card which supports DPMS (Display Power Management Signaling function). "**Blank Screen**" allows the BIOS to blank screen display by turning off the red-green-blue signals.

Conserve Mode:

When the Doze Mode of the system being happened, the Doze Mode is handled by hardware not by SMI function.

Modem use IRQ:
When the system is in green function, modem wakes up the system through IRQ.

HDD Power Down:
Selecting "Disabled" will turn off the hard disk drive (HDD) motor.
Selecting "1Min ...15Min" allows you to define the HDD idle time before the HDD enters Power Saving mode.
The option "When Suspend" lets the BIOS turn the HDD motor off when the system is in Suspend mode.
The options "1Min ... 15Min" and "When Suspend" will not work concurrently. When HDD is in Power Saving Mode, any access to the HDD will wake the HDD up.

Doze Mode:
When disabled, the system will not enter Doze mode. The specified time option define the idle time the system takes before it enters Doze mode.

Suspend Mode:
When disabled, the system will not enter Suspend mode. The specified time option defines the idle time the system takes before it enters Suspend mode.

VGA:
Selecting "ON" will enable the power management timers when a "no activity" events is detected in the VGA. Selecting "OFF" to disable the PM timer even if a "no activity" event is detected.

LPT & COM:
Selecting "**LPT & COM**" will enable the power management timers when a "no activity" event is detected in the LPT and COM ports. Selecting "**LPT**" ("**COM**") will enable the power management timers when a "no activity" event is detected in the LPT (COM) ports.
Selecting "**NONE**" to disable the PM timer even if a "no activity" event is detected.

HDD & FDD:
Selecting "ON" will enable the power management timers when a "no activity" event is detected in the hard disk drive and floppy disk drive. Selecting "OFF" to disable the PM timer event if a "no activity" event is detected.

DMA/Master:
When the master is working, the system will not have SMI signal until the master is finished.

Primary INTR:
When enabled, you can choose any IRQ#.

IRQ#:

When set at "**Primary**" the processor will power down only after the BIOS detects a "no IRQ activity" during the time specified by the Suspend time. If set at "**Secondary event**" the system will distinguish whether an interrupt accesses an I/O address or not. If it does, the system enters the standby mode. If not, the system enters the dreaming mode; that is the system goes back full-on status but leaves the monitor blank. For instance, if the system connects to a LAN and receives an interrupt from its file server, the system will enter the dreaming mode to execute the corresponding calling routine.

3-5 PNP/PCI Configuration

```
           ROM PCI/ISA BIOS (2A5LDL1C)
           PNP/PCI CONFIGURATION SETUP
               AWARD SOFTWARE, INC.
PNP OS Installed        : Yes      CPU to PCI Write Buffer   : Enabled
Resources Controlled By  : Manual   PCI Dynamic Bursting     : Enabled
Reset Configuration Data  : Disabled  PCI Master 0 WS Write    : Enabled
                                     PCI Peer Concurrency      : Disabled
IRQ-3   assigned to : Legacy ISA    PCI Delay Transaction     : Disabled
IRQ-4   assigned to : Legacy ISA
IRQ-5   assigned to : PCI/ISA PnP   PCI IRQ Actived By       : Edge
IRQ-7   assigned to : Legacy ISA    PCI IDE IRQ Map To       : PCI-AUTO
IRQ-9   assigned to : PCI/ISA PnP   Primary    IDE INT#      : A
IRQ-10 assigned to : PCI/ISA PnP    Secondary  IDE INT#      : B
IRQ-11 assigned to : PCI/ISA PnP
IRQ-12 assigned to : PCI/ISA PnP
IRQ-14 assigned to : Legacy ISA
IRQ-15 assigned to : Legacy ISA
DMA-0 assigned to : PCI/ISA PnP
DMA-1 assigned to : PCI/ISA PnP     ESC : Quit        □□□□ : Select Item
DMA-3 assigned to : PCI/ISA PnP     F1  : Help        PU/PD/+/- : Modify
DMA-5 assigned to : PCI/ISA PnP     F5  : Old Valucs  (Shift) F2  : Color
DMA-6 assigned to : PCI/ISA PnP     F7  : Load Setup Defaults
DMA-7 assigned to : PCI/ISA PnP
```

PCI IRQ Actived By:

If your IDE cards is triggered by edge, set it at "Edge".
The options are : Level, Edge (Default)

PCI IDE IRQ Map To:

Set to auto to allow the system BIOS to automatically detect which interrupt is used by the PCI master drive.

The options are : PCI-AUTO (Default), PCI-SLOT1, PCI-SLOT2, PCI-SLOT3, PCI-SLOT4, ISA

CPU to PCI Write Buffer:

When enabled, allows data and address access to the internal buffer of 82C586A so the processor can be released from the waiting state.

The options are : Enabled (Default), Disabled

PCI Dynamic Bursting:
When enabled, the PCI controller allows Bursting PCI transfer if the consecutive PCI cycles come with the address falling in same 1KB space. This improves the PCI bus through put.

The options are : Enabled (Default), Disabled.

PCI Master 0 WS Write:
When enabled, allows a zero-wait-state-cycle delay when the PCI master drive writes data to DRAM.

The options are : Enabled, Disabled (Default)

3-6 Load BIOS Defaults

The BIOS defaults contain the most appropriate values of the system parameters that allows minimum system performance. The OEM manufacturer may change the defaults through MODBIN before the binary image burns into the ROM.

3-7 Load Setup Defaults

Selecting this field loads the factory defaults for BIOS and Chipset Features which the system automatically detects.

3-8 Integrated Peripherals

```
┌─────────────────────────────────────────────────────────────────────┐
│                  ROM PCI/ISA BIOS (2A5LDL1C)                        │
│                    INTEGATED PERIPHEALS                              │
│                   AWARD SOFTWARE, INC.                              │
├───────────────────────────────────────┬─────────────────────────────┤
│ OnChip IDE First Channel    : Enabled │ Parellel Port Mode    : SPP │
│ Onchip IDE Second Channel   : Enabled │                             │
│ IDE Prefetch Mode           : Enabled │                             │
│ IDE HDD Block Mode          :Enabled  │                             │
│ IDE Primary Master PIO      : Auto    │                             │
│ IDE Primary Slave PIO       : Auto    │                             │
│ IDE Secondary Master PIO    : Auto    │                             │
│ IDE Secondary Slave PIO     : Auto    │                             │
│ IDE Primary Master UDMA     : Auto    │                             │
│ IDE Primary Slave UDMA      : Auto    │                             │
│ IDE Secondary Master UDMA: Auto       │                             │
│ IDE Secondary Slave UDMA  : Auto      │                             │
│                                       │                             │
│ Onboard FDC Controller      : Enabled │                             │
│ Onboard Serial Port 1       :3F8/IRQ4 ├─────────────────────────────┤
│ Onboard Serial Port 2        : 3F8/IRQ33│ ESC : Quit      □□□□ : Select Item │
│ IR Address Select           : Disabled│ F1 : Help       PU/PD/+/- : Modify │
│  Onboard Parallel Port      : 378/IRQ7│ F5 : Old Values  (Shift)F2  : Color │
│                                       │ F7 : Load Setup Defaults    │
└───────────────────────────────────────┴─────────────────────────────┘
```

OnChip IDE First Channel:
When enabled, allows the IDE driver to use the first channel of the primary IDE.

OnChip IDE Second Channel:
When enabled, allows the IDE drive to use the second channel of the primary IDE.

IDE Prefetch Mode:
When enabled, allows the system BIOS to utilize the prefetch buffer of the onboard IDE controller to prefetch the next sequential data of the current access.

IDE Primary Slave PIO:
The default value is Auto.
Auto: BIOS will automatically detect the Onboard Primary Slave PCI IDE HDD accessing mode.
Mode 0-4 : Manually set the IDE accessing mode.

IDE Secondary Master PIO:
The default value is Auto.
Auto   : BIOS will automatically detect the Onboard Secondary Master PCI IDE HDD accessing mode.
Mode 0-4 : Manually set the IDE accessing mode.

IDE Primary Master PIO:
The default value is Auto.

IDE Secondary Slave PIO:
The default value is Auto.

Onboard FDC Controller:
The default value is Enabled.

Enabled : Enabled the onboard I/O Chip's floppy drive interface controller.
Disabled : Disabled the onboard I/O Chip's floppy drive interface controller. When use
on-card ISA FDC's controller.

Onboard Serial Port 1:
The field allows the user to select the serial port. The default value is AUTO.
COM1: Enable onboard serial port1 and address is COM1/3F8H
COM2: Enable onboard serial port1 and address is COM2/2F8H
COM3: Enable onboard serial port1 and address is COM3/3E8H
COM4: Enable onboard serial port1 and address is COM4/2E8H
Disabled: Disable onboard I/O Chip's Serial port 1.
AUTO : BIOS will automatically detect the Onboard Serial Port.

Onboard Serial Port 2:
The field allows the user to select the serial port. The default value is AUTO.
COM1: Enable onboard serial port1 and address is COM1/3F8H
COM2: Enable onboard serial port1 and address is COM2/2F8H
COM3: Enable onboard serial port1 and address is COM3/3E8H
COM4: Enable onboard serial port1 and address is COM4/2E8H
Disabled: Disable onboard I/O Chip's Serial port 1.
AUTO : BIOS will automatically detect the Onboard Serial Port.

Onboard Parallel Port:
The field allows the user to select the LPT port. The default value is 378H/IRQ7.
378H : Enable onboard LPT port and address is 378H and IRQ7
278H : Enable onboard LPT port and address is 278H and IRQ5
3BCH : Enable onboard LPT port and address is 3BCH and IRQ7
Disabled : Disable onboard I/O Chip's LPT port

3-9 Password Setting

1.If CMOS is corrupted or the option was not used, a default password stored in the ROM
will be used. The screen will display the following message:
Enter Password
   Press the [Enter] key to continue after proper password is given
2.If CMOS is corrupted or the option was used earlier and the user wish to change default
password, the SETUP UTILITY will display a message and ask for a confirmation.
Confirm Password:
3.After pressing the [Enter] key (ROM password if the option was not used) or current
password (user-defined password), the user can change the password and store new one in
CMOS RAM. A maximum of 8 characters can be entered.

3-10 IDE HDD Auto Detection

The "**IDE HDD AUTO DETECTION**" utility is a very useful tool specially when you
do not know which kind of hard disk type you are using. You can use this utility to detect

the correct disk type installed in the system automatically. But now you can set HARD DISK TYPE to auto in the STANDARD CMOS SETUP.
You don't need the"IDE HDD AUTO DETECTION" utility. The BIOS will Auto-detect the hard disk size and model on display during POST.

ROM PCI/ISA BIOS (2A5LXXXX) CMOS SETUP UTILITY AWARD SOFTWARE, INC.								
HARD DISK	TYPE	SIZE	CYLS	HEADS	PRECOMP	LANDZONE	SECTORS	MODE
Primary Master		343	665	16	65535	664	63	Normal
Primary Slave								
Secondary Master								
Secondary Slave								

Note: HDD modes
The Award BIOS supports 3 HDD modes : Normal, LBA&LARGE.

Normal mode:
Generic access mode in which either the BIOS or the IDE controller will make any transformations during accessing.
The maximum number of cylinders, head & sectors for Normal mode are 1024, 16 & 63.

$$\begin{array}{ll} \text{no.Cyclinder} & (1024) \\ \text{x no.Head} & (16) \\ \text{x no.Sector} & (63) \\ \text{x no.per sector} & (512) \\ \hline \multicolumn{2}{c}{\text{528 Megabytes}} \end{array}$$

If user set in Normal mode, the maximum accessible HDD size will be 528 Megabyte even though its physical size may be greater than that !

LBA (Logical Block Addressing) mode:
A new HDD accessing method to overcome the 528 Megabyte bottleneck. The number of cylinders, head & sectors show in setup may not be the number physically contained in the HDD.
During HDD accessing, the IDE controller will transform the logic address described by sector, head & cylinder into its own physical address inside the HDD.
The maximum HDD size supported by LBA mode is 8.4 Gigabytes which is obtained by the following formula:

$$\begin{array}{ll} \text{no.Cylinder} & (1024) \\ \text{x no.Head} & (255) \\ \text{x no.Sector} & (63) \\ \text{x bytes.per sector} & (512) \\ \hline \multicolumn{2}{c}{\text{8.4 Gigabytes}} \end{array}$$

LARGE mode:
Extended HDD access mode supported by Award Software.

Some IDE HDDs contain more than 1024 cylinder without LBA support(in some cases, user do not want LBA). The Award BIOS provides another alternative to support these kinds of LARGE mode:

CYLS.	HEADS	SECTOR	MODE
1120	16	59	Normal
560	32	59	Large

BIOS tricks DOS (or other OS) that the number of cylinders is less than 1024 by dividing it by 2. At the same time, the number of heads is multiplied by 2. Averse transformation process will be made inside INT 12h in order to access the right HDD addess the right HDD address !

```
        no.Cylinder      (1024)
     x no.Head            (32)
     x no.Sector          (63)
     x bytes.per sector  (512)
     --------------------------------
               1 Gigabytes
```

> **Note:**
> **To support LBA or LARGE mode of HDDs, there must be some softwares involved. All these softwares are located in the Award HDD Service Routine (INT 13h). It may be failed to acc1ess a HDD with LBA (LARGE) mode selected if you are runing under a operating system which replaces the whole INT 13h. UNIX operating systems do not support either or LARGE and Must utilize the standard mode. UNIX can support drives large than 528MB.**

3-11 Save & Exit Setup

After you have made changes under Setup, press <ESC> to return to the main menu.
Move cursor to "Save and Exit Setup" or press "F10" and then press "Y" to change the CMOS setup. If you did not change anything, press <ESC> again or move cursor to "Exit Without Saving" and press "Y" to retain the Setup settings.
The following message will appear at the center of the screen to allow you to save data to CMOS and exit the setup utility.

SAVE to CMOS and EXIT (Y/N)?

3-12 Exit Without Saving

The "**EXIT WITHOUT SAVING**" option will bring you back to normal boot up procedure without saving any into CMOS RAM.
All of the old data in the CMOS will not be destroyed.
If you select this feature, the following message will appear at the center of the screen to allow you to exit the setup utility without saving CMOS modifications:

Quit Without Saving(Y/N)?

5VPX2

END

Addendum

Additional information about JV1:

Intel Pentium® Processor installation

CPU clock	SYS. clock	JCK 1	JCK2	JCK3	JCK 4	JBF0	JBF1	JPW1	**JV1**	Ratio
P54C 90 MHZ 3.3V	60 MHZ	1-2	2-3	2-3	2-3	open	open	1-2,5-6,7-8	**open**	1.5x
P54C 100 MHZ 3.3V	66 MHZ	2-3	1-2	2-3	2-3	open	open	1-2,5-6,7-8	**open**	1.5x
P54C 120 MHZ 3.3V	60 MHZ	1-2	2-3	2-3	2-3	close	open	1-2,5-6,7-8	**open**	2x
P54C 133 MHZ 3.3V	66 MHZ	2-3	1-2	2-3	2-3	close	open	1-2,5-6,7-8	**open**	2x
P54C 150 MHZ 3.3V	60 MHZ	1-2	2-3	2-3	2-3	close	close	1-2,5-6,7-8	**open**	2.5x

P54C 166 MHZ 3.3V	66 MHZ	2-3	1-2	2-3	2-3	close	close	1-2,5-6,7-8	**open**	2.5x
P55C 166 MHZ 2.8/3.3V	66 MHZ	2-3	1-2	2-3	2-3	close	close	7-8	**1-2, 3-4**	2.5x
P54C 200 MHZ 3.3V	66 MHZ	2-3	1-2	2-3	2-3	open	close	1-2,5-6,7-8	**open**	3x
P55C 200 MHZ 2.8/3.3V	66 MHZ	2-3	1-2	2-3	2-3	open	close	7-8	**1-2, 3-4**	3x
P55C 233 MHZ 2.8/3.3V	66 MHZ	2-3	1-2	2-3	2-3	open	open	7-8	**1-2, 3-4**	3.5x

Cyrix® 6x86 Processor installation

CPU clock	SYS. clock	JCK1	JCK2	JCK3	JCK4	JBF0	JBF1	JPW1	**JV1**	Ratio
120+ M1	50 MHZ	2-3	2-3	2-3	1-2	close	open	1-2,3-4,5-6,7-8	**open**	2x
133+ M1	55 MHZ	2-3	2-3	1-2	2-3	close	open	1-2,3-4,5-6,7-8	**open**	2x
150+ M1	60 MHZ	1-2	2-3	2-3	2-3	close	open	1-2,3-4,5-6,7-8	**open**	2x
166+ M1	66 MHZ	2-3	1-2	2-3	2-3	close	open	1-2,3-4,5-6,7-8	**open**	2x
6X68L 133	55 MHZ	2-3	2-3	1-2	2-3	close	open	7-8	**1-2, 3-4**	2x
6X86L 150	60 MHZ	1-2	2-3	2-3	2-3	close	open	7-8	**1-2, 3-4**	2x
6X86L 166	66 MHZ	2-3	1-2	2-3	2-3	close	open	7-8	**1-2, 3-4**	2x
6X86L 200	75 MHZ	1-2	2-3	1-2	2-3	close	open	7-8	**1-2, 3-4**	2x
6X86L 200	66 MHZ	2-3	1-2	2-3	2-3	close	close	7-8	**1-2, 3-4**	2.5x
6X86MX 166	66 MHZ	2-3	1-2	2-3	2-3	close	open	1-2, 7-8	**1-2, 3-4**	2x
6X86MX200	66 MHZ	2-3	1-2	2-3	2-3	close	close	1-2, 7-8	**1-2, 3-4**	2.5x
6X86MX 200	75 MHZ	1-2	2-3	1-2	2-3	close	open	1-2,7-8	**1-2, 3-4**	2x

AMD® K5/K6 Processor installation

CPU clock	SYS. clock	JCK1	JCK2	JCK3	JCK4	JBF0	JBF1	JPW1	**JV1**	Ratio
K5-PR90/PR120	60 MHZ	1-2	2-3	2-3	2-3	open	open	1-2,3-4,5-6,7-8	**open**	1.5x
K5-PR100/PR133	66 MHZ	2-3	1-2	2-3	2-3	open	open	1-2,3-4,5-6,7-8	**open**	1.5x
K5-PR166	66 MHZ	2-3	1-2	2-3	2-3	close	close	1-2,3-4,5-6,7-8	**open**	2.5x
K6-PR166	66 MHz	2-3	1-2	2-3	2-3	close	close	1-2,7-8	**1-2, 3-4**	2.5x
K6-PR200	66 MHZ	2-3	1-2	2-3	2-3	open	close	1-2,7-8	**1-2, 3-4**	3x
K6-PR233	66 MHZ	2-3	1-2	2-3	2-3	open	open	5-6,7-8	**1-2, 3-4**	3.5x

Please see the modified version related to JV1:

JCK1-4 - CPU Speed Selector

Jumper	50MHZ	55MHZ	60MHZ	66MHZ	75MHZ
JCK1	2-3	2-3	1-2	2-3	1-2
JCK2	2-3	2-3	2-3	1-2	2-3
JCK3	2-3	1-2	2-3	2-3	1-2
JCK4	1-2	1-2/2-3	1-2/2-3	1-2/2-3	1-2/2-3
PCICLK	25	27.5/32	30/32	33.3/32	37.5/32

Note: 1. JCK4 is PCI synchronous/asynchronous selection. Do not select "1-2" when using 75 MHz.

JPW1 - CPU Voltage Selector (FOR ONE REGULATOR)

Description	CPU Voltage	JPW1	JV1
3.3V	Core: 3.3V I/O: 3.3 V	1-2,5-6,7-8	OPEN
(P54C-STD,VR, AMD® K5-C,F, Cyrix 6X86-016)			
3.52V	Core: 3.4 ~ 3.6V I/O: 3.4 ~ 3.6V	1-2,3-4,5-6,7-8	OPEN
(P54C-VRE, AMD® K5-B, Cyrix® 6X86-028)			

(FOR TWO REGULATOR)

Description	CPU Voltage	JPW1	JV1
2.8V	Core: 2.8V I/O: 3.3V	7-8	**1-2, 3-4**
(INTEL P55C, AMD® K5-H,J, Cyrix® 6x86L)			
2.9V	Core: 2.9V I/O: 3.3V	1-2,7-8	**1-2, 3-4**
(AMD® K6, Cyrix® 6x86MX)			
3.2V	Core: 3.2V I/O: 3.3V	5-6,7-8	**1-2, 3-4**
(AMD® K6)			

*Note : INTEL P55C MMX, AMD® K6 AND CYRIX®
6X86L are "Dual Voltage CPUs" , "6X86L" is CYRIX® New
Low Power CPU.

ADDENDUM(5VPX2)

PLEASE FIND THE BELOW NEW CPU JUMPER SETTINGS:

REG: Cyrix® MX PR233 2.9/3.3V

CPU CLOCK	SYS. CLOCK	JCK1	JCK2	JCK3	JCK4	JBF0	JBF1	JPF2	JPW1	JV1	RATIO
MX PR233+ 2.9/3.3V	75 MHZ	1-2	2-3	1-2	2-3	CLOSE	CLOSE	OPEN	1-2, 7-8	1-2, 3-4	2.5X
MII 300 2.9/3.3V	66 MHZ	2-3	1-2	2-3	2-3	OPEN	OPEN	OPEN	1-2,7-8	1-2,3-4	3.5X

REG: AMD® K6 NEW CPUS

CPU CLOCK	SYS. CLOCK	JCK1	JCK2	JCK3	JCK4	JBF0	JBF1	JBF2	JPW1	JV1	RATIO
K6-PR233 3.3V/3.3V	66MHZ	2-3	1-2	2-3	2-3	OPEN	OPEN	OPEN	1-2, 5-6, 7-8	1-2, 3-4	3.5X
K6-PR266 3.3V/3.3V	66MHZ	2-3	1-2	2-3	2-3	CLOSE	OPEN	CLOSE	3-4	1-2, 3-4	4X
K6-PR300 2.2/3.45V	66MHZ	2-3	1-2	2-3	2-3	CLOSE	CLOSE	CLOSE	3-4	1-2, 3-4	4.5X