Part No. 03-0061X-03

586F61/F61-PB

User's Manual

Table Of Contents

Chapter 1
Introduction
586F61/F61-PB Mainboard Features 4
Static Electricity Precautions 6
586F61 Mainboard Layout 7
586F61 Mainboard Jumper & Connector Location 8
586F61-PB Mainboard Layout 9
586F61-PB Mainboard Jumper & Connector Location 10

Chapter 2
Hardware Guide
Setting Jumpers
CPU Bus Clock Selection 11
CPU Core to Bus Clock Ratio Selection 11
CPU Voltage Selection 12
Cache Memory Selection 12
A. 586F61 Cache Memory Selection 12
B. 586F61-PB Cache Memory Selection 15
CMOS RAM Clearance 17

Attaching Connectors
Front Panel Connectors 17
I/O Port Connectors 18
Cable Set 19
Power Supply Connector 19
Voltage Regulator Module (VRM) 19
PS/2 Mouse Connector 21

Installing System Memory 21

Chapter 3
Software Guide
Software Setup.
Running AWARD BIOS 23
The Main Program Screen 24
STANDARD CMOS SETUP 25
BIOS FEATURES SETUP 27
CHIPSET FEATURES SETUP 30
POWER MANAGEMENT SETUP 32
PCI CONFIGURATION SETUP 34
LOAD BIOS DEFAULTS 37
LOAD SETUP DEFAULTS 37
SUPERVISOR/USER PASSWORD 38
IDE HDD AUTO DETECTION 38
SAVE & EXIT SETUP 39
EXIT WITHOUT SAVING 39

1 Introduction

586F61/F61-PB Mainboard Features

The 586F61/F61-PB is a high performance, function enhanced computer Mainboard that combines the power of Pentium Class CPU and the PCI Local bus. The features integrated onto the 586F61/F61-PB Mainboard are as follows:

. **CPU:** Supports the following CPUs in a ZIF socket.
- Intel Pentium P54C/P54CT/P54CTB/P55C - 75/90/100/ 120/133/150/166/180/200+ MHz with VRM and Socket 7.
- AMD K5 (reserved)
- Cyrix M1 (reserved)

. **Chipset:** Intel 82430FX Chipset.

. **Cache Memory:** Supports Asynchronous / Synchronous (Burst or Pipelined Burst SRAM), 256KB or 512KB Cache Memory.

. **Main Memory:**
- 72-Pin DRAM SIMM modules in multiple configurations up to 128MB.
- Supports Fast Page Mode and Extended Data Output (EDO) SIMMs.
- Supports Symmetric and Asymmetric SIMMs.

. **On-Board I/O:**
- 32-bit enhanced PCI IDE controller with two connectors supports four IDE devices in two channels. The controller supports both PIO and Bus Master IDE, up to Mode 4 timing with transfer rates to 22 MB/Second.

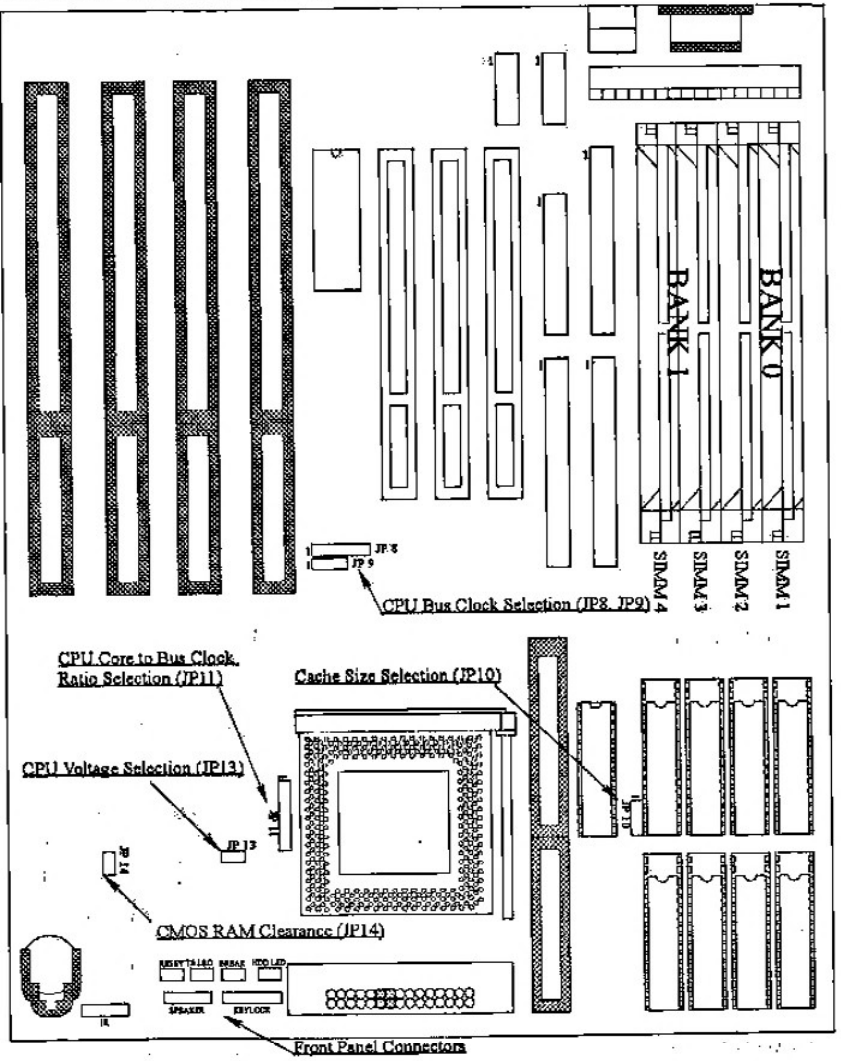
- Supports two 16550 Compatible high speed serial ports, one standard/ECP/EPP bi-directional parallel port, and one floppy disk controller.
- Supports one IrDA Compatible infra-red port for infra-red communication. (reserved).

. **Slots:**
- Four 16-bit ISA and three 32-bit Bus Master PCI expansion slots.

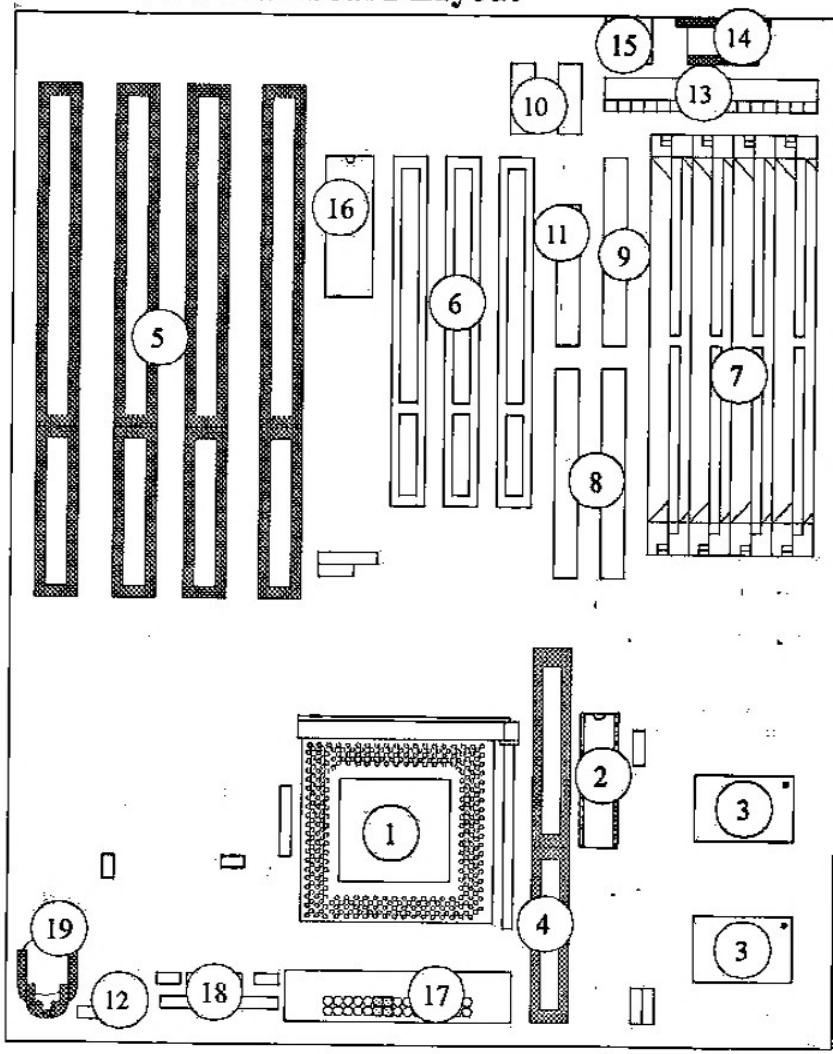
. **Keyboard / Mouse:**
- Provides Standard Keyboard connector for AT type keyboard and 6-pin header for PS2 mouse interface.
- PS2 Keyboard connector and PS2 Mouse connector are optional.

. **BIOS:**
- Award Pentium PCI BIOS.
- Flash with ESCD (Extended System Configuration Data) block to fully support Plug and Play.
- Supports Power Management, Plug and Play, and Enhanced IDE Devices.
- Built-in NCR SCSI BIOS firmware to support the NCR 53C810 PCI Fast SCSI controller.

586F61 Mainboard Jumper & Connector Location

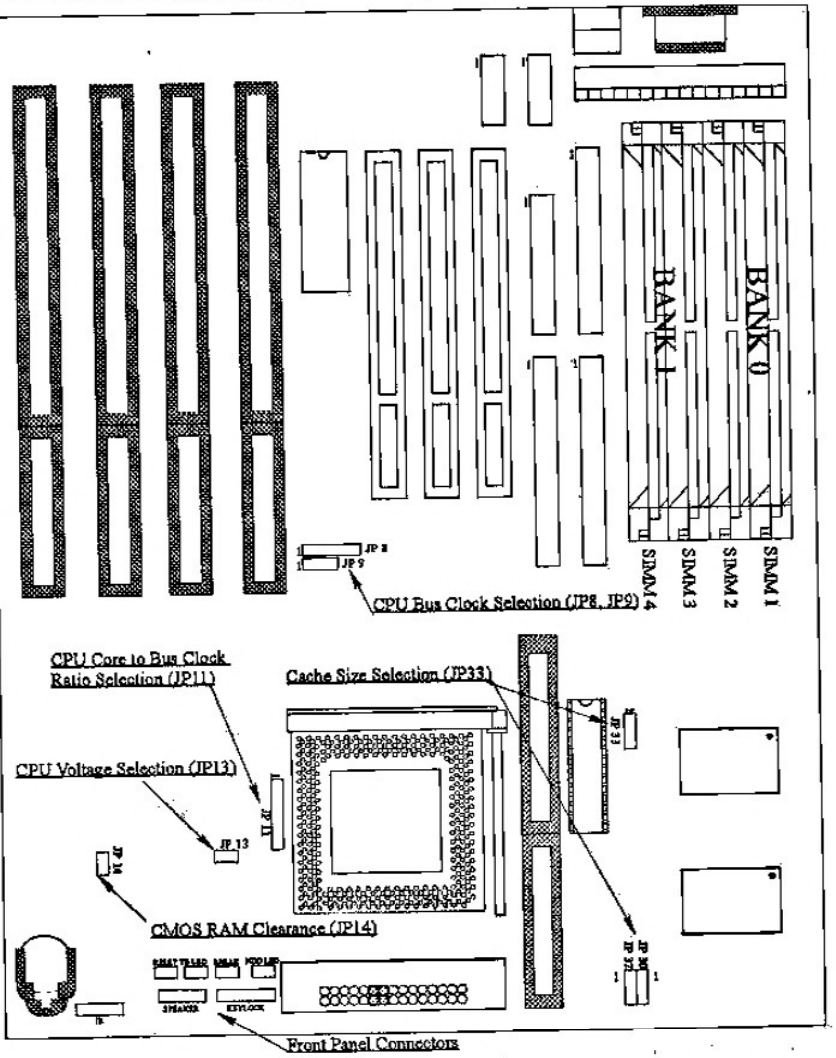


586F61-PB Mainboard Layout



1:CPU
2:TAG SRAM Chips
3:Cache SRAM Chips
4:Cache Slot
5:ISA Expansion Slots
6:PCI Expansion Slots
7:SIMM Module Sockets
8:IDE Connectors
9:Floppy Drive Connector
10:Serial Port Connectors
11:Parallel Port Connector
12:IR Port Connector
13:Power Connector
14:Keyboard Connector
15: PS/2 Mouse Header
16: BIOS ROM
17:VRM Header
18:Front panel Connector
19:Battery (CR2032 Lithium)

586F61-PB Mainboard Jumper & Connector Location



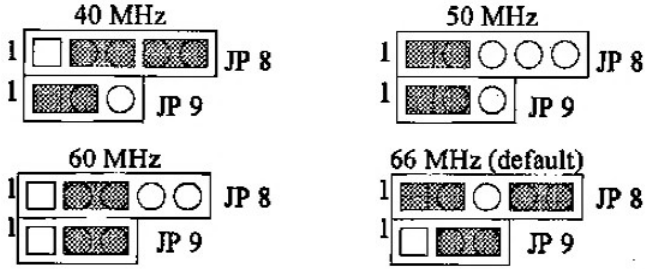
2 Hardware Guide

To install the Mainboard you need to set jumpers, attach connectors and install SIMM memory modules.

Setting Jumpers

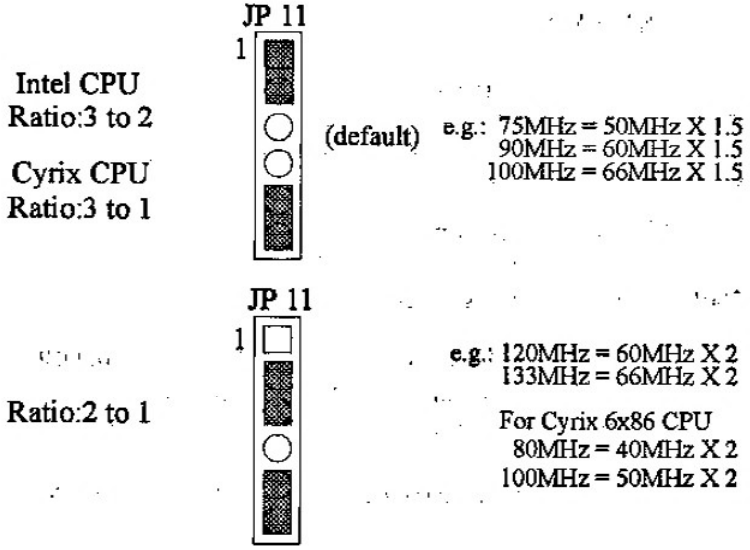
. CPU Bus Clock Selection

This jumper selects different CPU Bus Clock.

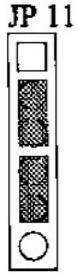


. CPU Core to Bus Clock Ratio Selection

This jumper selects different CPU core to bus clock ratio.

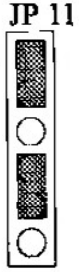


Ratio:5 to 2



e.g.: 150MHz = 60MHz X 2.5
167MHz = 66MHz X 2.5

Ratio:3 to 1



e.g.: 150MHz = 50MHz X 3
180MHz = 60MHz X 3
200MHz = 66MHz X 3

. CPU Voltage Selection

This jumper selects different voltages for the CPU.

JP13

3.3V+5% STD/VR (default)

JP13

3.45V-3.6V VRE

. Cache Memory Selection

A. 586F61 Cache Memory Selection:

The 586F61 Mainboard supports Asynchronous SRAMs in DIP Sockets or Cache Module in the Cache Slot. The 586F61 has two cache size options: 256KB or 512KB.

If using the cache module in the cache slot, neither TAG SRAM

nor DATA SRAMs are installed. Otherwise the system may not function properly. Also the JP10 connection is irrelevant.

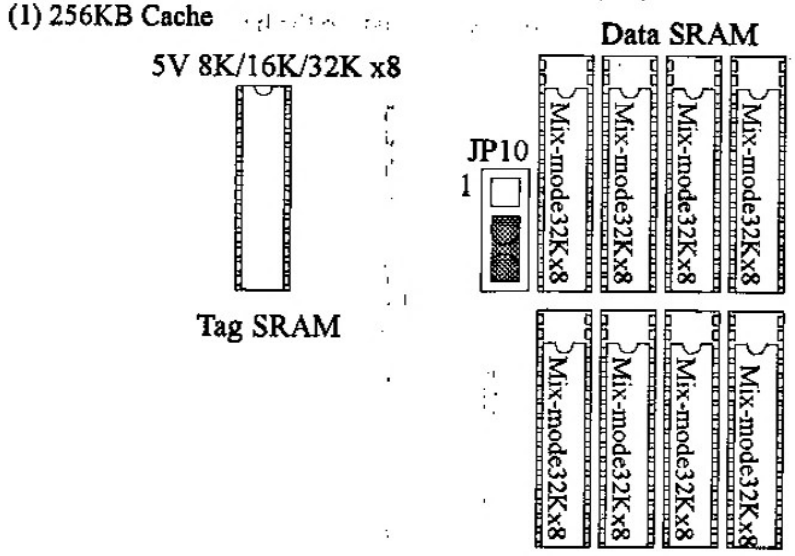
The Chart below shows the Asynchronous SRAM chips required for each configuration.

Cache Size	Tag RAM 15ns, 5V SRAM	Data RAM 15ns, 3.3/5V mix-mode SRAM
256 KB	one 8K/16K/32K x8	eight 32Kx8 chips
512 KB	one 16K/32K x8	eight 64Kx8 chips

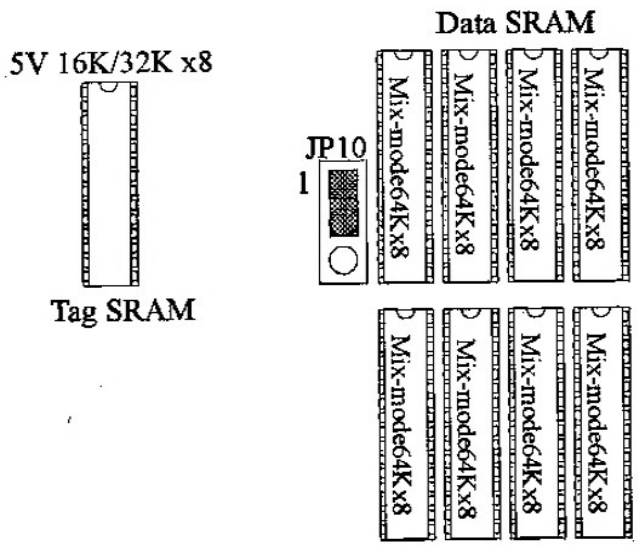
NOTE:
Top 4 socket pins must be open when install a 28-pin SRAM chip in a 32-pin socket.

The figures below show where to install the SRAM chips and jumper setting for each configuration.

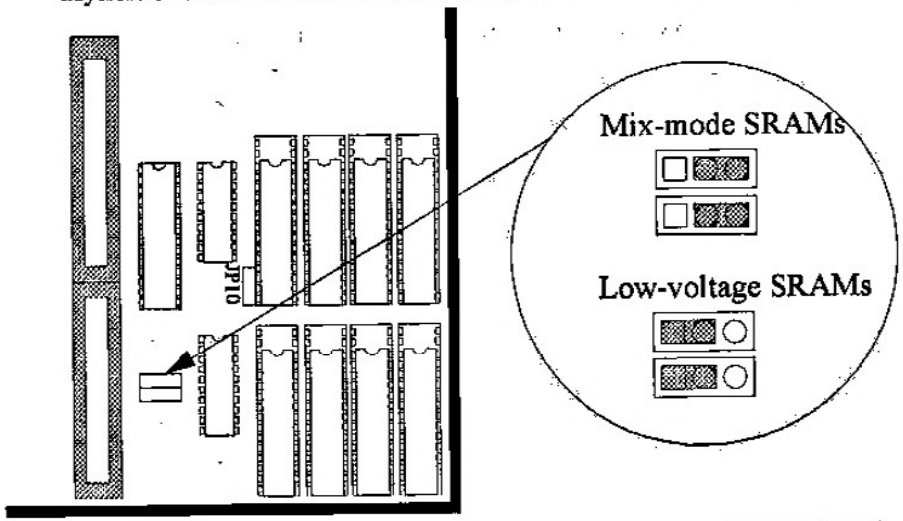
(1) 256KB Cache



(2) 512 KB Cache



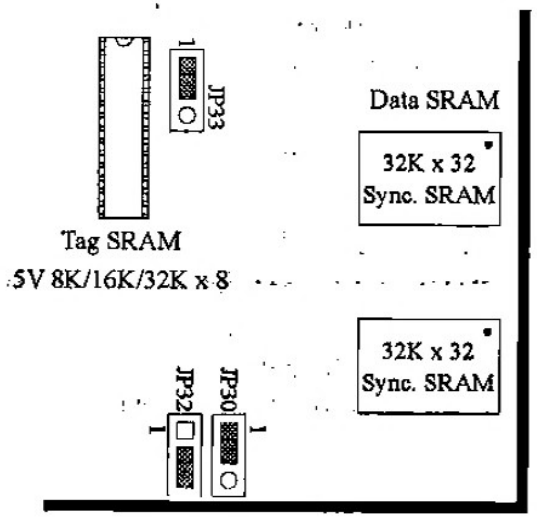
Note: Some 586F61 Mainboards are assembled with the option to use either mix-mode or low-voltage (3.3V) SRAMs as Data RAMs. Those boards are equipped with two 3-pin headers located between the cache slot and asynchronous SRAMs. Install shunts to the headers as follows:



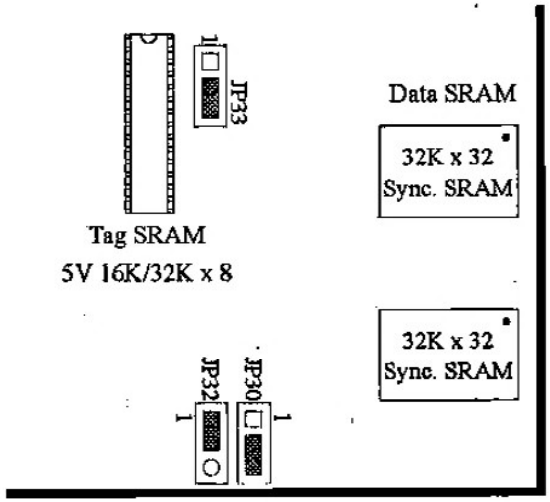
B. 586F61-PB Cache Memory Selection:

The 586F61-PB Mainboard supports Synchronous SRAMs on board and/or Cache module in the Cache Slot. The 586F61-PB has two cache size options: 256KB or 512KB. The figures below show jumper setting for each configuration.

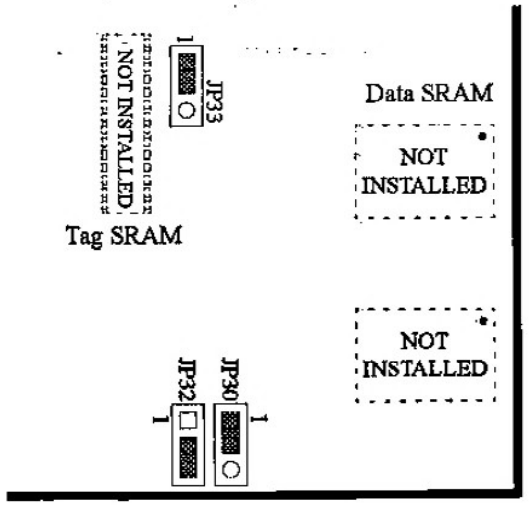
(1) 256KB Cache On Board



(2) 256KB Cache On Board and 256KB Cache Module, Total 512KB
Note: Only Cache Module designed following Intel COAST specification will work in this configuration.



(3) 256KB/512KB Cache Module:
Neither Tag SRAM nor DATA SRAMs are installed



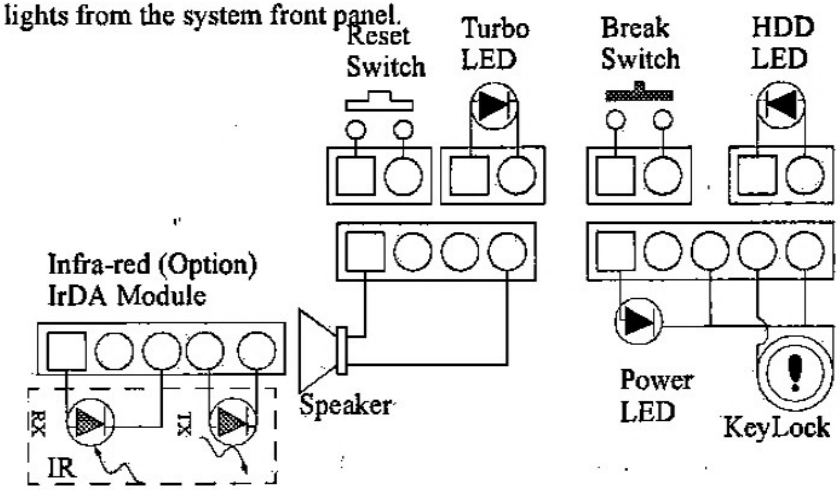
. CMOS RAM Clearance

If you need to clear the CMOS RAM data, put a shunt to short JP14 pin1 to pin2 for 5 seconds and the data stored in the CMOS RAM will be wiped out.

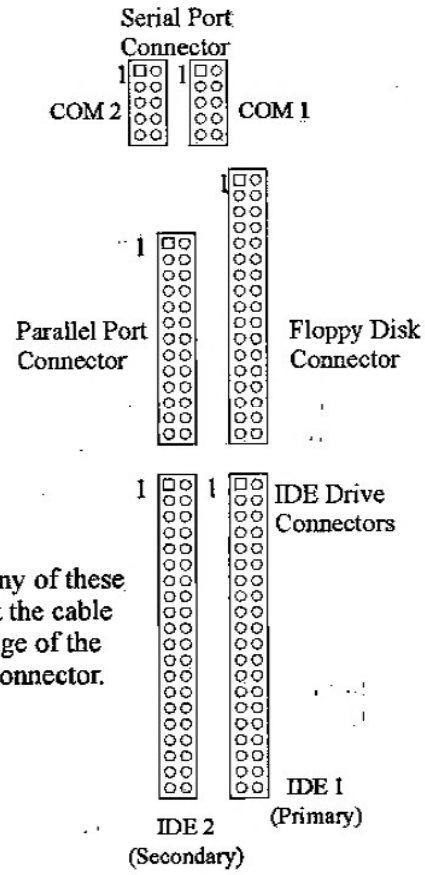
Attaching Connectors

. Front Panel Connectors

There are 7 connectors on the Mainboard for switches and indicator lights from the system front panel.



I/O Port Connectors



Pin 1 is the upper left pin on each port connector.

When you attach a ribbon cable to any of these I/O port connectors, you must orient the cable connector so that the pin 1(color) edge of the cable is at the pin 1 of the I/O port connector.

Cable Set

Included with 586F61/F61-PB Mainboard is a cable set which contains:

- one IDE Cable.
- one floppy disk drive cable.
- two serial ports cable with mounting bracket.
- one parallel port cable with mounting bracket.

Power Supply Connector

The Power Supply Connector on the Mainboard is a 12-pin male connector. **Make sure the power supply is unplugged before connect the leads from the power supply.** Most power supplies have two leads. Each lead has six wires, two of which are black. Connect the leads with the four black wires at the center.

Voltage Regulator Module (VRM)

The Voltage Regulator Module (VRM) Socket provides flexibility to support various Pentium processor with different voltage requirements in one mainboard.

The VRM can be defined as a voltage converter with a standardized pin-out capable of converting the system power supply voltage to the voltage required for the Processor Core.

:P54C/P54CT/P54CTB
0/100/120/133/150/167/180/200 MHz
Voltage 3.135 V ~ 3.60 V

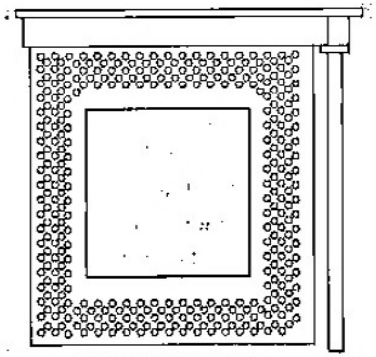
all 2 shunts to short VRM socket
11 to pin13 and pin12 to pin14.
VRM Required
CTB based on P55C requires
ket 7

:P54C/P54CT/P54CTB
0/100/120/133/150/167/180/200 MHz
Voltage 3.4 V ~ 3.6 V

all 2 shunts to short VRM socket
11 to pin13 and pin12 to pin14
all a shunt to short JP13 pin1 to
2 (see CPU Voltage Selection
umper Setting)
VRM Required
CTB based on P55C requires
ket 7

:P55C 150/167/180/200 MHz
Voltage 2.5 V

uires a 2.5 V VRM
uires Socket 7



. PS/2 Mouse Connector

The PS/2 Mouse connector (PS2MS) is a 6-pin header for the lead from a case-mounted PS/2 mouse port.

Installing System Memory

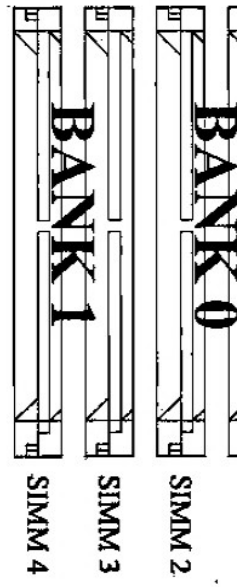
The 586F61/F61-PB Mainboard has four SIMM Sockets to support up to 128MB of system memory. The four SIMM sockets (SIMM1 ~ SIMM4) are divided into 2 Banks, Bank0 (SIMM1, SIMM2) and Bank1 (SIMM3, SIMM4).

Memory can be installed by using 4MB, 8 MB, 16MB, 32 MB, 72-pin EDO or Fast Page Mode SIMM memory modules. Due to the 586F61/F61-PB Mainboard high speed design, the memory modules for the 586F61/F61-PB must meet all of following requirements:

Modules Size: Single-sided 4MB, 16MB.
Double-side 8MB, 32MB.
DRAM Type: Fast page mode or
Extended Data Output (EDO).
DRAM Speed : 70ns or faster
RAS Access Time : 60ns ~ 70ns
CAS Access Time : 10ns ~ 25ns

SIMMs have cut-out at one end that matches an extension on one of the vertical posts of each socket.

You must use two SIMM modules at a time, and each pair of modules must be the same size, mode and speed.



The following are all available memory configuration:

SIMM Socket 1&2	SIMM Socket 3&4	Total Memory
4MB x 2	NONE	8MB
4MB x 2	4MB x 2	16MB
4MB x 2	8MB x 2	24MB
4MB x 2	16MB x 2	40MB
4MB x 2	32MB x 2	72MB
8MB x 2	NONE	16MB
8MB x 2	4MB x 2	24MB
8MB x 2	8MB x 2	32MB
8MB x 2	16MB x 2	48MB
8MB x 2	32MB x 2	80MB
16MB x 2	NONE	32MB
16MB x 2	4MB x 2	40MB
16MB x 2	8MB x 2	48MB
16MB x 2	16MB x 2	64MB
16MB x 2	32MB x 2	96MB
32MB x 2	NONE	64MB
32MB x 2	4MB x 2	72MB
32MB x 2	8MB x 2	80MB
32MB x 2	16MB x 2	96MB
32MB x 2	32MB x 2	128MB
NONE	4MB x 2	8MB
NONE	8MB x 2	16MB
NONE	16MB x 2	32MB
NONE	32MB x 2	64MB

3 Software Guide

Software Setup

After hardware configuration of 586F61/F61-PB Mainboard is completed, and system hardware has been assembled, the completed system may be powered up. At this point, software setup should be run to ensure that system information is correct.

Normally, system setup is needed when the system hardware is not consistent with the information contained in the CMOS RAM, whenever the CMOS RAM has lost power, or the system features need to be changed.

Running AWARD BIOS

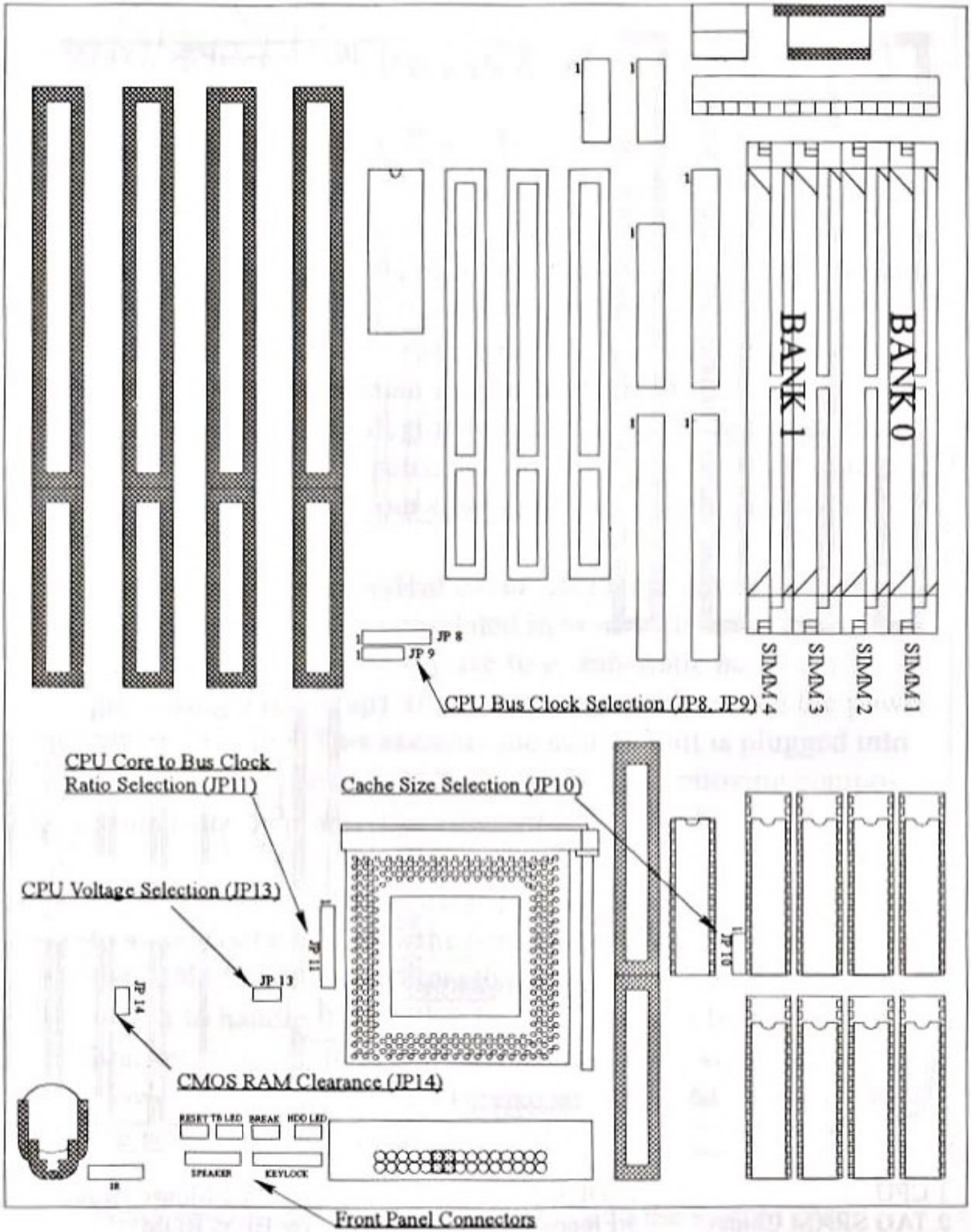
When the system is powered on, the BIOS will enter the Power-On Self Test (POST) routines. These routines perform various diagnostic checks at the time the system is powered up; if an error is encountered, the error will be reported in one of two different ways. If the error occurs before the display device is initialized, a series of beeps will be transmitted. If the error occurs after the display device is initialized, the screen will display the error message.

After the POST routines are completed, the following message appears:

"Press DEL to enter SETUP"

To access the AWARD BIOS SETUP program, press the <DEL> key. The main program screen will be displayed at this time.

586F61 Mainboard Jumper & Connector Location



586F61-PB Mainboard Jumper & Connector Location