FCC Notice:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy. If not installed and used properly, in strict accordance with the manufacturer's instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures :

Reorient or relocate the receiving antenna.

Increase the separation between the equipment and receiver.

Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

Consult the dealer or an experienced radio/television technician for help and for additional suggestions.

The user may find the following booklet prepared by the Federal Communications Commission helpful "How to Identify and Resolve Radio-TV Interference Problems." This booklet is available from the U.S. Government Printing Office. Washington, DC 20402, Stock 004-000-00345-4

FCC Warning

The user is cautioned that changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

Note : In order for an installation of this product to maintain compliance with the limits for a Class B device, shielded cables and power cord must be used.

CE Notice:

Following standards were applied to this product, in order to achieve compliance with the electromagnetic compatibility :

- Immunity in accordance with EN 50082-1: 1992
- Emissions in accordance with EN 55022: 1987 Class B.

NOTICE

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Manual Ver 1.3

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TABLE OF CONTENTS

1 DESCRIPTION 3
1.1 Overview 3
1.1.1 HOT-559S Layout 4
1.1.1 HOT-559 Layout 5
1.2 Form Factor 6
1.3 Microprocessor 6
1.4 Memory 6
1.5 Chipset 7
1.6 I/O Controller 8
1.7 Real-Time Clock, CMOS RAM 8
1.8 Main Board Connectors 9
1.9 Add-in Board Expansion Connectors 10

2 JUMPER SETTINGS 11
2.1 Jumper Block Overview 11
2.2 CPU Configuration JP12, JP14, JP15 and JP27 12
2.3 Onboard Regulator Output JP24, JP25 13
2.4 Other Jumpers Setting 14

3 BIOS AND SETUP UTILITY 15
3.1 Introduction 15
3.2 BIOS Upgrades 15
3.3 Entering Setup 15
3.4 The Main Menu 16
3.5 Standard CMOS Setup 18
3.6 BIOS Feature Setup 20
3.7 Chipset Features Setup 22
3.8 Power Management Setup 25
3.9 PCI Configuration Setup 27
3.10 Integrated Peripherals 29
3.11 Password Setting 32

1 Description

1.1 Overview

This manual applied to two HOT-559 main boards - with (HOT-559S) or without (HOT-559) SCSI onboard.

HOT-559 is an Intel 430VX ATX mainboard with 4 PCI/4 ISA slot onboard and HOT-559S the same with the HOT-559 except provides Adaptec AIC7880 Ultra Wide SCSI adapter onboard and support RAID(Redundant Array of Inexpensive Disks).

The HOT-559(S) main board integrates the Pentium microprocessor, memory, and I/O technologies into a standard ATX form factor.

The HOT-559(S) main board design support Pentium and Pentium MMX processors 75～233MHz, Cyrix/IBM 6x86 and 6x86L P120+～P166+, AMD K5 PR75～PR166 and K6 PR2-166～PR2-266. The other HOT-559 main board features include:

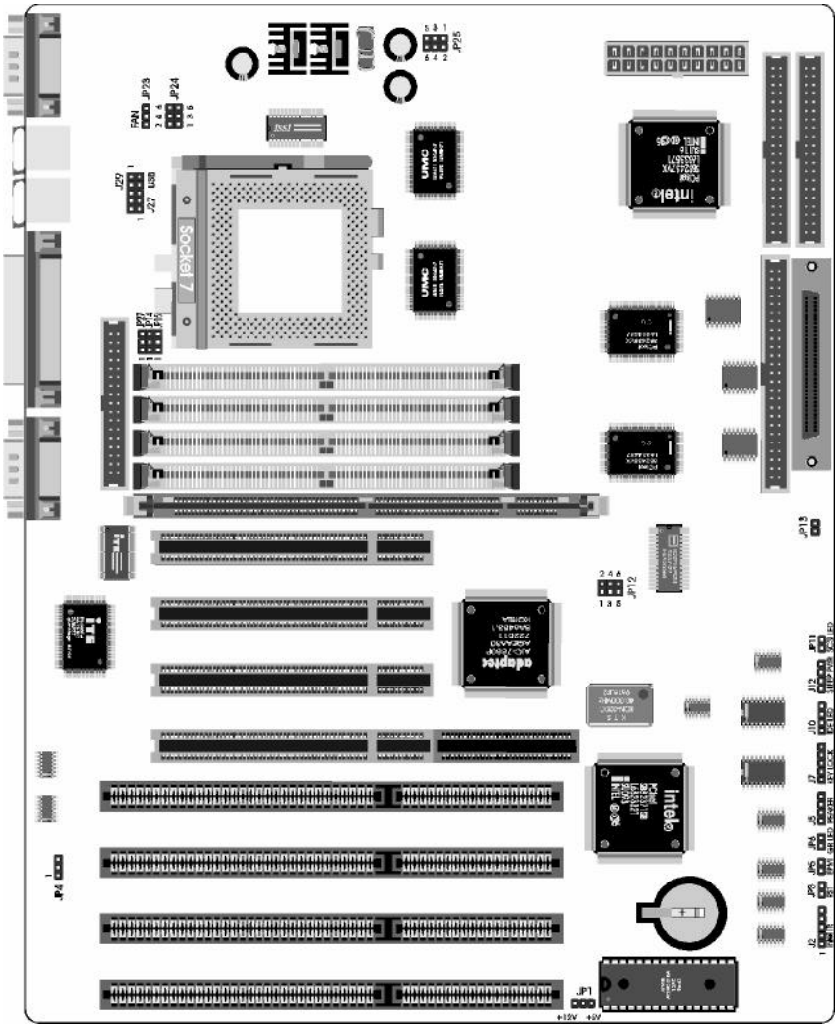
- ❒ Supports 8MB to 128 MB of Synchronous DRAM, EDO DRAM or standard Fast Page DRAM in 72-pin SIMM and 168-pin DIMM sockets.
- ❒ Type 7 Pentium OverDrive socket provides an upgrade to future OverDrive , Cyrix 6x86/6x86L and AMD K5/K6 processors
- ❒ Intel's 82430VX PCIset
- ❒ ITE 8680 Giga I/O controller
- ❒ Bus mastering IDE
- ❒ Supports pipeline burst cache with size of 512KB or 256KB
- ❒ Onboard Adaptec AIC-7880 16-bit Ultra Wide SCSI Controller (HOT-559S)
- ❒ Expansion

  32-bit PCI slot x 4 on HOT-559 - support four PCI bus masters
  32-bit PCI slot x 4 on HOT-559S - support three PCI bus masters (PCI1 support slave PCI device only)
  Expansion slot x 1 for RAID adapter (HOT-559S)
  16-bit ISA slot x 4
  50-pin SCSI-II connector x 1 (HOT-559S)
  68-pin Ultra Wide SCSI connector x 1 (HOT-559S)
  Enhance IDE port x 2
  Floppy port x 1
  Serial port x 2 (IrDA Infra-Red port including)
  USB port x 2

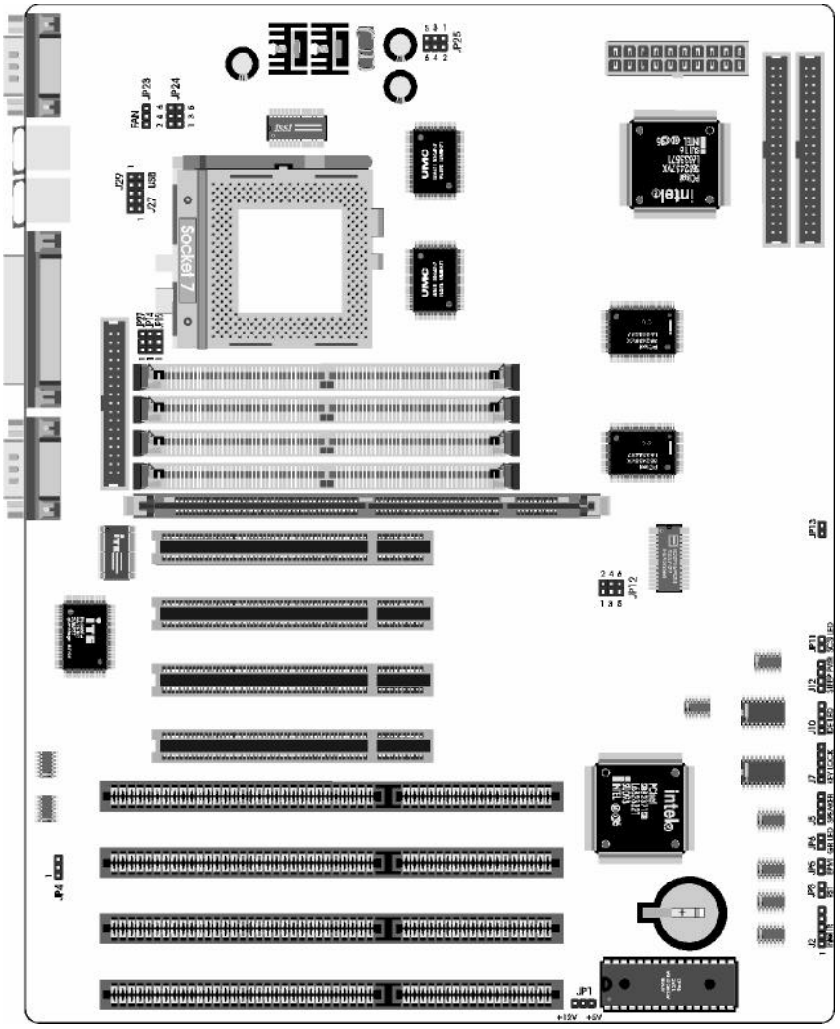
- ❒ BIOS

  Award 4.51PG PnP Green BIOS

1.1.1 HOT-559S Layout



1.1.2 HOT-559 Layout



1.2 Form Factor

The HOT-559(S) main board is designed to fit into a standard ATX form factor chassis. The ATX form factor does not adhere to the standard ATX guidelines in that the outer dimensions are 305mm x 240mm. Location of the I/O connectors, riser slot, and mounting holes are in strict compliance with the ATX specification.

1.3 Microprocessors

The HOT-559(S) main board is designed to operate with 3volt range Pentium/MMX Processor and Cyrix 6x86/6x86L and AMD K5/K6 processors. An onboard switching voltage regulator circuit provides the required 3 volts range from the 5.0 volt tap of the power supply. Pentium/MMX processors that run internally at 75, 90, 100, 120, 133, 150, 166, 200 and 233 MHz are supported.
Cyrix 6x86/6x86L processors that run internally at P120+, P133+, P150+ and P166+ are supported.
AMD K5 processors that run internally at PR75, PR90, PR120, PR100, PR133, PR150, PR166, and K6 processor that run internally PR2-166, PR2-200, PR2-233 and PR2-266 are supported.

1.4 Memory

Second-level Cache

The Intel 82430VX Xcelerated Controller PCIset supports 512KB or 256KB second level cache that uses the Synchronous Pipeline Burst SRAM. Pipeline Burst (PB) SRAM provides performance similar to Synchronous Burst SRAMs for only a slight cost premium over slower performing Asynchronous SRAMs.

Main System Memory

The HOT-559 mainboard provides four 72-pin SIMM sockets and one 168-pin DIMM socket that make it possible to install up to 128MB of RAM. The SIMM socket support 4MB, 8MB, 16MB, and 32MB 5V single- or double-side fast page or EDO DRAM modules, and DIMM socket support 8MB, 16MB, 32MB, . ., 3.3V single- or double-side SDRAM, fast page, or EDO modules.

Caution : The user should not populate both 5V SIMM modules & 3.3V DIMM modules at the same time.

The four SIMM sockets are arranged in two banks of two sockets each, the DIMM socket arranged in one bank provides a 64/72-bit wide data path.

Both SIMMs in a bank must be of the same memory size and type, although the different types of memory may differ between banks. It is possible to have 70 ns fast page DRAM in one bank and 60 ns EDO DRAM in the other.

1.5 Chipset

The Intel 82430VX PCIset consists of the 82437VX System Controller (TVX), 82438VX Data Path (TDX) and one 82371SB PCI ISA/IDE Xcelerator (PIIX3) bridge chip.

82437VX System Controller (TVX), 82438VX Data Path (TDX)

The Intel 430VX PCIset provides all control signals necessary to drive a second level cache and the DRAM array, including multiplexed address signals. The 430VX PCIset also controls system access to memory and generates snoop controls to maintain cache coherency. The 82437VX comes in a 208-pin QFP package and 82438VX comes in a 100-pin QFP package.

82371SB PCI ISA/IDE Xcelerator (PIIX3)

The PIIX3 provides the interface between the PCI and ISA buses and integrates a dual channel fast IDE interface capable of supporting up to 4 devices. The PIIX3 integrates seven 32-bit DMA channels, one 16-bit timer/counters, two eight-channel interrupt controllers, PCI -to-AT interrupt mapping circuitry, NMI logic, ISA refresh address generation, and PCI/ISA bus arbitration circuitry together onto the same device. The PIIX3 comes in a 208-pin QFP package.

IDE Support

The HOT-559(S) main board provides two independent high performance bus-mastering PCI IDE interfaces capable of supporting PIO Mode 3 and Mode 4 devices. The system BIOS supports Logical Block Addressing (LBA) translation modes as well as ATAPI (e.g. CD-ROM) devices on both IDE interfaces. Detection of IDE device transfer rate and translation mode capability is automatically determined by the system BIOS.

Onboard Adaptec AIC-7880 SCSI Controller (HOT-559 S)

The onboard Adaptec AIC-7880 SCSI controller is a Wide PCI-to-SCSI host adapters provide a powerful multitasking interface between system's PCI bus and SCSI devices (disk drives, CD-ROM drives, scanners, tape backups, removable media drives, etc). Up to a total of 15 SCSI devices can be connected to the onboard 50-pin 8-bit SCSI-II and 68-pin 16-bit Ultra wide SCSI connectors.

RAID (HOT-559S)

At today, the more network storage capacity expands, the more critical it becomes to find a solution that maximizes data availability and performance. While tape backup meets disaster recovery requirements, it does not ensure that continuous availability and data integrity necessary to keep your network up and running. TheRedundant Array of Inexpensive Disks (RAID) support on-line, real-tim data recovery that overcomes the physical limitations of hard disk drives to delevery uninterrupted data access.

RAID storage systems offer the potential for exceptional data availability and performance that is far superior to individual drives.

HOT-559S provides an optional RAID slot for Adaptec PCI RAID adapter to fulfill RAID solutions.

1.6 I/O Controller

Control for the integrated serial ports, parallel port, floppy drive, is incorporated into a single component, the ITE 8680F. This component provides :

- ❒ Two 16C550-compatible UARTs with send/receive 16 byte FIFO
- ❒ Support for an Infra Red interface
- ❒ Multimode bidirectional parallel port
  - – Standard mode; IBM and Centronics compatible
  - – Enhanced Parallel Port (EPP) with BIOS/Driver support
  - – High Speed mode; Extended Capabilities Port (ECP) compatible
- ❒ Industry standard floppy controller with 16 byte data FIFO (2.88 MB floppy support)

1.7 Real-Time Clock, CMOS RAM

The onboard real-time clock (RTC) is builted in ITE 8680 I/O chip which provide a 24-hour clock mode and totally nonvolatile with over 10 years of operation in the absence of power. The RTC can be set via the BIOS SETUP program. The RTC also supports 128byte battery-backed CMOS RAM in two banks which is reserved for BIOS use. The CMOS RAM can be set to specific values or cleared to the system default values using the BIOS SETUP program. Also, The CMOS RAM values can be cleared to the system defaults by using a configuration jumper on the HOT-559(S) main board.

1.8 Main Board Connectors

There are connectors on-board for Power supply, Floppy, IDE, back panel connector, and front panel I/O.

Front panel Connector

The HOT-559(S) main board provides header connectors to support function typically located on the chassis bezel. Front panel features support include :

* Infra-red (IrDA) Port
* System Reset
* EPMI
* Green LED
* System Speaker
* Power LED & KeyLock
* IDE Hard Drive active LED
* Sleep & Power Control Port
* SCSI Hard Drive active LED

Speaker

The external speaker provides error beep code information during the Power-on Self Test, if the system cannot use the video interface.

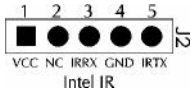
Sleep / Resume

When Advanced Power Management (APM) is activated in the system BIOS and the Operating System's APM driver is loaded, Sleep mode (Standby) can be entered in one of three ways: an optional front panel "Sleep/Resume" button, a user defined keyboard hot key, or prolonged system inactivity. The Sleep/Resume button is supported by a 2-pin header located on the front panel I/O connector. Closing the "Sleep" switch will generate an SMI (System Management Interrupt) to the processor which immediately goes into System Management Mode (SMM), the so called "Sleep" mode.

The front panel "Sleep mode" switch must be a momentary two pin SPST type that is normally open. The function of the Sleep/Resume button can also be achieved via a keyboard hot-key sequence, or by a time-out of the system inactivity timer. Both the keyboard hot-key and inactivity timer are programmable in the BIOS setup. To reactivate the system, or "Resume", the user must simply press the sleep/resume button again, or use the keyboard or mouse. Mouse activity will only "wake up" the system is a mouse driver is loaded. While the system is in Stand-by or "sleep" mode it is fully capable of responding to and servicing external interrupts (such as incoming FAX) even though the monitor will only turn on if a user interrupt (keyboard/mouse) occurs as mentioned above.

Infra-red (IrDA) connector

Serial port 2 can be configured to support an IrDA module via a 5-pin header connector. Once configured for IrDA, the user can transfer files to or from portable devices such as laptops, PDA's and printers using application software such as LapLink. The IrDA specification provides for data transfers at 115Kbps from a distance of 1 meter.



Reset

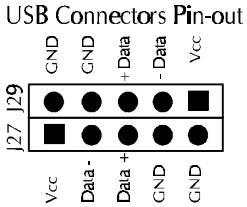
This 2-pin header can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the system will hard reset and run POST.

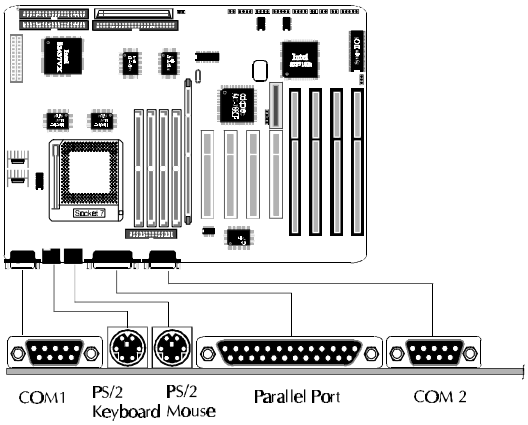
Back Panel Connectors

The back panel provides external access to PS/2 style keyboard and mouse connectors as well as two serial and one parallel port, which are integrated on the HOT-559 main board. (please refer to diagram on next page)

USB Connectors

The main board provides two sets USB (Universal Serial Bus) connectors - J27 and J29 for USB devices use.





1.9 Add-in Board Expansion Connectors

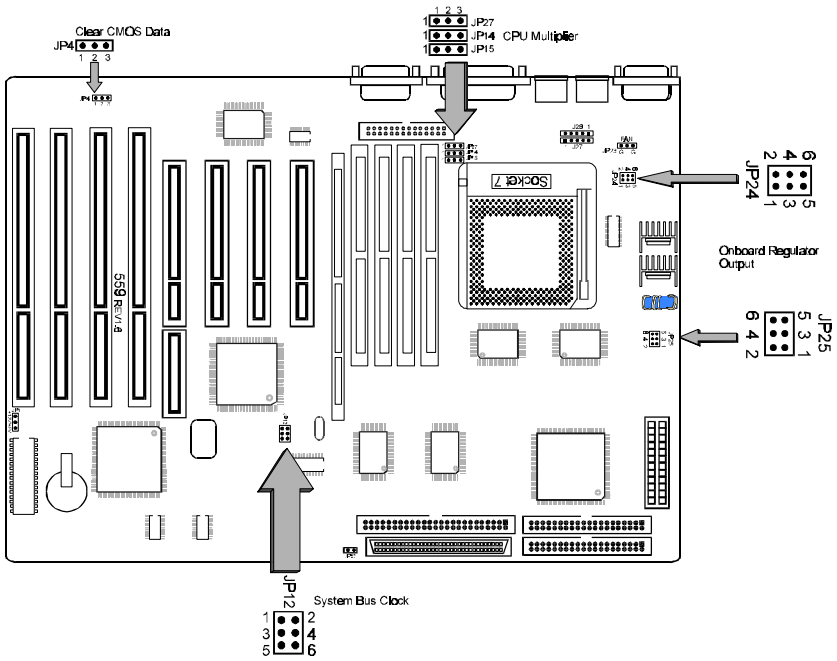
Expansion Slots support up to four PCI and up to four ISA add-in boards. The PCI bus is fully compliant with the PCI 2.1 specification and supports up to four bus master through the four PCI connectors (or three PCI connectors when Adaptec AIC-7880 SCSI controller on board.)

2 Jumper Settings

2.1 Jumper Block Overview

The HOT-559(S) main board contains configuration jumpers that make it possible to change the system configuration. The system has been properly configured at the factory. Normally, the only time you will ever change a jumper is if you need to:

- Change the processor operating speed (system bus clock x multiplier)
- Change the system regulator voltage output for the processor requiring
- Clear CMOS Data



2.2 CPU Clock Configuration - JP12, JP27, JP14 and JP15

These jumpers allow the HOT-559(S) main board to be switched between different speeds of the Pentium/MMX, AMD, and Cyrix processors. Jumper JP12 is used to set the system bus frequency from 50 MHz to 66 MHz and also affect the PCI clock (system clock /2) speeds. Jumpers JP27, JP14 and JP15 are used to set the processor multiplier from 1.5 to 4.

CPU Freq. (MHz)	JP12			Host Bus Freq. (MHz)	JP27	JP14	JP15	CPU Clock Multiplier
	Pin 1-2	Pin 3-4	Pin 5-6					
Pentium MMX 233 MHz	Close	Open	Close	66	Pin 2-3 Close	Pin 2-3 Close	Pin 2-3 Close	x 3.5
Pentium MMX 200 MHz	Close	Open	Close	66	Pin 2-3 Close	Pin 1-2 Close	Pin 2-3 Close	x 3
Pentium 200 MHz	Close	Open	Close	66	Pin 2-3 Close	Pin 1-2 Close	Pin 2-3 Close	x 3
Pentium MMX 166 MHz	Close	Open	Close	66	Pin 2-3 Close	Pin 1-2 Close	Pin 1-2 Close	x 2.5
Pentium 166 MHz	Close	Open	Close	66	Pin 2-3 Close	Pin 1-2 Close	Pin 1-2 Close	x 2.5
Pentium MMX 150 MHz	Open	Close	Close	60	Pin 2-3 Close	Pin 1-2 Close	Pin 1-2 Close	x 2.5
Pentium 150 MHz	Open	Close	Close	60	Pin 2-3 Close	Pin 1-2 Close	Pin 1-2 Close	x 2.5
Pentium 133 MHz	Close	Open	Close	66	Pin 2-3 Close	Pin 2-3 Close	Pin 1-2 Close	x 2
Pentium 120 MHz	Open	Close	Close	60	Pin 2-3 Close	Pin 2-3 Close	Pin 1-2 Close	x 2
Pentium 100 MHz	Close	Open	Close	66	Pin 2-3 Close	Pin 2-3 Close	Pin 2-3 Close	x 1.5
Pentium 90 MHz	Open	Close	Close	60	Pin 2-3 Close	Pin 2-3 Close	Pin 2-3 Close	x 1.5
Pentium 75 MHz	Close	Close	Close	50	Pin 2-3 Close	Pin 2-3 Close	Pin 2-3 Close	x 1.5

CPU Freq. (MHz)	JP12			Host Bus Freq. (MHz)	JP27	JP14	JP15	CPU Clock Multiplier
	Pin 1-2	Pin 3-4	Pin 5-6					
AMD K-6 PR2-266	Close	Open	Close	66	Pin 1-2 Close	Pin 2-3 Close	Pin 1-2 Close	x 4
AMD K-6 PR2-233	Close	Open	Close	66	Pin 2-3 Close	Pin 2-3 Close	Pin 2-3 Close	x 3.5
AMD K-6 PR2-200	Close	Open	Close	66	Pin 2-3 Close	Pin 1-2 Close	Pin 2-3 Close	x 3
AMD K-6 PR2-166	Close	Open	Close	66	Pin 2-3 Close	Pin 1-2 Close	Pin 1-2 Close	x 2.5
AMD K-5 PR166	Close	Open	Close	66	Pin 2-3 Close	Pin 1-2 Close	Pin 1-2 Close	x 1.75
AMD K-5 PR150	Open	Close	Close	60	Pin 2-3 Close	Pin 1-2 Close	Pin 1-2 Close	x 1.75
AMD K-5 PR133	Close	Open	Close	66	Pin 2-3 Close	Pin 2-3 Close	Pin 2-3 Close	x 1.5
AMD K-5 PR120	Open	Close	Close	60	Pin 2-3 Close	Pin 2-3 Close	Pin 2-3 Close	x 1.5
AMD K-5 PR100	Close	Open	Close	66	Pin 2-3 Close	Pin 2-3 Close	Pin 2-3 Close	x 1.5
AMD K-5 PR90	Open	Close	Close	60	Pin 2-3 Close	Pin 2-3 Close	Pin 2-3 Close	x 1.5
AMD K-5 PR75	Close	Close	Close	50	Pin 2-3 Close	Pin 2-3 Close	Pin 2-3 Close	x 1.5

CPU Freq. (MHz)	JP12			Host Bus Freq. (MHz)	JP27	JP14	JP15	CPU Clock Multiplier
	Pin 1-2	Pin 3-4	Pin 5-6					
Cyrix 6x86L PR166	Close	Open	Close	66	Pin 2-3 Close	Pin 2-3 Close	Pin 1-2 Close	x 2
Cyrix 6x86 PR166	Close	Open	Close	66	Pin 2-3 Close	Pin 2-3 Close	Pin 1-2 Close	x 2
Cyrix 6x86L PR150	Open	Close	Close	60	Pin 2-3 Close	Pin 2-3 Close	Pin 1-2 Close	x 2
Cyrix 6x86 PR150	Open	Close	Close	60	Pin 2-3 Close]	Pin 2-3 Close	Pin 1-2 Close	x 2
Cyrix 6x86 PR133	Close	Close	Open	55	Pin 2-3 Close	Pin 2-3 Close	Pin 1-2 Close	x 2
Cyrix 6x86 PR120	Close	Close	Close	50	Pin 2-3 Close	Pin 2-3 Close	Pin 1-2 Close	x 2

2.3 Onbaord Regulator Output- JP24, JP25

HOT-559(S) main board is designed with an advanced onboard switching voltage regulators to provide 3.3V ~3.52V range voltage ($V_{IO}=V_{CORE}$) for intel Pentium P54C, Cyrix 6x86 and AMD K5 processors; and also provide dual 3.3/2.8V~ 3.3/3.2V ranges voltage (V_{IO}, V_{CORE} separated) for Intel Pentium P55C, Cyrix/IBM 6x86L and AMD K6 processors. Single or dual voltages output according to the following tables.

Processors	Vcore	JP24	JP25
Pentium MMX 150~233 MHz	2.8 V	Pin 5-6 Close	Pin 1-3, 2-4 Close
AMD K-6 PR2-166/200	2.9 V	Pin 1-2, 5-6 Close	
AMD K-6 PR2-233/266	3.2 V	Pin 3-4 Close	
Cyrix 6x86L PR150/166	2.8 V	Pin 5-6 Close	

Processors	Vcore	JP24	JP25
Pentium 75~200 MHz	3.3 V	Pin 3-4, 5-6 Close	Pin 3-5, 4-6 Close
AMD K-5 PR75~166	3.52 V	Pin 1-3, 5-6 Close	
Cyrix 6x86 PR120~166(3.3V)	3.3 V	Pin 3-4, 5-6 Close	
Cyrix 6x86 PR120~166	3.52 V	Pin 1-3, 5-6 Close	

2.4 Other Jumper Setting

Adaptec AIC-7880 SCSI Termination - JP13 (HOT-559S)

To ensure reliable communication, the SCSI bus must be properly terminated. Termination is controlled by a set of resistors, called terminators. Terminators must be placed at the two extreme ends of the SCSI bus. HOT-559S onboard Wide SCSI controller provides 16-bit terminator that divided two 8-bit terminator - high byte and low byte, which low byte controls 8-bit SCSI; the low and high byte together control 16-bit Wide SCSI.

Termination on the HOT-559S is controlled by JP13. The default setting is OFF(Open). If Wide SCSI controller on HOT-559S is not a ends of the SCSI bus, set JP13 to ON(Close).

Clear CMOS (JP4)

HOT-559(S) supports jumper JP4 for discharging mainboard's CMOS memory. The CMOS memory retains the system configuration information in the component of R.T.C.

You should move the jumper cap from pin 1-2 to Pin 2-3 of JP4 for a brief moment when you wish to clear CMOS memory, and then make sure remove the jumper cap back to pin 1-2 for normal operation to retain your new CMOS data.

Flash EEPROM Vpp (JP1)

HOT-559(S) mainboard supports two types of flash EEPROM: 5 volt and 12 volt. By setting up jumper JP1, you can update both types of flash EPROM with new system BIOS files as they come available.

Pin 2-3 Close for 5V,
Pin 1-2 Close for 12V.

BIOS UPGRADES

Flash memory makes distributing BIOS upgrades easy. A new version of the BIOS can be installed from a diskette.

Please note the following when making the BIOS updates.

** Flash utility can't work under protected/virtual mode. Memorymanager like QEMM.386, EMM386 should not be loaded. (or Simply bypass all config.sys and autoexec.bat on system boot up.

** Flash utility supports both 5V and 12V Flash EPROM.

3 BIOS and Setup Utility

3.1 Introduction

The HOT-559(S) main board uses an Award BIOS, which is stored in Flash EEPROM and easily upgraded using a floppy disk-based program. In addition to the Award BIOS, the Flash EEPROM also contains the Setup utility, Power-on Self Tests (POST), APM 1.2, the PCI auto-configuration utility, and Windows 95 ready Plug and Play. This HOT-559 main board also supports system BIOS shadowing, allowing the BIOS to execute from 64-bit on-board write-protected DRAM.

3.2 BIOS Upgrades

Flash memory makes distributing BIOS upgrades easy. A new version of the BIOS can be installed from a diskette.

The disk-based Flash upgrade utility, AWDFLASH.EXE, please note the following when making the BIOS updates.

- The Flash BIOS can be updated from a file on a disk;
- The current BIOS code can be copied from the Flash EEPROM to a disk file as backup in the event that an upgrade cannot be successfully completed;
- Flash utility can't work under protected/virtual mode. Memorymanager like QEMM386, EMM386 should not be loaded. (or Simply bypass all config.sys and autoexec.bat)

3.3 Entering Setup

HOT-559 BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed RAM so that it retains the Setup information when the power is turned off.

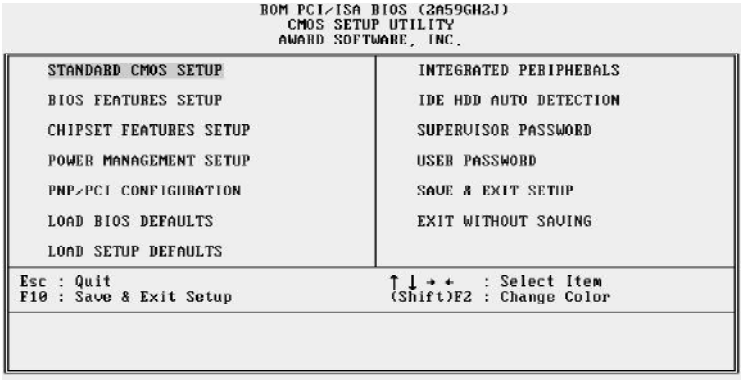
Power on the computer and press <Del> immediately will allow you to enter Setup. The other way to enter Setup is to power on the computer, when the below message appear briefly at the bottom of the screen during the POST (Power On Self Test), press <Del> key or simultaneously press <Ctrl>,<Alt>, and <Esc> keys.

TO ENTER SETUP BEFORE BOOT PRESS CTRL-ALT-ESC OR DEL KEY

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF the ON or pressing the "RESET" button on the system case. You may also restart by simultaneously press <Ctrl>,<Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to,

PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP

3.4 The Main Menu



Standard CMOS setup

This setup page includes all the items in a standard compatible BIOS.

BIOS features setup

This setup page includes all the items of Award special enhanced features.

Chipset features setup

This setup page includes all the items of chipset features.

Power Management Setup

This setup page includes all the items of Power Management features.

PCI Configuration setup

This item specifies the value (in units of PCI bus blocks) of the latency timer for the PCI bus master and the IRQ level for PCI device. Power-on with BIOS defaults

Load BIOS Defaults

BIOS defaults loads the values required by the system for the maximum performance. However, you may change the parameter through each Setup Menu.

Load Setup Defaults

Setup defaults loads the values required by the system for the O.K. performance. However, you may change the parameter through each Setup Menu.

Integrated Peripherals

This setup page includes all the items of peripheral features.

IDE HDD auto detection

Automatically configure IDE hard disk drive parameters.

Supervisor Password

Change, set, or disable supervisor password. It allows you to limit access to the system and Setup, or just to Setup.

User Password

Change, set, or disable user password. It allows you to limit access to the system and Setup, or just to Setup.

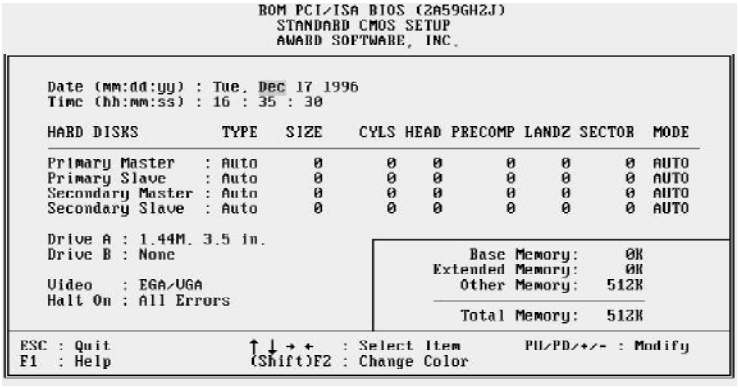
Save & Exit setup

Save CMOS value change to CMOS and exit setup

Exit without saving

Abandon all CMOS value changes and exit setup.

3.5 Standard CMOS Setup



Date

The date format is <day>, <month> <date> <year>. Press <F3> to show the calendar.

Time

The time format is <hour> <minute> <second>. The time is calculated base on the 24-hour military-time clock. For example. 5 p.m. is 17:00:00.

Drive C type/Drive D type

This item identify the types of hard disk drive C and drive D that has been installed in the computer. There are 46 predefined types and a user definable type.

Press PgUp or PgDn to select a numbered hard disk type or type the number and press <Enter>. Note that the specifications of your drive must match with the drive table. The hard disk will not work properly if you enter improper information for this item. If your hard disk drive type is not matched or listed, you can use Type User to define your own drive type manually.

If you select Type User, related information is asked to be entered to the following items. Enter the information directly from the keyboard and press <Enter>. Those information should be provided in the documentation from your hard disk vendor or the system manufacturer.

The user may also set those items to AUTO to auto configure hard disk drives parameter when system power-on.

If a hard disk drive has not been installed select NONE and press <Enter>.

Drive A type/Drive B type

This item specifies the types of floppy disk drive A or drive B that has been installed in the system.

Video

This item selects the type of adapter used for the primary system monitor that must matches your video display card and monitor. Although secondary monitors are supported, you do not have to select the type in Setup.

Error halt

This item determines if the system will stop, when an error is detected during power up.

Memory

This item is display-only. It is automatically detected by POST (Power On Self Test) of the BIOS.

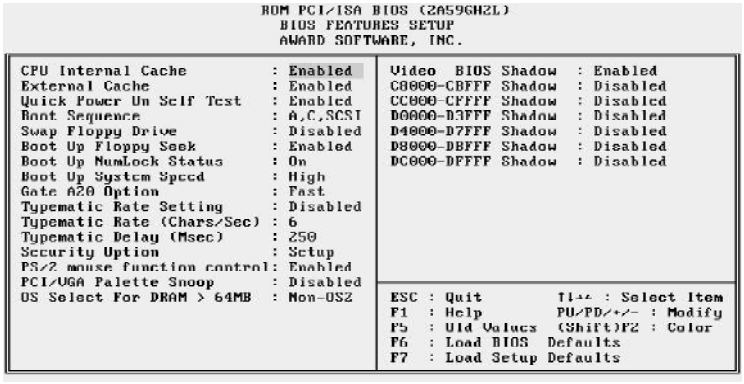
Base Memory

The POST of the BIOS will determine the amount of base (or conventional) memory installed in the system. The value of the base memory is typically 512K for systems with 512K memory installed on the mainboard, or 640K for systems with 640K or more memory installed on the mainboard.

Extended Memory

The BIOS determines how much extended memory is present during the POST. This is the amount of memory located above 1MB in the CPU's memory address map.

3.6 BIOS Features Setup



CPU Internal Cache

This item enables CPU internal cache to speed up memory access.

External Cache

This item enables the external cache to speed up memory access.

Quick Power On Self Test

This item speeds up Power On Self Test (POST) after you power on the computer. If it is set to Enabled, BIOS will shorten or skip some check items during POST.

Boot Sequence

This item determines which drive computer searches first for the disk operating system. The system supports feature of boot from IDE D:, E:, or F: drive (if there are present), boot from CD-ROM, and boot from SCSI drive. Default value is A, C, SCSI.

Swap Floppy Drive

When this item enables, the BIOS will swap floppy drive assignments so that Drive A: will function as Drive B: and Drive B: as Drive A:.

Boot Up Floppy Seek

During POST, BIOS will determine if the floppy disk drive installed is 40 or 80 tracks.

Boot Up NumLock Status

When this option enables, BIOS turns on Num Lock when system is powered on so the end user can use the arrow keys on both the numeric keypad and the keyboard.

Boot Up System Speed

This option sets the speed of the CPU at system boot time. The settings areHigh or Low.

Typematic Rate Setting

This determines if the typematic rate is to be used. when disabled, continually holding down a key on your keyboard will generate only one instance. In other words, the BIOS will only report that the key is down. When the typematic rate is enabled, the BIOS will report as before, but it will then wait a moment, and, if the key is still down, it will begin the report that the key has been depressed repeatedly. For example, you would use such a feature to accelerate cursor movements with the arrow keys.

Typematic Rate (Chars/Sec)

When the typematic rate is enabled, this selection allows you select the rate at which the keys are accelerated.

Typematic Delay (Msec)

When the typematic rate is enabled, this selection allows you to select the delay between when the key was first depressed and when the acceleration begins

Security Option

This item allows you to limit access to the system and Setup, or just to Setup.
When System is selected, the system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
When Setup is selected, the system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

PS/2 Mouse Control Function

This item to set the PS/2 mouse be used or not. If there a PS/2 mouse attached to your system, this item must be enabled, if not, please disabled this item to release IRQ12 for PCI device.

PCI VGA Palette Snoop

This item must be set to enabled if there is a MPEG ISA card installed in the system, and disabled if there is no MPEG ISA card installed in the system.

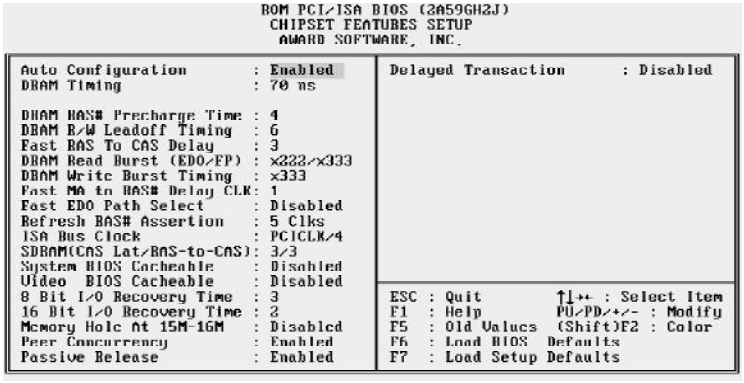
OS Select For DRAM > 64MB

This item allows you to access the memory that over 64 MB in OS/2.

Video BIOS Shadow/XXXXX-XXXXX Shadow

These items determine whether Video BIOS or optional ROM will be copied to RAM.

3.7 Chipset Features Setup



Auto Configuration

This item auto configure the following items: DRAM RAS# Precharge time, DRAM R/W Leadoff Timing, Fast RAS to CAS Delay, DRAM Read Burst, DRAM Write Burst Timing, Fast MA to RAS# Delay CLK, Fast EDO Path Select, Refresh RAS# Assertion, and ISA Bus Clock by different system clock.

DRAM Timing

This item set the DRAM Read/Write timings that the system uses. When item of "Auto Configuration" is disabled, this item will not show up.

DRAM RAS# Precharge Time

DRAM must continually be refreshed or it will lose its data. Normally, DRAM is refreshed entirely as the result of a single request. This option allows you to determine the number of CPU clocks allocated for Row Address Strobe to accumulate its charge before the DRAM is refreshed. If insufficient time is allowed, refresh may be incomplete and data lost.

This item sets the DRAM RAS Precharge Timing. The options are4 and 3 CLKs.

DRAM R/W Leadoff Timing

This item sets the number of CPU clocks allowed before reads and writes to DRAM are performed.

7/6 : Seven clocks leadoff for reads and six clocks leadoff for writes.
6/5 : Six clocks leadoff for reads and five clocks leadoff for writes.

Fast RAS To CAS Delay

When DRAM is refreshed, both rows and columns are address separately. This setup item allows you to determine the timing of the transition from Row Address Strobe (RAS) to Column Address Strobe (CAS). The options are 3 and 2 CLKs.

DRAM Read Burst (EDO/FP)

This item set the EDO/FP DRAM Read Burst Timing. The timing used depends on the type of DRAM (EDO burst mode or standard fast page mode) on a per-bank basis. The options are x222/x333, x333/x444, and x444/x444.

DRAM Write Burst Timing

This item set the DRAM Write Burst Timing. The timing used depends on the type of DRAM (standard page mode or EDO burst mode) on a per-bank basis. The options are x4444, x3333, and x2222.

Fast MA to RAS# Delay CLK

This item is used to set Fast MA (Memory Address) to RAS# Delay which control DRAM Row Miss timings

Fast EDO Path Select

This item is used to defined fast path is selected for CPU to DRAM read cycles for the leadoff, the options are "Enable" or "Disable".

Refresh RAS# Assertion

This item is used to set the number of clocks RAS# is asserted for Refresh cycles.

SDRAM (CAS Lat/RAS-to-CAS)

This item is used to set CAS# Latency and RAS# to CAS# clock for SDRAM. If SDRAMs absent, this item will not show up.

ISA Clock

This item allows the user to set ISA clock that divide from PCI clock by 3 or by 4. For example, if 166MHz Pentium processor is used, PCI clock will be 33MHz, ISA Clock will be 8.25MHz when PCI clock divided by 4, and 11MHz when PCI clock divided by 3.

System BIOS Cacheable

This item allows the user to set whether the system BIOS F000～FFFF areas are cacheable or non-cacheable.

Video BIOS Cacheable

This item allows the user to set whether the video BIOS C000～C7FF areas are cacheable or non-cacheable.

8 Bit I/O Recovery Time

The recovery time is the length of time, measured in CPU clocks, which the system will delay after the completion of an input/output request. This delay takes place because the CPU is operating so much after than the input/output bus that the CPU must be delayed to allow for the completion of the I/O.

This item allows you to determine the recovery time allowed for 8 bit I/O. Choices are from NA, 1 to 8 CPU clocks.

16-Bit I/O Recovery Time

This item allows you to determine the recovery time allowed for 16 bit I/O. Choices are from NA, 1 to 4 CPU clocks.

Memory Hole At 15M-16M

In order to improve performance, certain space in memory can be reserved for ISA cards. This memory must be mapped into the memory space below 16 MB.

Peer Concurrency

Peer concurrency means that more than one PCI device can be active at a time. Enabled this item allows multiple PCI devices can be active.

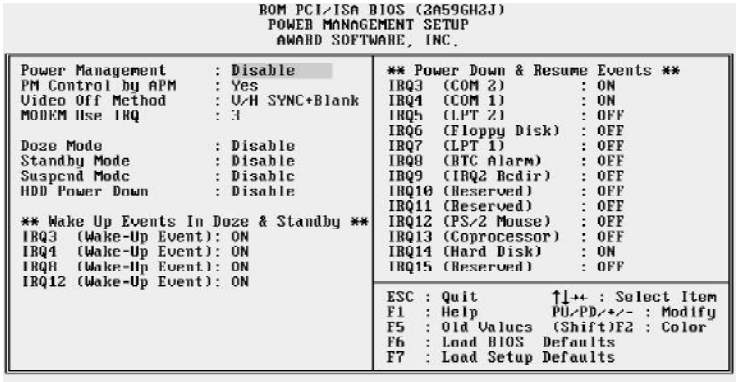
Passive Release

When enabled, the chipset provides a programmable passive release mechanism to meet the required ISA master latencies.

Delayed Transaction

Since the 2.1 revision of the PCI specification requires much tighter controls on target and master latency. PCI cycles to or from ISA typically take longer. When enabled, the chipset provides a programmable delayed completion mechanism to meet the required target latencies.

3.8 Power Management Setup



Power Management

This item determines the options of the power management function. Default value is Disable. The following pages tell you the options of each item & describe the meanings of each options.

Disabled	Global Power Management will be disabled.
User Define	Users can configure their own power management.
Min Saving	Predefined timer values are used such that all timers are in their maximum value.
Max Saving	Predefined timer values are used such that all timers minimum value.

PM Control by APM

If this item set to No, system BIOS will ignore and APM calls when the power is managed the system.
If this item setup to Yes, system BIOS will wait for APM's prompt before it enter any PM mode e.g. DOZE, STANDBY or SUSPEND.

Video Off Method

Blank Screen	The system BIOS will only blanks off the screen when disabling video.
V/H SYN +Blank	In addition to Blank Screen, BIOS will also turn off the V-SYNC & H-SYNC signals from VGA cards to monitor.
DPMS	This function is enabled for only the VGA card supporting DPM.

Doze Mode

1 Min ~ 1 Hr	Defines the continuous idle time before the system enters DOZE mode.

Disable	System will never enter DOZE mode.

Standby Mode

1 Min ~ 1 Hr	Defines the continues idle time before the system enters STANDBY mode.
Disable	System will never enter STANDBY mode.

Suspend Mode

1 Min ~ 1 Hr	Defines the continuous idle time before the system enters SUSPEND mode.
Disable	System will never enter SUSPEND mode.

HDD Power Down

1 ~ 15Min	Defines the continuous HDD idle time before the HDD enters power saving mode (motor off).
Suspend	BIOS will turn the HDD's motor off when system is in SUSPEND mode.
Disable	HDD's motor will not be turn off.

IRQ3, 5, 8, 12 **Wake-Up Events In Doze & Standby**

If these items set to Off, the IRQ3, 5, 8 or 12 event's activity will not reactivates the system from Doze and Standby mode.

If these items set to On, the IRQ3, 5, 8 or 12 event's activity will reactivate system from Doze and Standby mode.

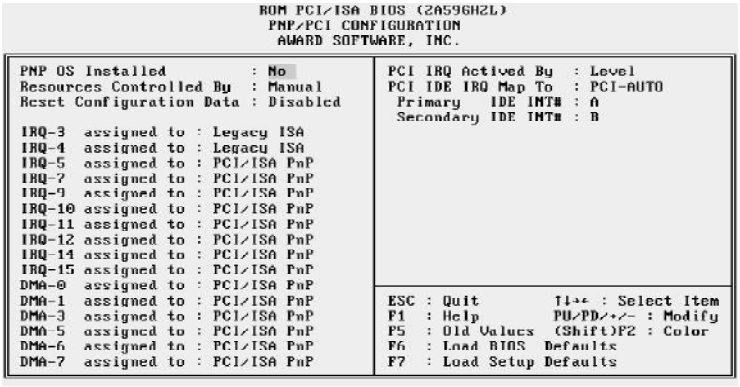
Power Down & Resume Events *

If this items sets to Off, the event's activity will not be monitored to entering power management.

If this items sets to On, the event's activity will be monitored to entering power management.

COM Post Accessed	LPT Ports Accessed	Drive Ports Accessed	IRQ 3 (COM 2)
IRQ 4 (COM1)	IRQ 5 (LPT 2)	IRQ 6 (Floppy Disk)	IRQ 7 (LPT 1)
IRQ 8 (RTC Alarm)	IRQ 9 (IRQ 2 Redir)	IRQ 10 (Reserved)	IRQ 11 (Reserved)
IRQ 12 (PS/2 Mouse)	IRQ 13(Copro-)	IRQ 14 (Hard Disk)	IRQ 15 (Reserved)

3.9 PCI Configuration Setup



PNP OS Installed

When this item is set to Yes, it will allow the PnP OS(Windows 95) control the system resources except PCI devices and PnP boot devices.
Default setting is No.

Resources Controlled By

The Award Plug and Play BIOS has the capability to automatically configure all of the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system as Windows 95.

Reset Configuration Data

This item allows you to determine reset the configuration data or not.

IRQ 3/4/5/7/9/10/11/12/14/15, assigned to

These items allow you to determine the IRQ assigned to the ISA bus and is not available to any PCI slot.

Choices are Legacy ISA and PCI/ISA PnP.

DMA 0/1/3/5/6/7 assigned to

These items allow you to determine the DMA assigned to the ISA bus and is not available to any PCI slot.

Choices are Legacy ISA and PCI/ISA PnP.

PCI IRQ Activated by

This items sets the method by which the PCI bus recognize that an IRQ service is being requested by a device. Under all circumstances, you should not change the default configuration unless advised otherwise by your system's manufacturer. Choices are Level(default) and Edge.

PCI IDE IRQ Map to

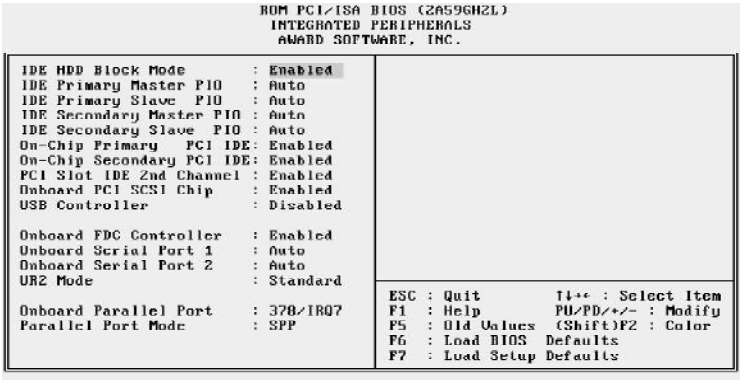
This items allows you to configure your system to the type of IDE disk controller in use. By default, Setup assumes that your controller is an ISA device rather than a PCI controller.

If you have equipped your system with a PCI controller, changing this allows you to specify which slot has the controller and which PCI interrupt (A, B, C or D) is associated with the connected hard drives.

Remember that this setting refers to the hard disk drive itself, rather than individual partitions. Since each IDE controller supports two separate hard disk drivers, you can select the INT# for each. Again, you will note that the primary has a lower interrupt than the secondary as described in "Slot x Using INT#" above.

Selecting "PCI Auto" allows the system to automatically determine how your IDE disk system is configured.

3.10 Integrated Peripherals



IDE HDD Block Mode

This item is used to set IDE HDD Block Mode. If your IDE Hard Disk supports block mode, then you can enable this function to speed up the HDD access time. If not, please disable this function to avoid HDD access error.

IDE Primary Master PIO

In this items, there are five modes defined in manual mode and one automatic mode. There are 0, 1, 2, 3, 4, and AUTO is the default settings for on board Primary Master PIO timing.

IDE Primary Slave PIO

In this items, there are five modes defined in manual mode and one automatic mode. There are 0, 1, 2, 3, 4, and AUTO is the default settings for on board Primary Slave PIO timing.

IDE Secondary Master PIO

In this items, there are five modes defined in manual mode and one automatic mode. There are 0, 1, 2, 3, 4, and AUTO is the default settings for on board Secondary Master PIO timing.

IDE Secondary Slave PIO

In this items, there are five modes defined in manual mode and one automatic mode. There are 0, 1, 2, 3, 4, and AUTO is the default settings for on board Secondary Slave PIO timing.

On-Chip Primary PCI IDE

As stated above, your system includes two built-in IDE controllers, both of which operate on the PCI bus. This setup item allows you either to enable or disable the primary controller. You might choose to disable the controller if you were to add a higher performance or specialized controller.

On-Chip Secondary PCI IDE

As above for the Primary controller, this setup item you either to enable or disable the secondary controller. You might choose to disable the controller if you were to add a higher performance or specialized controller.

Onboard PCI SCSI Chip

This items allows you to set your onboard Adaptec PCI SCSI adapter in use or not. By default, this item set to enable.

This item will not show up when your main board is HOT-559S.

Onboard FDC Control

This item specifies onboard floppy disk drive controller. This setting allows you to connect your floppy disk drives to the onboard floppy connector. Choose the "Disabled" settings if you have a separate control card.

Onboard Serial 1

This item is used to define onboard serial port 1 to 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3, Auto or Disabled.

Onboard Serial 2

This item is used to define onboard serial port 2 to 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3, Auto or Disabled.

UR2 Mode

The main board support IrDA(HPSIR) and Amplitudes Shift Keyed IR(ASKIR) infrared through COM 2 port. This item specifies onboard Infra Red mode to IrDA 1.0, ASKIR, MIR 0.57M, MIR 1.15M, FIR or Standard (Disabled).
Note : FIR is not available currently.

IR Duplex Mode

This item specifies onboard infrared transfer mode to full-duplex or half-duplex. This item will not show up when IrDA, ASKIR, or MIR UR2 modes are selected.

Onboard Parallel Port

This item specifies onboard parallel port address to 378H, 278H, 3BCH or Disabled.

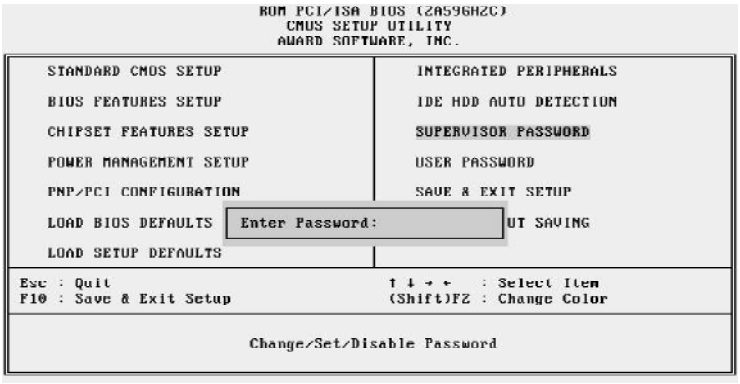
Parallel Port Mode

This item specifies onboard parallel port mode. The options are SPP (Standard Parallel Port), EPP(Enhanced Parallel Port), ECP (Extended Capabilities Port), and EPP+ECP.

ECP Mode Use DMA

This item specifies DMA (Direct Memory Access) channel when ECP device is in use. The options are DMA 1 and DMA 3. This item will not show up when SPP and EPP

3.11 Password Setting



Supervisor Password and User Password

The options on the Password screen menu make it possible to restrict access to the Setup program by enabling you to set passwords for two different access modes: Supervisor mode and User mode.

In general, Supervisor mode has full access to the Setup options, whereas User mode has restricted access to the options. Thus by setting separate Supervisor and User password, a system supervisor can limit who can change critical Setup values.

Enter Password

Type the password, up to eight characters, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password.

To disable password, just press <Enter> when you are prompted to enter password. A message will confirm the password being disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

Password Disable

If you select System at Security Option of BIOS Features Setup Menu, you will be prompted for the password every time the system is rebooted or any time you try to enter Setup. If you select Setup at Security Option of BIOS Features Setup Menu, you will be prompted only when you try to enter Setup.

Warning : Retain a safe record of your password. If you've forgotten or loosed the password, the only way to access the system is to clear CMOS memory, please refer to "Other Jumper Setting" section.

HOT-559

Pentium Processor Based PCI MAIN BOARD

User's Manual