HOT-553

Pentium processor Based PCI MAIN BOARD

User's Manual

CE Notice:

Following standards were applied to this product, in order to achieve compliance with the electromagnetic compatibility: - Immunity in accordance with EN 50082-1: 1992 - Emmitions in accordance with EN 55022: 1987 Class B.

FCC Notice:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy. If not installed and used properly, in strict accordance with the manufacturer's instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures :

Reorient or relocate the receiving antenna.

Increase the separation between the equipment and receiver.

Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

Consult the dealer or an experienced radio/television technician for help and for additional suggestions.

The user may find the following booklet prepared by the Federal Communications Commission helpful "How to Identify and Resolve Radio-TV Interference Problems." This booklet is available from the U.S. Government Printing Office. Washington, DC 20402, Stock 004-000-00345-4

FCC Warning

The user is cautioned that changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

Note : In order for an installation of this product to maintain compliance with the limits for a Class B device, shielded cables and power cord must be used.

NOTICE

Manual Ver 1.6

All information, documentation, and specifications contained in this manual are subject to change without prior notification by the manufacturer.

The author assumes no responsibility for any errors or omissions which may appear in this document nor does it make a commitment to update the information contained herein.

TRADEMARKS

Intel is a registered trademark of Intel Corporation

Pentium™ Processor is a registered trademark of Intel Corporation

PC/AT is a registered trademark of International Business Machine Corporation.

PS/2 is a registered trademark of IBM Corporation.

All other brand and product names referred to in this manual are trademarks or registered trademarks of their respective holders.

TABLE OF CONTENTS

Preface

HOT-553 mainboard is a highly integrated IBM PC/AT compatible system board. The design will accept Intel Pentium, Cyrix/IBM 6x86/L and AMD K5 processors and also features high-performance pipeline burst secondary cache memory support with size of 256KB and 512KB. The memory subsystem is designed to support up to 256 MB of EDO RAM or standard Fast Page DRAM in standard 72-pin SIMM socket. A type 7 Pentium processor socket provides access to future processor enhancements.

HOT-553 provides a new level of I/O integration. Intel's 82430HX PCIset chip set provides increased integration and improved performance over other chip set designs. The 82430HX PCIset chipset provides an integrated Bus Mastering IDE controller with two high performance IDE interfaces for up to four IDE devices.

The onboard Super I/O controller provides the standard PC I/O functions: floppy interface, two FIFO serial ports, an IR device port and a SPP/EPP/ECP capable parallel port.

Up to four PCI local bus slots provide a high bandwidth data path for data-movement intensive functions such as graphics, and up to four ISA slots complete the I/O function.

The HOT-553 provides the foundation for cost effective, high performance, highly expandable platforms, which deliver the latest in Pentium processor and I/O standard

Chapter 1 Introduction

Specification

CPU Function

- Pentium processors: 75~200MHz
- Cyrix/IBM 6x86/L CPU : P90+~P166+ (80~133MHz)
- AMD5k86 CPU clock : PR75~PR166
- Optional VRM is required for Pentium P55C and Cyrix/IBM 6x86 above P120+ and Cyrix/IBM 6x86/L processors

Chipset

- Intel PCISet 82437HX, and 82371SB

Memory

- Supports two banks of EDO RAM and Fast Page DRAM ranging from 8MB to 256MB
- Supports 4MB, 8MB, 16MB, 32MB and 64MB 72-pins SIMMs
- Supports DRAM Error Checking and Correcting (ECC)

Cache Memory

- Integrated L2 write-back cache controller

  - 256KB or 512KB Direct Mapped Pipeline Burst Cache

Power Management Function

- Provides four power management modes : Full on, Doze, Standby and Suspend
- Supports Microsoft APM
- Provides EPMI (External Power Management Interrupt) pin

Expansions

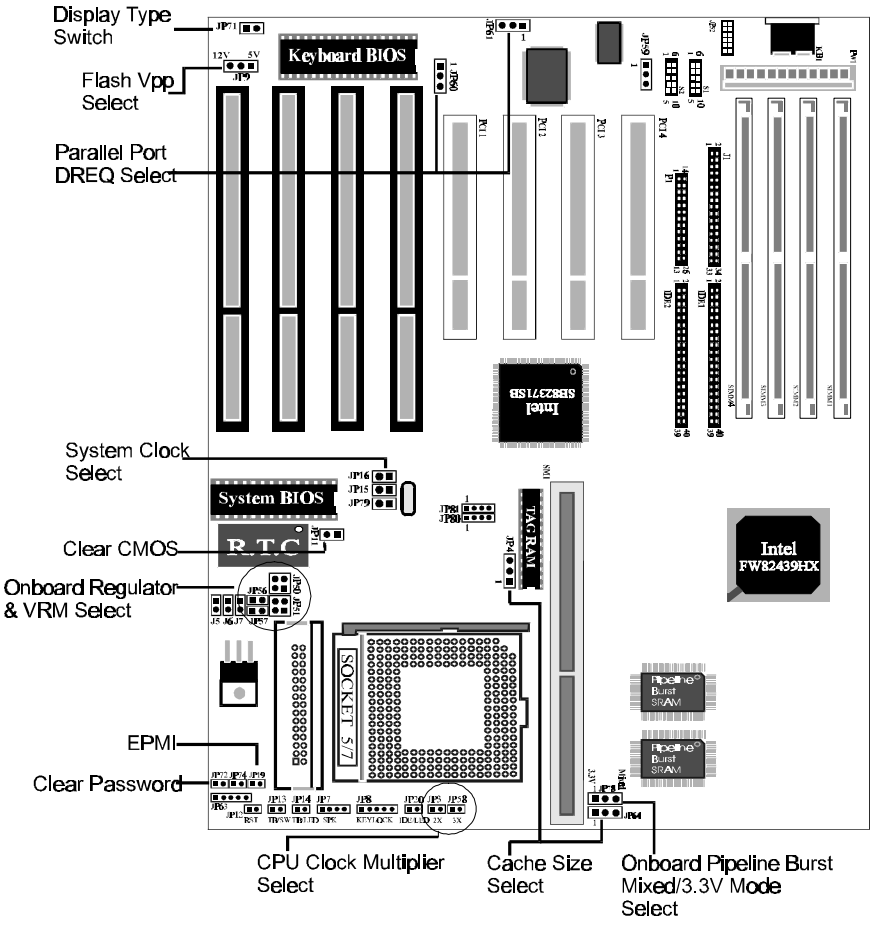
- ❑ 32-bit PCI bus slot x 4
- ❑ 16-bit ISA bus slot x 4
- ❑ 2-channel PCI IDE port
  - Support up to 4 IDE devices
  - PIO Mode 4 transfers up to 16 MB/sec
  - Integrated 8 x 32-bit buffer for PCI IDE burst transfers
- ❑ One floppy port
- ❑ One parallel port
  - Supports **SPP** (PS/2 compatible bidirectional Parallel Port), **EPP** (Extended Parallel Port), and **ECP** (Extended Capabilities Port) high performance parallel port.
- ❑ Two serial ports
  - Supports 16C550 compatible UARTS.
  - Supports serial InfraRed communication.
- ❑ One PS/2 mouse port
- ❑ USB (Universal Serial Bus) port

Board Design

- ❑ Dimension 22cm x 28cm

Chapter 2 Hardware Installation

Jumpers

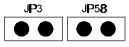
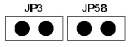


CPU Clock Speed Selection

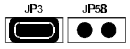
HOT-553 mainboard features a clock generator to provide adjustable system clock frequency. JP15, JP16 and JP79 are all 2-pin jumpers which determine the system clock frequency from 40MHz to 66MHz.

HOT-553 mainboard also provides JP3 and JP58 to figure up CPU core clock multiplier. By inserting or removing jumper caps on JP3 and JP58, the user can change the **Host Bus Clock** /**CPU Core Clock** ratio from 1 : 1.5 to 1 : 3.

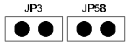
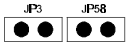
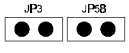
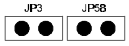
Intel Pentium

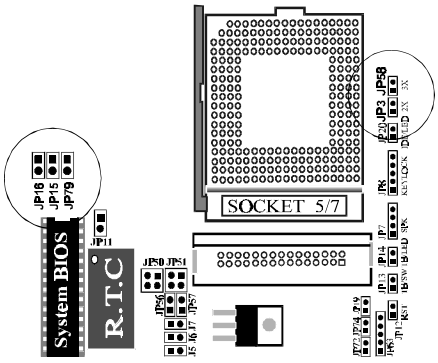
CPU Clock Speed	JP16, JP15, JP79	System Clock	JP3 & JP58	CPU Bus/Core Ratio
75 MHz Pentium Processor		50 MHz		1 : 1.5
90 MHz Pentium Processor		60 MHz		1 : 1.5
100 MHz Pentium Processor		66 MHz		1 : 1.5
120 MHz Pentium Processor		60 MHz		1 : 2
125 MHz Pentium Processor		50 MHz		1 : 2,5
133 MHz Pentium Processor		66 MHz		1 : 2
150 MHz Pentium Processor		60 MHz		1 : 2,5
150 MHz Pentium Processor		50 MHz		1 : 3
166 MHz Pentium Processor		66 MHz		1 : 2.5
180 MHz Pentium Processor		60 MHz		1 : 3
200 MHz Pentium Processor		66 MHz		1 : 3

Cyrix 6x86

CPU Clock Speed	JP16, JP15, JP79	System Clock	JP3, JP58	CPU Bus/Core Ratio
80 MHz Cyrix/IBM 6x86-P90+		40 MHz		1 : 2
100 MHz Cyrix/IBM 6x86-P120+		50 MHz		1 : 2
120 MHz Cyrix/IBM 6x86-P150+		60 MHz		1 : 2
133 MHz Cyrix/IBM 6x86-P166+		66 MHz		1 : 2

AMD 5k86

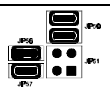
CPU Clock Speed	JP16, JP15, JP79	System Clock	JP3, JP58	CPU Bus/Core Ratio
75 MHz AMD K5 - PR75		50 MHz		1 : 1.5
90 MHz AMD K5 - PR90		60 MHz		1 : 1.5
100 MHz AMD K5 - PR100		66 MHz		1 : 1.5
90 MHz AMD K5 - PR120		60 MHz		1 : 1.5
100 MHz AMD K5 - PR133		66 MHz		1 : 1.5
105 MHz AMD K5 - PR150		60 MHz		1 : 1,75
116,7 MHz AMD K5 - PR166		66 MHz		1 : 1,75

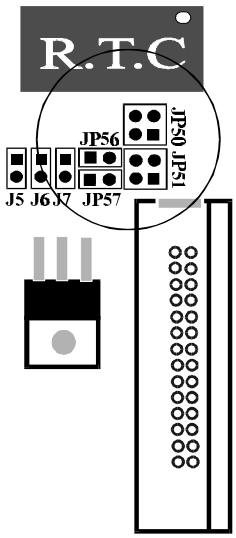


Onboard regulator & VRM Selection - JP50,51,56,57

HOT-553 mainboard is designed an onboard voltage regulator to provide single 3V ranger for pentium P54C, AMD K5, and Cyrix/IBM 6x86. Optional VRM (voltage regulator module) socket for adding VRM to provide 3.3/2.8V dual voltages for Pentium P55C and Cyrix/IBM 6x86L processors.

Normally, VRM supports both 3.3V and 2.8V output, but some particular VMRs only provide 2.8V and require onboard regulator to completement 3.3V.

Voltage Output	JP50, 51, 56, 57	Power Supply Path
Onboard Regulator (default)		3.3~3.6V ranger from onboard regulator
Add-on VRM		3.3V & 2.5V from add-on VRM
Onboard regulator and Add-on VRM		3.3V ranger from onboard regulator, 2.5V from add-on VRM

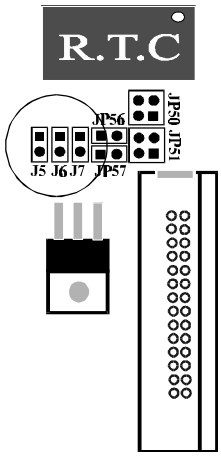


Onboard Voltage Regulator Output Selection - JP5, 6, 7

HOT-553 mainboard is designed to offer several CPU voltages level for Pentium processor, Cyrix/IBM 6x86, and AMD K5 family requirements.

Note: When using Cyrix/IBM 6x86 above P120+ or Cyrix/IBM 6x86L (all series) processor on HOT-553 mainboard, an add-on VRM is required.

Voltage Output	J5, J6, J7	Processors
3.3 V±5%		Pentium P54C STD/VR
3.45 V±5%		Pentium P54C VR/VRE
3.6 V±5%		Pentium P54C VRE Cyrix 6x86 AMD K5



Cache Type Selection

HOT-553 mainboard support onboard pipeline burst cache SRAM, and pipeline burst cache module.

Onboard pipeline burst cache RAM

A factory option on HOT-553 mainboard is an integrated 256KB external cache implemented with two 32K x 32 pipeline burst SRAM devices soldered to the mainboard. A 32KB x 8 external Tag SRAM is required.

Pipeline Burst cache module

If the HOT-553 is ordered with no cache installed, the cache can be added later in a field upgrade by installing a 256KB pipeline burst cache module into the CELP socket.

If factory option on HOT-553 mainboard integrate 256KB pipeline burst cache installed already, the cache size can be field upgrade to 512KB by installing a 256KB pipeline burst cache module into the CELP socket.

(please refer to section of " **Pipeline Burst Type Cache Size Selection** ")

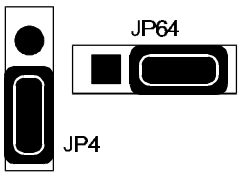
Pipeline Burst Type Cache Size Selection - JP4, JP64

HOT-553 mainboard supports 256KB or 512KB pipeline burst cache size.

If the HOT-553 is ordered with no cache installed, the cache can be field upgraded by installing a **first 256KB pipeline burst cache module** into the CELP socket.

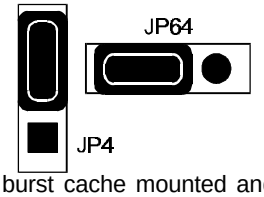
If factory option on HOT-553 mainboard integrate 256KB pipeline burst cache onboard mounted already, the cache size can be field upgraded to 512KB by installing a **secondary 256KB pipeline burst cache module** into the CELP socket.

256KB Cache Memory

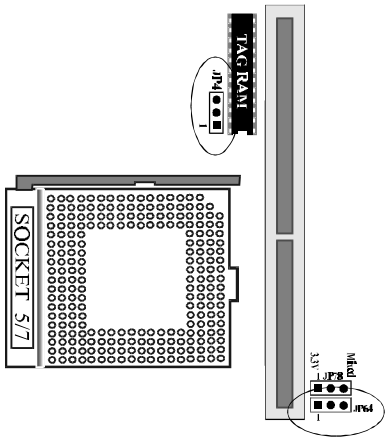


On mainboard integrate 256KB pipeline burst cache mounted, or a first 256KB pipeline burst cache module in the CELP socket.

512KB Cache Memory



On mainboard integrate 256KB pipeline burst cache mounted and a secondary 256KB pipeline burst cache module in the CELP socket.



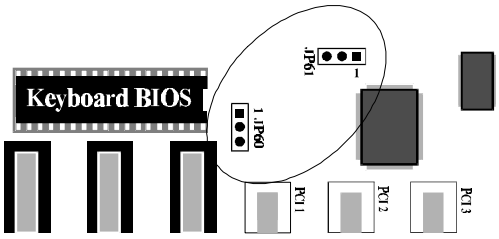
Note : *There are some technical difference between first 256KB pipeline burst cache module and secondary one, if 512KB cache memory are required, please contact your supplier for help .*

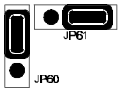
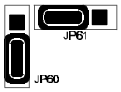
Parallel Port DREQ Selection - JP60, JP61

HOT-553 mainboard onboard parallel port supports ECP mode (Extended Capabilities Port), and provide two available DMA Request lines DREQ1 and DREQ3 for it.

When an ECP mode device is in use, the user may assign DREQ1 or DREQ3 for parallel port. If SPP/EPP mode is selected, the user may ignore those jumpers.

Jumper JP59 factory default on 



Parallel Port DMA Selection	JP60, JP61
Parallel Port ECP Mode DMA Request 1 (default)	
Parallel Port ECP Mode DMA Request 3	

Clear Password - JP72

Allows system password to be cleared by shorting jumper JP72 and turning the system on, "**Password is cleared by jumper, (JCP) !** " message will shown up on power-on screen. The system should then be turned off and the jumper JP72 should be returned to OPEN to restore normal operation. The procedure should only be done if the user password has been forgotten. (This function may not available when Cyrix 6x86 CPU is in use)

Flash EPROM Jumper - JP9

HOT-553 mainboard supports two types of flash EPROM, 5 volt and 12 volt. By setting up jumper JP9, you can update both types of flash EPROM with new system BIOS files as they come available.
JP9 open for 5V, Pin 2-3 close for 12V.

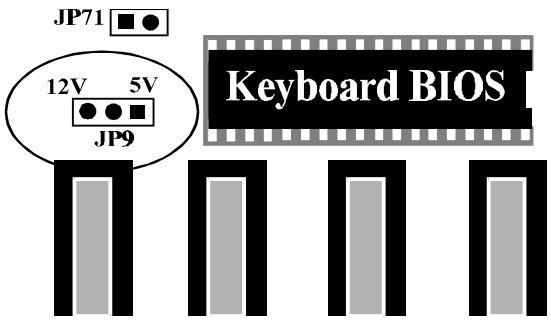
BIOS UPGRADES

Flash memory makes distributing BIOS upgrades easy. A new version of the BIOS can be installed from a diskette.

The flash upgrade utility, **Awdflash.exe** , has two notice for BIOS upgrades:

Flash utility can't work under protected/virtual mode. Memory manager like **QEMM.386** , **EMM386** should not be loaded. (or Simply bypass all **config.sys** and **autoexec.bat** on system boot up.

Flash utility supports both 5V and 12V Flash EEPROM.



Clear CMOS - JP11

HOT-553 mainboard supports jumper **JP11** for discharge mainboard's CMOS memory. The CMOS memory retains the system configuration information in the component of R.T.C.

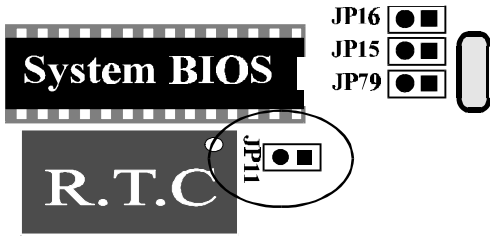
You should short this jumper for a moment when you wish to clear CMOS memory, and then make sure open this jumper for normal operation to retain your new CMOS data.

Note: Clear CMOS & R.T.C function available only when "DS12887A" or "DS12B887" are in use.

There are different ways to discharge CMOS memory between "DS12887A" and "DS12B887".

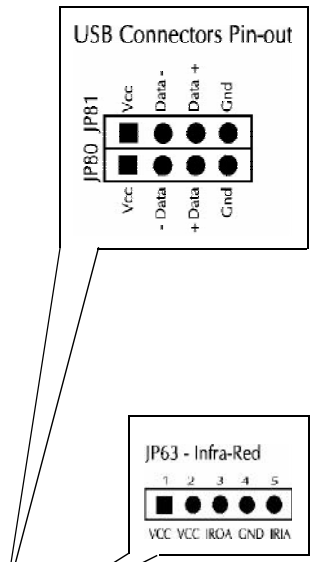
DS12887A - Turn off power, close jumper JP11 for 2 to 3 seconds then release and CMOS will be discharged.

DS12B887 - Close jumper JP11, turn on power durning 2 to 3 seconds then release JP11 and turn off power, CMOS will be discharged.



Connectors

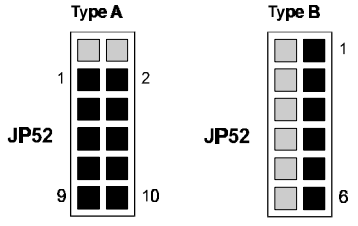
Connectors	
ITEM	FUNCTION
IDE1	On-board PCI Primary IDE Connector
IDE2	On-board PCI Secondary IDE Connector
J1	On-board Floppy Controller Connector
P1	On-board Parallel Port Connector
S1	On-board Serial port-1 Connector
S2	On-board Serial Port-2 Connector
JP52	On-board PS/2 Mouse Port Connector
JP8	Power LED and Keylock Connector
JP7	PC Speaker Connector
JP12	Hardware Reset Switch Connector
JP14	Turbo LED Connector
JP72	Clear BIOS Password
JP74	Green LED
JP19	EPMI Connector
JP20	On-board Enhanced IDE R/W LED Connector
JP80, JP81	Universal Serial Bus (USB) Connectors
JP63	IR Communication Port Connector
JP71	Display type (Color/Mono) Switcher



PS/2 Mouse Connector

HOT-553 mainboard provides two type of PS/2 style mouse connectors, type A and type B, the right table shows the pinout connection for each type.

PIN	TYPE A	TYPE B
1	Empty	Data
2	Ground	Empty
3	Clock	Ground
4	Ground	VCC
5	VCC	Clock
6	Empty	Empty
7	Empty	
8	Empty	
9	Data	
10	Empty	



Chapter 3 Memory Configuration

HOT-553 mainboard support great flexibility of different on-board fast page mode and EDO mode memory up to 256MB.

On-board four SIMM sockets are organized into two banks, with two SIMM sockets assigned to one memory bank. HOT-553 mainboard supports 4MB, 8MB, 16MB, 32MB and 64MB single-side or double-side 72-pin SIMMs.

The table on next page shows the possible memory combinations of HOT-553 mainboard.

Notes: *Fast page mode SIMM and EDO SIMM can not mixed within the same memory bank.*

HOT-553 Memory Configuration Reference Table		
SIMM 1, 2	SIMM 3, 4	TOTAL
4 MB	Empty	8 MB
8 MB	Empty	16 MB
16 MB	Empty	32 MB
32 MB	Empty	64 MB
64 MB	Empty	128 MB
Empty	4 MB	8 MB
Empty	8 MB	16 MB
Empty	16 MB	32 MB
Empty	32 MB	64 MB
Empty	64MB	128 MB
4 MB	4 MB	16 MB
4 MB	8 MB	24 MB
4 MB	16 MB	40 MB
4 MB	32 MB	72 MB
4 MB	64 MB	136 MB
8 MB	4 MB	24 MB
8 MB	8 MB	32 MB
8 MB	16 MB	48 MB
8 MB	32 MB	80 MB
8 MB	64 MB	144 MB
16 MB	4 MB	40 MB
16 MB	8 MB	48 MB
16 MB	16 MB	64 MB
16 MB	32 MB	96 MB
16 MB	64 MB	160 MB
32 MB	4 MB	72 MB
32 MB	8 MB	80 MB
32 MB	16 MB	96 MB
32 MB	32 MB	128 MB
32 MB	64 MB	192 MB
64 MB	64 MB	256 MB

Chapter 4 Award BIOS Setup

HOT-553's BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed RAM so that it retains the Setup information when the power is turned off.

Entering Setup

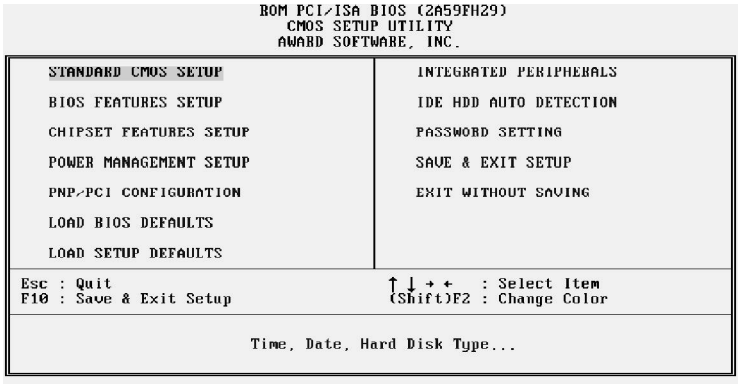
Power on the computer and press <Del> immediately will allow you to enter Setup. The other way to enter Setup is to power on the computer, when the below message appear briefly at the bottom of the screen during the POST (Power On Self Test), press <Del> key or simultaneously press <Ctrl>,<Alt>, and <Esc> keys.

TO ENTER SETUP BEFORE BOOT PRESS CTRL-ALT-ESC OR DEL KEY

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF the ON or pressing the "RESET" button on the system case. You may also restart by simultaneously press <Ctrl>,<Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to,

PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP

The Main Menu



Standard CMOS setup

This setup page includes all the items in a standard compatible BIOS.

BIOS features setup

This setup page includes all the items of Award special enhanced features.

Chipset features setup

This setup page includes all the items of chipset features.

Power Management Setup

This setup page includes all the items of Power Management features.

PCI Configuration setup

This category specifies the value (in units of PCI bus blocks) of the latency timer for this PCI bus master and the IRQ level for PCI device. Power-on with BIOS defaults

Load BIOS Defaults

BIOS defaults loads the values required by the system for the maximum performance. However, you may change the parameter through the Option Setup Menu.

Load Setup Defaults

Setup defaults loads the values required by the system for the minimum performance. However, you may change the parameter through the Setup Menu.

IDE HDD auto detection

Automatically configure IDE hard disk drive parameters.

Password setting

Change, set, or disable password. It allows you to limit access to the system and Setup, or just to Setup.

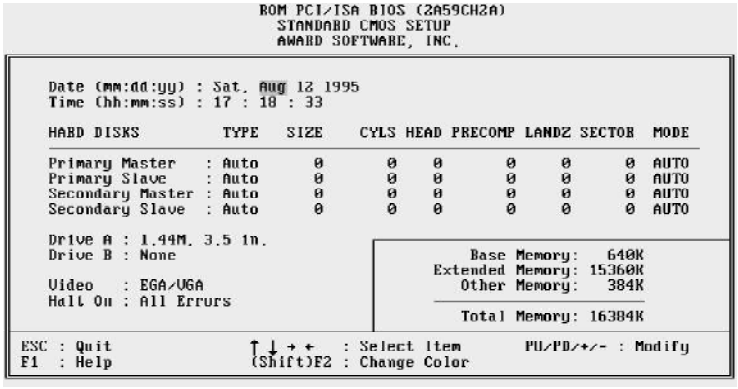
Save & Exit setup

Save CMOS value change to CMOS and exit setup

Exit without saving

Abandon all CMOS value changes and exit setup.

Standard CMOS Setup



Date

The date format is <day>, <date> <month> <year>. Press <F3> to show the calendar.

Time

The time format is <hour> <minute> <second>. The time is calculated base on the 24-hour military-time clock. For example. 5 p.m. is 17:00:00.

Daylight saving

The category adds one hour to the clock when daylight-saving time begins. It also subtracts one hour when standard time begins.

Drive C type/Drive D type

The category identify the types of hard disk drive C or drive D that has been installed in the computer. There are 46 predefined types and a user definable type. Type 1 to Type 46 are predefined. Type User is user-definable.

Press PgUp or PgDn to select a numbered hard disk type or type the number and press <Enter>. Note that the specifications of your drive must match with the drive table. The hard disk will not work properly if you enter improper information for this category. If your hard disk drive type is not matched or listed, you can use Type User to define your own drive type manually.

If you select Type User, related information is asked to be entered to the following items. Enter the information directly from the keyboard and press <Enter>. Those information should be provided in the documentation from your hard disk vendor or the system manufacturer.

If a hard disk drive has not been installed select NONE and press <Enter>.

Drive A type/Drive B type

The category identify the types of floppy disk drive A or drive B that has been installed in the computer.

Video

The category selects the type of adapter used for the primary system monitor that must matches your video display card and monitor. Although secondary monitors are supported, you do not have to select the type in Setup.

Error halt

The category determines whether the computer will stop off an error is detected during power up.

Memory

The category is display-only which is determined by POST (Power On Self Test) of the BIOS.

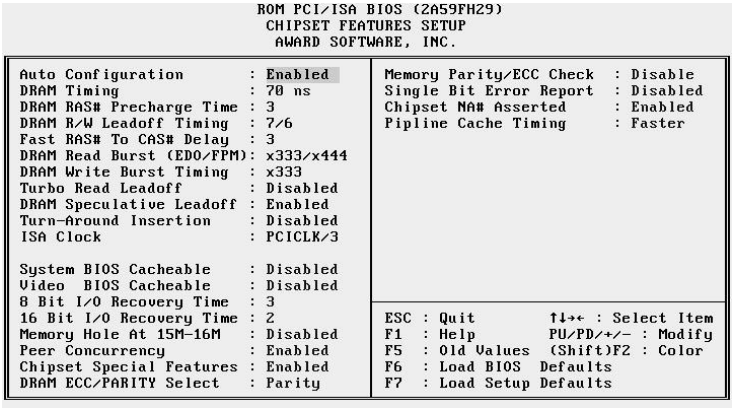
Base Memory

The POST of the BIOS will determine the amount of base (or conventional) memory installed in the system. The value of the base memory is typically 512K for systems with 512K memory installed on the mainboard, or 640K for systems with 640K or more memory installed on the mainboard.

Extended Memory

The BIOS determines how much extended memory is present during the POST. This is the amount of memory located above 1MB in the CPU's memory address map.

BIOS Features Setup



CPU Internal Cache

This category enables CPU internal cache to speed up memory access.

External Cache

This category enables external cache to speed up memory access.

Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power on the computer. If it is set to Enabled, BIOS will shorten or skip some check items during POST.

Boot Sequence

This category determines which drive computer searches first for the disk operating system. Default value is A, C.

Swap Floppy Drive

When this category enables, the BIOS will swap floppy drive assignments so that Drive A: will function as Drive B: and Drive B: as Drive A:.

Boot Up Floppy Seek

During POST, BIOS will determine if the floppy disk drive installed is 40 or 80 tracks.

Boot Up NumLock Status

When this option enables, BIOS turns on ***Num Lock*** when system is powered on so the end user can use the arrow keys on both the numeric keypad and the keyboard.

Boot Up System Speed

This option sets the speed of the CPU at system boot time. The settings are ***High*** or ***Low***.

Gate A20 Option

When this category sets to Normal, the A20 signal is controlled by keyboard controller. When this category sets to Fast, the A20 signal is controlled by post 92 or chipset specific method.

Security Option

This category allows you to limit access to the system and Setup, or just to Setup.
When ***System*** is selected, the system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
When ***Setup*** is selected, the system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

PS/2 Mouse Control Function

This category to set the PS/2 mouse be used or not. If there a PS/2 mouse attached to your system, this category must be enabled, if not, please disabled this category to release IRQ12 for PCI device.

PCI VGA Palette Snoop

This category must be set to enabled if there is any ISA VGA adapter card installed in the system, and disabled if there is any PCI VGA adapter card installed in the system.

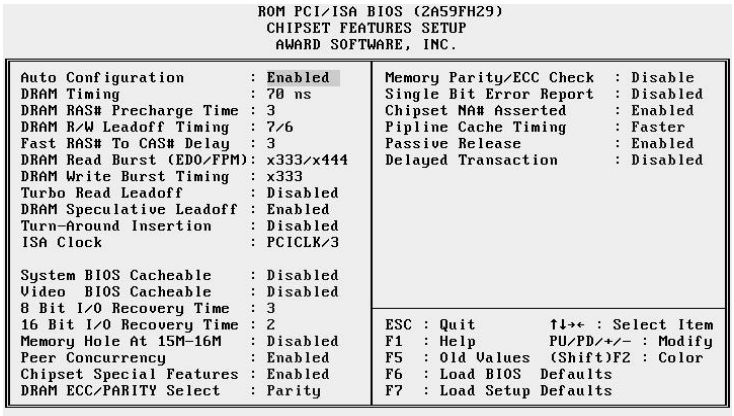
OS Select For DRAM > 64MB

If there over 64MB memory on your system, please set this category to **OS2** for total memory detection under OS/2 operating system, otherwise set to **Non-OS2** .

Video BIOS Shadow/XXXXX-XXXXX Shadow

These categories determine whether Video BIOS or optional ROM will be copied to RAM.

Chipset Features Setup



Auto Configuration

Pre-defined values for DRAM, cache. . . timing acccording to CPU type & system clock. The choice : Enabled and Disabled.

When this item is enabled, the pre-defined items will become show-only.

DRAM Timing

The DRAM timing is controlled by the DRAM Timing Registers. The timings programmed into this register are dependent on the system design. Slower rates may be required in certain system designs to support loose layouts or slower memory.

DRAM RAS# Precharge Time

This option allows you to determine the number of CPU clocks allocated for the Row Address Strobe to accumulate its charge before the DRAM is refreshed.

DRAM R/W Leadoff Timing

This sets the number of CPU clocks allowed before reads and writes to DRAM are performed.

Fast RAS To CAS Delay

When DRAM is refreshed, both rows and columns are addressed separately. This setup item allows you to determine the timing of the transition from RAS to CAS.

DRAM Read Burst Timing

This category set the DRAM Read Burst Timing. The timing used depends on the type of DRAM (standard page mode or EDO burst mode) on a per-bank basis. The options are ***x4444***, ***x3333***, and ***x2222***.

DRAM Write Burst Timing

This category set the DRAM Write Burst Timing. The timing used depends on the type of DRAM (standard page mode or EDO burst mode) on a per-bank basis. The options are ***x4444***, ***x3333***, and ***x2222***.

Turbo Read Leadoff

This category is used to defined Turbo Read Leadoff is " ***Enable***" or "***Disable***" setting.

DRAM Speculative Leadoff

The 430HX is capable of allowing a DRAM read request to be generated slightly before the address has been fully decoded. This can reduce all read latencies.

Turn-Around Insertion

When this is enabled, the chipset will insert one extra clock to the turn-around of back-to-back DRAM cycle.

ISA Clock

This item allows you to select the PCI clock type.

System/Video BIOS Cacheable

This category allows the user to set whether the system BIOS F000~FFFF and video BIOS C000~C7FF areas are cacheable or non-cacheable.

8 /16 Bit I/O Recovery Time

The recovery time is the length of time, measured in CPU clocks, which the system will delay after the completion of an input/output request.

Memory Hole At 15M-16M

In order to improve performance, certain space in memory can be reserved for ISA cards. This memory must be mapped into the memory space below 16 MB.

Peer Concurrency

Peer concurrency means that more than one PCI device can be active at a time.

Chipset Special Features

When disabled, the chipset behaves as if it were the earlier.

DRAM ECC/PARITY Select

This item allows you to select between two methods of DRAM error checking, ECC and Parity.

Memory Parity/ECC Check

This item allows you to select between three methods of memory error checking, Auto, Enabled and Disabled.

Single Bit Error Report

When a single bit error is detected, the offending DRAM row ID lateched. The lateched valued is held until software explicity clears the error status flag.

Chipset NA# Asserted

This item allows you to select between two method of chipset NA# asserted during CPU write cycles /CPU line fills, Enabled and Disabled.

Pipeline Cache Timing

This item allows you to select two timing of pipeline cache, Faster and Fastest.

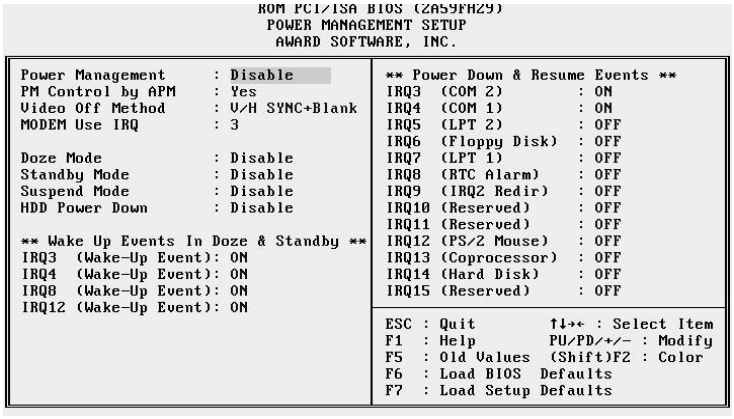
Passive Release

When enabled, the chipset provides a programmable passive release mechanism to meet the required ISA master latencies.

Delayed Transaction

Since the 2.1 revision of the PCI specification requires much tighter controls on target and master latency. PCI cycles to or from ISA typically take longer. When enabled, the chipset provides a programmable delayed completion mechanism to meet the required target latencies.

Power Management Setup



Power Management

This category determines the options of the power management function. Default value is Disable. The following pages tell you the options of each item & describe the meanings of each options.

Disabled	Global Power Management will be disabled.
User Define	Users can configure their own power management.
Min Saving	Predefined timer values are used such that all timers are in their maximum value.
Max Saving	Predefined timer values are used such that all timers minimum value.

PM Control by APM

If this category set to No, system BIOS will ignore APM when power is managing the system.
If this category setup to Yes, system BIOS will wait for APM's prompt before it enter any PM mode e.g. ***DOZE***, ***STANDBY*** or ***SUSPEND***.

Video Off Method

Blank Screen	The system BIOS will only blanks off the screen when disabling video.
V/H SYN +Blank	In addition to Blank Screen, BIOS will also turn off the V-SYNC & H-SYNC signals from VGA cards to monitor.

DPMS This function is enabled for only the VGA card supporting DPM.

Doze Mode

1 Min~1 Hr Defines the continuous idle time before the system entering DOZE mode.

Disable System will never enter DOZE mode.

Standby Mode

1 Min~1 Hr Defines the continues idle time before the system entering STANDBY mode.

Disable System will never enter STANDBY mode.

Suspend Mode

1 Min~1 Hr Defines the continuous idle time before the system entering SUSPEND mode.

Disable System will never enter SUSPEND mode.

HDD Power Down

1~15Min Defines the continuous HDD idle time before the HDD entering power saving mode (motor off).

Suspend BIOS will turn the HDD's motor off when system is in SUSPEND mode.

Disable HDD's motor will not off.

IRQ3, 5, 8, 12 **Wake-Up Events In Doze & Standby**

If this category sets to Off, the IRQ3, 5, 8 or 12 event's activity will not reactivates the system from Doze and Standby mode.

If this category sets to On, the IRQ3, 5, 8 or 12 event's activity will reactivate system from Doze and Standby mode.

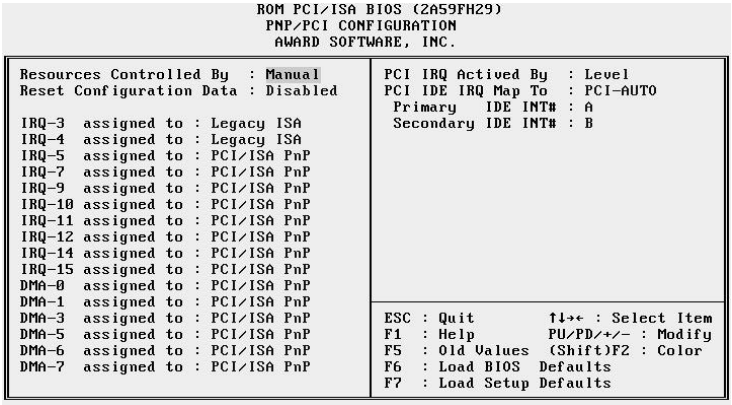
Power Down & Resume Events *

If these categories sets to Off, the event's activity will not be monitored to enter power management.

If this category sets to On, the event's activity will be monitored to enter power management.

COM Post Accessed	LPT Ports Accessed	Drive Ports Accessed	IRQ 3 (COM 2)
IRQ 4 (COM1)	IRQ 5 (LPT 2)	IRQ 6 (Floppy Disk)	IRQ 7 (LPT 1)
IRQ 8 (RTC Alarm)	IRQ 9 (IRQ 2 Redir)	IRQ 10 (Reserved)	IRQ 11 (Reserved)
IRQ 12 (PS/2 Mouse)	IRQ 13(Copro-)	IRQ 14 (Hard Disk)	IRQ 15 (Reserved)

PCI Configuration Setup



Resources Controlled By

The options in these categories are Auto, Manual.

Auto : BIOS will auto configurate system IRQs and DMAs resources.

Manual : System IRQs and DMAs are adjusted by the user.

IRQ 3 assigned to

The system BIOS will assign IRQ 3 to **legacy ISA** or **PCI/ISA PnP** .

IRQ3 default assign to legacy ISA for COM2.

IRQ 4 assigned to

The system BIOS will assign IRQ 4 to **legacy ISA** or **PCI/ISA PnP** .

IRQ4 default assign to legacy ISA for COM1.

IRQ 5 assigned to

The system BIOS will assign IRQ 5 to **legacy ISA** or **PCI/ISA PnP** .

IRQ5 default assign to PCI/ISA PnP for PCI or ISA PnP devices.

IRQ 7 assigned to

The system BIOS will assign IRQ 7 to **legacy ISA** or **PCI/ISA PnP** .

IRQ7 default assign to legacy ISA for LPT1.

IRQ 9 assigned to

The system BIOS will assign IRQ 9 to **legacy ISA** or **PCI/ISA PnP** .

IRQ9 default assign to PCI/ISA PnP for PCI or ISA PnP devices.

IRQ 10 assigned to

The system BIOS will assign IRQ 10 to **legacy ISA** or **PCI/ISA PnP** .

IRQ10 default assign to PCI/ISA PnP for PCI or ISA PnP devices.

IRQ 11 assigned to

The system BIOS will assign IRQ 11 to **legacy ISA** or **PCI/ISA PnP** .

IRQ11 default assign to PCI/ISA PnP for PCI or ISA PnP devices.

IRQ 12 assigned to

The system BIOS will assign IRQ 12 to **legacy ISA** or **PCI/ISA PnP** .

IRQ12 default assign to PCI/ISA PnP for PCI or ISA PnP devices. Since PS/2 mouse uses the same IRQ, if there are a PS/2 mouse on your system, assign IRQ12 to legacy ISA to avoid system conflict.

IRQ 14 assigned to

The system BIOS will assign IRQ 14 to **legacy ISA** or **PCI/ISA PnP** .

IRQ14 default assign to legacy ISA for primary IDE controller.

IRQ 15 assigned to

The system BIOS will assign IRQ 15 to **legacy ISA** or **PCI/ISA PnP** .

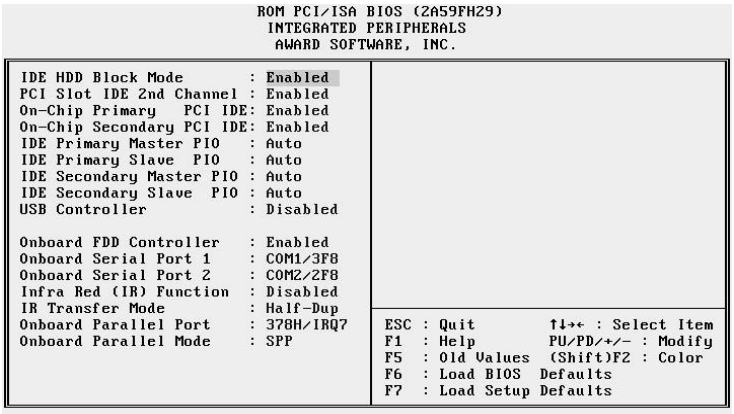
IRQ15 default assign to legacy ISA for secondary IDE controller.

DMA-0, 1, 3, 5, 6, 7 assigned to

The system BIOS will assign DMAs to **legacy ISA** or **PCI/ISA PnP** .

DMA 0, 1, 3, 5, 6 and 7 channel default assign to PCI/ISA PnP.

Peripheral Setup



IDE HDD Block Mode

This category is used to set IDE HDD Block Mode. If your IDE Hard Disk supports block mode, then you can enable this function to speed up the HDD access time. If not, please disable this function to avoid HDD access error.

PCI Slot IDE 2nd channel

This category is used to defined add-on PCI IDE secondary controller is "***Enable***" or "***Disable***" setting.

On-Chip Primary PCI IDE

This category is used to defined on chip Primary PCI IDE controller is "***Enable***" or "***Disable***" setting.

On-Chip Secondary PCI IDE

This category is used to defined on chip Secondary PCI IDE controller is "***Enable***" or "***Disable***" setting.

IDE Primary/Secondary Master PIO

In this category, there are five modes defined in manual mode and one automatic mode. There are ***0***, ***1***, ***2***, ***3***, ***4***, and ***AUTO***. The default settings for on board Primary/Secondary Master PIO timing is Auto.

IDE Primary/Secondary Slave PIO

In this category, there are five modes defined in manual mode and one automatic mode. There are ***0***, ***1***, ***2***, ***3***, ***4***, and ***AUTO***. The default settings for on board Primary/Secondary Slave PIO timing is Auto.

Onboard FDC Control

This category specifies onboard floppy disk drive controller. This setting allows you to connect your floppy disk drives to the onboard floppy connector. Choose the "Disabled" settings if you have a separate control card.

Onboard Serial Port 1/Port 2

This category is used to define onboard serial port 1/Port2 to ***COM1/ 3F8H***, ***COM2/2F8H***, ***COM3/3E8H***, ***COM4/2E8H*** or ***Disabled***.

Infra Red (IR) Function

HOT-553 main board support IrDA(HPSIR) and Amplitudes Shift Keyed IR(ASKIR) infrared through COM 2 port. This category specifies onboard Infra Red mode to ***HPSIR***, ***ASKIR*** or ***Disabled***.

IR Transfer Mode

This category specifies onboard infrared transfer mode to ***full-duplicate*** or ***half-duplicate***.

Onboard Parallel Port

This category specifies onboard parallel port address to ***378H***, ***278H***, ***3BCH*** or ***Disabled***.

Onboard Printer Mode

This category specifies onboard parallel port mode. The options are ***EPP***(Extended Parallel Port), ***ECP*** (Extended Capabilities Port), Extended, and Compatible.(Extended Capabilities Port), Extended, and Compatible.

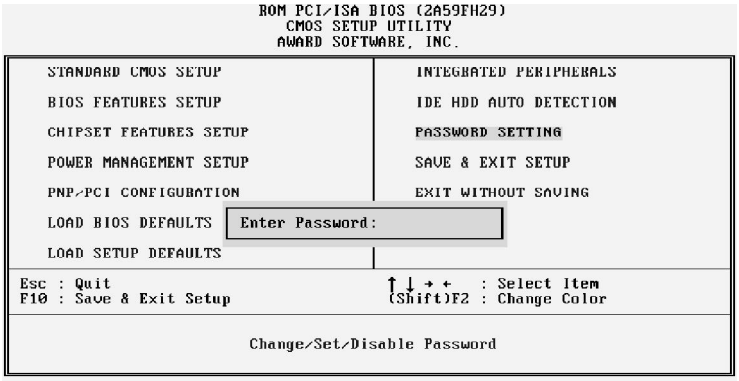
ECP Mode Use DMA

This category specifies DMA (Direct Memory Access) channel when ECP device is in use. The options are DMA ***1*** and DMA ***3.***

Password Setting

When you select this function, the following message will appear at the center of the screen to assist you in creating a password.

ENTER PASSWORD



Type the password, up to eight characters, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password.

To disable password, just press <Enter> when you are prompted to enter password. A message will confirm the password being disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED

If you select System at Security Option of BIOS Features Setup Menu, you will be prompted for the password every time the system is rebooted or any time you try to enter Setup. If you select Setup at Security Option of BIOS Features Setup Menu, you will be prompted only when you try to enter Setup.

Warning : ***Retain a safe record of your password. If you've forgotten or loosed the password, the only way to access the system is to clear CMOS memory, please refer to*** **"Clear CMOS"** ***or*** **"Clear Password** ***" section on chapter 2.***