AR-B5500VG
Intel® Pentium® IV LGA775 PROCESSOR
Networking Board
User's Guide

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Book Number: AR-B5500VG-08.0325

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0. PREFACE

0.1 COPYRIGHT NOTICE AND DISCLAIMER

0.2 WELCOME TO THE AR-B5500VG NETWORKING BOARD

This guide introduces the Acrosser AR-B5500VG networking board.

Use information provided in this manual describes this board's functions and features. It also helps you start, set up and operate your AR-B5500VG. General system information can also be found in this publication.

Please refer to the chapter introduction if you have not already installed this board. Check the packing list before you install and make sure the accessories are completely included.

0.3 BEFORE YOU USE THIS GUIDE

Please refer to the Chapter 1, "Introduction" in this guide, if you have not already installed this AR-B5500VG. Check the packing list before you install and make sure the accessories are completely included.

AR-B5500VG CD provides the newest information regarding the board. Please refer to the files of the enclosed utility CD. It contains the modification and hardware & software information, and adding the description or modification of product function after manual printed.

0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires any services, contact the distributor or sales representative from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original shipping container for this purpose.

You can help assure efficient servicing for your product by following these guidelines:
1. Include your name, address, daytime telephone, facsimile number and E-mail.
2. A description of the system configuration and/or software at the time of malfunction.
3. A brief description of the problem occurred.

0.5 TECHNICAL SUPPORT AND USER COMMENTS

Users comments are always welcome as they assist us in improving the quality of our products and the readability of our publications. They create a very important part of the input used for product enhancement and revision.
We may use and distribute any of the information you provide in any way appropriate without incurring any obligation. You may, of course, continue to use the information you provide.

If you have any suggestions for improving particular sections or if you find any errors on it, please send your comments to Acrosser Technology Co., Ltd. or your local sales representative and indicate the manual title and book number.
Acrosser Worldwide: **http://www.acrosser.com/Contact/gc.asp**
Acrosser Distributors: **http://www.acrosser.com/contact/gd.asp**

0.6 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions. Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always best to safeguard against accidents that may result in expensive repairs. The following measures should be sufficient to protect your equipment from static discharge.

Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
When unpacking and handling the board or other system components, place all materials on an anti-static surface.
Be careful not to touch the components on the board, especially the "golden finger" connectors on the bottom of the board.

1. INTRODUCTION

Welcome to the AR-B5500VG networking board computer. AR-B5500VG provides a flexible system that allows user to choose the performance of system as their wish. It has an LGA775 socket for Intel Pentium IV processors in the 775-Land LGA package, and equipped with Intel 945G express chipset: 82945G plus 82801GR.

This product is designed for the system manufacturers, integrators, or VARs that want to provide all the performance, reliability, and quality at a reasonable price.

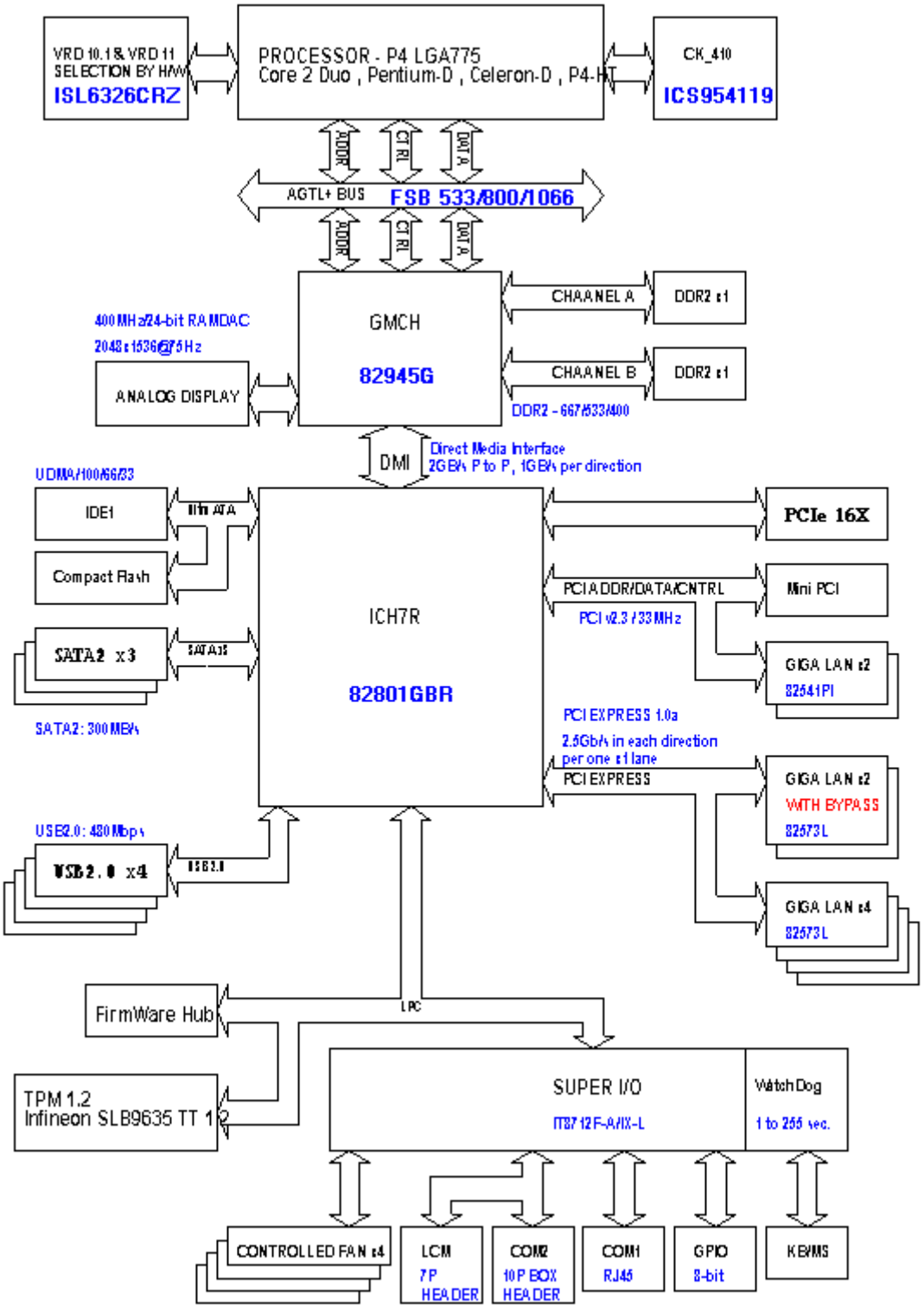
AR-B5500VG provides two 240-pin DIMM sockets to support DDR Ⅱ 667/533/400 (PC5300/PC4200/PC3200) non-ECC DIMM up to 2 GBs physical memories. The memory interface supports up to 10.7 GB/s of bandwidth and 4GB memory addressability for faster system responsiveness and support for 64-bit computing.

AR-B5500VG also provides on-board VGA (82945G integrated), six / eight LANs that support 1000BASE-T, (two ports support BYPASS), four USB 2.0 ports with resettable fuses protection, two RS232 ports, three SATA2 ports, 8-bit bidirectional GPIOs, WATCHDOG, PCIe X16, Mini PCI, and Trusted Platform Module.

The most eyes popping characteristic of AR-B5500VG is its eight Giga-LAN ports. They were constructed by six PCI express gigabit Ethernet controllers – Intel 82573L, and two PCI gigabit Ethernet controllers – Intel 82541PI. They provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab, respectively).

Based on all of the features above, AR-B5500VG is an ideal solution for consumers that are looking for high networking performance with flexible option for further upgrade at a reasonable price.

1.1 SYSTEM BLOCK DIAGRAM



1.2 SPECIFICATIONS

- **CPU:** a LGA775 socket for Intel Pentium IV processors in the 775-Land LGA package.
- **DMA channels:** 7.
- **Interrupt levels:** 16 (24 APIC interrupts).
- **Chipset:** Intel 945G express chipset 82945G + 82801GR + IT8712-A/IX-L.
- **Memory:** provides two 240-pin DIMM sockets to support DDR Ⅱ 667/533/400 non-ECC DIMM. The memory capability can up to 2GB.
- **VGA Controller:** 82945G integrated.
- **Analog Display Interface:** 10-pin box header, and resolution up to 2048x1536@75Hz.
- **Serial ATA Interface:** supports three SATA devices, and data transfer rates up to 300MB/s per device.
- **Ultra ATA100/66/33 IDE Interface:** one IDE controller that supports two devices. A specified cable (80-conductor ribbon cable) must be available for ATA100/66.
- **Compact flash interface:** supports TYPE-I compact flash card with UDMA supported.
- **USB2.0 interface:** one stacked USB connector and one 10-pin pin header to support four USB2.0 compatible devices. All resettable fuses protected.
- **Ethernet interface:** on-board six PCI express gigabit Ethernet controllers and two PCI gigabit Ethernet controllers to support eight LAN ports. They provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab, respectively).
- **BYPASS function:** supports by ports LAN1 and LAN2 and software programmable.
- **PCIE X16 interface:** One PCI Express x16 slot.
- **Mini PCI interface:** a 3.3V / 33MHz / 32-bit TYPE-III mini PCI slot supported.
- **TPM:** on-board Trusted Platform Module supported by Infineon SLB 9635 TT 1.2.
- **Serial ports (RS232):** Two high-speed 16550 compatible UARTs ports with 16-byte send/receive FIFOs.
  COM1: RJ45 connector.
  COM2: on-board 10-pin box header.
- **LCM interface:** a 7-pin pin header could be used to LCM for chassis' control panel.
- **General Purpose Input/Output:** 8-bit, 5V TTL level, bidirectional, and software programmable GPIOs.
- **Keyboard & Mouse interface:** one JST 6-pin connector supports PS/2 keyboard and mouse.
- **WATCHDOG:** software programmable 1~255 second(s) / minute(s).
- **Power Consumption:** **+12V [8.3A], +5V [1.4A], +3.3V [5.7A], -12V [0.6A], +5Vsb [2.0A] typically.**
  Test equipments list as below:
  Main board: AR-B5500VG.
  Processor: Intel Pentium IV 531 3.0GHz / FSB800 / 1MB L2 cache / 90nm.
  Memory: one Kingston KVR667D2N5/1G/DDR2.
  One 3.5" HDD
  OS: Windows XP SP2.
  Eight LAN ports linked at 1000Base-T mode.
  Processor was running at 100% loading.

  Note: A proper power supply unit choice means that we should consider at least about
  a.) Protection of overload, short-circuit, and other safeties.
  b.) Summation of all devices' power requirements.
  c.) Thermal de-rating.
- **Operating Temperature:** 0℃ ~ 60℃

1.3 PACKING LIST

In addition to this User's Manual, the AR-B5500VG package includes the following items:

- A quick setup manual.
- One AR-B5500VG networking board.
- One Software utility CD.
- One adaptable cable for COM1.
- One D-SUB-15 adaptable cable for VGA.
- One D-SUB-9 adaptable cable for COM2.
- One Keyboard/Mouse adaptable cable.
- One SATA cable.
- One USB adaptable cable. (Optional) (ACROSSER's P/N.**190030531-G**)

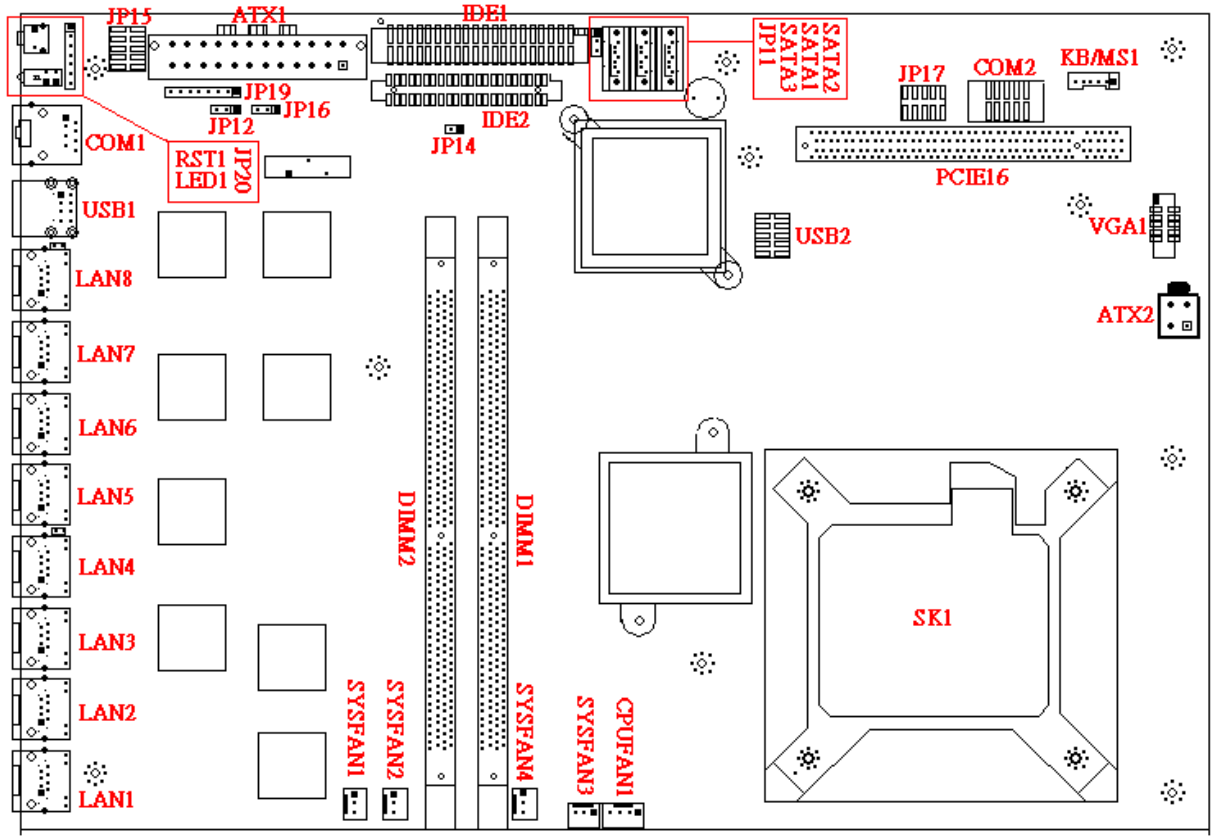
1.4 HISTORY

Date	Discription
2008/03/25	Initial release.

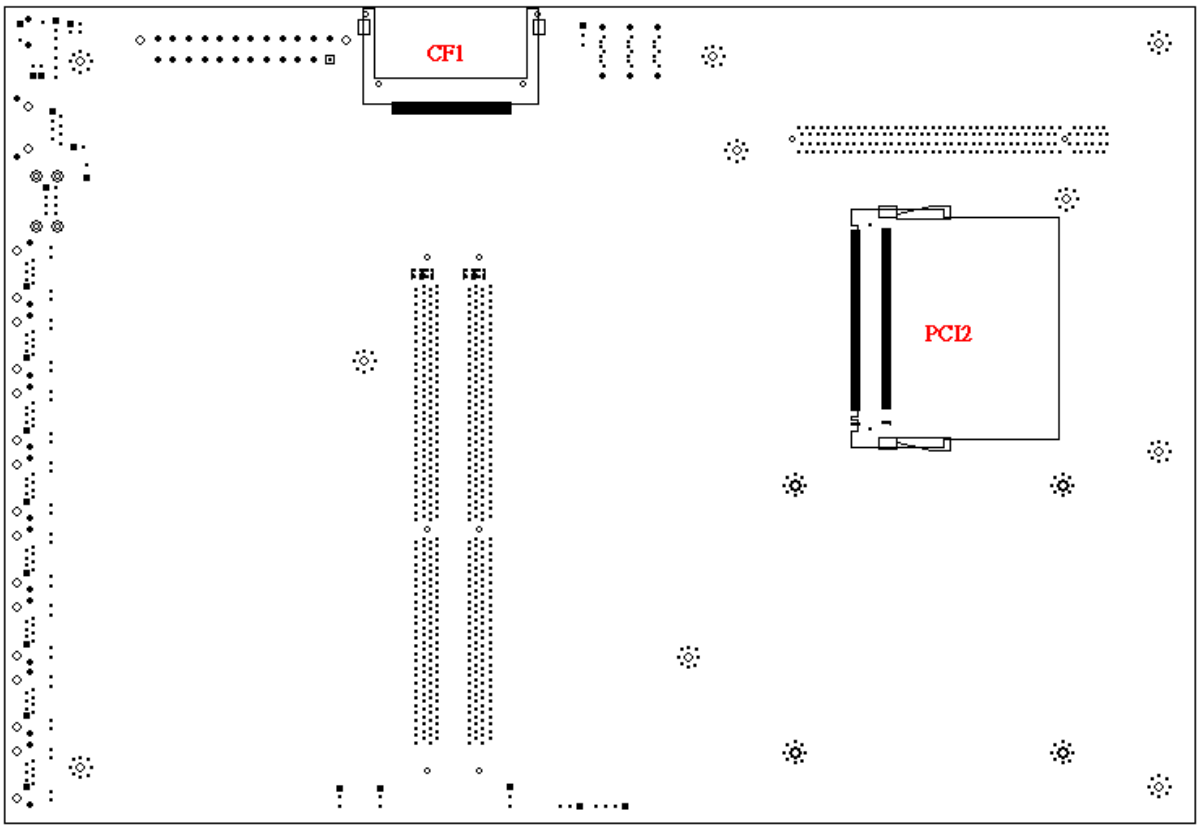
2. INSTALLATION AND CONNECTION

This chapter describes how to install the AR-B5500VG. At first, the layout of AR-B5500VG is shown, and the unpacking information that you should be careful is described. The following lists the jumpers and switches setting for the AR-B5500VG's configuration.

2.1 AR-B5500VG'S LAYOUT



Topside



Bottom side

2.2 JUMPERS AND CONNECTORS LIST

SK1	Socket for Intel LGA775 Processor.
DIMM1 **DIMM2**	Socket for DDR Ⅱ 667/533/400 non-ECC DIMM. Socket for DDR Ⅱ 667/533/400 non-ECC DIMM.
CPUFAN1	Fan connector for processor heat sink module.
SYSFAN1 **SYSFAN2** **SYSFAN3** **SYSFAN4**	Fan connectors for system fan modules.
ATX1	20-pin / 24-pin ATX power input for system.
ATX2	4-pin ATX power input (+12V only) for processor.
JP11	CMOS data keeping or resetting selection.
SATA1 **SATA2** **SATA3**	Serial ATA (SATA) device's connector.
IDE1	Parallel ATA (PATA) device's connector.
CF1	Socket for compact Flash card.
JP14	Compact Flash card master / slave selection.
JP15	Panel connection.
VGA1	Analog display signals' adaptable cable connection.
KB/MS1	PS/2 Keyboard and mouse adaptable cable connection.
JP17	General Purpose Input and Output (GPIO) connection.
COM1	RS232 port1 connection.
COM2	RS232 port2 connection.
JP20	RS232 port2 expanded usage connection.
USB1	USB2.0 port0 & port1 connection.
USB2	USB2.0 port2 & port3 adaptable cable connection.
LAN1~8	1000BASE-T, 100BASE-TX, and 10BASE-T Ethernet ports for twisted pair cable connection.
JP12	LAN1 and LAN2 BYPASS control selection.
PCIE16	PCIE 16x card connection.
PCI2	3.3V / 33MHz / 32-bit TYPE-III mini PCI card connection.
RST1	On-board reset button.
LED1	Dual LEDs for H.D.D. status and power-on indication.
IDE2	Optional. Parallel ATA (PATA) device's connector.
JP16 **JP19**	Reserved jumper.

2.3 [SK1] - SOCKET FOR INTEL LGA775 PROCESSOR.

Before inserting the processor into socket, you may read the processor integration guide which inside the processor packing box or refer to the Intel website http://www.intel.com/cd/channel/reseller/asmo-na/eng/99345.htm#integrating as priority.

Processor supported list:

E6400 (2.13GHz / FSB1066 / 2MB shared L2 cache / 65nm / dual-core)
651 (3.4GHz / FSB800 / 2MB L2 cache / 65nm)
531 (3.0GHz / FSB800 / 1MB L2 cache / 90nm)
352 (3.2GHz / FSB533 / 512KB L2 cache / 65nm)
341 (2.93GHz / FSB533 / 256KB L2 cache / 90nm)

2.4 [DIMM1, DIMM2] - SOCKET FOR DDRⅡ 667/533/400 NON-ECC DIMM.

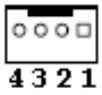
AR-B5500VG provides two DDRⅡ 667/533/400 non-ECC DIMMs to maximize the system physical memory up to **2GBs**.

Please inserting the DIMM into socket carefully to avoid damaging DIMM or socket, and tightly to avoid failed booting.

2.5 [CPUFAN1] - FAN CONNECTOR FOR PROCESSOR HEAT SINK MODULE.

This fan connector can either support fan-speed-controlled fan module to optimize the thermal control, or general DC fan module to dissipate the heat from heat sink.

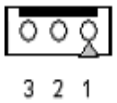
The item "Fan Speed Control" is disabled and hidden in BIOS menu.



1. GND
2. +12V
3. Sense
4. Control

2.6 [SYSFAN1 ~ 4] - FAN CONNECTORS FOR SYSTEM FAN MODULES.

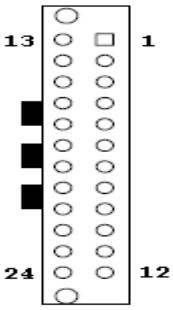
These fan connectors are for general DC fan using to dissipate the heat from system.



1. GND
2. +12V
3. Sense

2.7 [ATX1] - 20-PIN / 24-PIN ATX POWER INPUT FOR SYSTEM.

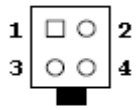
Please choosing a proper power supply unit and connecting the connectors carefully.



PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+3.3V	9	+5VSB	17	GND
2	+3.3V	10	+12V	18	GND
3	GND	11	+12V	19	GND
4	+5V	12	+3.3V	20	NC
5	GND	13	+3.3V	21	+5V
6	+5V	14	-12V	22	+5V
7	GND	15	GND	23	+5V
8	PWROK	16	PS_ON#	24	GND

2.8 [ATX2] - 4-PIN ATX POWER INPUT (+12V ONLY) FOR PROCESSOR.

Please choosing a proper power supply unit and connecting the connectors carefully.



PIN	SIGNAL	PIN	SIGNAL
1	GND	2	GND
3	+12V	4	+12V

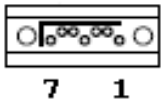
2.9 [JP11] - CMOS DATA KEEPING OR RESETTING SELECTION.

The CMOS data can be reset (clear) by removing battery from corresponding circuit, or pulling signal "RTCRST#" to GND (preferred).

1-2 : On-board battery
(Factory preset)
2-3 : Clear CMOS

2.10 [SATA1 ~ 3] - SERIAL ATA (SATA) DEVICE'S CONNECTOR.

AR-B5500VG provides three SATA connectors for data storage. The data transfer rate can up to **300MB/s** ideally.

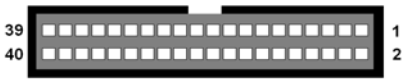


PIN	SIGNAL	PIN	SIGNAL
1	**GND**	5	Rx-
2	Tx+	6	Rx+
3	Tx-	7	**GND**
4	**GND**		

SATA1: Primary SATA channel and Master device.
SATA2: Secondary SATA channel and Master device.
SATA3: Secondary SATA channel and Slave device.

2.11 [IDE1] - PARALLEL ATA (PATA) DEVICE'S CONNECTOR.

AR-B5500VG provides one PATA connectors for data storage. The data transfer rate can up to **100MB/s (Ultra ATA100 / 66 / 33) ideally**, and independent timing of up to two devices.



PIN	SIGNAL	PIN	SIGNAL
1	/RESET	2	**GND**
3	PDATA 7	4	PDATA 8
5	PDATA 6	6	PDATA 9
7	PDATA 5	8	PDATA 10
9	PDATA 4	10	PDATA 11
11	PDATA 3	12	PDATA12
13	PDATA 2	14	PDATA 13
15	PDATA 1	16	PDATA 14
17	PDATA 0	18	PDATA 15
19	**GND**	20	NC
21	PDDREQ	22	**GND**
23	/PDIOW	24	**GND**
25	/PDIOR	26	**GND**
27	PIORDY	28	**GND**
29	/PDDACK	30	**GND**
31	IRQ14	32	NC
33	PDA1	34	66DET
35	PDA0	36	PDA2
37	/PDCS1	38	/PDCS3
39	/HD_LED	40	**GND**

2.12 [CF1] - SOCKET FOR COMPACT FLASH CARD.

AR-B5500VG provides one CF card connector for data storage. The data transfer rate can up to **100MB/s (Ultra ATA100 / 66 / 33) ideally if CF card supports Ultra DMA**.

Notice: The CF1 and IDE1 share the same channel and so two devices can be used by CF1 and IDE1 simultaneously. Some test notes as below:

c	Condition	Hardware or BIOS confirmation
UDMA & UDMA	ATA33 supported only.	Device's limitation? 40-conductor or 80-conductor cable used? BIOS IDE setting is Auto (default)?
UDMA & UDMA	IDE detecting halt.	Device's Master and Slave setting are correct?
UDMA & CF card	IDE detecting halt.	CF card supports UDMA? Device's Master and Slave setting are correct? 40-conductor or 80-conductor cable used? Had been changed BIOS IDE setting PIO mode for non-UDMA CF card?

2.13 [JP14] - COMPACT FLASH CARD MASTER / SLAVE SELECTION.

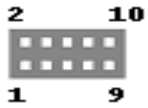
Pulling the CF card pin #39 - "/CSEL" - to GND as CF Master or otherwise as CF Slave. AR-B5500VG' CF1 can be set as Master by shortening JP14.

Short: CF card is master

Open: CF card is slave (Factory preset)

2.14 [JP15] - PANEL CONNECTION.

For Power button, reset button, H.D.D LED, power standby LED, and power-on LED connection.



PIN	Function description
1, 2	H.D.D. active LED (Pin.1 anode)
3, 4	STAND BY LED (Pin.3 anode)
5, 6	POWER ON LED (Pin.5 anode)
7, 8	POWER BUTTON
9, 10	RESET BUTTON

2.15 [VGA1] - ANALOG DISPLAY SIGNALS' ADAPTABLE CABLE CONNECTION.

PIN	SIGNAL	PIN	SIGNAL
1	**Red**	2	**GND**
3	**Green**	4	**GND**
5	**Blue**	6	**GND**
7	VSync	8	SCLK
9	HSync	10	SDATA

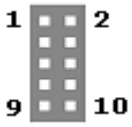
2.16 [KB/MS1] - PS/2 KEYBOARD AND MOUSE ADAPTABLE CABLE CONNECTION.

Pin #	Signal Name
1	MOUSE DATA
2	KB DATA
3	GND
4	VCC
5	MOUSE CLOCK
6	KB CLOCK

2.17 [JP17] - GENERAL PURPOSE INPUT AND OUTPUT (GPIO) CONNECTION.

AR-B5500VG provides eight bits bi-directional and programmable digital I/O for user's application, and also integrates an independent +5V power with self-recoverable fuse protection.

PIN	SIGNAL	PIN	SIGNAL
1	+5V	2	**GND**
3	GP30	4	GP34
5	GP31	6	GP35
7	GP32	8	GP36
9	GP33	10	GP37



2.18 [COM1] - RS232 PORT1 CONNECTION.

AR-B5500VG provides two 16C550 standard compatible enhanced UARTs to perform asynchronous communication. One port named as COM1 – RJ45 connector, and another port named as COM2 – 10-pin box header.

PIN	SIGNAL	PIN	SIGNAL
1	/RTSA	2	/DTRA
3	TXDA	4	**GND**
5	**GND**	6	RXDA
7	/DSRA	8	/CTSA

2.19 [COM2] - RS232 PORT2 CONNECTION.

PIN	SIGNAL	PIN	SIGNAL
1	/DCDB	2	/DSRB
3	RXDB	4	/RTSB
5	TXDB	6	/CTSB
7	/DTRB	8	/RIB
9	**GND**	10	**GND**

2.20 [JP20] - RS232 PORT2 EXPANDED USAGE CONNECTION.

AR-B5500VG provides a 7-pin header **(signals shares with COM2)** for specific application.

PIN	SIGNAL	PIN	SIGNAL
1	Level high	2	+5V
3	TXDB	4	RXDB
5	/RTSB	6	/CTSB
7	GND		

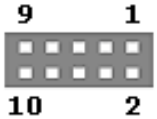
2.21 [USB1] - USB2.0 PORT0 & PORT1 CONNECTION.

USB1 integrated an independent +5V power with self-recoverable fuse protection.

PIN	SIGNAL	PIN	SIGNAL
1	+5V	5	+5V
2	D0-	6	D1-
3	D0+	7	D1+
4	**GND**	8	**GND**

2.22 [USB2] - USB2.0 PORT2 & PORT3 ADAPTABLE CABLE CONNECTION.

USB2 integrated an independent +5V power with self-recoverable fuse protection.



PIN	SIGNAL	PIN	SIGNAL
1	+5V	2	+5V
3	D2-	4	D3-
5	D2+	6	D3+
7	**GND**	8	**GND**
9	**GND**	10	**GND**

2.23 [LAN1 ~ 8] - 1000BASE-T, 100BASE-TX, AND 10BASE-T ETHERNET PORTS.

LAN1 and LAN2 support BYPASS and controllable by hardware (JP12) or software. LAN5 and LAN6 are optional.

Left LED: Color yellow for activity.
Right dual-LED: Non-lighted for 10Mbps linking.
Color green for 100Mbps linking.
Color orange for 1000Mbps linking.

2.24 [JP12] - LAN1 AND LAN2 BYPASS CONTROL SELECTION.

1-2: forced Normal.
2-3: controlled by software (factory preset).
Otherwise: forced BYPASS.

Notice: The Ethernet cable Cat.5e is preferable for 1000BASE-T linking. If user would like to use Cat.5 or other degraded cable, that may cause linked fault or lower performance by given cable length.

2.25 [PCIE16] – PCI EXPRESS X16 CARD CONNECTION.

IDSEL: AD21	**INT(ABCD): FGHE**	**REQ: 0**	**GNT: 0**

2.26 [PCI2] - 3.3V / 33MHZ / 32-BIT TYPE-III MINI PCI CARD CONNECTION.

IDSEL: AD22	**INT(ABCD): GHEF**	**REQ: 1**	**GNT: 1**

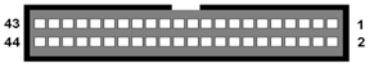
2.27 [RST1] - ON-BOARD RESET BUTTON.

2.28 [LED1] - DUAL LEDS FOR H.D.D. STATUS AND POWER-ON INDICATION.

Upper LED: color green for power-on.
Lower LED: color yellow for H.D.D. action.

2.29 [IDE2] - OPTIONAL. PARALLEL ATA (PATA) DEVICE'S CONNECTOR.

IDE2 signals share with IDE1 and CF1. They are the same channel.



PIN	SIGNAL	PIN	SIGNAL
1	/RESET	2	**GND**
3	PDATA 7	4	PDATA 8
5	PDATA 6	6	PDATA 9
7	PDATA 5	8	PDATA 10
9	PDATA 4	10	PDATA 11
11	PDATA 3	12	PDATA 12
13	PDATA 2	14	PDATA 13
15	PDATA 1	16	PDATA 14
17	PDATA 0	18	PDATA 15
19	**GND**	20	NC
21	PDDREQ	22	**GND**
23	/PDIOW	24	**GND**
25	/PDIOR	26	**GND**
27	PIORDY	28	**GND**
29	/PDDACK	30	**GND**
31	IRQ14	32	NC
33	PDA1	34	66DET
35	PDA0	36	PDA2
37	/PDCS1	38	/PDCS3
39	/HD_LED	40	**GND**
41	+5V	42	+5V
43	**GND**	44	NC

2.30 [JP16, JP19] – RESERVED JUMPER.

Notice: Please do not use.

4. WATCHDOG, GPIO, AND BYPASS PROGRAMMING.

4.1 WATCHDOG PROGRAMMING

This section describes the usage of WATCHDOG. AR-B5500VG integrated the WATCHDOG that enable user to reset the system after a time-out event. User can use a program to enable the WATCHDOG and program the timer in range of 1~255 second(s)/minute(s). Once user enables the WATCHDOG, the timer will start to count down to zero except trigger the timer by user's program continuously. After zeroize the timer (stop triggering), the WATCHDOG will generate a signal to reset the system. It can be used to prevent system crash or hang up. The WATCHDOG is disabled after reset and should be enabled by user's program.

Please refer to the following table to program WATCHDOG properly, and user could test WATCHDOG under 'Debug' program.

Address port: 2E and Data port: 2F	
C:>debug	To enter debug mode.
-o 2E 87 **-o 2E 01** **-o 2E 55** **-o 2E 55**	To enter configuration.
-o 2E 07	To point to Logical Device Number Reg.
-o 2F 07	To select logical device 7 (WATCHDOG).
-o 2E 72 **-o 2F 40**	To select "keyboard reset" as WATCHDOG output to reset system.
-o 2E 72	Preparing to select the unit of timer equals minute or second.
-i 2F	To read the value of index "2F".
-o 2F xx	The value "xx" equals [(value of index "2F") OR (80)]. OR (80): unit is second. OR (00): unit is minute.
-o 2E 73	Preparing to set the WATCHDOG timer value.
-o 2F ##	The value "##" ranges between 01 ~ FF (1 ~ 255 seconds). **00: To disable WATCHDOG.**
-q	To quit debug mode

Notice: The "actual" timer value may not match with the "theoretical". That is because of the tolerance of internal oscillating clock and cannot be adjusted or optimized.

The WATCHDOG sample code of C language as below:

```
//=============================================================================
//   Language include files
//=============================================================================
#include <conio.h>
#include <stdlib.h>
#include <stdio.h>
#include <dos.h>

//=============================================================================
//   Normal procedure
//=============================================================================
void Show_Help();

//=============================================================================
//   Main procedure
//=============================================================================
```

```
int main(int argc, char *argv[])
{
    unsigned char IO_Port_Address=0x2E;
    unsigned char Time;
    int Temp;

    if ( argc != 2 )
      {   Show_Help();     return 1;        }

    clrscr();
    Time=atoi(argv[1]);

    // To set Watchdog.
    outportb(IO_Port_Address,0x87);        // To enter configuration.
    outportb(IO_Port_Address,0x01);
    outportb(IO_Port_Address,0x55);
    outportb(IO_Port_Address,0x55);

    outportb(IO_Port_Address,0x07);        // To point to Logical Device Number Reg.
    outportb(IO_Port_Address+1,0x07);    // To select logical device 7 (Watchdog Function).

    outportb(IO_Port_Address,0x72);        // To select "keyboard reset" as WATCHDOG output to reset system.
    outportb(IO_Port_Address+1,0x40);

    outportb(IO_Port_Address,0x72);        // Preparing to select the unit of timer equals minute or second.
    outportb(IO_Port_Address+1,inportb(IO_Port_Address+1)|0x80); // Unit is second.

    outportb(IO_Port_Address,0x73);        // Preparing to set the WATCHDOG timer value.
    outportb(IO_Port_Address+1,Time);    // The "Time" ranges between 01 ~ FF and 00 is disabled.

    textcolor(YELLOW);
    for(Temp=Time;Temp>0;Temp--)
     {

        gotoxy(20,10);
        cprintf(">>> After %3d Second will reset the system. <<<",Temp);

        delay(1000);
     }

    textcolor(LIGHTRED);
    gotoxy(18,10);
    cprintf("If you can see this message, Reset system is Fail");
    return 0;
}

//==========================================================================
// Function   : Show_Help()
// Input      : -
// Change     : -
// Return     : -
// Description    : Show Title string.
//==========================================================================
void Show_Help()
{
    clrscr();
    printf("WatchDog Test for ITE8712F\n");
    printf("Sample:                              \n");
```

```
    printf("            WDT.EXE 10              \n");
    printf("( For 10 seconds to reset. )\n");
}
```

4.2 GPIO PROGRAMMING

This section describes the usage of GPIO. AR-B5500VG integrated eight bits, 5V TTL level, bidirectional, and software programmable GPIOs for user's application. They are all capable of 5 mA source current for output and 8 mA sink current for input individually. The electrical characteristics of GPIOs as following table:

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		µA
I_{IH}	High Input Leakage	V_{IN} = VCC			-10	µA
I_{oz}	3-state Leakage				20	µA

Address port: 2E and Data port: 2F								
GP##	GP37	GP36	GP35	GP34	GP33	GP32	GP31	GP30
Bit #	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)

The GPIO sample code of C language as below:

```
//=============================================================================
//   Language include files
//=============================================================================
#include <conio.h>
#include <stdio.h>

//=============================================================================
//   Normal procedure
//=============================================================================
void Show_Help();
void Show_Fail();
void Show_Pass();

//=============================================================================
//   Main procedure
//=============================================================================
int main(int argc)
{
   char *Model_Name="AR-B5500VG";
   unsigned char IO_PORT_BASE=0x2E;   // DATA_PORT = IO_PORT_BASE + 1;
   unsigned short int SIMPLE_IO_BASE;
   unsigned char data;
   int result=0;

   if ( argc >1 )
      {   Show_Help();     return 1;   }

   clrscr();
   textcolor(WHITE);
   gotoxy(1,                                                                    1);
cprintf("<>=============================================================================<>");
   gotoxy(1, 2);   cprintf("|| ITE8712F GPIO Test Utility v1.0 Acrosser Technology Co., Ltd.                ||");
   gotoxy(1,                                                                    3);
```

```
cprintf("<>================================================================================<>");
   gotoxy(1,                                                                                4);
cprintf("<>================================================================================<>");
   gotoxy(1, 5);   cprintf("|| Model Name   :                                                  ||");
   gotoxy(1, 6);   cprintf("|| SIO IO Base :                                                 ||");
   gotoxy(1, 7);   cprintf("|| Simple I/O Base :                                            ||");
   gotoxy(1,                                                                                8);
cprintf("<>================================================================================<>");

   // To enter configuration.
   outportb(IO_PORT_BASE,0x87);
   outportb(IO_PORT_BASE,0x01);
   outportb(IO_PORT_BASE,0x55);
   outportb(IO_PORT_BASE,0x55);

   // To select logic device number 7.
   outportb(IO_PORT_BASE,0x07);
   outportb(IO_PORT_BASE+1,0x07);

   // To set multi-function pins to GPIO30~GPIO37
   outportb(IO_PORT_BASE,0x27);
   outportb(IO_PORT_BASE+1,0xFF);

   // GPIO30~GPIO37 use simple I/O function.
   outportb(IO_PORT_BASE,0xC2);
   outportb(IO_PORT_BASE+1,0xFF);

   // To get simple I/O base address.
   outportb(IO_PORT_BASE,0x62);          // Simple I/O base address MSB
   SIMPLE_IO_BASE=inportb(IO_PORT_BASE);
   SIMPLE_IO_BASE=SIMPLE_IO_BASE<<8;
   outportb(IO_PORT_BASE,0x63);          // Simple I/O base address LSB
   SIMPLE_IO_BASE=SIMPLE_IO_BASE|inportb(IO_PORT_BASE);

   // To show parameters.
   textcolor(LIGHTGRAY);
   gotoxy(18,5);      cprintf("%s",Model_Name);
   gotoxy(18,6);      cprintf("%X",IO_PORT_BASE);
   gotoxy(22,7);      cprintf("%X",SIMPLE_IO_BASE);

   // To set GPIO30~33 as output, and GPIO34~GPIO37 as input.
   outportb(IO_PORT_BASE,0xCA);
   outportb(IO_PORT_BASE+1,0x0F);      // bit value "1" = output.

   // To set GPIO30~33 output as HIGH.
   outportb(SIMPLE_IO_BASE+2,0x0F);

   // To read GPIO34~37 and make sure the values are matched.
   data=inportb(SIMPLE_IO_BASE+2)&0xF0;
   if(data!=0xF0)
       result=1;

   // To set GPIO30~33 output as LOW.
   outportb(SIMPLE_IO_BASE+2,0x00);

   // To read GPIO34~37 and make sure the values are matched.
   data=inportb(SIMPLE_IO_BASE+2)&0xF0;
   if(data!=0x00)
```

```
        result=1;

    // To set GPIO30~33 as input, GPIO34~GPIO37 as output.
    outportb(IO_PORT_BASE,0xCA);
    outportb(IO_PORT_BASE+1,0xF0);       // bit value "1" = output.

    // To set GPIO34~37 as HIGH.
    outportb(SIMPLE_IO_BASE+2,0xF0);

    // To read GPIO30~33 and make sure the values are matched.
    data=inportb(SIMPLE_IO_BASE+2)&0x0F;
    if(data!=0x0F)
        result=1;

    // To set GPIO34~37 as LOW.
    outportb(SIMPLE_IO_BASE+2,0x00);
    // To read GPIO30~33 and make sure the values are matched.
    data=inportb(SIMPLE_IO_BASE+2)&0x0F;
    if(data!=0x00)
        result=1;

    // To exit Configuration.
    outportb(IO_PORT_BASE,0x02);
    outportb(IO_PORT_BASE+1,0x02);

    if(result)
       Show_Fail();
    else
       Show_Pass();

    return result;
}

//===========================================================================
// Function   : Show_Help()
// Input      : -
// Change     : -
// Return     : -
// Description    : Show Title string.
//===========================================================================
void Show_Help()
{
     clrscr();
     printf("GPIO Test utility for ITE8712F\n\n");
     printf("Vcc   ?                    ? GND \n");
     printf("GP30 ?  ?迂迂迂迂? ? GP34\n");
     printf("GP31 ?  ?迂迂迂迂? ? GP35\n");
     printf("GP32 ?  ?迂迂迂迂? ? GP36\n");
     printf("GP33 ?  ?迂迂迂迂? ? GP37\n");
}

//===========================================================================
// Function   : Show_Fail()
// Input      : -
// Change     : -
// Return     : -
// Description    : Show Fail Message.
//===========================================================================
```

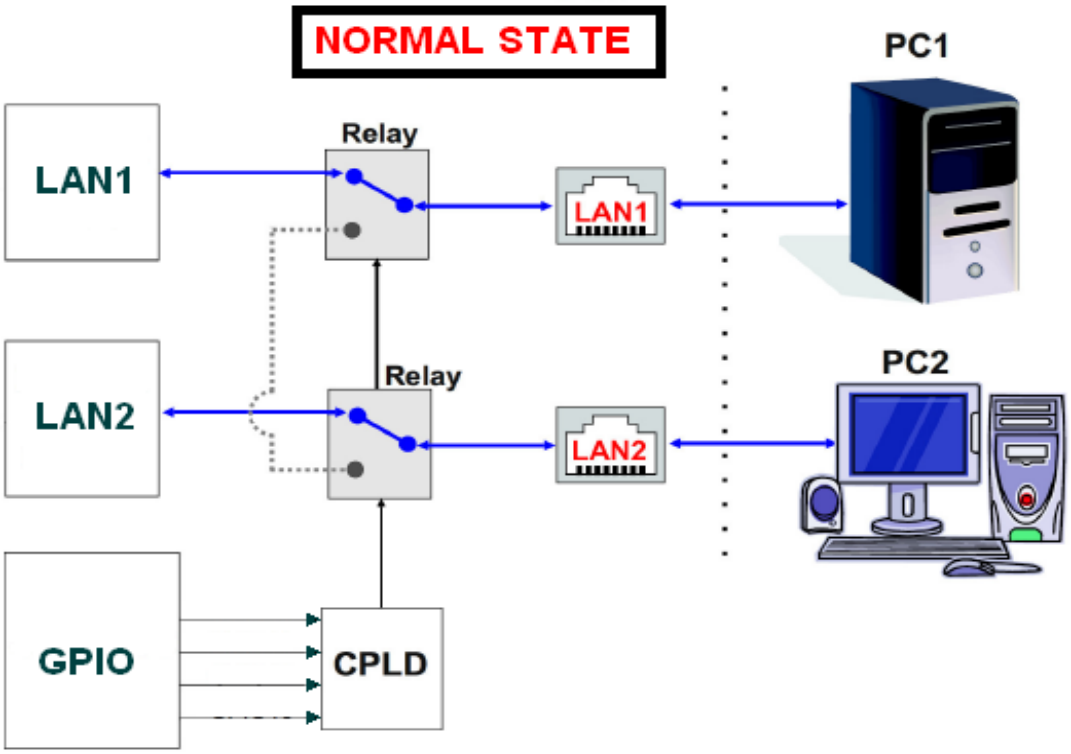
```
void Show_Fail()
{
    textcolor(LIGHTRED);
    gotoxy(20,10);    cprintf("  訶訶訶訶   訶訶訶訶     訶訶訶    訶          ");
    gotoxy(20,11);    cprintf("  訶           訶   訶       訶      訶          ");
    gotoxy(20,12);    cprintf("  訶訶訶訶?  訶訶訶訶訶     訶      訶          ");
    gotoxy(20,13);    cprintf("  訶           訶      訶      訶      訶          ");
    gotoxy(20,14);    cprintf("  訶           訶      訶     訶訶     訶訶訶訶訶");
}

//=============================================================================
// Function  : Show_Pass()
// Input     : -
// Change    : -
// Return    : -
// Description   : Show Pass Message.
//=============================================================================
void Show_Pass()
{
    textcolor(LIGHTGREEN);
    gotoxy(20,10);    cprintf("  訶訶訶訶   訶訶訶訶   訶訶訶訶訶  訶訶訶訶訶");
    gotoxy(20,11);    cprintf("  訶      訶   訶   訶   訶          訶          ");
    gotoxy(20,12);    cprintf("  訶訶訶訶訶  訶訶訶訶訶  訶訶訶訶訶  訶訶訶訶訶");
    gotoxy(20,13);    cprintf("  訶           訶      訶          訶          訶");
    gotoxy(20,14);    cprintf("  訶           訶      訶  訶訶訶訶訶  訶訶訶訶訶");
}
```

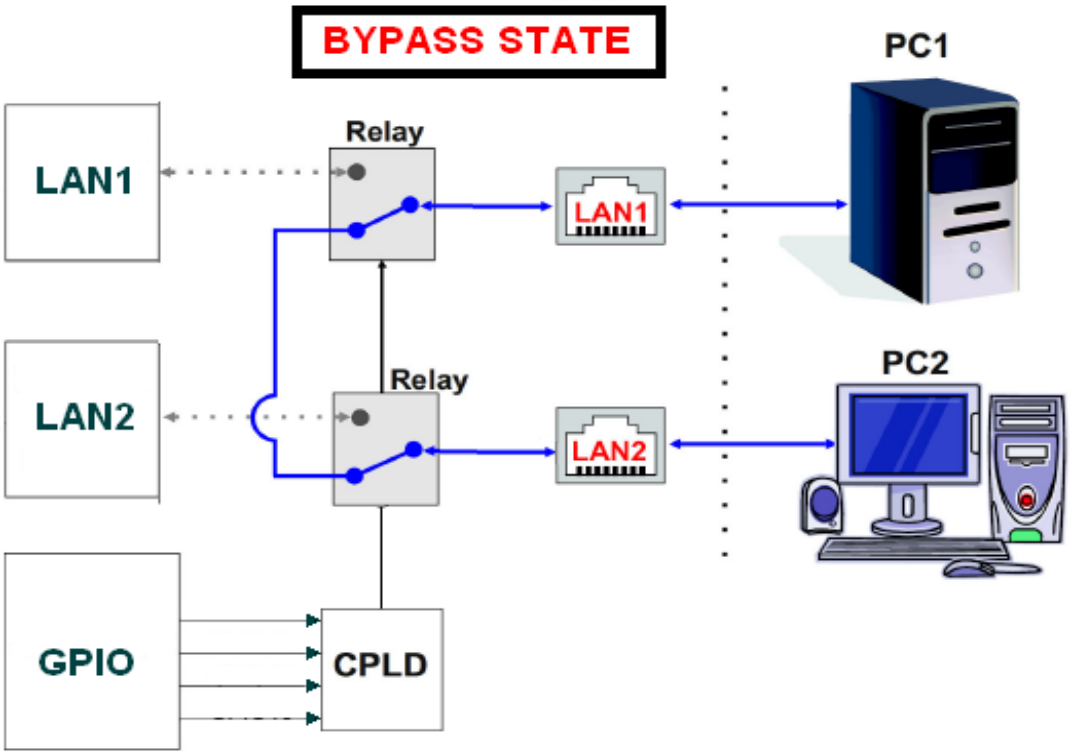
4.3 BYPASS PROGRAMMING

This section describes the usage of BYPASS. AR-B5500VG integrated BYPASS by Ethernet ports LAN1 and LAN2, and also provides a jumper and four bits GPIOs - BYPASS WATCHDOG - to do BYPASS control selection. Please refer to section 2.24 "[JP12] - LAN1 and LAN2 BYPASS controlling selection" to get jumper setting, and obtain the BYPASS illustrations, flow chart, test notes, and software programming guide as below.

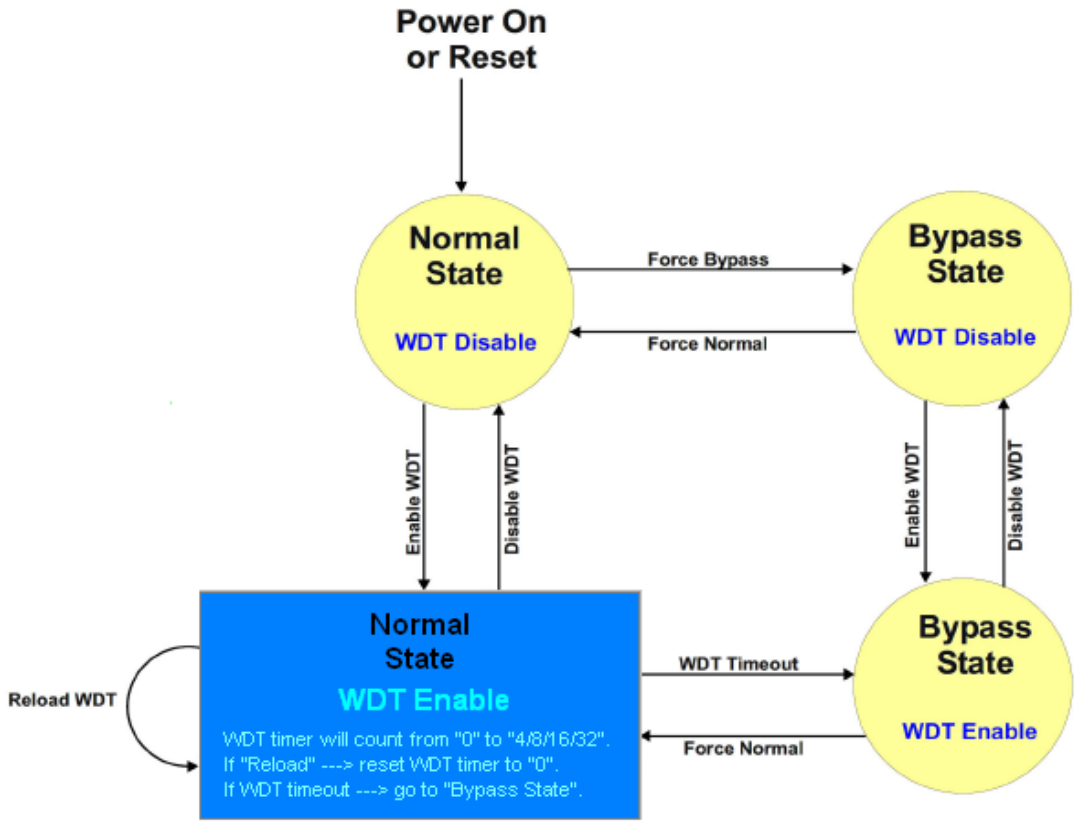
BYPASS illustration – NORMAL STATE



BYPASS illustration – BYPASS STATE



BYPASS flow chart



Test notes

Jumper (JP12) setting / Software control	Notes
1-2: forced Normal.	a. System power-off: forced BYPASS state. b. System power-on: forced NORMAL state. c. Software's control is ignorant.
2-3: controlled by software.	a. System power-off: forced BYPASS state. b. System power-on: forced NORMAL state as default. c. Software's control is attendant. d. To disable the bypass watchdog timer first before setting timer value. e. During the timer counting, user can always command "reload" to reset timer value to beginning.
Otherwise: forced BYPASS.	a. System power-off: forced BYPASS state. b. System power-on: forced BYPASS state. c. Software's control is ignorant.

BYPASS software programming guide

Data port: 281				
GP##	GP23	GP22	GP21	GP20
Bit #	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)

Command	GP23	GP22	GP21	GP20
Enable WDT	Low			
Disable WDT				
Reload WDT			Low	Low
Force Normal	Low	Low		Low
Force Bypass		Low		Low
Set WDT to 4 second	Low	Low	Low	
Set WDT to 8 second		Low	Low	
Set WDT to 16 second			Low	
Set WDT to 32 second	Low	Low		

C:>debug	Statement in C language	To enter debug mode.
-o 281 0A	**outportb(0x281,0x0A);**	Forced bypass state.
-o 281 02	**outportb(0x281,0x02);**	Forced normal state.
-o 281 0F	**outportb(0x281,0x0F);**	To disable bypass watchdog timer.
-o 281 01	**outportb(0x281,0x01);**	To set timer value as 4 seconds. 0x09: 8 seconds. 0x0D: 16 seconds. 0x03: 32 seconds.
-o 281 07	**outportb(0x281,0x07);**	To enable bypass watchdog timer. To count to timer value then forced bypass sate.
-o 281 02	**outportb(0x281,0x02);**	Forced normal state. To Wait for command "reload" or "forced bypass".
-o 281 0C	**outportb(0x281,0x0C);**	To reload. To recount the recent timer value again.
-o 281 02	**outportb(0x281,0x02);**	Forced normal state.

5. BIOS CONSOLE

This chapter describes the AR-B5500VG BIOS menu displays and explains how to perform common tasks needed to get up and running, and presents detailed explanations of the elements found in each of the BIOS menu. The following topics are covered:

- **Main**
- **Advanced**
- **Power**
- **PnP/PCI**
- **Peripherals**
- **PC Health**
- **Boot**
- **Exit**

BIOS SETUP OVERVIEW

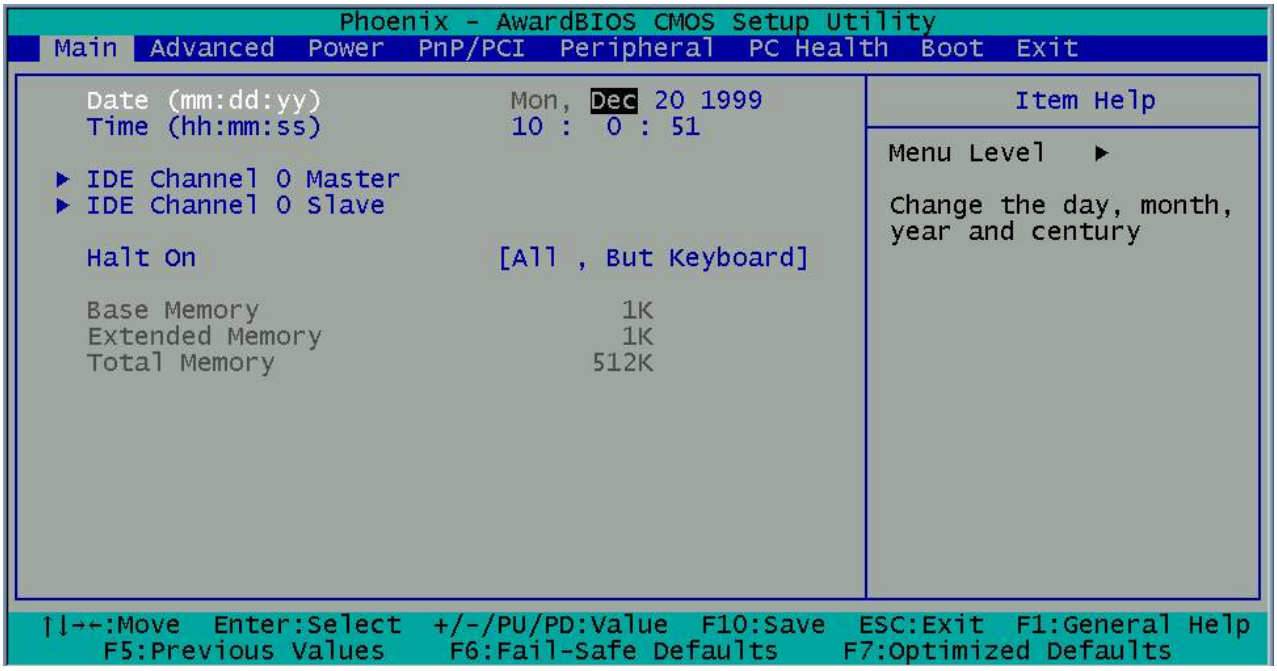
The BIOS is a program used to initialize and set up the I/O system of the computer, which includes the PCI bus and connected devices such as the video display, diskette drive, and the keyboard. The BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS default values ensure that the system will function at its normal capability. In the worst situation, maybe the user have corrupted the original setting.

After the computer power-on, BIOS will perform diagnostics on the system and display the size of the memory that is being tested. **Press the [Del] key to enter the BIOS setup program**, and then the main menu will show on the screen.

5.1 MAIN

The BIOS setup main menu includes some options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to select the item and configure the functions.



The <Main> menu allows you to record some basic system hardware configuration and set the system time and error handling. If the board had already installed in a working system, you will not need to select this option anymore.

Date & Time Setup

Highlight the <Date> field and then press the [Page Up]/[Page Down] or [+] / [-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up]/[Page Down] or [+] / [-] keys to set the current date. Follow the hour, minute and second format.

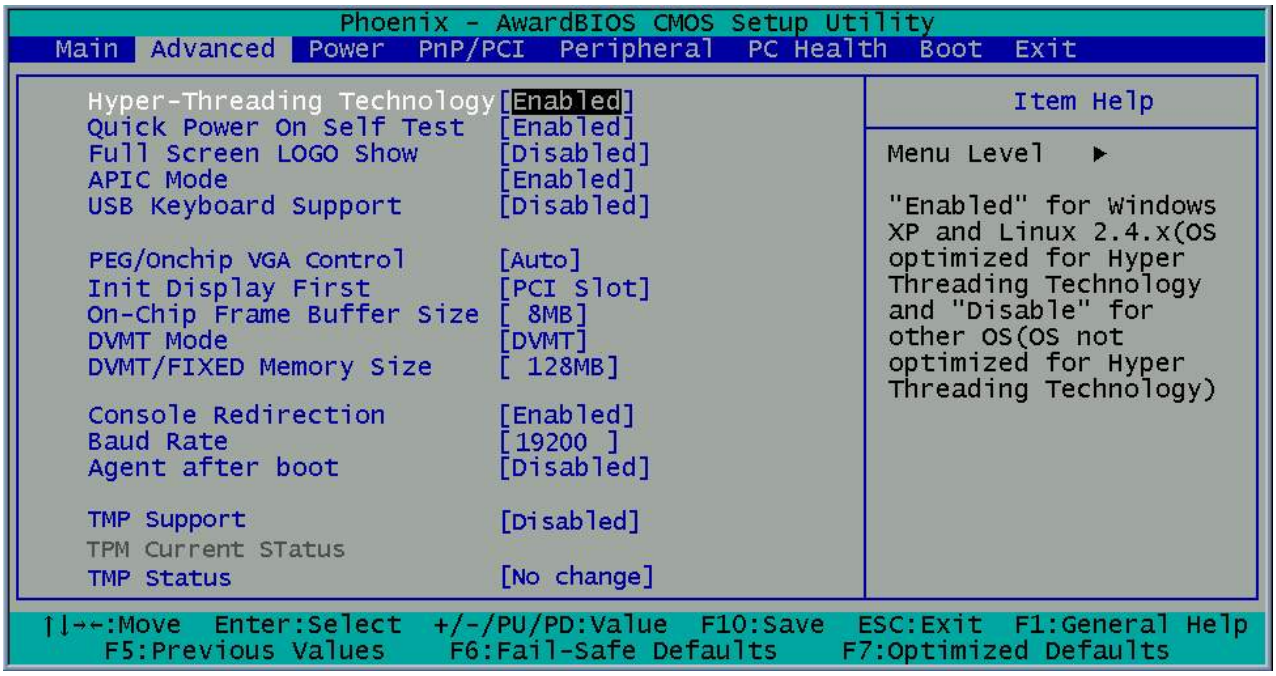
The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri. Master> and <Pri. Slave>, so user can install up to two hard disks (devices). For the master and slave jumpers, please refer to the hard disk's installation guide.

5.2 ADVANCED

The <Advanced > menu consists of configuration entries that allow you to improve your system performance, or let you modify some system features according to your preference. Some entries are required and reserved by the board's design.



Hyper-Threading Technology

This item only presents for Intel processor, which supports Hyper-Threading technology.

Quick Power On Self Test

This item speeds up Power On Self Test (POST) after you power-on the computer. If it is [Enabled], BIOS will shorten or skip some check items during POST.

APIC Mode

Advanced Programmable Interrupt Controller.
This item [Enabled] for more system INTerrupts that AR-B5500VG required.

USB Keyboard Support

This item [Enabled] or [Disabled] for USB keyboard support or nonsupport.

DVMT Mode

Dynamic Video Memory Technology.
[Enabled] for optimizing amount of memory is located for balanced graphics and system performance.

Console Redirection

[Enabled] for user who want to remote control the system via serial port.

Baud Rate

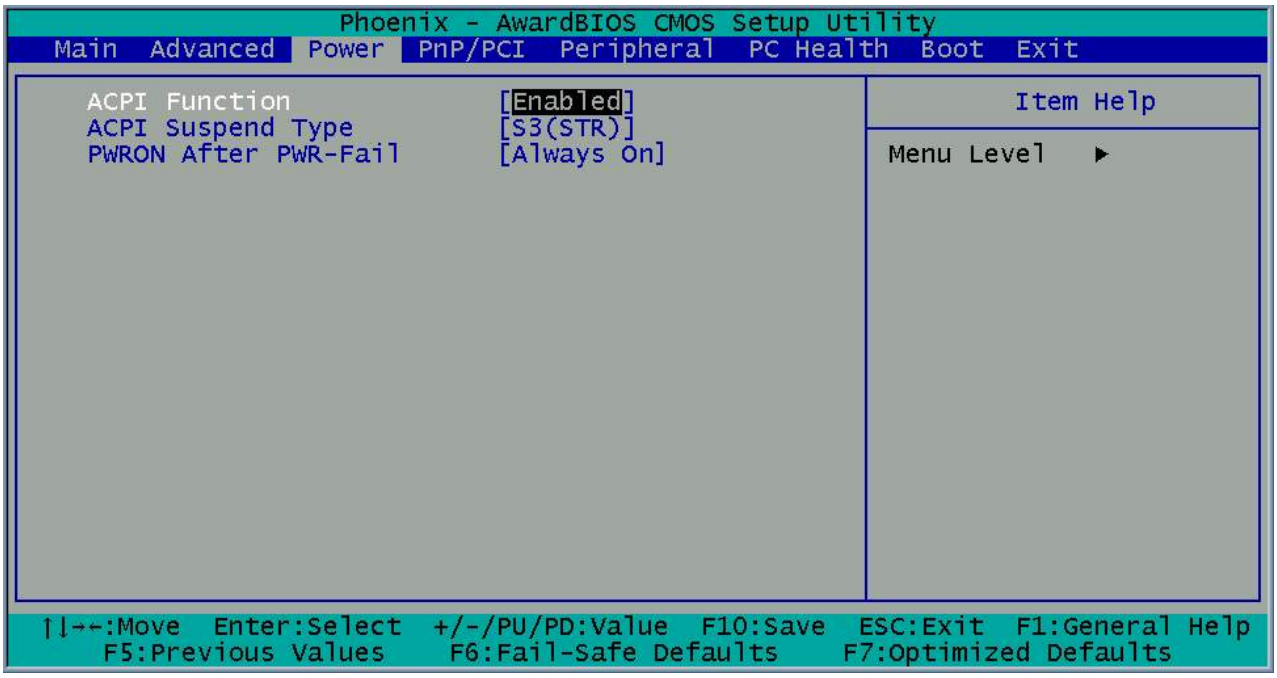
The baud rate of remote control machine should the same as the system for communication.

TPM Support

[Enabled] for on-board Trusted Platform Module support.

5.3 POWER

This option determines the configuration of power management.



ACPI Function

Advanced Configuration and Power Interface.
[Enabled] for advanced power management - power saving.

ACPI Suspend Type

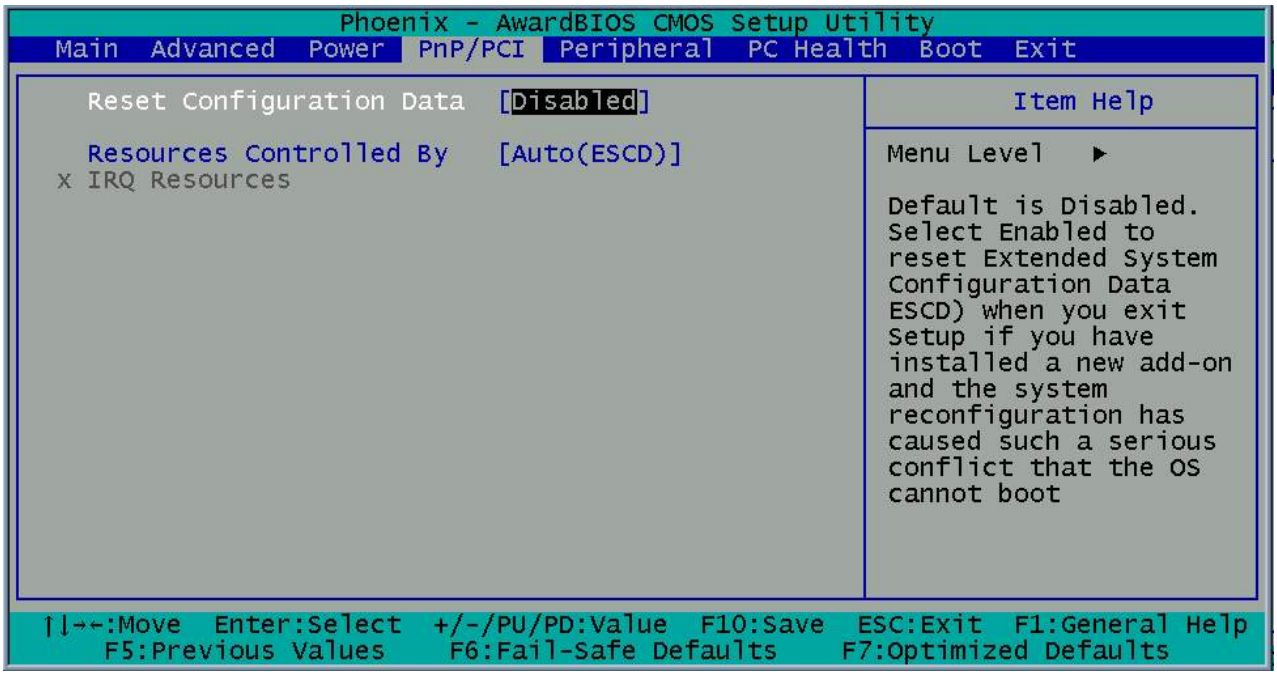
[S1 (POS)]: Power-on Suspend.
[S3 (STR)]: Suspend To RAM.
[**S4 (STD)]:** Suspend To Disk.

PWRON After PWR-Fail

[Always On]: After power-loss or sudden power cut-off, system will power-on automatically when power recovered.
[Always Off]: System needs a wake-up event such as triggering power button, WOL (Wake On Lan), and WOM (Wake On Modem), etc. for power-on once more.
[Last State]: If the system was shutdown unexpectedly, then behaves as [Always On]. Otherwise as [Always Off].

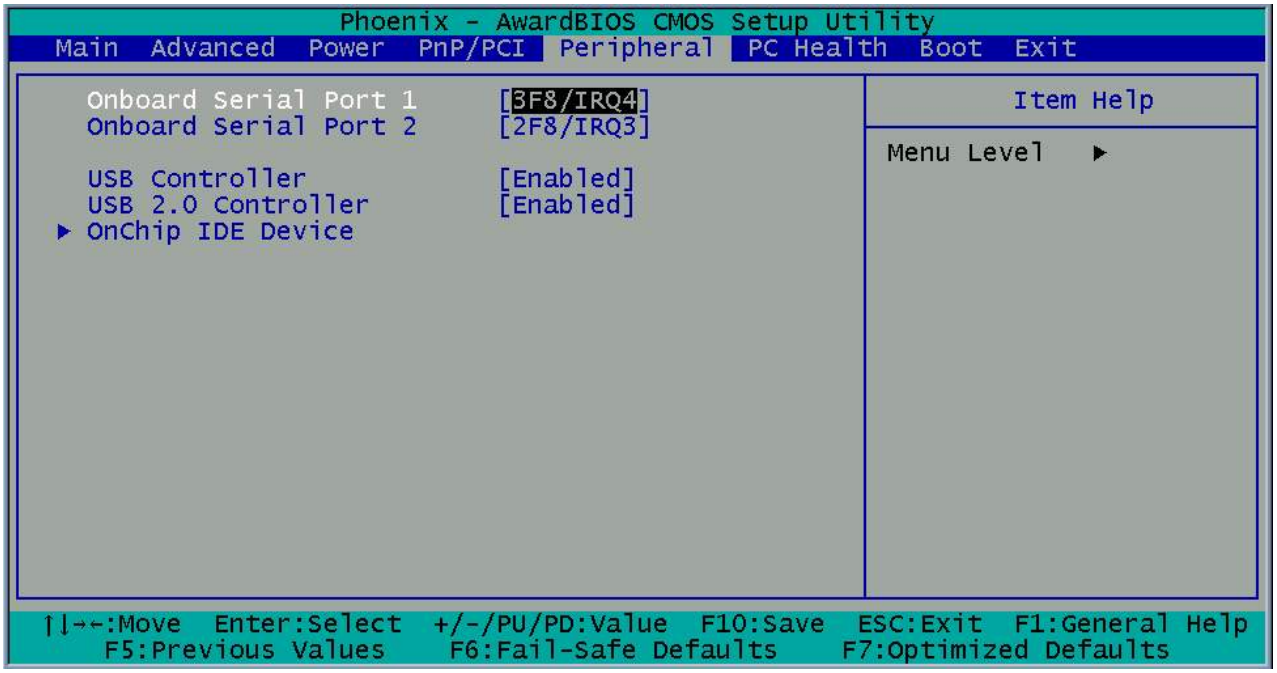
5.4 PCI/PNP

This option determines the configuration of IRQ resources.



5.5 PERIPHERALS

This option determines the configuration of peripheral devices.

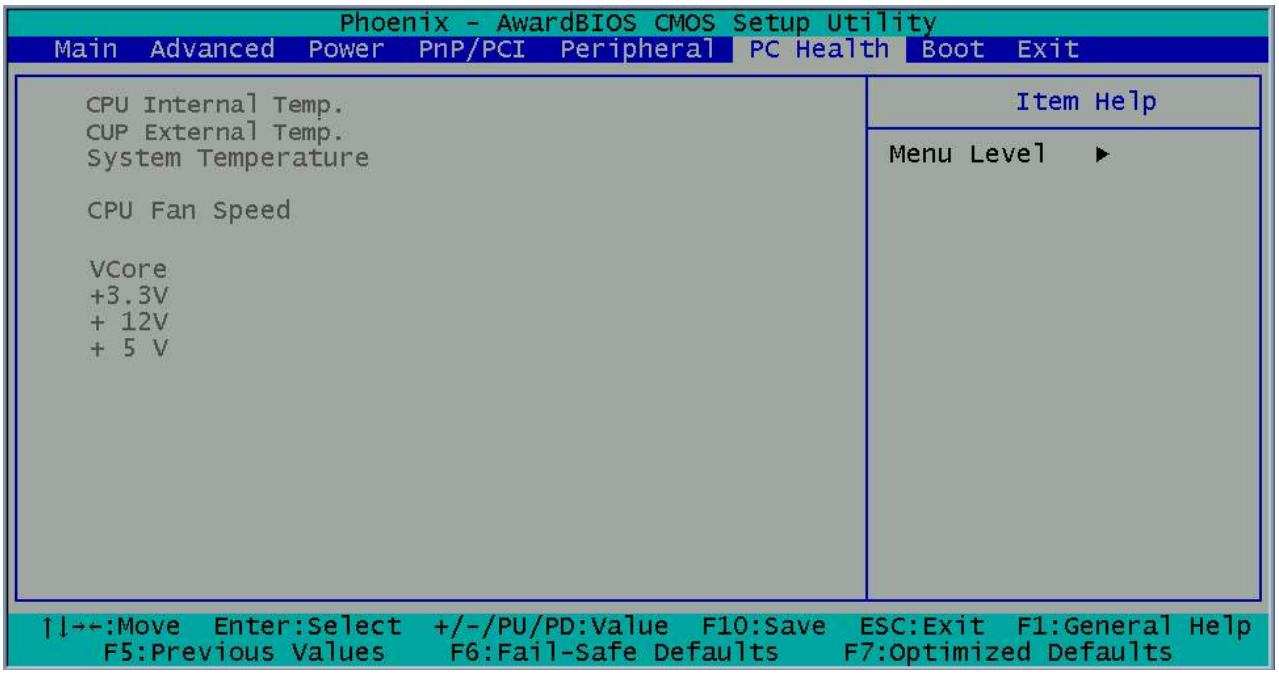


Onchip IDE Device

Tuning Parallel ATA interface and Serial ATA interface for device(s).

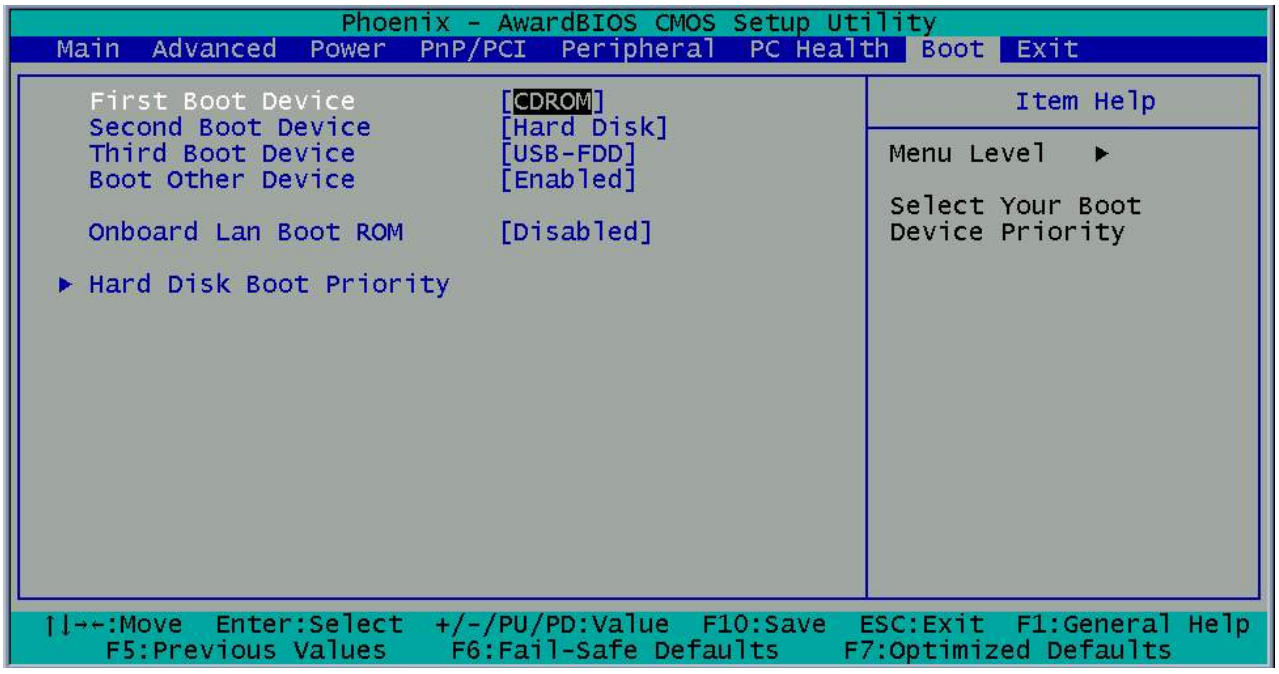
5.6 PC HEALTH

This option allows user to monitor the values/status of temperatures, fan speed, and voltage(s).



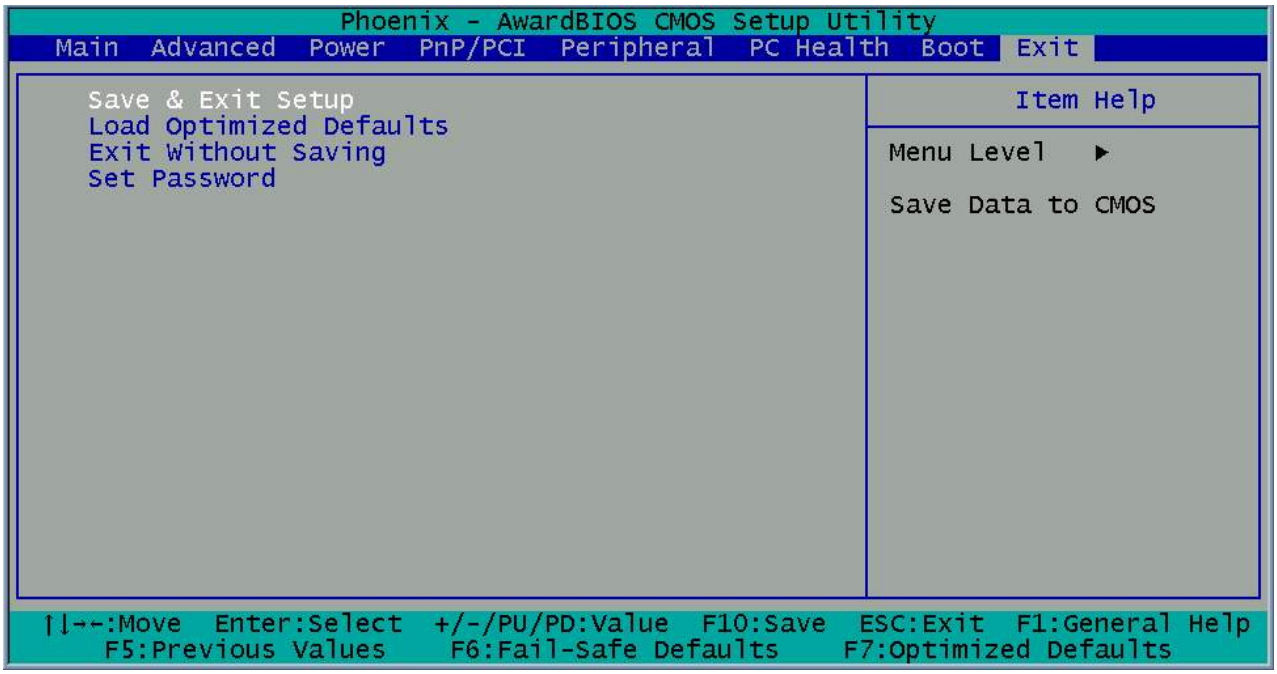
5.7 BOOT

This option allows user to select sequence/priority of boot device(s) and Boot From Lan.



5.8 EXIT

This option is used to exit the BIOS main menu and change password.



5.9 BIOS UPDATING

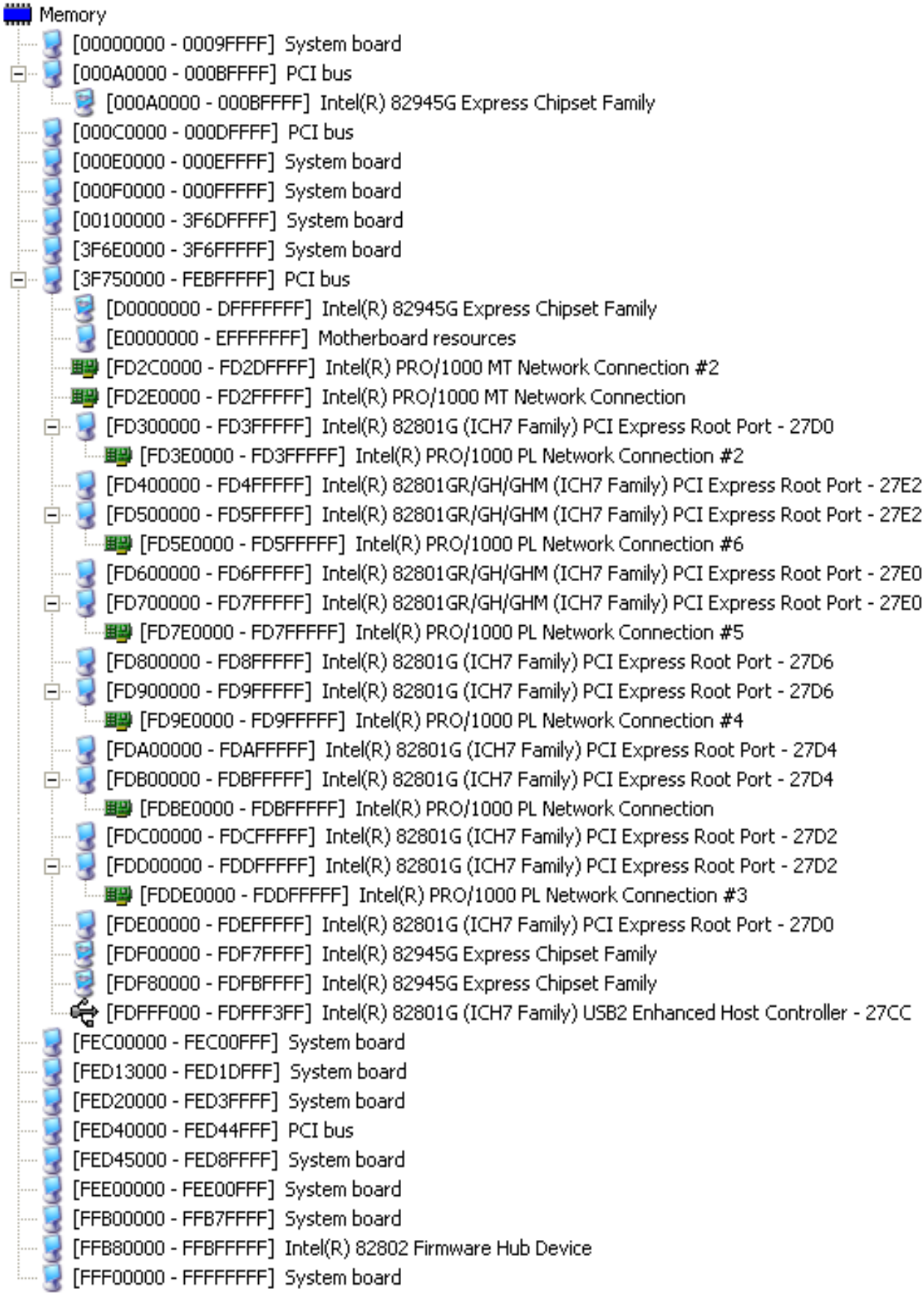
The BIOS program instructions are contained within computer chips called FLASH ROMs that are located on your system board. The chips can be electronically reprogrammed, allowing you to update your BIOS firmware without removing and installing chips.

The AR-B5500VG provides the FLASH BIOS update function for you to easily to update BIOS.

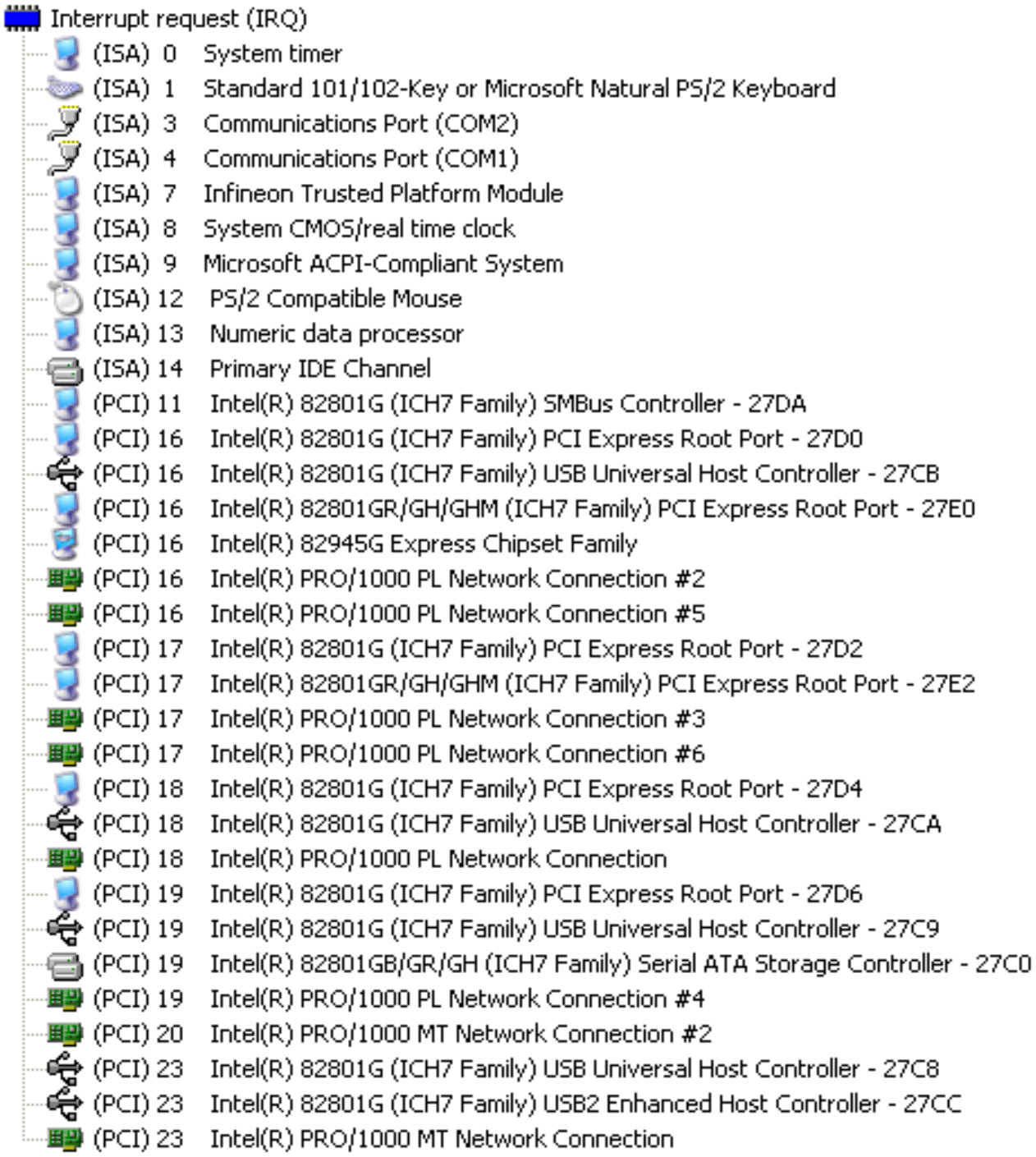
Please follow these operating steps to update BIOS:

Step 1:	You must boot up system into MS-DOS first and please don't detect files CONFIG.SYS and AUTOEXEC.BAT.
Step 2:	In the MS-DOS mode, you should execute the AWDFLASH program to update BIOS.
Step 3:	Follow all messages then you can update BIOS smoothly.

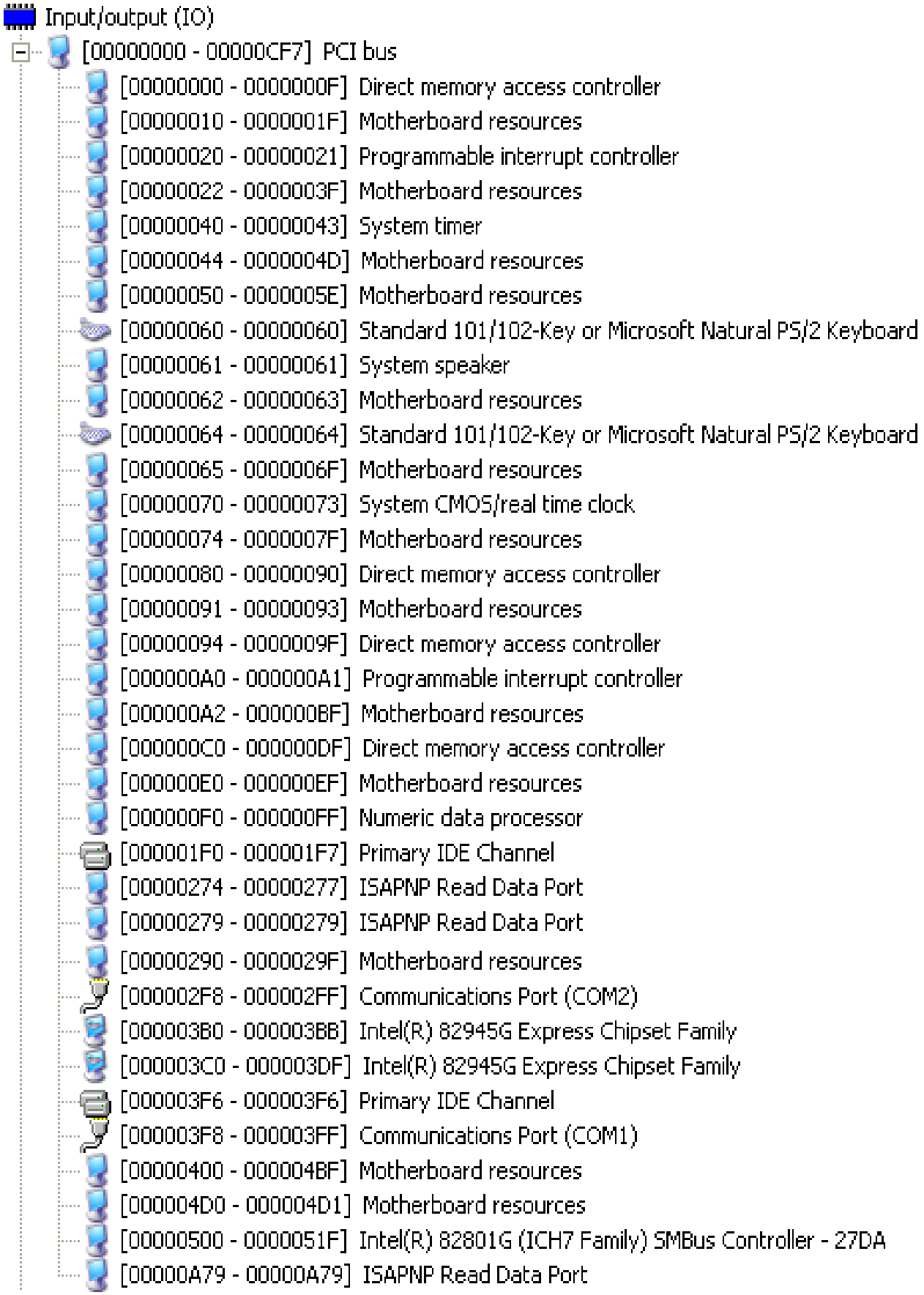
APPENDIX A. MEMORY MAP

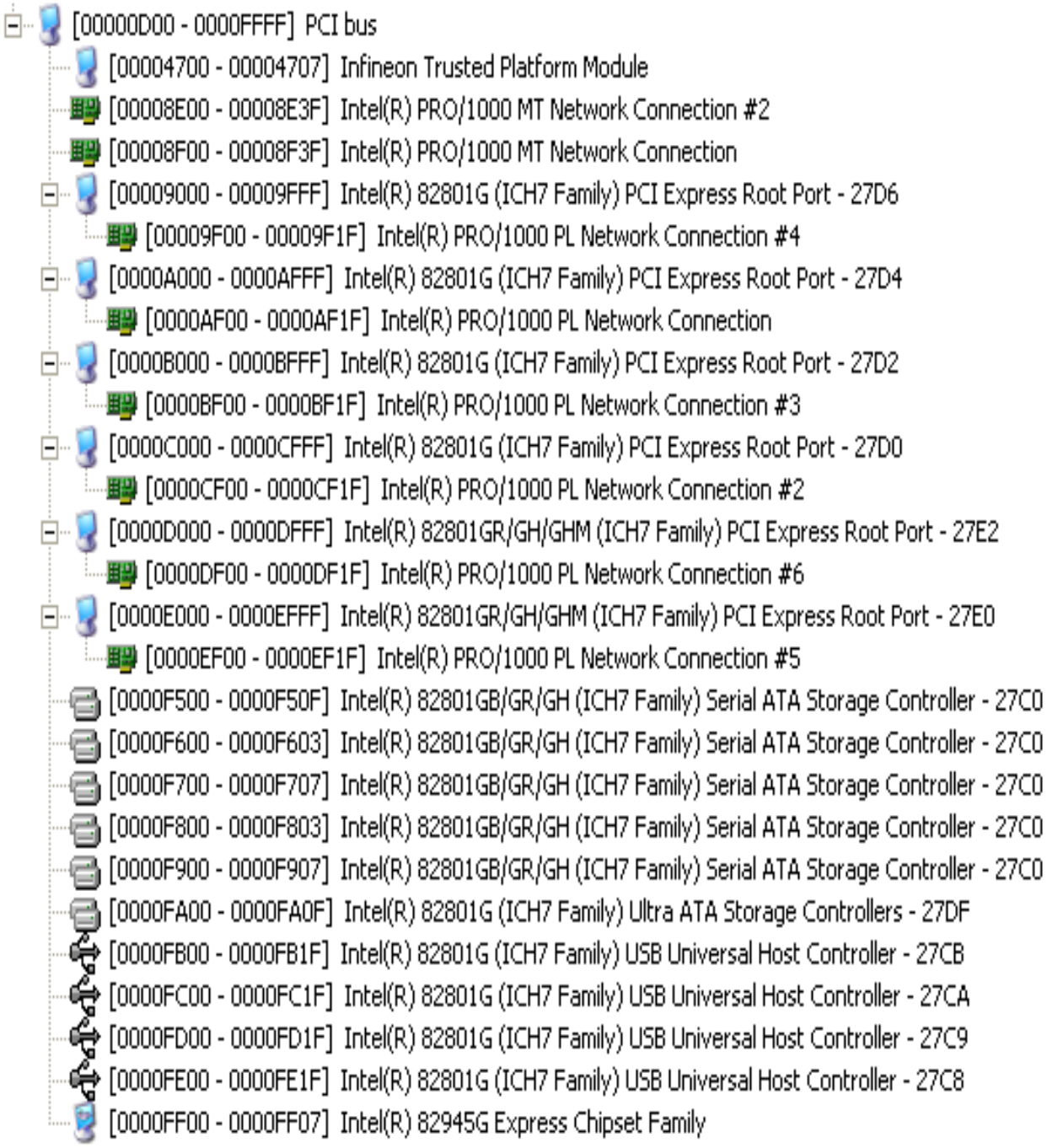


APPEXDIX B. IRQ MAP



APPENDIX C. I/O PORT MAP




[00000D00 - 0000FFFF] PCI bus
[00004700 - 00004707] Infineon Trusted Platform Module
[00008E00 - 00008E3F] Intel(R) PRO/1000 MT Network Connection #2
[00008F00 - 00008F3F] Intel(R) PRO/1000 MT Network Connection
[00009000 - 00009FFF] Intel(R) 82801G (ICH7 Family) PCI Express Root Port - 27D6
[00009F00 - 00009F1F] Intel(R) PRO/1000 PL Network Connection #4
[0000A000 - 0000AFFF] Intel(R) 82801G (ICH7 Family) PCI Express Root Port - 27D4
[0000AF00 - 0000AF1F] Intel(R) PRO/1000 PL Network Connection
[0000B000 - 0000BFFF] Intel(R) 82801G (ICH7 Family) PCI Express Root Port - 27D2
[0000BF00 - 0000BF1F] Intel(R) PRO/1000 PL Network Connection #3
[0000C000 - 0000CFFF] Intel(R) 82801G (ICH7 Family) PCI Express Root Port - 27D0
[0000CF00 - 0000CF1F] Intel(R) PRO/1000 PL Network Connection #2
[0000D000 - 0000DFFF] Intel(R) 82801GR/GH/GHM (ICH7 Family) PCI Express Root Port - 27E2
[0000DF00 - 0000DF1F] Intel(R) PRO/1000 PL Network Connection #6
[0000E000 - 0000EFFF] Intel(R) 82801GR/GH/GHM (ICH7 Family) PCI Express Root Port - 27E0
[0000EF00 - 0000EF1F] Intel(R) PRO/1000 PL Network Connection #5
[0000F500 - 0000F50F] Intel(R) 82801GB/GR/GH (ICH7 Family) Serial ATA Storage Controller - 27C0
[0000F600 - 0000F603] Intel(R) 82801GB/GR/GH (ICH7 Family) Serial ATA Storage Controller - 27C0
[0000F700 - 0000F707] Intel(R) 82801GB/GR/GH (ICH7 Family) Serial ATA Storage Controller - 27C0
[0000F800 - 0000F803] Intel(R) 82801GB/GR/GH (ICH7 Family) Serial ATA Storage Controller - 27C0
[0000F900 - 0000F907] Intel(R) 82801GB/GR/GH (ICH7 Family) Serial ATA Storage Controller - 27C0
[0000FA00 - 0000FA0F] Intel(R) 82801G (ICH7 Family) Ultra ATA Storage Controllers - 27DF
[0000FB00 - 0000FB1F] Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CB
[0000FC00 - 0000FC1F] Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CA
[0000FD00 - 0000FD1F] Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C9
[0000FE00 - 0000FE1F] Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C8
[0000FF00 - 0000FF07] Intel(R) 82945G Express Chipset Family