Little Board™/386SX-IIA

Technical Manual

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Revision: C

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Warning

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REVISION HISTORY

Revision	Reason for Change	Date
1/A	Initial Release	3/96
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PREFACE

This manual is for integrators and programmers of systems based on the Ampro Little Board/386SX-IIA single board system. It contains information on hardware requirements and interconnection, and details of how to program the system.

There are four chapters and one appendix, organized as follows:

Chapter 1—Introduction. General information pertaining to the Little Board/386SX-IIA, its features, and specifications.

Chapter 2—Hardware Configuration. A description of how to configure and connect the Little Board/386SX-IIA for use with a variety of onboard and external devices. Included are tables listing the pinouts of each of the board's connectors, board jumpering, Configuration Memory initialization with the SETUP function, and considerations and specifications regarding peripheral devices.

Chapter 3—Software Configuration. An overview of the system features, configuration options, and utilities that are available under the Disk Operating System (PC-DOS, MS-DOS, or DR DOS), including system setup guidelines.

Chapter 4—Advanced Topics. Detailed technical information on Little Board/386SX-IIA onboard hardware and peripheral interfaces.

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CHAPTER 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The Little Board ™/386SX-IIA is a high performance, 32-bit 80386SX based AT-compatible single board microcomputer system that requires no more space than a half height 5-1/4 inch disk drive. This unique *single board system* is functionally equivalent to an 80386SX AT motherboard and three or four expansion cards. It runs standard IBM/PC and PC/AT software. This includes disk operating systems such as DOS, UNIX, QNX, VRTX, OS9000, FlexOS, and so forth. It also runs languages such as C, Pascal, Fortran, Basic, and industrial and commercial application software.

The Little Board/386SX-IIA is ideal for embedded applications that require PC/AT software, hardware, and bus compatibility. The Little Board/386SX-IIA also features low power consumption, small size, and high reliability over a wide temperature range. The ability to use EPROM, Flash EPROM, or SRAM as solid state disk drives instead of normal disk drives makes it well suited to harsh environments.

Typical applications for the Little Board/386SX-IIA include:

- Data acquisition and control
- Diskless workstations
- Portable instruments
- Remote data logging
- Protocol conversion
- Point-of-sale terminals
- Telecommunications
- Network servers
- Security systems
- Machine control
- Intelligent terminals
- Medical instruments

The board's dimensions are: 5.75 inches x 8 inches x 1.1 inches. It uses a powerful 25 MHz 80386SX microprocessor, with standard DMA, timers, and interrupt controllers. It accepts 512K to 16M bytes of onboard, parity-checked DRAM. It has a full complement of AT compatible controllers including peripheral controllers for serial, parallel, keyboard, speaker, and floppy disk interfacing. There is a PLCC socket for a math coprocessor. The BIOS features Shadow RAM capability for fast execution of ROM BIOS and video BIOS. Three industry standard system expansion options -- a PC/104 Version 2 bus, a Small Computer System Interface (SCSI), and an Integrated Device Electronics (IDE) interface -- enhance system expandability.

You can easily expand the system by stacking Ampro MiniModule™ products on the Little Board/386SX-IIA. They attach directly to the bus interface connector J9. When installed, one onboard MiniModule fits entirely within the board's space envelope. Additional modules increase system thickness by 0.8 inches each. Ampro also offers several methods to add conventional PC and AT expansion cards to the Little Board/386SX-IIA.

The ROM BIOS includes support for SCSI devices. The SCSI BIOS feature allows the use of a variety of hard disks, floppy drives, tape drives, and other SCSI devices. The SCSI BIOS makes system integration, maintenance, and upgrade much easier.

The Little Board/386SX-IIA also provides an interface for one or two Integrated Device Electronics (IDE) hard disk drives. These drives have the hard disk controller built-in. You can easily install an AT hard drive and drive controller by connecting an IDE drive to the IDE interface. Manufacturers offer a large variety of IDE hard disks.

The board provides sockets for EPROM, Flash EPROM or SRAM devices that you can use as one or more bootable DOS compatible Solid State Disk (SSD) drive(s). SSD drives offer improved speed, reliability, and ruggedness, and reduced power consumption and cost compared to conventional magnetic media drives. Ampro's optional SSD support software converts DOS based applications into EPROM format automatically, without special programming. The board has three byte-wide sockets. You can add more with one or more Ampro SSD expansion modules.

Compatibility is a key advantage of the **Little Board/386SX-IIA**. Full AT compatibility allows it to run the thousands of software applications and utility packages developed for the IBM PC and PC/AT. Language compilers, debugging aids, and software support packages for graphics, windowing, multi-tasking, and user interfaces are readily available. There is also a large and growing selection of DOS programs for industrial and commercial applications. These include communications, data acquisition and control, terminal emulation, and protocol conversion, among others.

The Little Board/386SX-IIA is a member of Ampro's growing family of IBM compatible single board systems. The Little Board family offers a broad range of price, performance, and features in a consistent physical and functional format. Thus, as an OEM or system integrator, you can maximize cost effectiveness with Ampro's family of compatible single board systems as the basis of your system design.

1.2 LITTLE BOARD/386SX-IIA FEATURES

A Complete AT Compatible System on One Board.

- All the functions of a motherboard and 3-4 expansion cards in the space of a half-height 5-1/4 inch disk drive
- Runs standard IBM PC and PC/AT software, including:
  --Disk Operating Systems
  --Languages (C, Pascal, Fortran, Basic, . . .)
  --Industrial and commercial application software
- Standard AT DMA, timers, and interrupt controllers
- Complete onboard system memory: 512K, 1M, 2M, 4M, 8M, 10M, or 16M bytes DRAM, and up to 2M bytes of EPROM, 512K of SRAM, or 1.5M of Flash EPROM
- Complete set of AT-compatible peripheral ports and controllers:
  --Floppy controller supports 250K byte and 500K byte/sec 3-1/2 inch and 5-1/4 inch floppy drives
  --Two RS232C serial ports, parallel printer port, keyboard port, and speaker port
  --Battery-backed real time clock
  --IDE hard disk interface
  --SCSI controller and BIOS support for SCSI peripherals including hard disks
- Expansion options:
  --Most popular display controllers: VGA, Super VGA, CRT and flat panel
  --Additional dual-serial/parallel interface
  --Ethernet and Ethernet Twisted Pair LAN interfaces
  --Solid State Disk expansion
  --Future onboard modules available (contact factory)
- Industrialized ROM BIOS, with support for a variety of SCSI devices (hard disk, tape, and so forth) and bootable Solid State Disk

Ideal for Embedded Applications

- Low power (mostly CMOS):
  --Uses only 5 watts of power with 1M byte of DRAM installed
  --Single supply operation (+5V)
- Wide operating temperature range (0-70^{o} C)

- Reliable:
  --Low component count
  --No backplanes or edgecard connectors required
- Onboard bootable Solid State Disk drive (EPROM/NOVRAM/Flash EPROM) option allows diskless DOS operation
- Same form-factor and mounting dimensions as a 5-1/4 inch disk drive
- Two Industry Standard Expansion Buses
  --AT bus (header) for connection of standard IBM PC, PC/AT, and PC/104 expansion cards
  --SCSI bus for addition of Disk/Tape/Optical drives, Scanners, and other peripheral devices

1.3 LITTLE BOARD/386SX-IIA SPECIFICATIONS

CPU

- 25 MHz 80386SX microprocessor
- Socket for 25 MHz math coprocessor

Onboard Memory

- 512K, 1M, 2M, 4M, 8M, 10M or 16M bytes DRAM with parity
- Award ROM BIOS with Ampro extensions (with shadowing capability)
- Three 32-pin byte-wide sockets. Two PLCCs, one DIP.
- Flexible addressing and window size
  PLCC usable with:
  --128K to 1M byte EPROMs
  --32K to 512K Flash EPROMs
  DIP usable with:
  --32K to 1M byte EPROMs
  --32K to 512K byte Flash EPROMs
  --32K to 512K byte SRAMs. Onboard battery makes SRAM storage nonvolatile
- 2K bit serial EEPROM for system parameter storage, with 512 bits for OEM use.

AT-Compatible Controllers

- Standard DMA, interrupt and counter-timer support:
  7 DMA channels
  15 interrupt channels
  3 programmable counter-timers
- Two RS232 serial ports
  16C550-type UARTs
  16 byte FIFO buffers
- Parallel printer port
  8 bidirectional data lines for digital I/O
  IEEE 1284 enhanced mode available
- AT keyboard port
- Speaker port - 100 mW
- Standard battery-backed real time clock and CMOS RAM
- AT-compatible 5-1/4 inch and 3-1/2 inch floppy controller:
  2 drive selects, 1-2 sided, 250/500K byte/sec data rates
  BIOS supports all standard formats (360K /720K /1.2M /1.44M bytes)

Reliable all-digital phase-locked loop and write precompensation
Disk change support

SCSI Interface

- Full ANSI X3.131 (SCSI) compatible
- Uses 53C80 SCSI asynchronous controller
- Up to 400K byte/sec with SCSI BIOS

Physical

- 8.0 x 5.75 x 1.1 inches (5-1/4 disk drive form factor)
- Provision for system expansion with one or more onboard Ampro MiniModules.
- Power required:
  +5V ±5% at 1.07A (1M DRAM)
- 6-layer PCB using latest surface mount technology
- Operating environment:
  --0-70^{o} C (with adequate airflow)
  --5-95% relative humidity (non-condensing)
- Storage temperature: -55^{o} to +85^{o} C
- Weight: 9.6 oz. (272 gm)

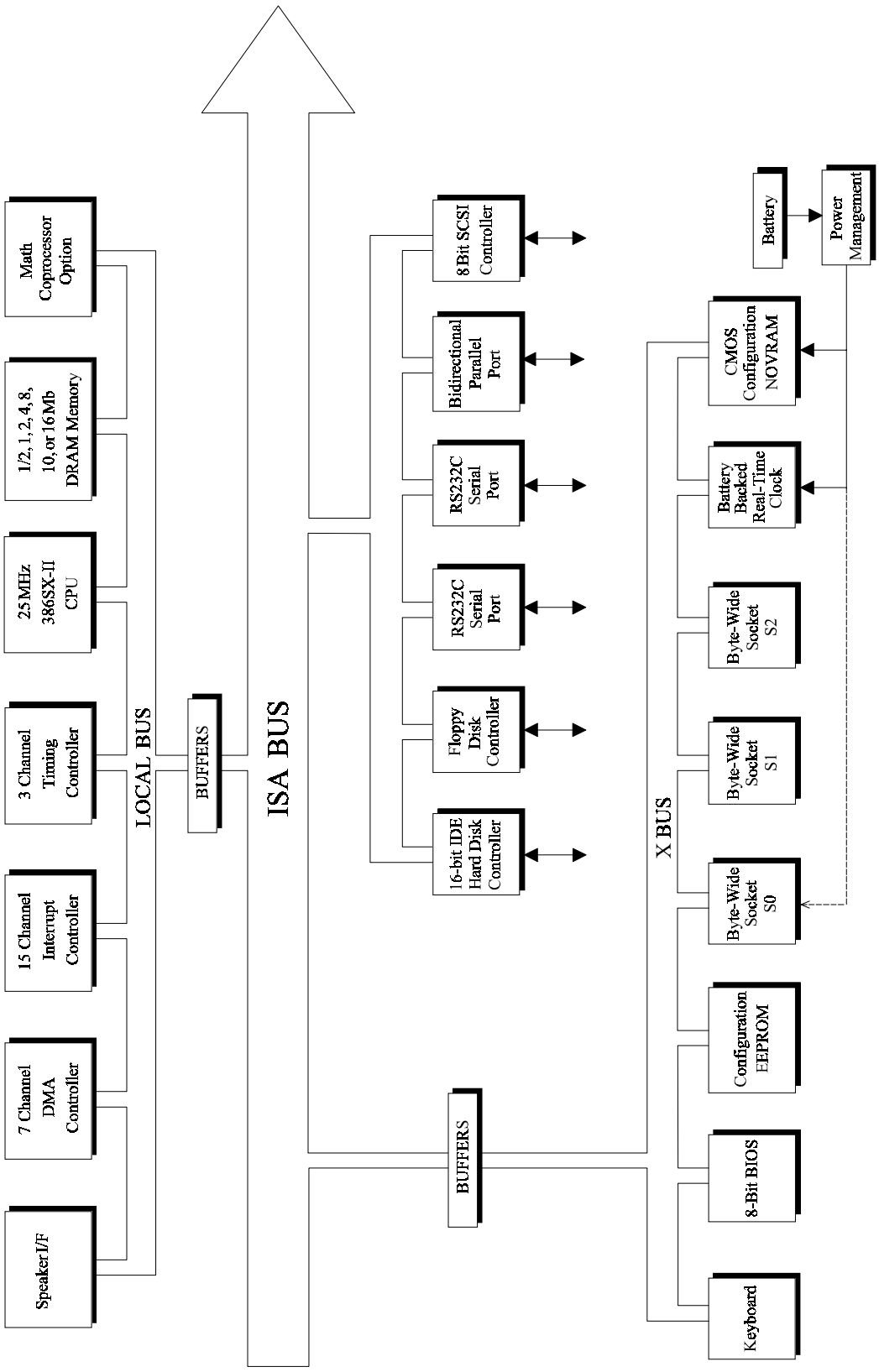


Figure 1-1 Little Board/386SX-IIA Block Diagram

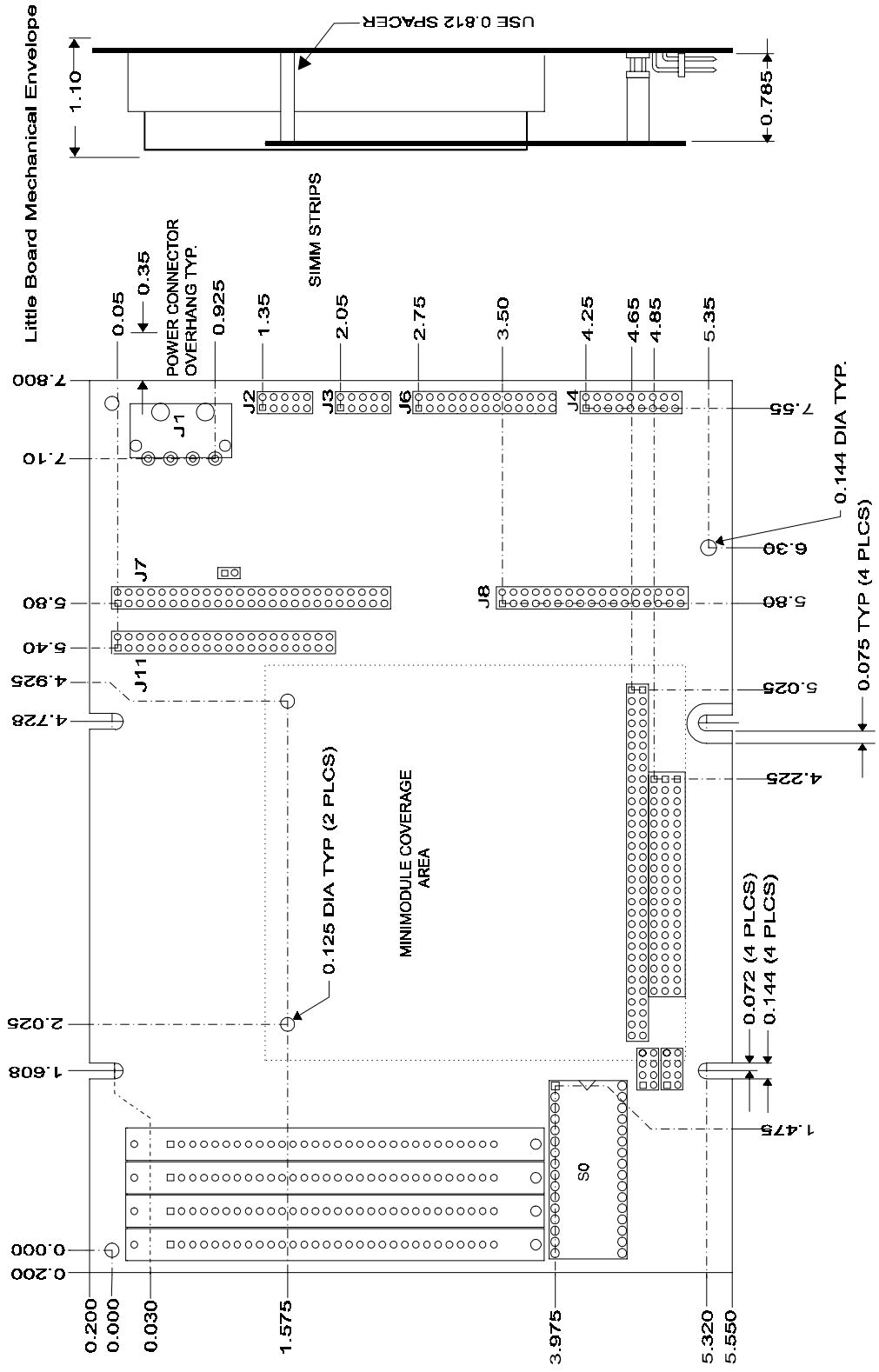


Figure 1-2 Mechanical Dimensions

CHAPTER 2

HARDWARE CONFIGURATION

2.1 INTRODUCTION

This chapter covers configuration of the Little Board/386SX-IIA and its integration with a variety of onboard and peripheral devices. Standard onboard functions include DRAM, battery-backed real-time clock, and CPU speed control. Options include a math coprocessor socket, three byte-wide device sockets, and onboard expansion capability, including the Ampro MiniModules. Many of the board's functions are software controlled. This manual presumes use of the standard Ampro ROM BIOS. Peripheral devices include keyboards, monitors, printers, modems, floppy and hard disk drives, and other peripherals. It includes data on the board's connector signals and pinouts, external device requirements, interconnection cable wiring, and board configuration.

2.1.1 Interface Connectors

Figure 2-1 shows the location of the interface connectors (J1-J11) and configuration jumpers (W1-W25). Table 2-1 summarizes the use of the connectors. The sections on each interface give connector pinouts, signal definitions, and mating connector part numbers.

Many of the connectors have a key pin removed. Block the corresponding socket to minimize the chance of misaligning the connector. Table 2-1 lists key pins, and Figure 2-1 shows their locations.

CONNECTOR	FUNCTION	SIZE	KEY PIN
J1	Power input	4-pin	none
J2	Secondary serial port	10-pin	10
J3	Primary serial port	10-pin	10
J4 (*)	Utility	12-pin	none
J5 (*)	Keyboard	6-pin	none
J6	Parallel port	26-pin	26
J7	SCSI port	50-pin	25
J8	Floppy drive	34-pin	6
P1A, P1B	AT Bus	64-pin	B10
P2C, P2D	AT Bus	40-pin	C19
J11	IDE drive interface	40-pin	20
(*) A single 18-pin array comprises J4 and J5			

Table 2-1. Connector Usage Summary

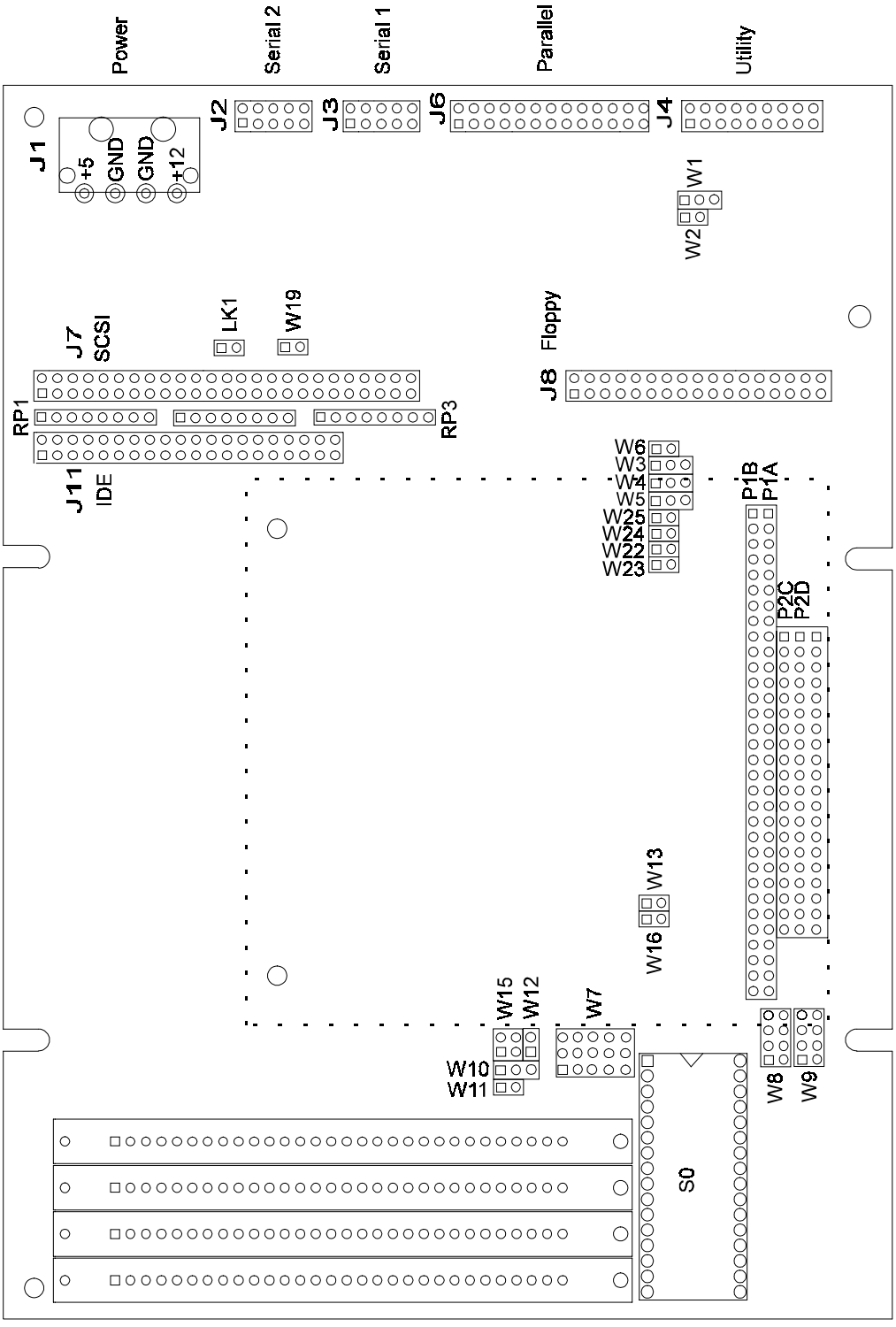


Figure 2-1 Connector and Jumper Locations

The I/O connectors are dual-row headers for use with flat ribbon (IDC) or discretely wired connectors. You can use a specialized connector or PC board assembly. You might do this to eliminate cables, meet packaging requirements, add EMI filtering, or customize your installation in other ways. The PC/AT expansion bus appears on two connectors (J9 and J10). You can expand the system with onboard MiniModules, or use conventional or custom expansion hardware, including solutions available from Ampro.

2.1.2 Jumper Configuration Options

The Little Board/386SX-IIA requires no special jumpering for standard AT operation. You can connect the peripherals and operate it immediately. The only jumpers you need be concerned with are those that configure the byte-wide sockets for the devices you use.

The jumper arrays are designated W1, W2, and so forth. A square solder pad identifies pin 1 of each array. Table 2-2 is a summary of jumper use. A slash (1/2) means to short the indicated pins.

JUMPER GROUP	FUNCTION	DEFAULT
W1	Watchdog Timer output selection	OFF
W2	Power Fail NMI enable	OFF
W3	EPP/ECP DACK* select	OFF
W4	EPP/ECP DRQ select	OFF
W5	Parallel Port IRQ selection (IRQ7)	1/2
W6	Floppy Drive DRQ2 enable	ON
W7	Byte-wide S0 config. (128K SRAM)	4/5, 7/10, 8/11, 13/14
W8	Byte-wide S1 config. (+12V Flash)	3/4, 5/6
W9	Byte-wide S2 config. (+12V Flash)	3/4, 5/6
W10	Battery backed S0 (no backup)	2/3
W11	Battery backed S0 (no battery)	OFF
W12	SCSI enable	ON
W13	+12V Flash programming power	OFF
W15	BIOS Chip selection (U24/U28 BIOS)	1/2, 3/4
W16	BIOS Vpp enable	OFF
W19	SCSI Terminator power	OFF
W22	SCSI Terminal Count	OFF
W23	SCSI DRQ3	ON
W24	SCSI DACK3*	ON
W25	SCSI IRQ5	OFF

Table 2-2. Configuration Jumper Summary

2.1.3 SETUP Options

To configure the board, install the appropriate jumpers, and run SETUP. The SETUP function, included in the ROM BIOS and on the Little Board/386SX-IIA Utilities diskette, stores the configuration parameters in a 2 Kbit nonvolatile EEPROM and in the battery backed CMOS RAM in the real time clock. These two memories comprise the Configuration Memory. During the boot process, the ROM BIOS initializes system parameters based on the contents of these memories. The contents of the CMOS RAM (except time and date) are also stored in the EEPROM. Even without battery power, the SETUP parameters are saved.

You can enter SETUP two ways. One is a hot-key entry (pressing CTRL-ALT-ESC at the same time) just prior to boot. The other is through SETUP.COM, a program on the utilities diskette. You can initiate SETUP from the command line by entering SETUP <ENTER> with the utilities diskette in the default floppy drive. Use of SETUP is covered in detail in Chapter 3.

Table 2-3 lists the user accessible functions controlled by the Configuration Memory.

• DOS date and time	• Floppy drive quantity and type
• Hard disk drive quantity and type	• Video controller mode and type
• Memory size and configuration	• Halt on errors option
• BIOS and video BIOS shadowing	• CPU speed options
• Enable/Disable Ampro extended BIOS	• Enable/disable serial ports
• Enable/Disable parallel port	• Enable/disable floppy interface
• Enable/Disable IDE interface	• Mono/color video jumper
• Byte-wide socket sizes and locations	• Byte-wide default at power up
• Enable/disable serial boot loader	• Watchdog timer timeout selection
• Enable/disable hot-key SETUP function	• Enable/disable SCSI hard disk services
• Hard disk DOS mapping	• Default boot device selection
• Extended Serial Console configuration	• Serial Console installation

Table 2-3. SETUP Options

Using the SETUP program, you can load system setup parameters from a disk file. This is useful when configuring production systems.

2.2 DC POWER

The pinout of the power connector, J1, is identical with the power connectors on almost all 5-1/4 inch disk drives. See Figure 2-1 and Figure 2-2. Refer to Table 2-4 for power connections and mating connector information, and Figure 2-2 for typical connector wiring.

CAUTION

Be sure the power plug is wired correctly before applying power to the board! See Figure 2-2.

PIN	SIGNAL	FUNCTION
1	+12VDC	+12VDC ±5%
2	Ground	Ground return
3	Ground	Ground return
4	+5VDC	+5VDC ±5% input

Table 2-4. Power Connector (J1)

CONNECTOR TYPE	MATING CONNECTOR
DISCRETE WIRE	AMP HOUSING 1-480424-0 AMP PIN 60619-1

Table 2-5. J1 Mating Connector

2.2.1 Power Requirements

The Little Board/386SX-IIA requires only +5 VDC (±5%) for operation. The ±9 volts for the RS232 ports is generated onboard. However, if you use +12 volt Flash EPROMS, you must supply them with 12 volts during programming. Consult the documentation for your Flash EPROMs for their programming current and voltage requirements.

The exact power requirements of the Little Board/386SX-IIA depend on several factors: the functions present on the board (quantity of DRAM, byte-wide memory devices, math coprocessor); SCSI bus termination; CPU speed; and the peripherals connected. For example, AT keyboards draw their power from the board. MiniModules or other expansion products connected to the AT expansion bus may draw their power through the Little Board/386SX-IIA power connector. A fully populated Little Board/386SX-IIA with 1 Mbyte DRAM, but with no math coprocessor or expansion modules installed, draws about 1.07 Amp (5.35 watts). The SCSI bus terminators draw about 800 milliwatts. Remove them unless you use the SCSI port.

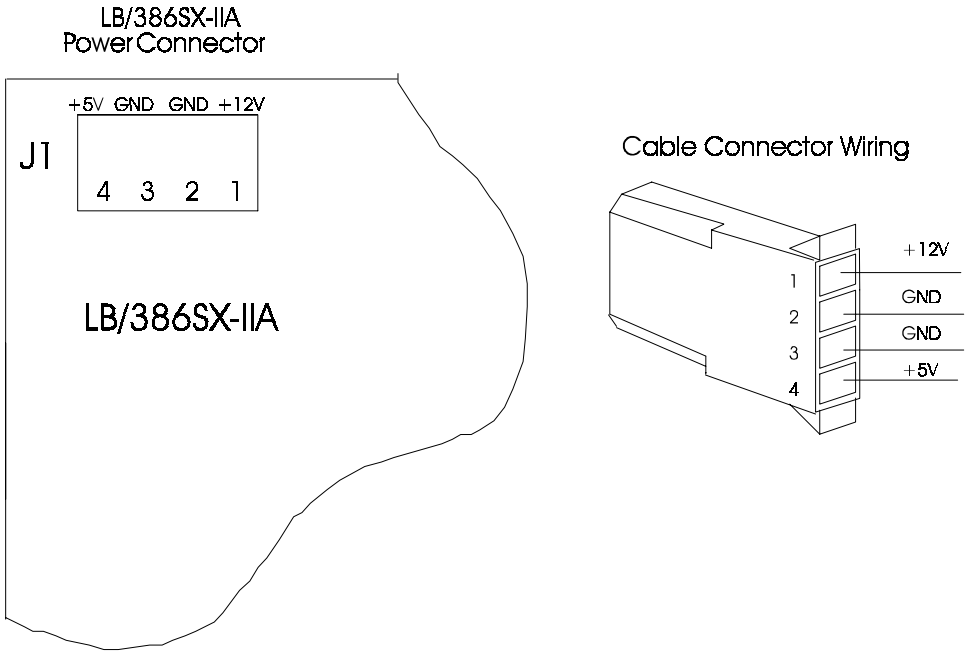


Figure 2-2 Power Connector Wiring

If you use a switching power supply, be sure it regulates properly with this load. If not, consult the manufacturer about additional loading, or use a linear power supply or batteries.

2.2.2 Powerfail Options

The Little Board/386SX-IIA includes power failure monitoring. Configuring the board for the power failure options involves jumper arrays W2 and W11. If you short W2, the powerfail circuitry is enabled. When the supply voltage falls below 4.7 volts, the logic produces a non-maskable interrupt (NMI). The BIOS detects the NMI and displays the message "Power Fail NMI" on the screen. You have two options at this point. One is to mask the NMI and continue. The other is to reboot the system. If you want another response to the NMI, provide your own NMI handler and patch the NMI interrupt vector address to install it. This is covered in Chapter 4. If you don't want the power fail NMI, leave W2 open.

If the supply voltage falls below 4.5 volts, the logic initiates a hardware reset (the same as if the Reset button were pressed). This reset remains asserted for about 100 mS after the voltage returns to above 4.5 volts.

Jumper arrays W10 and W11 determine whether backup battery power is routed to byte-wide socket S0 during a power failure. To enable Battery Backup, set jumpers W10 (1/2) and W11 ON. To disable Battery Backup set W10 (2/3) and W11 OFF. With the first jumper setting (with jumper W11 ON and W10 (1/2)), the power monitor circuit switches the power supply for byte-wide socket S0 from the +5 volt power supply (Vcc) to the backup battery. This effectively makes an SRAM in S0 into non-volatile RAM (NOVRAM). However, if you use an EPROM or Flash EPROM in S0, set W11 to OFF and W10 (2/3). With this setting the power supply to S0 is always Vcc, and battery power is not wasted.

While Battery Backup is enabled, the chip select for S0 is held off while power is below 4.7 volts. This is to prevent writing bad data to S0 when the voltage is low.

2.2.3 Backup Lithium Battery Considerations

CAUTION

Lithium batteries can explode if mistreated. Do not attempt to recharge a Lithium battery. See manufacturers instructions for proper disposal of used batteries. Be careful not to overheat the battery when changing it.

With only the real time clock drawing current, this battery should last 10 years. If it supplies only the clock, replace the battery every ten years as a routine maintenance procedure.

If the battery supports an SRAM, calculate battery life and replace the battery as necessary. To calculate battery life, add the current drawn by the SRAM and the current the clock draws (1 uA) and divide the 750 milliamp-hour battery rating by the sum. Then, multiply the result of that calculation by the duty cycle of the battery, that is, the percentage of time the system is off and the battery is supplying the current.

Here is the formula for calculating battery life:

$$\frac{750 \text{ milliamp - hours}}{1\mu A + \text{SRAM backup current}} \times \text{Duty Cycle}$$

2.2.4 Cooling Requirements

Although this is a low power system, it is important to provide adequate air flow for cooling. If you use a math coprocessor, system cooling becomes even more important. The CPU, DRAM, and math coprocessor draw most of the power and generates most of the heat.

2.3 ONBOARD DEVICE OPTIONS AND CONFIGURATION

This section includes the configuration and installation of onboard devices and options including the DRAM and the byte-wide memory devices, the math coprocessor, the serial ports, the parallel port and the floppy, SCSI, and IDE controllers. It includes system expansion with MiniModules and conventional expansion boards.

2.3.1 DRAM

The board has positions for four single in-line memory modules (SIMMs). You need not install memory in all four positions. Use either 256 Kb x 9, 1 Mb x 9, or 4 Mb x 9 SIMM modules, depending on the amount of memory desired. Table 2-6 gives possible DRAM configurations.

NOTE

System performance depends on DRAM configuration. For maximum speed, install enough DRAM for shadowing.

One way to improve system performance is to use shadowing. When the system operates directly from ROM, it accesses an 8-bit device at 8 MHz. Shadowing is the copying of the ROM contents to RAM where they are accessed as 16-bit wide data and at normal system speed. Shadowing the system BIOS or the video BIOS substantially enhances system performance. Shadowing is possible with 1M byte of onboard DRAM or more. See Table 2-6 for a summary of memory configuration.

MEMORY SIZE	BANK 0 (U1/2) SIMMs	BANK 1 (U3/4) SIMMs	SHADOW
512 K	256 K	None	No
1 M	256 K	256 K	Yes
2 M	1 M	None	Yes
4 M	1 M	1 M	Yes
8 M	4 M	None	Yes
16 M	4 M	4 M	Yes
All memory must have access times of 70 nS or less			

Table 2-6. DRAM Configurations

The Little Board/386SX-IIA can directly address 16M bytes of system RAM. This is limited by the microprocessor and the PC/AT bus specification. You can locate memory on the board or on the AT expansion bus. In most cases it is preferable to add onboard memory with SIMMs. This is because access to RAM located on the bus is slower than the onboard memory due to memory configuration and to the wait states added to bus operations.

Onboard memory is allocated as follows:

In a 512K byte system, all the memory is mapped to the DOS region 00000h to 7FFFFh.

In larger systems, the first 640K bytes of DRAM are assigned to the DOS region 00000h to 9FFFFh, leaving 384K bytes of the first 1M byte unused. You can *only* use that 384K bytes to shadow ROM BIOS and video BIOS.

The remaining memory is mapped to extended memory starting at the 1 megabyte boundary, 100000h.

The BIOS measures the amount of memory installed and displays it on the first page of SETUP. Saving SETUP automatically saves the amount of memory in the Configuration Memory. If you change the amount of memory installed, you must run SETUP again to save the new information in the Configuration Memory.

Some programs are designed to use *expanded* or *EMS* memory. You can convert extended memory into expanded memory. MS-DOS and DR DOS include utilities that conform to the LIM 4.0 specification for EMS memory.

2.3.2 Math Coprocessor

You can install an 80387SX or equivalent floating point math coprocessor in U6. The coprocessor must be rated for the same speed as the CPU. The coprocessor operates in synchronous mode, using the same clock as the CPU. A 25 MHz 80387SX may be used

NOTE

Some math coprocessors dissipate up to 1 watt. Be sure to provide adequate clearance for air flow. The coprocessor socket and the silkscreening show how to install the coprocessor. Be careful to align the device correctly to prevent damage.

2.3.3 Byte-Wide Sockets

The Little Board/386SX-IIA has three onboard byte-wide memory sockets. One is a 32-pin DIP, and the other two are 32-pin PLCC (Plastic Leaded Chip Carrier) sockets. All of these sockets accept a variety of EPROM and Flash EPROM devices. The DIP socket (S0) also accepts SRAMs and nonvolatile RAM (NOVRAM) devices. You can make an SRAM in S0 non-volatile with the connection of battery backup power by shorting W11-2/3. You can use these devices for simple program storage, BIOS extensions, or as Solid State Disk (SSD) drives. Table 2-7 shows some byte-wide devices and in which sockets you can use them.

You can use either 28- or 32-pin devices in S0. If you use a 28-pin device, install it so device pin 1 is in socket pin 3 and so forth. See Figure 2-3.

NOTE

When a byte-wide device is enabled, the memory address space it uses is unavailable for other devices. You must disable the byte-wide sockets in SETUP before you can use the memory space for other purposes.

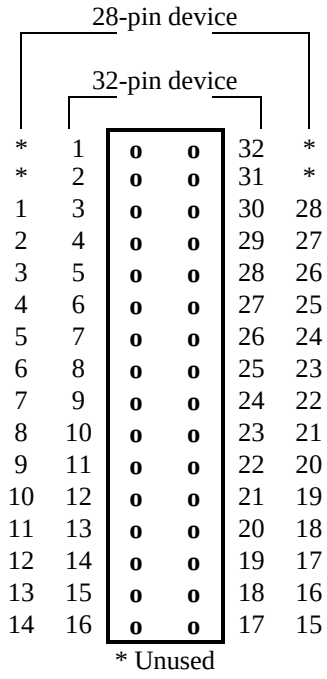


Figure 2-3 Using a 28-Pin Device in a 32-Pin Socket

DEVICE TYPE	SIZE	PART NUMBER	USABLE IN
NORMAL EPROMS			
EPROM32	32 Kbyte	27C256	S0
EPROM64	64 Kbyte	27C512	S0
EPROM128	128 Kbyte	27C010	S0, S1, S2
EPROM256	256 Kbyte	27C020	S0, S1, S2
EPROM512	512 Kbyte	27C040	S0
EPROM1024	1024 Kbyte	27C080	S0
PAGE ADDRESSED EPROMS			
PPROM64	64 Kbytes	27513	S0
STATIC RAMS			
SRAM32	32 Kbytes	43256	S0
SRAM128	128 Kbytes	628128	S0
SRAM512	512 Kbytes	434000	S0
FLASH EPROMS			
EPROM128	128 Kbytes	28F010	S0, S1, S2
EPROM256	256 Kbytes	28F020	S0, S1, S2

Maximum access time for byte-wide devices is 250 nS.

Table 2-7. Typical Byte-wide Devices

After installing the devices, use SETUP to specify the size and starting address of each one, and which device the BIOS enables upon system initialization. Table 2-8 gives the possible sizes and address ranges for the byte-wide devices.

Direct Program Access

Application software can access the memory devices in S0, S1 and S2 if the program knows about them. To access a byte-wide socket you must enable it individually with a BIOS call to access the device. See Chapter 4 for more details on this BIOS call.

WINDOW	ADDRESS
DISABLE	N/A
64K	D0000-DFFFFh
64K	E0000-EFFFFh
128K	D0000-EFFFFh

Table 2-8. Window Size and Address Selection

The system can run its entire application from memories in the byte-wide sockets, instead of from disk drives. This technique, known as a ROM BIOS extension, is discussed in Ampro Application Note AAN-8702.

Using the byte-wide sockets can adversely affect system performance. The system can only access one byte-wide device at a time. Also, byte-wide devices are slow as it is operation from 8-bit memory at slow speed. You can improve performance substantially by copying the ROM contents to RAM and running the software directly from RAM.

Solid State Disk (SSD) Drives

Using the Ampro Solid State Disk (SSD) Support Software, you can configure a Little Board/386SX-IIA system to boot, operate, and store data using one or more EPROM and/or SRAM solid-state drives under DOS control. You need no custom programming. With the Ampro SSD support software, the byte-wide sockets can serve as individual SSD drives, or a single larger drive. You can use SSD drives in addition to, or instead of normal floppy and hard disk drives. You can increase system SSD capacity by adding one or more of Ampro's SSD expansion modules.

Byte-Wide Socket Configuration

You must jumper the byte-wide sockets for the devices you install in them. Jumper arrays W7, W10, and W11 configure S0. Array W8 configures S1. Array W9 configures S2. Figures 2-4 to 2-8 list supported memory devices and their jumper settings. See Chapter 4 for a description of the byte-wide socket signals that correspond to each jumper pin. Besides jumpering each socket, you must use SETUP to select which one the BIOS will enable on power up.

2.3.4 Battery-Backed Clock

An AT compatible battery-backed real time clock (with CMOS RAM) is standard on the Little Board/386SX-IIA. The clock is powered by a 3.6 volt 1/2 AA Lithium battery soldered to the board. The battery is rated at 750 milliamp-hours. As the clock draws about 5 uA, this battery will support the clock for over ten years.

The factory initializes the real time clock date and time and various parameters in the Configuration Memory for a standard configuration. The factory also sets the date and time, but it may not be set for your time zone. Use the Ampro SETUP utility to change these values as needed (see Chapter 3).

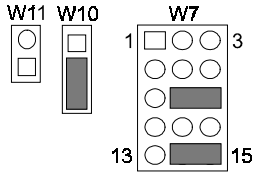
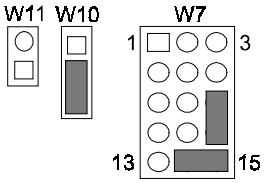
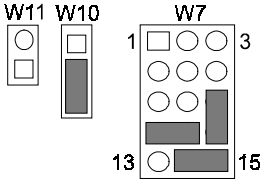
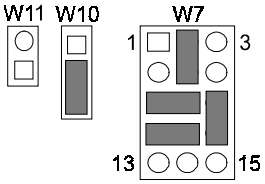
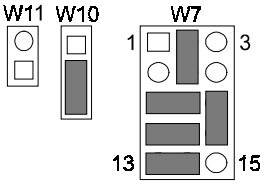
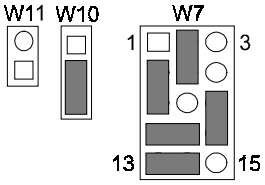
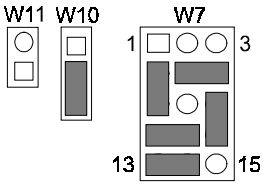
EPROM (Typical Devices)	Pins	Jumper Diagram
8K EPROM 27C64 16K EPROM 27C128 8K EEPROM 28C64	28	
32K EPROM 27C256	28	
64K EPROM 27C512	28	
128K EPROM 27C010	32	
256K EPROM 27C020	32	
512K EPROM 27C040	32	
1M EPROM 27C080	32	
NOTE: W10 and W11 configure S0 only.		

Figure 2-4 EPROM Jumpering for S0

2.3.5 Using Flash EPROMs

Flash programming power for +12V Flash devices is provided by the external power supply. You need to insure that the +12V supply meets the voltage specifications for programming the +12V Flash device. Programming power is switched under software control so that it is applied only during the actual programming process (to prevent accidental corruption of the data). A utility for programming supported Flash devices is included on the utility disk that is provided with the LB/386SX-II Development Kit.

Some Flash EPROMs draw current through their chip select lines (or other pins) when powered down. If you install a Flash EPROM in socket S0, make sure the jumper on W11 is removed and the jumper on W10 is on 2/3 to prevent premature discharge of the on-board backup battery.

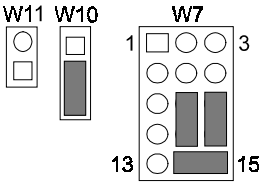
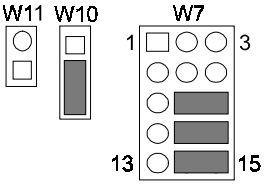
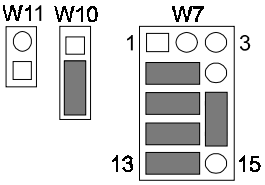
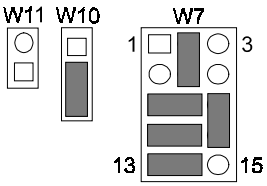
Flash EPROM Typical Devices	Pins	Jumper Diagram
32K 5V Flash EPROM 29C256	28	
32K 5V Flash EPROM 28C256	28	
64K 5V Flash EPROM 29F512 128K 5V Flash EPROM 29F010 256K 5V Flash EPROM 29F020 512K 5V Flash EPROM 29F040	32	
32K 12V Flash EPROM 28F256 64K 12V Flash EPROM 28F512 128K 12V Flash EPROM 28F010 256K 12V Flash EPROM 28F020	32	
NOTE: W10 and W11 configure S0 only.		

Figure 2-5 Flash EPROM Jumpering for S0

2.3.6 Using SRAMs

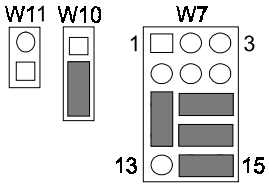
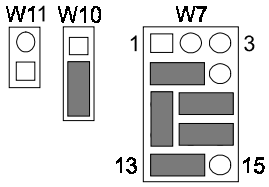
If you install an SRAM in socket S0, you can provide backup power from the battery when power is off by shorting W11 and W10-1/2.

Battery backup is provided for S0 only.

The external battery power is combined with the internal battery using low forward voltage drop Schottky diodes. The 750 milliamp-hour battery provides sufficient current for the onboard real-time clock for a 10 year life, but if you are going to battery-back-up a device in S0, Ampro recommends that you calculate the battery lifetime.

Note

Some byte-wide devices draw battery backup current through their chip select lines when power is off. When using memory devices that do not require battery backup power, remove the jumper on W11 and set W10 to 2/3. This prevents the backup battery from being drained prematurely.

SRAM Typical Devices			Pins	Jumper Diagram
32K SRAM	43256		28	
32K NOVRAM	Dallas	DS1235Y	32	
	Benchmarq	BQ4013Y		
128K SRAM	628128		32	
512K SRAM	628512			
512K NOVRAM	Dallas	DS1650Y		
	Benchmarq	BQ4015Y		

NOTE: W11 and W10 are shown configured for NOVRAMs. To configure W11 and W10 for SRAM battery backup (on S0), install a jumper on W11 and move the jumper on W10 to 1/2. See text for details.

Figure 2-6 SRAM and NOVRAM Jumpering for S0

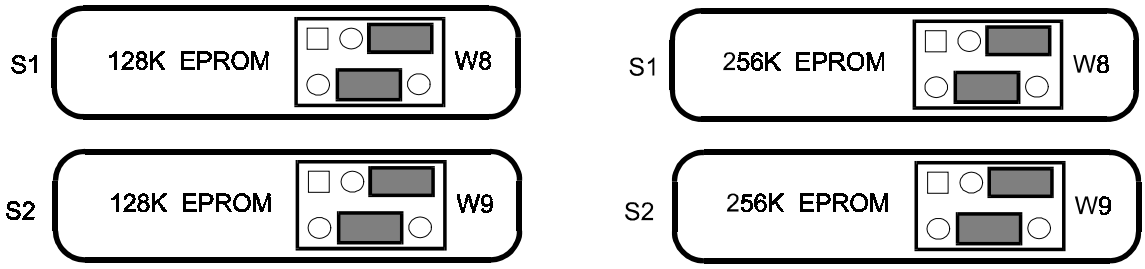


Figure 2-7 EPROM Jumpering for S1 and S2

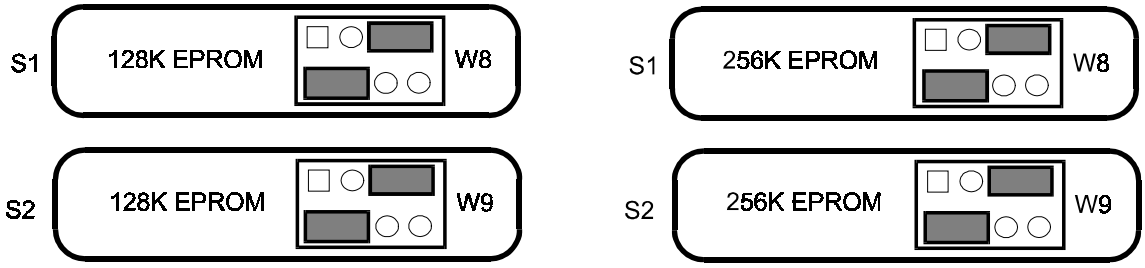


Figure 2-8 Flash EPROM Jumpering for S1 and S2

2.3.7 Watchdog Timer Option

A unique feature of the onboard clock circuitry is a watchdog timer. You can program this timer to generate an interrupt or reset signal if the programmed time interval expires before the timer is reinitialized. Use SETUP to select the time interval. The options are: Disable, 30 seconds, 60 seconds, and 90 seconds.

The watchdog timer will not work while the system is booting either PC DOS or MS DOS. However, the WATCHDOG utility provided will work normally once the system is booted. Use DR DOS if you require the watchdog timer to operate while the system is booting.

The watchdog timer uses the standard alarm feature of the real time clock. In a standard AT, the alarm output is connected to IRQ8. On the Little Board/386SX-IIA you can connect the alarm output to I/O Channel Check (-IOCHCK) or Reset with W1. I/O Channel Check is the bus signal that triggers a non-maskable interrupt (NMI). Reset is a hard reset signal, the same as pressing the Reset button. For the watchdog timer to generate I/O Channel Check, short W1-1/2. For Reset, short W1-2/3. To disable the watchdog timer, leave W1 open, and select *Disable* in SETUP. See Table 2-9.

If you enable the Watchdog timer in SETUP, but do not install a jumper on W1, IRQ8 turns off the interrupt and the system is unaffected. If you select I/O Channel Check, the timer will generate a message on the screen. If you select Reset, no interrupt handler is required.

SELECTION	W1
Disabled	Open
-IOCHCK	1/2
RESET	2/3

Table 2-9. Watchdog Timer Configuration

2.3.8 Video Display Mode

No matter what type of video controller you use -- an onboard MiniModule or a board on the AT expansion bus -- you have to use SETUP to establish the powerup (or reset) video state as color or monochrome. Table 2-10 shows which setting to use for various video modes.

VIDEO MODE	SETUP OPTIONS	
	VIDEO	MONO/COLOR JUMPER
Mono (MDA or Hercules)	MONO	MONO
Mono (EGA, or VGA)	EGA/VGA	COLOR
Color (CGA, EGA, or VGA)	COLOR 40	COLOR
	COLOR 80	
	EGA/VGA	

Table 2-10. Video Mode Options

When using an EGA or VGA controller for monochrome, set the MONO/COLOR Jumper on the second SETUP screen to "COLOR". When using an EGA or VGA controller in monochrome or CGA mode, set the video controller type on the first SETUP screen to "EGA/VGA".

Be sure to set any appropriate switches or jumpers on the video display controller for the video mode you use. Refer to your video controller's technical manual.

2.4 PERIPHERAL CONNECTIONS AND CONFIGURATION

This section covers the interface requirements of the external devices. It provides information on interface and device characteristics, connector pinouts, mating connector part numbers, signal definitions, jumper configuration, and Configuration Memory setup.

2.4.1 Utility Connector

Five functions appear on a single 12 pin connector at J4. These are the speaker, external Reset, Power Indicator LED, auxiliary power connections, and a Power Good status input signal. Table 2-11 shows the pinout and signal definitions of the Utility Connector. Connectors J4 and J5 appear on a single 18-pin header array to facilitate use of a single connector for both.

PIN	SIGNAL NAME	FUNCTION
1	Speaker +	Audio signal
2	Speaker -	Ground
3	Ground	To one side of Reset button
4	Reset	To other side of Reset button
5	LED Cathode	Ground return
6	LED Anode	Current source (+5V through 330 ohms)
7	Ground	Ground return
8	+12V power	Connected to J9 pin B9
9	-5V power	Connected to J9 pin B5
10	-12V power	Connected to J9 pin B7
11	Ground	Ground return
12	POWERGOOD	Power supply status

Table 2-11. Utility Connector (J4)

CONNECTOR TYPE	MATING CONNECTOR
RIBBON	3M 3473-7010
DISCRETE WIRE	MOLEX HOUSING 22-55-2101 PIN 16-02-0103

Table 2-12. J4 and J5 Mating Connector

Speaker

The board supplies about 100 milliwatts for a speaker on pins 1 and 2 of the Utility Connector. A transistor amplifier buffers the speaker signal. Use a small general purpose 2 or 3 inch permanent magnet speaker with an 8 ohm voice coil. Refer to an AT technical reference manual for custom speaker programming information.

Pushbutton Reset

Two pins (3 and 4) of the Utility Connector provide connections for an external normally open momentary switch to manually reset the system. Pin 4 is the Reset (active low) input, and pin 3 is the logic ground.

Power Indicator LED

Two pins (5 and 6) of the Utility Connector provide connections for an external power indicator LED. This output sources 15 mA (+5V through 330 ohms). Pin 5 goes to the LED's cathode and pin 6 to its anode.

AT Bus Power Options

You can use 4 pins (7, 8, 9, and 10) of the Utility Connector in two ways. You can connect +12V, -5V, and -12V to them to supply power to the board instead of using J1. Or you can power the board from J1 and use these pins to source power to plug-in expansion cards, or other devices in the system.

2.4.2 Keyboard

You can connect an AT (*not* PC) keyboard to the keyboard port. The first five pins (1-5) of connector J5 provide this function. Normally, AT keyboards include a cable that terminates in a male 5-pin DIN plug for

connection to an AT. Table 2-13 gives the keyboard connector pinout and signal definitions, and includes corresponding pin numbers of a normal AT DIN keyboard connector.

You can connect pin 6 of J5 to a keyboard inhibit switch. If you ground this pin, the system ignores keyboard inputs. You can use this with key switches for system security.

J5 PIN	SIGNAL NAME	DIN PIN
1	Keyboard clock	1
2	Keyboard data	2
3	Key pin	N/A
4	Ground	4
5	Keyboard power	5
6	Keyboard inhibit	N/A

Table 2-13. Keyboard Connector (J5)

2.4.3 Parallel Port

The Little Board/386SX-IIA includes an AT compatible parallel port at J6. Table 2-14 gives this connector's pinout and signal definitions. You can use a flat ribbon cable between the header and a female DB25 connector. The table also gives the connections from the header pins to the DB25 connector.

You can use the parallel port either as a standard PC/AT printer port, or as a bidirectional data bus. Refer to Chapter 4 for information on bidirectional use of this port.

NOTE

For maximum reliability, keep the cable between the board and the device it drives to 10 feet or less in length.

SIGNAL NAME	FUNCTION	IN/OUT	J6 PIN	DB25 PIN	Drive (mA) (LOW/HIGH)
Data 0	LSB of printer data	I/O	3	2	
Data 1	:	I/O	5	3	
Data 2	:	I/O	7	4	
Data 3	:	I/O	9	5	24/12
Data 4	:	I/O	11	6	
Data 5	:	I/O	13	7	
Data 6	:	I/O	15	8	
Data 7	MSB of printer data	I/O	17	9	
-ERROR	Printer error	IN	4	15	
SEL OUT	Printer selected	IN	25	13	
PAPER	Out of paper	IN	23	12	N/A
-ACK	Character accepted	IN	19	10	
BUSY	Cannot receive data	IN	21	11	
-STROBE	Output data strobe	OUT	1	1	
-AUTOFD	Autofeed	OUT	2	14	24/0.5
-INIT	Initialize printer	OUT	6	16	
-SEL IN	Selects printer	OUT	8	17	
N/A	Key pin	N/A	26		
GROUND	Signal ground	N/A	10,12, 14,16, 18,20, 22,24	18-25	N/A

Table 2-14. Parallel Port Connector (J6)

CONNECTOR TYPE	MATING CONNECTOR
RIBBON	3M 3473-7010
DISCRETE WIRE	MOLEX HOUSING 22-55-2101 PIN 16-02-0103

Table 2-15. J6 Mating Connector

Printer Port Configuration

With SETUP, you can configure the parallel port as the primary port (LPT1), the secondary port (LPT2), or disabled. Table 2-16 lists the parallel port addresses for the primary and secondary port.

SELECTION	I/O ADDR.
Primary	378-37Fh
Secondary	278-27Fh

Table 2-16. Parallel Port Address Configuration

Normally, DOS assigns the name LPT1 to the primary parallel port, and LPT2 to the secondary parallel port (if present). However, DOS scans for both choices (primary and secondary) and if it only finds a secondary port, it assigns LPT1 to that one. Configure the parallel port for the primary assignment shown in Table 2-16, unless the system includes another primary parallel port.

Parallel Port Interrupt

Interrupts are seldom used with parallel ports. When they are, the convention is to use IRQ7 with the primary port (LPT1) and IRQ5 with the secondary port (LPT2). You can select the interrupt with W24. Table 2-17 shows the options.

SELECTION	W5
No Interrupt	OPEN
IRQ5	2/3
IRQ7	1/2

Table 2-17. Parallel Port Interrupt Selection

Bidirectional Parallel Port Use

You can use the parallel printer port as a standard AT printer port, or you can use it for general purpose programmable I/O. You can create interfaces for specialized devices with the port's input and output handshake signals, and its 8-bit bidirectional data lines. You might use it for writing data to LCD display panels, scanning custom keyboards, and so forth.

The bidirectional feature is controlled by software. Refer to Chapter 3 for typical system software configuration information, and to Chapter 4 for hardware details regarding nonstandard uses of this interface.

IEEE 1284 Mode Use

You can set the parallel port to EPP or ECP mode. Jumpers W3 and W4 select the DMA channel. To select DMA channel 1 set jumpers W3 and W4 to (1/2). To select DMA channel 3 set the jumpers to (2/3)

2.4.4 Serial Ports

The Little Board/386SX-IIA provides two standard RS232 serial ports at J2 and J3. Table 2-18 gives the connector pinout and signal definitions for J2 and J3. In addition, the table gives the pins each signal must be wired to for compatibility with DB25 and DB9 connectors. The serial port pinout is arranged so that you can use a flat ribbon cable between the header and a standard DB9 connector. Normally PC serial ports use male DB connectors.

Both ports support software selectable standard baud rates up to 19.2K bits/second (limited by the RS232C specification), 5-8 data bits, and 1, 1.5, or 2 stop bits. The serial ports appear at the standard port addresses of 3F8-3FFh (primary port) and 2F8-2FFh (secondary port), using interrupts IRQ4 and IRQ3, respectively.

You can use the serial ports for printers, modems, terminals, remote hosts, or other RS232C serial devices. Many devices, such as printers and modems, require handshaking in one or both directions. Consult the documentation for the device(s) you use for information about handshaking and other interface considerations.

Unique to Ampro is ROM BIOS support for using a serial console (keyboard and display) in place of the conventional video controller, monitor, and keyboard. See Chapter 3 for details about the serial console option.

Connector J3 is the primary serial port. The ROM BIOS supports it as the DOS COM1 device. The secondary serial port is J2. The ROM BIOS supports it as the COM2 device. It is possible to disable either or both serial ports with SETUP. If you disable the primary port and enable the secondary port, and there is no other primary port in the system, then the secondary port is installed as COM1 by DOS.

PIN	SIGNAL NAME	FUNCTION	IN/OUT	DB25 PIN	DB9 PIN
1	DCD	Data Carrier Detect	IN	8	1
2	DSR	Data Set Ready	IN	6	6
3	RXD	Receive Data	IN	3	2
4	RTS	Request To Send	OUT	4	7
5	TXD	Transmit Data	OUT	2	3
6	CTS	Clear to Send	IN	5	8
7	DTR	Data Terminal	OUT	20	4
8	RI	Ring Indicator	IN	22	9
9	GND	Signal Ground	--	7	5
10	N/A	Key pin	--	--	--

Table 2-18. Serial Port Connectors (J2, J3)

CONNECTOR TYPE	MATING CONNECTOR
RIBBON	3M 3473-7010
DISCRETE WIRE	MOLEX HOUSING 22-55-2101 N PIN 16-02-0103

Table 2-19. J2 and J3 Mating Connector

2.4.5 Floppy Disk Interface

The onboard floppy disk controller and ROM BIOS support one or two floppy disk drives in any of the standard DOS formats shown in Table 2-20.

CAPACITY	DRIVE SIZE	TRACKS	DATA RATE
360K	5-1/4 inch	40	250 KHz
1.2M	5-1/4 inch	80	500 KHz
720K	3-1/2 inch	80	250 KHz
1.44M	3-1/2 inch	80	500 KHz

Table 2-20. Supported Floppy Formats

Floppy Drive Considerations

Nearly any type of soft-sectored, single or double-sided, 40 or 80 track, 5-1/4 inch or 3-1/2 inch floppy disk drive is usable with this interface. Using higher quality drives improves system reliability. Here are some considerations about the selection, configuration, and connection of floppy drives to the Little Board/386SX-IIA.

- **Drive Interface** -- The drives must be compatible with the board's floppy disk connector signal interface, as described below. Any standard PC or AT compatible 5-1/4 inch or 3-1/2 inch floppy drive will work fine.
- **Drive Quality** -- Use high quality, DC servo, direct drive motor floppy disk drives.
- **Drive Combinations** -- Any combination of supported drives can be used.
- **Drive Select Jumpering** -- Both drives must be jumpered to the second drive select. Use a floppy cable with conductors 10-16 twisted between the two drives. This is standard practice in PC and AT compatible systems.
- **Drive Termination** -- Resistive terminations should be installed only on the drive connected to the last interface cable connector (farthest from the board).
- **Head Load Jumpering** -- When using drives with a Head Load option, jumper the drive for head load with motor on rather than head load with drive select.
- **Drive Mounting** -- If you mount the Little Board directly on a disk drive, place a thin metal shield between the disk drive and the CPU board, to reduce the possibility of electromagnetic interactions.
- **Dual Capacity Drives** -- The Little Board/386SX-IIA's ROM BIOS allows dual-capacity use of 1.2M byte and a 1.44M byte high density drives: that is, 360 Kbyte diskettes can be read on a 1.2 megabyte drive, and 720 Kbyte diskettes read on a 1.44 megabyte drive. However, don't write to low density diskettes on the high density drive, as incomplete erasure may occur.

Floppy Interface Configuration

In SETUP, specify the number and type of floppy drives connected to the system. See Chapter 3.

If you don't use the floppy interface, disable it in SETUP, and by removing the jumper from W6. This frees DRQ2 for use by other devices.

Floppy Interface Connector

Table 2-21 shows the pinout and signal definitions of the floppy disk interface connector, J8. The pinout of J8 meets the AT standard for floppy drive connectors.

PIN	SIGNAL NAME	FUNCTION	IN/OUT
2	-RPM/-RWC	Speed/Precomp	OUT
4	N/A	(Not used)	N/A
6	N/A	Key pin	N/A
8	-IDX	Index Pulse	IN
10	-MO1	Motor On 1	OUT
12	-DS2	Drive Select 2	OUT
14	-DS1	Drive Select 1	OUT
16	-MO2	Motor On 2	OUT
18	-DIRC	Direction Select	OUT
20	-STEP	Step	OUT
22	-WD	Write Data	OUT
24	-WE	Write Enable	OUT
26	-TRK0	Track 0	IN
28	-WP	Write Protect	IN
30	-RDD	Read Data	IN
32	-HS	Head Select	OUT
34	-DCHG	Disk Change	IN
1-33	(all odd)	Signal grounds	N/A

Table 2-21. Floppy Disk Interface Connector (J8)

CONNECTOR TYPE	MATING CONNECTOR
RIBBON	3M 3473-7034
DISCRETE WIRE	MOLEX HOUSING 22-55-2341 PIN 16-02-0103

Table 2-22. J8 Mating Connector

2.5 INTEGRATED DEVICE ELECTRONICS (IDE) HARD DISK INTERFACE

The Little Board/386SX-IIA provides an interface for one or two Integrated Device Electronics (IDE) hard disk drives. These drives have the hard disk controller built-in. The IDE interface appears at connector J11, a 40-pin, dual-row connector. Table 2-23 shows the interface signals and pin outs for the IDE interface connector. The Ampro ROM BIOS allows you to use both IDE and SCSI drives on the same system.

NOTE

For maximum reliability, keep all IDE drive cables less than 18 inches long.

2.5.1 IDE Interface SETUP

Use SETUP to specify one or two hard disk drives and their drive type connected to the IDE interface. The section on SETUP covers this in detail. This interface is only for IDE drives. To use conventional MFM or

RLL drives you must install an appropriate hard disk controller on the AT bus. Use the same section of SETUP for IDE or conventional drive installations.

2.5.2 IDE Interface Connector

Table 2-23 shows the pinout and signal definitions of the IDE interface connector, J11. Table 2-24 gives the part numbers of two mating connectors.

PIN	SIGNAL NAME	FUNCTION	IN/OUT
1	-HOST RESET	Reset signal from host	OUT
2	GND	Ground	OUT
3	HOST D7	Data bit 7	I/O
4	HOST D8	Data bit 8	I/O
5	HOST D6	Data bit 6	I/O
6	HOST D9	Data bit 9	I/O
7	HOST D5	Data bit 5	I/O
8	HOST D10	Data bit 10	I/O
9	HOST D4	Data bit 4	I/O
10	HOST D11	Data bit 11	I/O
11	HOST D3	Data bit 3	I/O
12	HOST D12	Data bit 12	I/O
13	HOST D2	Data bit 2	I/O
14	HOST D13	Data bit 13	I/O
15	HOST D1	Data bit 1	I/O
16	HOST D14	Data bit 14	I/O
17	HOST D0	Data bit 0	I/O
18	HOST D15	Data bit 15	I/O
19	GND	Ground	OUT
20	KEY	Keyed pin	N/C
21	RSVD	Reserved	N/C
22	GND	Ground	OUT
23	-HOST IOW	Write strobe	OUT
24	GND	Ground	OUT
25	-HOST IOR	Read strobe	OUT
26	GND	Ground	OUT
27	RSVD	Reserved	N/C
28	HOST ALE	Address latch enable	OUT
29	RSVD	Reserved	N/C
30	GND	Ground	OUT
31	HOST IRQ14	Drive interrupt request	IN
32	-HOST IO16	Send/receive 16-bit data	IN
33	HOST A1	Drive address 1	OUT
34	-HOST PDIAG	Pass diagnostic	IN
35	HOST AD0	Drive address 0	OUT
36	HOST AD2	Drive address 2	OUT
37	-HOST CS0	Chip select	OUT
38	-HOST CS1	Chip select	OUT
39	SLV/ACT	Drive active/drive slave	N/A
40	GND	Ground	OUT

Table 2-23. IDE Drive Interface Connector (J11)

CONNECTOR TYPE	MATING CONNECTOR
RIBBON	3M 3417-7040
DISCRETE WIRE	MOLEX HOUSING 22-55-2401 PIN 16-02-0103

Table 2-24. J11 Mating Connector

2.6 SCSI INTERFACE

The Little Board/386SX-IIA features a Small Computer System Interface (SCSI) controller. The SCSI port uses a 50-pin male header connector (J7) to interface with SCSI compatible peripherals. Table 2-25 shows the pinout and signal definitions of this interface. Refer to your SCSI device documentation, or the ANSI X3.131 SCSI specification for detailed information on the signal functions. Be sure that the maximum SCSI bus cable length, from the board to the most distant SCSI peripheral, is less than 18 feet. If you don't use the SCSI, disable it in SETUP, remove the jumpers from arrays W12, W23, W24, and W25, and remove RP1, RP2, and RP3 from the board.

PIN	SIGNAL	FUNCTION
2	-DB0	Data Bit 0 (LSB)
4	-DB1	" " 1
6	-DB2	" " 2
8	-DB3	" " 3
10	-DB4	" " 4
12	-DB5	" " 5
14	-DB6	" " 6
16	-DB7	" " 7 (MSB)
18	-DBP	Data Parity
26	TERMPWR	Termination +5VDC
32	-ATN	Attention
34	GROUND	Signal Ground
36	-BSY	Busy
38	-ACK	Transfer Acknowledge
40	-RST	Reset
42	-MSG	Message
44	-SEL	Select
46	-C/D	Control/Data
48	-REQ	Transfer Request
50	-I/O	Data direction
25	N/A	Key pin
1-49 (odd) 20,22,24 28,30	GROUND	Signal Grounds

Table 2-25. SCSI Interface Connector (J7)

CONNECTOR TYPE	MATING CONNECTOR
RIBBON	3M 3425-7050
DISCRETE WIRE	MOLEX HOUSING 22-55-2501 PIN 16-02-0103

Table 2-26. J7 Mating Connector

2.6.1 Normal Use of SCSI

The SCSI interface can serve many purposes, including controlling hard disk drives, tape drives, text scanners, and printer and communications servers. The ROM BIOS supports booting DOS from a SCSI device such as a hard disk. With the ROM BIOS support, you can use any device compatible with the SCSI Common Command Set for direct access devices.

The Little Board/386SX-IIA comes with a diskette containing software utilities for normal DOS operation. It includes a powerful SCSI hard disk formatting utility that allows low-level formatting, changing the disk interleaving, and mapping out bad sectors. Refer to Chapter 4 for information on software setup and drive preparation.

PC-DOS version 3.x requires you to divide drives larger than 32 Mbytes into more than one partition. Under PC-DOS or MS-DOS 3.x, you can logically divide each drive into as many as four partitions, of 32 megabytes each or smaller. This allows the use of physical drives as large as 128 megabytes. MS-DOS 4.x, PC-DOS 4.x and DR DOS (any version) support a maximum drive size of 512M bytes without partitioning.

Besides direct access, SCSI devices include sequential access devices (tape), printer devices, read-only devices (CD-ROM), and processor devices (CPUs). These device types require special application programs, utilities, or driver software not included in the Ampro Utilities.

Hard disk support for operating systems other than DOS may or may not be available through the ROM BIOS hard disk driver. This depends on two things: whether the operating system in question uses BIOS calls exclusively for the hard disk function; and whether the operating system has any special ROM BIOS constraints, such as reentrancy. Some operating systems -- multitasking ones in particular such as Unix -- bypass the BIOS and attempt to program the hard disk controller directly. With such systems, you must modify the operating system to add an appropriate SCSI hard disk driver that can take advantage of the SCSI interface. An alternative is to use the IDE interface instead of SCSI.

2.6.2 The Ampro SCSI BIOS

You can use a variety of mass storage devices with the SCSI universal bus interface and command protocols. To this, Ampro has added a further layer of universality: the SCSI BIOS.

The SCSI BIOS, a set of low level functions in the ROM BIOS, is a hardware independent interface between system software and SCSI peripherals. The advantage of the Ampro SCSI BIOS is in interfacing to devices. Programmers can write software for SCSI devices without concern for the operational details of the SCSI interface. Also, the SCSI BIOS enables you to import software from other environments more safely, quickly and easily.

Chapters 3 and 4 discuss the SCSI interface, and the Ampro SCSI BIOS (in the ROM BIOS) in greater detail. In addition, application note AAN-8804, available from Ampro, provides details of the SCSI BIOS functions.

2.6.3 SCSI Interface Configuration

Configure the SCSI interface according to your system's needs. This is covered in the following paragraphs.

SCSI Bus Termination

Three 8-pin 220/330 ohm SIP resistor networks (RP1, RP2, and RP3) provide host termination for the bus. Usually SCSI peripherals have terminations as well. With several devices on the bus, only the host and the physically most remote SCSI device need terminations. An improperly terminated SCSI bus may interfere with normal system operation due to indeterminate signal levels.

NOTE

Be sure to install the SCSI termination networks so pin 1 of the SIP, generally marked with a dot or a colored band, is in socket pin 1.

Internally, pins 2-7 of the SIP networks have 220 ohm resistors connected to +5 volts (pin 8), and 330 ohm resistors connected to ground (pin 1). The three terminators draw a total of about 800 milliwatts. If system power consumption is critical, consider locating the terminators off the board, and powering them externally. If you don't use the SCSI port, remove RP1-3 to save power.

External Termination Power Option

You can power external SCSI terminations from the board. A jumper option (W19), connects power (+5V) to the SCSI bus TERMPWR signal (J7, pin 26). The board includes a Shottky protection diode to prevent damage to the board by current flowing from the SCSI bus.

The default jumpering of W19 is open; that is, termination power is not normally supplied by the Little Board/386SX-IIA.

SETUP Options

Every SCSI device must be configured for a specific SCSI bus ID, between 0 and 7. Normally, set the SCSI initiator ID to 7. Set the IDs of the disk drives and other SCSI target devices to 0, 1, and so forth.

Using SETUP, disable or enable the SCSI BIOS services. If you disable them, there will only be BIOS support available to device drivers. This might be desirable for several reasons:

To speed system booting when you don't use SCSI. Otherwise, there is a delay while the system waits for a SCSI device.

To disable SCSI BIOS control of the SCSI hardware, when you have a non-standard use for the interface.

2.7 AT EXPANSION BUS

Warning

The male PC/104 Bus Headers supplied on this Second Generation Little Board CPU are not compatible with backplanes and cable adapters intended for use with Third Generation Little Boards. Damage to the Little Board will occur if used with these components. Use only Bus Expansion components intended for use with Second Generation products.

Warning

The DST Cable Adapter and AT Bus backplane supplied with Second Generation Development Chassis, Kits, and Systems are not compatible with Third Generation Little Board CPUs. Damage to the Little Board will occur if used with these components.

The standard AT I/O channel expansion bus appears on a pair of header connectors at P1A, P1B, P2C,and P2D. P1A and P1B are dual 32-pin headers. P2C and P2D are dual 20-pin headers. The PC-bus subset of the AT

expansion bus connects to the first 31 pins of P1A and P1B. The two additional pins of P1A and P1B (A32 and B32) are added grounds to enhance system reliability. Connectors P2C and P2D replace the 36-pin edgecard connector of a conventional AT expansion bus. It has extra ground pins at each end of the connector (C0, D0, D19).

The buffered output signals to the AT Expansion Bus are standard TTL level signals. All inputs to the Little Board/386SX-IIA operate at TTL levels and present a typical CMOS load to the AT bus. The current sinking rating for output signals driving the AT expansion bus is given in Tables 2-27A through 2-27D. Certain control signals have 33 ohms in series to limit ringing. Other signals are pulled up through the values indicated in Tables 2-27A through 2-27D. You can find further information about these signals in many publications, including the IBM technical reference manuals for the PC and AT computers, and from the reference documents listed in this manual.

The numbering of the AT expansion bus pins is different from the other header connectors on the board. The AT bus pin numbers correspond to the scheme normally used on the PC and AT expansion bus. Rather than numerical designations (1, 2, 3) they have alpha-numeric (A1, A2, . . . , B1, B2, . . .) designations.

2.7.1 Onboard MiniModule Header and Bus Expansion

The AT expansion bus appears on the header connectors P1A, P1B, P2C, and P2D. You can install one or more MiniModules on these connectors. MiniModules have Stackthrough connectors with straight pins, so you can stack several modules on the headers. Each module increases the thickness of the package by about 0.8 inches (20 mm). Stack 16-bit MiniModules closest to the Little Board/386SX-IIA as the 8-bit modules do not have the 40 pin Stackthrough connector. See Figure 2-9.

Ampro MiniModule display controllers offer a variety of standard PC and AT video modes, including Super VGA, VGA, and Hercules display compatibility. Ampro also offers a wide variety of MiniModules, including serial/parallel interfaces. Contact Ampro for information on additional MiniModules.

2.7.2 Using Standard PC and AT Bus Cards

Ampro offers several options that allow you to add conventional PC and PC/AT expansion cards to the Little Board/386SX-IIA system. Contact Ampro for further information on optional bus expansion products.

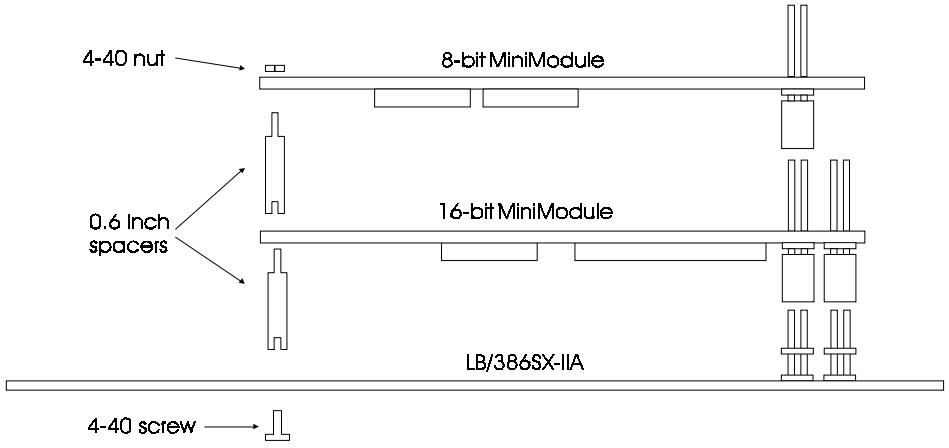


Figure 2-9 Stacking MiniModules on the Little Board/386SX-IIA

2.7.3 Bus Expansion Guidelines

One way to expand the AT bus is by connecting cables to the header connectors. A Double Stackthrough Cable Adapter is used. Install the DST Adapter on the Little Board/386SX-IIA header connectors, then connect the bus expansion cables to the DST Adapter. Several options, available from Ampro and others, allow expansion with standard PC or AT bus plug-in cards. Use the following guidelines about the length and quality of the cables.

Cable Length and Quality -- In general, keep the bus expansion cable as short as possible. Long cables reduce system reliability.

- For cables up to 6 inches, use a high quality standard cable, such as 3M 3365/64 (64 conductor) and 3365/40 (40 conductor).
- For cables between 6 to 12 inches long, use a high quality ground plane cable, such as 3M part number 3353/64 (64 conductor) and 3353/40 (40 conductor).
- Do not use cables over 12 inches long.

Backplane Quality -- Be sure to use a high quality backplane that minimizes signal crosstalk. Use of power and ground planes, and guard traces between bus signals will improve system reliability.

Eliminating Reset and TC Noise -- Some cards have asynchronous TTL logic inputs that are susceptible to noise and crosstalk. The active high RESET and TC bus lines are especially vulnerable. You can make these signals more reliable by adding a 200 pF to 500 pF capacitor between the signal and ground to prevent false triggering by filtering noise on the signals. These RESET and TC filters are included on most Ampro backplane expansion products.

Bus Termination -- Many backplanes include bus termination to improve system reliability by matching backplane impedance to the rest of the system. The IEEE-P996 draft specification for the AT expansion bus recommends the use of AC termination rather than resistive termination. The recommended AC termination is a 50 to 100 pF capacitor, in series with a 50 to 100 ohm resistor, from each signal to ground. Ampro provides positions for OEM addition of AC termination on most bus expansion products.

CAUTION

Do not use resistive bus termination! If the signal requires termination, use AC termination only.

Here are some manufacturer part numbers for 9-pin, eight-terminator devices with 100 pF capacitors in series with 100 ohm resistors:

- Dale CSRC-09C30-101J-101M
- Bourns 4609H-701-101/101

The actual requirements for signal termination depend on system configuration, interconnecting bus cable, and on the number and type of expansion modules used. It is the system engineer's responsibility to determine the need for termination.

2.7.4 Expansion Bus Connector Pinouts

Tables 2-27A through 2-27D indicate the pinout and signal functions on the AT expansion bus connectors. Further information about these signals is available in various publications, including the IBM technical reference manuals for the PC and AT computers, and from the other reference documents listed in this manual.

The Little Board/386SX-IIA does not generate ±12VDC or -5VDC for the AT expansion bus. If devices on the AT expansion bus require these voltages, they can be supplied to the AT expansion bus connector from the

utility connector (J4). Some Ampro expansion products provide for DC-to-DC converters for all bus voltages except +5VDC.

PIN	SIGNAL NAME	FUNCTION	IN/OUT	CURRENT	PU/PD/SER*
A1	-IOCHCK	Bus NMI input	IN	N/A	4.7K PU
A2	SD7	Data bit 7	I/O	24 mA	10K PU
A3	SD6	Data bit 6	I/O	24 mA	10K PU
A4	SD5	Data bit 5	I/O	24 mA	10K PU
A5	SD4	Data bit 4	I/O	24 mA	10K PU
A6	SD3	Data bit 3	I/O	24 mA	10K PU
A7	SD2	Data bit 2	I/O	24 mA	10K PU
A8	SD1	Data bit 1	I/O	24 mA	10K PU
A9	SD0	Data bit 0	I/O	24 mA	10K PU
A10	IOCHRDY	Processor Ready	IN	N/A	1K PU
A11	AEN	Address Enable	I/O	12 mA	
A12	SA19	Address bit 19	I/O	12 mA	
A13	SA18	Address bit 18	I/O	12 mA	
A14	SA17	Address bit 17	I/O	12 mA	
A15	SA16	Address bit 16	I/O	12 mA	
A16	SA15	Address bit 15	I/O	12 mA	
A17	SA14	Address bit 14	I/O	12 mA	
A18	SA13	Address bit 13	I/O	12 mA	
A19	SA12	Address bit 12	I/O	12 mA	
A20	SA11	Address bit 11	I/O	12 mA	
A21	SA10	Address bit 10	I/O	12 mA	
A22	SA9	Address bit 9	I/O	12 mA	
A23	SA8	Address bit 8	I/O	12 mA	
A24	SA7	Address bit 7	I/O	12 mA	
A25	SA6	Address bit 6	I/O	12 mA	
A26	SA5	Address bit 5	I/O	12 mA	
A27	SA4	Address bit 4	I/O	12 mA	
A28	SA3	Address bit 3	I/O	12 mA	
A29	SA2	Address bit 2	I/O	12 mA	
A30	SA1	Address bit 1	I/O	12 mA	
A31	SA0	Address bit 0	I/O	12 mA	
A32	GND (**)	Ground	N/A	N/A	

* PU=pull up; PD=pull down; SER=resistance in series. All values in ohms.

** Added ground. Not needed with conventional expansion cards.

Table 2-27A. AT Expansion Bus Connector, A1-A32 (P1A)

PIN	SIGNAL NAME	FUNCTION	IN/ OUT	CURRENT	PU/PD/SER*
B1	GND	Ground	N/A	N/A	
B2	RESETDRV	System reset signal	OUT	24 mA	
B3	+5V	+5V Power	N/A	N/A	
B4	IRQ9	Interrupt request 9	IN	N/A	27K PU
B5	-5V	To J4 pin 9	N/A	N/A	
B6	DRQ2	DMA request 2	IN	N/A	10K PD
B7	-12V	To J4 pin 10	N/A	N/A	
B8	-ENDXFR	Zero wait state	NC	N/A	
B9	+12V	To J4 pin 8	N/A	N/A	
B10	N/A	Keyed pin	N/A	N/A	
B11	-SMEMW	Memory Write (lower	I/O	12 mA	33 SER
B12	-SMEMR	Memory Read (lower	I/O	12 mA	33 SER
B13	-IOW	I/O Write	I/O	12 mA	33 SER
B14	-IOR	I/O Read	I/O	12 mA	33 SER
B15	-DACK3	DMA Acknowledge 3	OUT	6 mA	
B16	DRQ3	DMA Request 3	IN	N/A	10K PD
B17	-DACK1	DMA Acknowledge 1	OUT	6 mA	
B18	DRQ1	DMA Request 1	IN	N/A	10K PD
B19	-REFRESH	Memory Refresh	I/O	24 mA	470 PU
B20	SYSCLK	System (bus) clock	OUT	6 mA	
B21	IRQ7	Interrupt Request 7	IN	N/A	27K PU
B22	IRQ6	Interrupt Request 6	IN	N/A	27K PU
B23	IRQ5	Interrupt Request 5	IN	N/A	27K PU
B24	IRQ4	Interrupt Request 4	IN	N/A	27K PU
B25	IRQ3	Interrupt Request 3	IN	N/A	27K PU
B26	-DACK2	DMA Acknowledge 2	OUT	6 mA	
B27	TC	DMA Terminal Count	OUT	12 mA	
B28	BALE	Address latch enable	OUT	12 mA	33 SER
B29	+5V	+5 volts power	N/A	N/A	
B30	OSC	14.3 MHz clock	OUT	6 mA	33 SER
B31	GND	Ground	N/A	N/A	
B32	GND**	Ground	N/A	N/A	

* PU=pull up; PD=pull down; SER=resistance in series. All values in ohms.

** Added ground. Not needed with conventional expansion cards.

Table 2-27B. AT Expansion Bus Connector, B1-B32 (P1B)

PIN	SIGNAL NAME	FUNCTION	IN/OUT	CURRENT	PU/PD/SER*
C0	GND (*)	Ground	N/A	N/A	
C1	-SBHE	Bus High Enable	I/O	N/A	
C2	LA23	Address bit 23	I/O	12 mA	
C3	LA22	Address bit 22	I/O	12 mA	
C4	LA21	Address bit 21	I/O	12 mA	
C5	LA20	Address bit 20	I/O	12 mA	
C6	LA19	Address bit 19	I/O	12 mA	
C7	LA18	Address bit 18	I/O	12 mA	
C8	LA17	Address bit 17	I/O	12 mA	
C9	-MEMR	Memory Read	I/O	12 mA	33 SER
C10	-MEMW	Memory Write	I/O	12 mA	33 SER
C11	SD8	Data bit 8	I/O	24 mA	10K PU
C12	SD9	Data bit 9	I/O	24 mA	10K PU
C13	SD10	Data bit 10	I/O	24 mA	10K PU
C14	SD11	Data bit 11	I/O	24 mA	10K PU
C15	SD12	Data bit 12	I/O	24 mA	10K PU
C16	SD13	Data bit 13	I/O	24 mA	10K PU
C17	SD14	Data bit 14	I/O	24 mA	10K PU
C18	SD15	Data bit 15	I/O	24 mA	10K PU
C19	N/A	Keyed Pin	N/A	N/A	

* PU=pull up; PD=pull down; SER=resistance in series. All values in ohms.

** Added ground. Not needed with conventional expansion cards.

Table 2-27C. AT Expansion Bus Connector, C0-C19 (P2C)

PIN	SIGNAL NAME	FUNCTION	IN/OUT	CURRENT	PU/PD/SER*
D0	GND**	Ground	N/A	N/A	
D1	-MEMCS16	16-bit mem access	IN	N/A	330 PU
D2	-IOCS16	16-bit I/O access	IN	N/A	330 PU
D3	IRQ10	Interrupt Request 10	IN	N/A	27K PU
D4	IRQ11	Interrupt Request 11	IN	N/A	27K PU
D5	IRQ12	Interrupt Request 12	IN	N/A	27K PU
D6	IRQ15	Interrupt Request 15	IN	N/A	27K PU
D7	IRQ14	Interrupt Request 14	IN	N/A	27K PU
D8	-DACK0	DMA Acknowledge 0	OUT	6 mA	
D9	DRQ0	DMA Request 0	IN	N/A	10K PD
D10	-DACK5	DMA Acknowledge 5	OUT	6 mA	
D11	DRQ5	DMA Request 5	IN	N/A	10K PD
D12	-DACK6	DMA Acknowledge 6	OUT	6 mA	
D13	DRQ6	DMA Request 6	IN	N/A	10K PD
D14	-DACK7	DMA Acknowledge 7	OUT	6 mA	
D15	DRQ7	DMA Request 7	IN	N/A	10K PD
D16	+5V	+5 volts power	N/A	N/A	
D17	-MASTER	Bus master assert	IN	N/A	330 PU
D18	GND	Ground	N/A	N/A	
D19	GND**	Ground	N/A	N/A	

* PU=pull up; PD=pull down; SER=resistance in series. All values in ohms

** Added ground. Not needed with conventional expansion cards.

Table 2-27D. AT Expansion Bus Connector, D0-D19 (P2D)

2.7.5 Interrupt and DMA Channel Usage

The AT bus provides several interrupt and DMA control signals. When you expand the system with MiniModules or plug-in cards that require either interrupt or DMA support, you must select which interrupt or DMA channel the added device uses. Typically this involves switches or jumpers on the module. It is important that you configure the added module to use an interrupt or DMA channel not already in use. For your convenience, Tables 2-28 and 2-29 provide a summary of the normal assignment of interrupt and DMA channels on the Little Board/386SX-IIA.

INTERRUPT	FUNCTION
IRO0*	ROM BIOS clock tick function, from Timer 0
IRQ1*	Keyboard interrupt
IRQ2*	Cascade input for IRQ8-15
IRQ3	Secondary serial port (if present)
IRQ4	Primary serial port (if present)
IRQ5	Reserved for secondary parallel printer
IRQ6	Floppy controller (if present)
IRQ7	Parallel printer (if present)
IRQ8*	Reserved for battery-backed clock alarm
IRQ9**	Some EGA, VGA controllers (if present)
IRQ10	Available
IRQ11	Available
IRQ12	Available
IRQ13*	Reserved for math coprocessor
IRQ14	Hard disk controller
IRQ15	Available

* Unavailable on PC/AT bus.

** Corresponds to IRQ2 on a PC's expansion bus.

Table 2-28. Interrupt Channel Assignment

CHANNEL	FUNCTION
0	Available for 8-bit transfers
1	Available for 8-bit transfers
2	Floppy controller (if present)
3	SCSI (if present)
4	Cascade for channels 0-3
5	Available for 16-bit transfers
6	Available for 16-bit transfers
7	Available for 16-bit transfers

Table 2-29. DMA Channel Assignment

CHAPTER 3

SOFTWARE CONFIGURATION

3.1 INTRODUCTION

This chapter provides an overview of the system features, configuration options, and utilities that are available under a disk operating system. A combination of standard DOS and Ampro-supplied utilities and drivers allows you to create a highly customized system based on the Little Board/386SX-IIA.

This chapter discusses configuration of the operating system and system utilities. It is easy to boot the system under DOS after connecting appropriate peripherals. You can use the flexibility of the ROM BIOS and utilities to customize a DOS-based installation.

This manual presumes you have some familiarity with DOS (PC-DOS, MS-DOS, or DR DOS). Refer to the appropriate DOS reference manuals for further information on the DOS, its drivers and utilities. The Common Utilities manual contains detailed descriptions of the Ampro driver and utility programs.

3.1.1 Conventions

In the descriptions that follow, keyboard inputs that you make are underlined. This is to make it easy for you to distinguish the computer's prompts from your input. For example,

```
A>DIR<Enter>
```

means that you type "DIR" and then press the <Enter> key on your keyboard. (On some keyboards this key is called <Return>.)

Generally, upper and lower case letters can be used interchangeably when you supply parameters to a program. For example:

```
A>SETUP @ SYSTEM.A<Enter>
```

has the same effect as:

```
A>setup @ system.a<Enter>
```

3.2 OPERATION WITH DOS

The Little Board/386SX-IIA ROM BIOS allows the use of version 3.3 (or later) of IBM's PC-DOS or Microsoft's MS-DOS, or of any version of Digital Research's DR DOS as the disk operating system. Throughout this chapter, *DOS* refers to any of these operating systems, unless a difference in operation exists.

CAUTION

Some variations of MS-DOS are customized for operation on specific computer systems. These may not function properly on the Little Board/386SX-IIA. Use DR DOS as supplied by Ampro, IBM PC-DOS, or the generic IBM compatible version of MS-DOS *supplied directly by Microsoft on an OEM basis.*

The Little Board/386SX-IIA includes the following standard AT devices: a keyboard port, a speaker port, a parallel (printer) port, two serial ports, a programmable timer, DMA controllers, interrupt controllers, and a battery-backed clock with an internal CMOS RAM.

DOS normally supports the board's two 8250-compatible RS232C serial ports as the COM1 and COM2 ports. The Parallel Printer port is normally the DOS LPT1 device. The ROM BIOS supports these devices, and the keyboard and speaker ports as in a standard AT.

The ROM BIOS maintains the real-time clock. It is incremented approximately 18.2 times per second by an interrupt from one of the timer/counters. The ROM BIOS automatically initializes it, upon system reset or powerup, to the correct time and date stored in the onboard battery-backed clock.

Older versions of DOS requires you to divide disk drives larger than 32M bytes into more than one *partition*. They will allow four partitions, enabling the use of physical drives as large as 128M bytes. MS-DOS or PC-DOS versions 4.0 (or later), or any version of DR DOS support hard disks as large as 512M bytes.

3.2.1 Configuration Options

System configuration is widely variable through options in: (1) the disk operating system and its drivers and utilities; (2) the Ampro Common Utilities.

Typical configuration options include:

- Console selection and setup
- Parallel and serial port selection and setup
- Choice of floppy disk drives
- One or more SCSI hard disk drives
- One or more IDE hard disk drives
- Modem interface
- LAN adapter

Examples of how a typical system can be configured for many of these options are given later in this chapter.

The following section briefly summarizes the features of the software included in the Ampro Little Board/386SX-IIA utilities and drivers. The Common Utilities technical manual contains detailed program descriptions.

3.2.2 Little Board/386SX-IIA Utilities Overview

The Common Utilities diskette contains the following programs. Actual utility names and descriptions may vary. In these cases, the utilities diskette includes appropriate .DOC files.

- SCSICOMP -- A SCSI utility that compares data from two SCSI direct access devices.
- SCSICOPY -- A SCSI copy utility that copies data between two SCSI direct access devices.
- SCSIFMT -- A hard disk utility for low level SCSI drive formatting.
- SCSIPARK -- A hard disk park utility.
- SCSITOOL -- A SCSI debugger utility that allows the user to issue low level commands to any SCSI bus device.
- SCSI-ID -- A test that reports the SCSI initiator ID of the board. Usable from batch files.
- SETUP -- Provides command line access to the SETUP function.
- SERLOAD -- A serial loader utility. Allows downloading files serially from a remote host, prior to system boot.

This chapter discusses the use of many of these utilities in typical system configurations.

3.2.3 The Ampro SETUP Function

Use the Ampro SETUP function to initialize or modify the contents of the nonvolatile Configuration Memory. The Configuration Memory comprises the NOVRAM in the battery-backed clock chip, and the Configuration EEPROM. SETUP takes effect at system boot time.

The SETUP function is in the ROM BIOS and on the utilities diskette. You can access SETUP in two ways. One is by entering SETUP.COM from the command line with the utilities diskette in the default drive. The other is by pressing the CTRL-ALT-ESC keys simultaneously at powerup or reset time.

The SETUP.COM utility also allows you to save or restore Configuration Memory contents to or from disk files.

DESCRIPTION

The Ampro SETUP function resides in the ROM BIOS. Use it to initialize the nonvolatile Configuration Memory on the Little Board/386SX-IIA. System configuration parameters, used by the ROM BIOS to establish the system setup at boot time (powerup or reset), are stored in two nonvolatile memory components on the board:

- AT compatible battery backed CMOS RAM within the clock device
- Ampro-unique configuration EEPROM

One utility, SETUP, initializes and modifies parameters in both memory devices. These two memories are called the Configuration Memory.

The configuration memory stores the following parameters

- Date and time values of the battery-backed real-time clock
- Floppy drive quantity and type
- Hard disk drive quantity and type
- Video controller powerup/reset mode
- DRAM configuration display
- Shadow RAM enable/disable
- CPU cache enable/disable
- Option of halting on powerup self test (POST) errors
- Set byte-wide memory sockets' window size and address
- Select which byte-wide socket the BIOS enables on power up or reset
- Enable/disable Integrated Device Electronics hard disk interface
- Enable/disable floppy drive interface
- Set the system's mono/color jumper
- Enable/disable for each two RS232C serial ports
- Enable/disable for the parallel printer port
- Parallel printer port configuration, primary or secondary
- Install ROM BIOS resident console device driver
- Baud rate and data characteristics for a console serial port
- Choice of default boot drive (hard disk or floppy)
- Various SCSI interface and device related parameters
- Enable/disable the SCSI BIOS services
- Enable/disable hot key access to SETUP
- Watchdog timer
- POST speed
- POST screen blanking

Table 3-1. Configuration Parameters

There are two ways to use the SETUP function. It can be used from its interactive menu-based user interface, or it can be directed to automatically take its inputs from a file. The first of these methods is the normal way you initialize and modify a system's configuration. The file-based mode of operation allows you to automate the process -- for example in volume system production.

NOTE

Changes made using the SETUP function do not take effect until the next time the system boots.

INTERACTIVE MODE OF OPERATION

There are two ways to invoke SETUP's interactive mode of operation. You can invoke SETUP at system powerup or reset time by holding down the following hot key combination:

```
CTRL-ALT-ESC
```

When you power up or reset the system, a message at the bottom of the screen tells you when you can use the hot key entry into SETUP.

Or, you can invoke SETUP during system operation with the Ampro SETUP program by typing the program's name at the DOS command line, as follows:

```
A>SETUP <Enter>
```

SETUP has four menu pages, one page for standard settings and three pages for extended settings as follows:

PAGE	MENU CONTENT	FUNCTIONS
1	Standard (CMOS/EEPROM) Setup	Date and time; floppies; hard disks; video; RAM; error halt; Shadow RAM; POST speed; and cache.
2	Little Board/386SX-IIA Options/Peripheral	Extended BIOS; Serial/Parallel ports; Byte-wide sockets enable and size; IDE enable; Serial boot loader; Watchdog timer; Hot Key SETUP enable; POST screen blank.
3*	Extended SCSI and Hard Disk Configuration	SCSI parameters, SCSI Disk maps, DOS Disk maps
4*	Extended Serial Console Configuration	Console Input and Output device configuration

* SETUP Pages 3 and 4 are available when you enable Extended BIOS at SETUP page 2 (Little Board/386SX-IIA Options/Peripheral Configuration)

Table 3-2. SETUP Pages

Standard (CMOS/EEPROM) Setup (Page 1)

The options on this menu allow you to:

- Set the correct time and date
- Specify the number and type of floppy drives
- Specify drive characteristics for one or more hard disk drives connected to an AT bus hard disk controller. (Includes IDE drives.)
- Specify the system's initial video mode
- Specify whether the system should halt on a variety of power on self-test (POST) errors
- Specify the state of the CPU cache
- Specify shadowing of ROM BIOS or Video BIOS (or both) in RAM
- Set the POST speed option, NORMAL, FAST, EXPRESS

Little Board/386SX-IIA Options/Peripheral Configuration (Page 2)

- The options on this menu allow you to:
- Enable the Extended BIOS
- Enable or disable serial Ports 1 and 2
- Specify the parallel port as Primary, Secondary, or disabled.
- Enable or disable Floppy interface
- Enable or disable the Integrated Device Electronics (IDE) hard disk interface
- Specify the mono or color jumper
- Specify the socket size and address for the byte-wide sockets
- Specify which (if any) byte-wide socket is BIOS enabled on power up or reset
- Enable or disable the Serial Boot Loader
- Enable or disable the Watchdog Timer
- Enable or disable blanking of the POST test
- Enable or disable the Hot Key SETUP function

The Hot Key setup option allows the disabling of the Crtl-Alt-Esc entry of SETUP. When you disable the hot key, you must use SETUP Version 3.00 or later, to invoke the SETUP function.

CAUTION

If you disable the SETUP hot key and no boot device is present (or SETUP disables all boot devices), you must disconnect the serial console and short pins 7/8 of the serial port connector on the CPU board to recover. Therefore use the disable SETUP hot key option with care!

Extended SCSI and Hard Disk Configuration: Page 3

The options on this menu allow you to:

- Enable/Disable SCSI BIOS Hard Disk Services
- Specify characteristics of the SCSI interface.
  - Specify the SCSI Initiator ID (0-7) of the Little Board/386SX-IIA
  - Specify the number of read/write retries during DOS accesses to SCSI devices.
- Specify the SCSI disk map for up to seven SCSI bus devices
  - Specify the SCSI target IDs
  - Specify the SCSI device Logical Unit Number (LUN) for each SCSI disk drive
- Define up to eight physical DOS hard disk drives (SCSI or AT Bus Controller interfaced)
- Select the default boot device

Use the following SCSI and Disk Setup menu options to specify the SCSI and hard disk parameters and options:

SCSI BIOS Services

The SCSI BIOS disable function does not prevent the use of the module's SCSI hardware controller for non-SCSI I/O. It simply disables the DOS hard disk support for SCSI drives. Disable SCSI BIOS services in applications that do not require them, so the ROM BIOS does not waste time waiting for a possible SCSI drive to become available at boot time.

SCSI Initiator ID

Enter a value for the Little Board/386SX-IIA's SCSI Initiator ID (0-7). This must be a unique ID for this system. Use 7 as it has the highest priority for SCSI Bus arbitration.

SCSI Read/Write Retries

This option specifies how many times the ROM BIOS retries when accessing SCSI devices as DOS disk drives.

SCSI Disk Map (SCSI Drive Definitions)

Up to seven SCSI drives may be defined to be usable as BIOS-installed hard disk devices. These can be any SCSI Direct Access Device. These include hard disk drives, SCSI magnetic bubble memory cartridges, SCSI RAM drives, SCSI floppy drives, and many SCSI tape drives. Do not specify other types of SCSI devices that will not be accessed as DOS disk drives. These require special utilities, drivers, or application specific code.

Enter the SCSI ID and LUN values for each BIOS-installed SCSI device, and set the status of the SCSI device to Active. If your system has less than the maximum number of SCSI devices, be sure to set the status of unused SCSI device numbers to Not Active. Once you have defined a SCSI device (that is, specified ID and LUN numbers, and set the status set to Active), you can specify it as a physical DOS hard disks. Use the DOS Disk Map options of this menu.

DOS Disk Map (Physical DOS Hard Disk Selections)

These menu options define up to four drives that are to be BIOS-installed DOS hard disk devices. Only two are available.

NOTE

PC-DOS and MS-DOS allow installing one or two hard disk drives, while DR DOS allows up to eight.

As with the SCSI Disk Map options, do not specify SCSI devices that will not be accessed as DOS disk drives. These require special utilities, drivers, or application specific code.

You must provide two configuration parameters for each drive that you are defining as a BIOS-installed DOS disk drive: device type; and device number. The three device type choices are: SCSI Disk, AT BUS HDC, and Not Active.

When the device type is SCSI, the device number can be 0 to 7. This number indicates which of the SCSI Devices (defined in the SCSI Disk Map) are identified as the particular physical DOS hard disk (1st through 8th).

When the device type is AT BUS HDC, the device number can be 0 or 1, which indicates which of the AT bus hard disk controller drives defined in the Little Board/386SX-IIA Setup menu as the particular physical DOS hard disk (1st through 8th). This type of drive includes IDE connected drives.

You can define drives through this menu's SCSI Disk Map options, but not specify them as DOS hard disks (with the DOS Disk Map options). You can access these drives through the Little Board/386SX-IIA's ROM

BIOS with special software. Refer to the Ampro SCSI BIOS interface specification, which appears in Ampro application note AAN-8804.

Any DOS drive positions in the SETUP screen that do not have physical hard drives associated with them, should be specified Not Active.

NOTE

Refer to the installation procedures in Chapter 3 for additional details on how to prepare (format, partition, etc.) the SCSI device for DOS access.

Default Boot Device Selection

This menu options allows you to select the device that is to be the primary device for system bootstrap loading. The choices are Floppy Drive and Hard Drive.

When you specify Floppy Drive as the primary boot device, the ROM BIOS will first attempt to boot from a floppy diskette in the A drive. If a floppy diskette is not present, the ROM BIOS will attempt to boot from the 1st DOS Hard Disk (as defined in Extended Hard Disk Configuration). If booting from the DOS Hard Drive is not possible (not defined, not present, or not ready), the bootstrap process will start over with the Floppy Drive.

When you specify DOS Hard Drive as the primary boot device, the ROM BIOS will not search for a floppy in its boot process. Instead, it will attempt to boot directly from the device defined in Extended Hard Disk Configuration, DOS Disk Map. If the defined device is not present or not ready, the ROM BIOS will begin the bootstrap process over, looping in this manner until it finds the defined device. When you specify hard disk as the primary boot device, you can force the system to boot from floppy drive A by pressing the <Esc> key after the self-test and prior to the boot process.

Extended Serial Console Configuration: Page 4

The options on this menu allow you to:

- Select the Serial Console Output Device
  - Video
  - Serial 1
  - Serial 2
  - None

    If you select Serial 1 or Serial 2, you may specify:

    - Data Length: 5,6,7,or 8 bits. The default is 8.
    - Stop Bits: 1 or 2. The default is 2.
    - Parity: Odd, Even, or None. The default is Even.
    - Baud rate: 150, 300, 600, 1200, 2400, 9600 or 19200. The default is 9600.
    - Delete from Com Port Table: Yes or No. The default is Yes.
    - Console Output Handshake: Enabled or Disabled. The default is Disabled.
- Select the Serial Console Input Device
  - Keyboard
  - Serial 1
  - Serial 2
  - None

    If you select Serial 1 or Serial 2, you may specify:

    - Data Length: 5,6,7,or 8 bits. The default is 8.
    - Stop Bits: 1 or 2. The default is 2.
    - Parity: Odd, Even, or None. The default is Even.
    - Baud rate: 150, 300, 600, 1200, 2400, 9600 or 19200. The default is 9600.

The ROM BIOS contains the serial keyboard/display console driver. Console input can be standard AT keyboard, primary serial port, or secondary serial port. Console output can be standard video (for example, MDA, CGA, EGA, or VGA controller), primary serial port, or secondary serial port. On most serial display devices, SETUP can be operated from a serial console. You can also select None for the console input and output.

ALTERNATIVE MODES OF OPERATION

The Ampro SETUP utility, SETUP.COM, offers the following options for command line entry:

```
SETUP [-switches] [ @file.ext | Wfile.ext ]
```

The supported switches and their meaning are as follows:

?	Display a usage help screen
T	Set the NOVRAM time and date to the DOS time and date
O	Enter SETUP even if the Ampro Extended BIOS service has been disabled.
0	Set the EEPROM write count to zero
@file.ext	Set the contents of the Little Board/386SX-IIA's EEPROM Configuration Memory to the data in the file specified. The file name may contain an optional drive and path.
Wfile.ext	Write NOVRAM and EEPROM contents to the file specified. The file name may contain an optional drive and path.

You can save a copy of the current contents of the board's Configuration Memory to a disk file by using the W switch. The data saved includes the entire contents of the nonvolatile configuration EEPROM, except the current time and date. The first 512 bits are the SETUP information, the last 512 bits are available for OEM storage (See Ampro Application Note AAN-8805). The file you create with this menu option can be used as a source for programming the Configuration Memory of a Little Board/386SX-IIA at a later time.

Following is an example of a file's contents:

```
NOVRAM 00:  24 00 35 00 08 00 07 05 - 12 89 26 02 50 80 00 00
NOVRAM 10:  12 00 00 00 41 80 02 80 - 01 00 00 00 00 00 00 00
NOVRAM 20:  00 00 00 00 00 00 00 00 - 00 00 00 00 00 00 01 56
NOVRAM 30:  80 01 19 80 00 00 00 00 - 00 00 00 00 39 00 38 e8
EEPROM 00:  eb 33 10 19 19 1a a8 bf - f4 ff ff ff ff ff 3e 00
EEPROM 10:  81 e1 ff fa ff ff ff ff - ff ff ff ff ff ff ff ff
EEPROM 20:  ff ff ff ff ff ff ff ff - ff ff ff ff ff ff ff ff
EEPROM 30:  ff ff ff ff ff ff ff ff - ff ff ff ff ff ff ff ff
EEPROM 40:  ff 00 ff ff ff ff ff ff - ff ff ff ff ff ff ff ff
EEPROM 50:  ff ff ff ff ff ff ff ff - ff ff ff ff ff ff ff ff
EEPROM 60:  ff ff ff ff ff ff ff ff - ff ff ff ff ff ff ff ff
EEPROM 70:  ff ff ff ff ff ff ff ff - ff ff ff ff ff ff ff 00
```

For information regarding the file's content and format, contact Ampro Technical Support.

As an example, the following command initializes the EEPROM values with a previously saved configuration:

```
C>SETUP  @SYSTEM.A <Enter>
```

Assuming you created the file SYSTEM.A with SETUP's write option, SETUP will initialize the EEPROM Configuration Memory using the contents of SYSTEM.A.

NOTE

Word addresses not specifically named are not changed. For example, if you have a file with an entry for EEPROM 20, only the entry at that location is changed. All other contents of Configuration Memory remain the same.

Using SETUP with the write and read parameters can be useful when many boards must be initialized automatically. Another use for this SETUP mode might be to change between several predefined system configurations.

3.2.4 EMS Option

The Little Board/386SX-IIA can emulate the Lotus-Intel-Microsoft Expanded Memory Specification Version 4.0 (LIM EMS 4.0) with the memory management capability of the 80386SX under control of a device driver. Such drivers and other EMS software are available from third parties. An EMS driver is available from Ampro as part of the DR DOS operating system.

3.3 USING A PARALLEL PRINTER

No special configuration is required to use the system with a PC compatible parallel printer. SETUP allows you to enable the parallel port as the *primary*, or *secondary* port, or to disable it entirely. Most application software uses LPT1 as the default printer port. If you enable the port, printing to it is automatic.

The following DOS commands will result in printing to the parallel printer:

```
A>COPY CONFIG.SYS LPT1<Enter>
```
. . . prints contents of CONFIG.SYS

```
A>DIR >LPT1<Enter>
```
. . . prints the directory

In addition, the <PrtSc> (Print Screen) key will print the contents of the video screen to the LPT1 device. Also, you can use the Printer Echo function to print all characters written to the console. The command <Ctrl-P> enables the Printer Echo function. Entering <Ctrl-P> again disables Printer Echo.

NOTE

LPTn (n=1, 2) is a logical designation, not a physical value. When the system boots, the ROM BIOS scans both parallel port addresses, and installs the first one it finds as LPT1. If it finds a second one, it installs that one as LPT2. Changing the port's designation to secondary with SETUP does not change it from LPT1 to LPT2. There must be an LPT1 elsewhere in the system for the onboard parallel port to become LPT2.

3.4 USING THE SERIAL PORTS

This section discusses use of the two RS232C serial ports, and gives some examples of typical installations.

3.4.1 Serial Port Initialization

Before you can use the board's serial ports, they must be properly enabled and initialized. Sometimes the application program that accesses the port's hardware does this automatically. Usually the system configuration and boot process does this. When the system boots, the ROM BIOS enables or disables each port based on parameters in the Configuration Memory. You can enable or disable either port with SETUP. When you use SETUP to enable or disable a port, the change does not take effect until you reboot the system.

At boot time, DOS initializes the serial ports. Although this might vary with different types and versions of DOS, typical settings are 2400 baud, even parity, 7 bits, and 1 stop bit.

NOTE

COMn (n=1, 2) is a logical designation, not a physical value. When the system boots, the ROM BIOS scans both serial port addresses, and installs the first port it finds as COM1. If it finds a second one, it installs that one as COM2. If you disable serial port 1, then serial port 2 becomes COM1, not COM2. There must be a COM1 elsewhere in the system for the onboard secondary serial port to become COM2.

3.4.2 Serial Console Option

You may want to substitute an RS232C serial device (terminal, remote computer, and so forth) for the standard video controller, monitor, and keyboard normally used as the DOS console device. Connect the serial console device to one of the serial ports; the ROM BIOS contains support for serial input and output. The Configuration Memory stores serial console support parameters. Use SETUP to install the serial console support.

CAUTION

Be careful when changing the console configuration using SETUP. If you specify *none* for console input and output, there is no console access to the system. You can recover from this by unplugging the serial console from the serial port connector and shorting pins 7/8 on the connector.

SETUP parameters provide separate support for serial console input, and output. You can use a serial keyboard or modem or other device for input, and a serial display terminal or remote computer for output. Or, you can use a standard AT keyboard with a serial display, or use serial input with a standard video display. For example, to use a terminal as the console device for your system, set both the input and output parameters to Serial Port 1, and set the serial baud rate, data length, and stop bits to match the setting of your terminal.

You can use IEEE compatible terminals that implement certain cursor commands, without custom terminal drivers. The commands required and their hexadecimal codes are given in Table 3-3.

HEX	COMMAND
05	Backspace
0A	Line Feed
0B	Vertical Tab
0C	Non-destructive Space
0D	Carriage Return

Table 3-3. Required Commands

After booting this system, the keyboard and screen of the terminal become the system console. The programs you use this way must use ROM BIOS video functions (rather than direct screen addressing) for their display I/O. You can enter keyboard data from both the external serial device and the standard AT keyboard. You can revert to the standard keyboard and monitor by removing the plug from the serial port connector and shorting pins 7/8 of that connector.

NOTE

You cannot use DOS programs that write directly to video RAM on a serial console device.

The Little Board/386SX-IIA CPU is shipped from Ampro with the serial console option disabled. If you do not have a video controller, or if for any other reason you cannot run SETUP, you can force the Little Board/386SX-IIA CPU into serial console mode by shorting pins 4 and 8 (RTS, R1) of J3 (Serial 1). The port will become active at 9600 baud, 8 data bits, 1 stop bit, and no parity.

When the system boots DOS, it initializes the serial ports to 2400 baud (typical). To preserve the serial port parameters stored in SETUP, the ROM BIOS deletes the *console port(s)* from the internal COM-Port Table normally used by DOS to locate the serial ports. With the port(s) deleted from the COM port table, DOS cannot change parameters configured in SETUP. There is an option in SETUP to retain the console ports in the COM table. This means the ports are returned to DOS default values when the system boots. If you use a serial console, be sure to select the option that *deletes* the console ports from the COM Table. See Appendix A for more information on installing serial console driver options with SETUP.

Serial Console Cabling and Setup

Set the serial console device to the same data format as the board's serial port. Normally, the serial port's Data Set Ready (DSR) and Clear To Send (CTS) input handshake signals must be true (*active*), for the ROM BIOS to send data out. (This hardware handshake can be disabled with SETUP). When hardware handshaking is enabled, be sure to connect the DSR and CTS signal inputs to appropriate handshake signals from the external serial device's serial interface connector. As an alternative, loop the board's serial output handshake signals to its input signals as follows: DTR out, to DSR in; RTS out, to CTS in (J2 or J3, 2/7 and 4/6).

3.4.3 Using a Serial Modem

You can use either of the RS232C ports as a modem interface. Most PC communications programs control the serial port hardware directly, rather than using DOS or ROM BIOS functions.

When installing a modem, be sure to connect appropriate input and output handshake signals, depending on what your communications software requires. Most communications programs initialize the serial port's baud rate and data characteristics; if yours does not, use the DOS MODE command to initialize the port.

Many powerful communications programs are available to control modem communications. Some of these programs offer powerful "script" languages that allow you to generate complex automatically functioning applications with little effort. Examples are: PCTALK, PROCOMM and XTALK.

3.5 USING FLOPPY DRIVES

The ROM BIOS includes DOS-compatible floppy disk functions. Use standard DOS commands for all floppy functions, including formatting, copying, verifying, and so forth. This includes all the DOS 5-1/4 inch and 3-1/2 inch floppy formats -- 360K, 720K, 1.2M, and 1.44M -- if you use an appropriate DOS (see Chapter 2). In addition, the ROM BIOS supports dual capacity use of high density floppy drives. That is, you can read and boot from 360K floppies in a 1.2M 5-1/4 inch drive, and 720K floppies in a 1.44M 3-1/2 inch drive.

When the board is shipped, the Configuration Memory is initialized to expect the first physical floppy drive (A) to be a 360K 5-1/4 inch drive. However, the ROM BIOS automatically adapts to whatever type of drive you have connected as drive A. Therefore, you can boot your system from any standard drive.

3.5.1 Drive Parameter Setup

The Configuration Memory contains the information on the number and type of floppy drives in the system. If the drives connected to the system do not match the parameters in the Configuration Memory, an error message

is displayed indicating the mismatch, and instructing you to *Run SETUP*. Once you have booted DOS, you can reconfigure the system for your floppy drive configuration with SETUP.

3.5.2 Single-Floppy Configurations

A handy feature of DOS is built-in support for single-drive systems. If you specify one floppy in SETUP, DOS automatically assigns drive letters A and B to that drive. You can copy files between two diskettes on one drive; DOS will prompt you to change diskettes when needed.

3.6 USING SCSI HARD DISK DRIVES

One unique feature of the Little Board/386SX-IIA is that its ROM BIOS contains hard disk support functions that map to the Small Computer System Interface, as well as the IDE drive interface, or a conventional AT bus hard disk controller (not included). This offers added flexibility with SCSI device support. SCSI features interchangeable peripherals, flexible configuration, and easy system upgrading and support.

SCSI hard disks are available to DOS through standard ROM BIOS functions (INT 13). These are in the SCSI BIOS, part of the ROM BIOS. The ROM BIOS hard disk support allows direct system booting from SCSI Common Command Set *direct access devices*. Other types of SCSI direct access devices can be used to provide a compatible hard disk function. These include RAM disks, optical disks, tape drives, and other peripherals.

Most DOS applications run normally in this SCSI-based hard disk environment. Programs nearly always use either DOS or ROM BIOS functions for disk drive access. It is extremely rare for DOS environment software to attempt to access hard disk controller *hardware* directly. If a program does require disk controller *hardware* access, it will need to be modified to use the board's SCSI hardware or SCSI-BIOS functions. You can use low level SCSI functions (in the ROM BIOS) to simplify the task.

A combination of Ampro and DOS utilities are used in the formatting and preparation of SCSI hard disk drives. Utilities for SCSI drive formatting and parking, and other SCSI functions included on the Ampro Common Utilities diskette, and discussed in the Common Utilities technical manual.

3.6.1 Drive Parameter Setup

Several parameters need to be set in the Configuration Memory with SETUP. The following section outlines these.

- **SCSI Initiator ID** -- the Ampro Little Board/386SX-IIA is the SCSI Initiator in its transactions with SCSI Target devices such as hard disk drives. Every SCSI device (Target or Initiator) must have a unique ID, between 0 and 7. Set the CPU ID to 7, because this is the highest priority ID, and the SCSI BIOS resets the SCSI bus on system powerup or reset if the CPU's ID is 7.
- **SCSI Target Device IDs and LUNs** -- the specification of SCSI target device IDs and Logical Unit Numbers (LUNs) are stored in the Configuration Memory. The SCSI ID for Target devices can be 0 to 7. This is usually set by jumpers or switches on the device. Unless you operate multiple devices from a single SCSI Target controller, use LUN 0. For example, a typical system with a SCSI drive has the drive configured as ID0, LUN0. If you have multiple, properly formatted SCSI drives, the ROM BIOS will install them as multiple DOS hard disk drives when the system boots.
- **BOOT Device Specification** -- the choice to boot the system from a hard or floppy drive is stored in the Configuration Memory. Select this option from SETUP's Extended Options/Peripheral Configuration menu. When you select Hard Drive, the drive shown on this menu as 1st Hard Disk becomes the boot drive.
- **SCSI Disk I/O Retries** -- specify the number of read/write retries when using SCSI drives as DOS drives.
- **SCSI BIOS Services Enable/Disable** -- enable or disable the SCSI functions in the ROM BIOS with SETUP. If you use SCSI under DOS, you must enable this option. Disabling the SCSI BIOS services will speed up system booting when you don't use the SCSI port.

NOTE

Do not define disk drive parameters for the "AT HDC Disk" options in SETUP's Standard (CMOS) Setup menu for SCSI-connected drives. These parameters are for defining drives connected to an AT bus hard disk controller, or for drives connected to the IDE drive interface.

3.6.2 Preparation for DOS Use

To use a hard disk drive on the SCSI port, you must properly connect and jumper it. Set the appropriate parameters in SETUP. Usually, formatting and other preparation for use are simple.

Here is a brief procedure you can use to prepare a SCSI hard disk drive for use with DOS:

1. **Setting the SCSI Device IDs** -- using the options in SETUP's Extended SCSI and Hard Disk Configuration menu, specify the appropriate SCSI device IDs for both the drive (this ID must match jumpers on the drive or drive controller) and the Ampro CPU board. If you set the CPU board to SCSI ID 7, a SCSI bus Reset will be issued on system powerup or system reset. Typically, SCSI drives come preset to SCSI ID 0, LUN 0. The "SCSI Initiator ID" option sets the CPU board's SCSI Initiator ID; *SCSI Disk Map* options are used to specify the ID and LUN of up to seven SCSI drives; *DOS Disk Map* options designate one or more SCSI devices for access by DOS. For example, in a system with one SCSI drive, set *SCSI Initiator* to 7, *SCSI Disk 1* to Id 0, Lun 0, and *1st Hard Disk* to SCSI Disk 1.

2. **Low Level Formatting** -- The low level format erases all data from the drive and prepares it for use. Often, the low level format function eliminates bad blocks from the usable area of the drive. It replaces bad blocks with spare ones. Most manufacturers of embedded SCSI drives format them prior to shipment. Still, it is best to perform a low level format prior to using a drive for the first time. Use the Ampro SCSIFMT utility to perform the low level format of the drive. The drive must be SCSI *Common Command Set* (CCS) compatible, to be formatted by the SCSIFMT utility.

3. **Drive Partitioning** -- Reboot the system from a floppy diskette in drive A containing the operating system, and run the DOS FDISK utility as described in your DOS documentation. You may be creating one or multiple partitions, depending on the size of the drive and the partition limitations of the particular DOS you are using.

4. **Final Preparation for System Access** -- Again, reboot the system from a floppy diskette in drive A. What you do next depends on which operating system you use.

   DR DOS: Run the DOS SYS command, to copy the operating system to the hard disk drive(s) that you have created in the above steps. Finally, copy anything else you need to the drive(s), and then reboot the system *without* the floppy diskette in drive A to verify that you have installed everything properly.

   PC-DOS or MS-DOS: Use the FORMAT /S command to copy the operating system to the DOS *boot* drive (drive C); or the FORMAT command for drives or drive partitions other than the DOS boot partition. Finally, copy anything else you need to the drive(s), and then reboot the system *without* the floppy diskette in drive A to verify that you have installed everything properly.

3.7 USING IDE HARD DISK DRIVES

The ROM BIOS supports one or two hard disk drives connected to the IDE interface. You can use IDE drives exclusively, or with SCSI hard disk drives. In DOS applications, the total number of drives used (SCSI and IDE) can be up to eight under DR DOS, but is limited to two under older versions of PC-DOS or MS-DOS. Check the documentation for the DOS you use.

One advantage of using the IDE interface is that you can use operating systems or programs that *talk* directly to AT hard disk controllers. This includes multitasking operating systems such as Unix, Xenix, QNX, etc. To

configure the system for use with one or two IDE drives, set several parameters with SETUP. As outlined in the next section. When using the setup program or other Ampro software utilities, refer to IDE drives as drives connected to an *AT bus hard disk controller*.

- **Drive Types** -- The Configuration Memory contains the parameters that specify the physical format of the each IDE drive. It includes the total number of cylinders, number of heads, cylinder to begin precompensation, landing zone cylinder number, and the number of sectors per cylinder. The drive manufacturer supplies these parameters. Use the SETUP drive definition options (first menu page of the Standard (CMOS) Setup) to configure your system for the drive(s) you use.
- **Drive Selection** -- besides specifying the physical characteristics of each IDE drive, you also must specify how they are to be used by the ROM BIOS. Use the *SETUP Extended SCSI and Hard Disk Configuration menu* (third menu page) for this. Specify one or two IDE drives in the DOS disk map as DOS drives to be installed by the ROM BIOS at system boot time.
- **BOOT Device Specification** -- The choice to boot from hard or floppy disk is on the *Extended Options/Peripheral Configuration menu* in SETUP. Select either Floppy *Drive* or *DOS Hard Drive*. When you select *DOS Hard Drive*, the *1st Hard Disk* in the *DOS Disk Map*, (above), becomes the boot device.

Once you have set the system's Configuration Memory, the IDE drive(s) can be formatted and otherwise prepared normally. Refer to your operating system, and disk drive documentation for specific procedures and requirements.

3.8 WATCHDOG TIMER

A watchdog timer is included in the Little Board/386SX-IIA. It is based on using the alarm function of the onboard battery-backed real time clock. This timer is set to an initial value with the SETUP function. This value can be changed from the DOS command line of from a batch file, using the WATCHDOG utility, available on the Common Utilities diskette. Or, you may use the watchdog timer functions from within an application. Chapter 4 explains how software can access a ROM-BIOS watchdog timer function provided for this purpose.

CHAPTER 4

ADVANCED TOPICS

4.1 INTRODUCTION

Except for the unique functions discussed in this chapter, the Little Board/386SX-IIA is functionally identical, in terms of hardware and software, with the IBM PC/AT computer. This chapter briefly discusses standard PC/AT features and functions. However, it focuses on the non-standard functions unique to the Ampro Little Board/386SX-IIA.

For detailed technical information on the architecture and functions of a PC/AT and its normal software environment, consult publications such as:

- **Microsoft Disk Operating System** -- Version 3.3 or later
  Microsoft Corporation
  One Microsoft Way
  Redmond, WA 98052-6399
- **The Peter Norton Programmer's Guide to the IBM PC**
  Microsoft Press
  A Division of Microsoft Corporation
  10700 Northrup Way
  Box 97200
  Bellevue, Washington 98009
- **Interfacing to the IBM Personal Computer**
  Lewis C. Eggebrecht
  Howard W. Sams & Co., Inc.
  A Subsidiary of Macmillan, Inc.
  4300 West 62nd Street
  Indianapolis, IN 46268 USA
- **Personal Computer Bus Standard P996 (Draft) and P996.1 (PC/104 specification)**
  IEEE
  445 Hoes Lane
  Piscataway, NJ 08854

Many of the devices on the Little Board/386SX-IIA are programmable. The following explanations presume use of the standard Ampro ROM BIOS.

4.2 OVERALL ARCHITECTURE

The Little Board/386SX-IIA is essentially a complete PC/AT compatible system, including the equivalent of a motherboard and three or four expansion cards. It is constructed on a single board with the same dimensions as a 5-1/4 inch floppy disk drive.

The following sections discuss the Little Board/386SX-IIA's onboard subsystems. These features are grouped as standard AT functions and unique functions, those not found in standard AT systems.

4.2.1 Standard AT Compatible Functions

- **AT Motherboard Logic** -- this includes the CMOS 80386SX CPU, system and extended memory (up to 16M bytes), ROM BIOS, DMA controller, interrupt controllers, system clocks, programmable timers,

keyboard interface, speaker port, battery-backed real-time clock and CMOS RAM, and a socket for a math coprocessor.

- **AT Expansion Bus** -- standard 8 MHz AT bus (I/O channel interface) expandable with Ampro MiniModules. You can use conventional AT and PC compatible expansion cards with additional hardware available from Ampro.
- **Floppy Disk Controller** -- a complete PC/AT floppy disk controller.
- **Serial Controller** -- Two RS232C serial ports with 16 byte FIFO buffers.
- **Parallel Controller** -- One parallel (printer) port (with bidirectional data option, IEEE 1284 compatible).
- **Integrated Device Electronics (IDE) Hard Disk Interface** -- an interface for hard disk drives with built-in disk controllers.

4.2.2 Unique Functions

- **Small Computer System Interface (SCSI) Host Adapter** -- a full-function ANSI X3.131 compatible asynchronous SCSI bus interface. The board's ROM BIOS supports one or more SCSI direct access devices as AT compatible hard disks.
- **Byte-wide Memory Sockets** -- three byte-wide sockets, a 32-pin DIP, and two 32-pin PLCCs. All support Flash EPROMS from 32K to 512K and EPROMs from 128K to 1M. The DIP socket supports SRAMs from 32K to 512K. You can use all three byte-wide devices as directly accessible data or program memory, BIOS extensions, or as DOS solid state disk (SSD) drives (with Ampro SSD Support Software). All three byte-wide sockets feature software controlled write-protect for SRAMs and Flash EPROMS.
- **Flash Programming Control** -- Flash programming voltage is hardware and software controlled. Supply +12 volts (typically, 30 mA) during Flash EPROM programming. This power is controlled by jumper W16 and a BIOS call. The BIOS call is discussed later in this chapter. Jumpering is covered in Chapter 2.
- **Configuration EEPROM** -- a 2 Kbit serial Electrically Erasable, Programmable ROM. It stores system configuration data and 512 bits of OEM data. Ampro battery-free operation safeguards battery dependent CMOS RAM data (except date and time) by copying it to the system Configuration Memory EEPROM.
- **Power Fail NMI** -- a power monitor circuit that generates a non-maskable interrupt and ultimately switches certain circuits to battery backup power as input voltage falls.
- **Watchdog Timer** -- a timer with a SETUP selectable period. Should it time out, various results occur, depending on board jumpering.

4.2.3 System Memory Map

The 80386SX CPU has 24 address lines that appear on the PC/AT bus, enabling addressing of 16M bytes of physical memory, and up to 64 terabytes of virtual memory. The maximum segment size is 4G bytes. Table 4-1 shows the allocation of the 16M bytes of memory space.

The DRAM, the byte-wide sockets, and ROM BIOS occupy the first megabyte (starting at 00000h). You can locate up to 16M bytes of DRAM onboard with 256K, 1M and 4M byte SIMMs. Or, you can use conventional memory expansion boards on the AT bus. Memory on the bus limits system performance as it is accessed much more slowly than onboard DRAM. Optional onboard extended memory begins at 100000h.

Memory Address	Function
FE0000-FFFFFFh	Duplicates BIOS at 0E0000-0FFFFFh.
100000-FDFFFFh	Extended memory
0F0000-0FFFFFh	64K ROM BIOS.

0D0000-0EFFFFh	Byte-wide memory sockets S0, S1, and S2 if enabled. Otherwise, free.
0C0000-0CFFFFh	Reserved for expansion bus ROM's; May contain
	DRAM for a video BIOS if shadowing is enabled.
0A0000-0BFFFFh	Normally contains video RAM, as follows: CGA Video: B8000 - BFFFFh Monochrome: B0000 - B7FFFh EGA and VGA Video: A0000 - AFFFFh
000000-09FFFFh	Onboard DRAM.

Table 4-1. Little Board/386SX-IIA Memory Map

I/O Address	Function
03F8 - 03FFh	Primary serial port
03F0 - 03F7h	Floppy disk controller ports (37C665) 3F2 - FDC Digital output register 3F4 - FDC Main status register 3F5 - FDC Data register 3F7 - FDC Control register
03F6h, 03F7h	IDE Control registers
03D0 - 03DFh	CGA display adapter (option)
03C0 - 03CFh	EGA or VGA display adapter (option)
03B0 - 03BFh	Monochrome display adapter (option)
0378 - 037Fh	Primary parallel printer port
X370 - X377h	Ampro controls
0330 - 0337h	SCSI controller ports
02F8 - 02FFh	Secondary serial port
0278 - 027Fh	Secondary parallel printer port
01F0 - 01F7h	IDE controller
00C0 - 00DFh	DMA controller 2 (8237 equivalent)
00A0 - 00A1h	Interrupt controller 2 (8359 equivalent)
0080 - 008Fh	DMA page registers (74LS61 equivalent)
0070 - 0071h	Real time clock and NMI mask
0061	Port B register
0060, 0064h	Keyboard controller (8042 equivalent)
0040 - 0043h	Programmable timer (8254 equivalent)
0022, 0023	Reserved
0020 - 0021h	Interrupt controller 1 (8359 equivalent)

Table 4-2. Little Board/386SX-IIA I/O Map

4.2.4 System I/O Map

Table 4-2 is a list of the I/O port assignments used on the Little Board/386SX-IIA. Except for the SCSI controller, an Ampro-specific control port, and control ports in the ASIC chip set, the I/O port functions and addresses shown in Table 4-2 are all equivalent to their counterparts in a standard AT system from both a hardware and software perspective.

Typically, the ROM BIOS provides all the services needed to use the onboard devices and devices connected to I/O ports. If you need to directly program the standard functions, refer to a programming reference for the IBM PC and PC/AT.

4.3 AT MOTHERBOARD LOGIC

The Little Board/386SX-IIA contains the equivalent of an entire PC/AT motherboard. This section briefly describes the motherboard subsystem in the Little Board/386SX-IIA.

4.3.1 CPU

A powerful 80386SX microprocessor is the central element in the Little Board/386SX-IIA. It features full 32-bit internal architecture with 8 general purpose 32-bit registers. It supports 8-, 16-, and 32-bit data types.

The Little Board/386SX-IIA operates at 25 MHz. Clock frequency is determined by the value of the master clock generator at U13, which operates at twice the CPU clock rate.

The 80386SX, a high performance microprocessor, features a 32-bit internal architecture and 16-bit external data bus. It has a versatile integrated memory management unit that can support virtual memory operating systems while remaining fully compatible with other 80286 and 80386DX microprocessors. It includes a "virtual 8086" mode that permits running multiple 8086 processes with all the protection features needed to handle multiprocessing issues. In addition, the 80386SX uses instruction pipelining, on-chip address translation, and high bus bandwidth to execute code more efficiently than other 80x86 microprocessors.

4.3.2 ROM BIOS Socket

The BIOS can be stored in an EPROM in socket U28 or in a reprogrammable Flash EPROM at U24. The BIOS is by Award, with substantial augmentations by Ampro. The functions in this manual presume use of the standard Ampro ROM BIOS. The ROM BIOS is on the 8-bit internal XD bus from location 0F0000h to 0FFFFFh and appears also at the very top of the 16M byte address space at FF0000h to FFFFFFh. Unlike some AT implementations, the BIOS is *not* mirrored at 0E0000h - 0EFFFFh.

To improve system performance, you can shadow the ROM BIOS, the Video BIOS, or both. A SETUP option controls shadowing. To shadow, the ROM contents are copied to DRAM, and run from there rather than ROM. DRAM access is done at *normal* speed. It is 16-bits wide, and (if you install enough memory) interleaved. ROM is 8 bits wide, and it is accessed at *slow* speed. The minimum DRAM for shadowing is 1M byte. Shadowing is more than three times as fast as non-shadowed operation.

4.3.3 Powerfail Handling

If you have jumpered W2, the power management circuitry generates a power-fail NMI if the +5 volt power falls below 4.7 volts. When this occurs, the BIOS detects the NMI and displays the message "Power Fail NMI." At this point you have two options; to mask the NMI and continue, or reboot the system.

If you want to do something else with the NMI, you must provide your own power fail NMI handler and patch the NMI interrupt vector address to install it. To discriminate between the power-fail NMI and NMIs from other sources, execute a C0 command to the keyboard controller to read the P1 input port. The power-fail NMI signal only lasts 200 µSec, so interrogate it first. For additional information on installing NMI handlers, consult standard PC/AT documentation.

Here is a simple assembly language routine that you can use in a power fail NMI handler. It detects if the source of the NMI is the power fail logic.

```
; Test for source of I/O channel check.
; Power-Fail NMI lasts only 200 uSec, interrogate it first.
         IN AL,60h      ;  Clear keyboard input buffer.
         JMP $+2
         MOV AL, 0C0h   ;  Read kbd controller input line.
         OUT 64h,AL     ;

  Kloop: JMP $+2        ;  Wait for data ready
         IN   AL,64h    ;
         TEST AL,1      ;
         JZ Kloop       ;
         IN  AL,60h     ;  Get data
         AND AL,01h     ;
         JNZ NOT-PF     ;

; Power fail handler code
         XXX            ;  XXXX

  NOT_PF         ;  Service I/O Channel check
```

4.3.4 DRAM and System Performance

There is a performance issue related to the amount of memory installed on the board. System performance may be improved by shadowing the ROM BIOS (and video BIOS, if you choose).

If you select the shadow option, the contents of the ROM are copied to RAM and executed from there. Programs execute from RAM much faster than from ROM, as RAM is 16-bits wide and ROM is 8-bits wide. Also, ROM is accessed at low speed and RAM is accessed at normal speed. To shadow the BIOS you must have at least 1M byte of memory. You must also enable shadowing in SETUP.

Shadowing both the ROM and VIDEO BIOS results in maximum system performance. Section 2.3.2 shows the various memory configurations you may use.

Application and utility programs can access extended memory, that is memory above the 1 MB address boundary. You must use special programming techniques when writing software that accesses extended memory.

DRAM is refreshed in the standard manner, with a 15 μSec time base generated by Timer 1. The REFRESH signal on the AT bus is true (Logic 1) whan a DRAM refresh cycle occurs.

4.3.5 Interrupt Controllers

A pair of 8259A compatible interrupt controllers in the core control logic provide fifteen prioritized interrupt levels. The onboard interfaces and controllers use some of these. You can use the others for peripherals or devices on the AT expansion bus. Table 4-3 lists the typical interrupt usage.

INTERRUPT	FUNCTION
IRO0	ROM BIOS clock tick function, from Timer 0
IRQ1	Keyboard controller output buffer full
IRQ2	Cascade input for IRQ8-15
IRQ3	Secondary serial port (if present)
IRQ4	Primary serial port (if present)
IRQ5	Parallel port option
IRQ6	Floppy controller (if present)
IRQ7	Parallel port option
IRQ8	Battery-backed clock alarm (watchdog timer)
IRQ9*	Some EGA or VGA controllers (if present)
IRQ10	Available
IRQ11	Available
IRQ12	Available
IRQ13	Internal use, not available
IRQ14	IDE or bus hard disk controller (if present)
IRQ15	Available
* Corresponds to IRQ2 on a PC's expansion bus.	

Table 4-3. Interrupt Channel Assignment

4.3.6 DMA Controllers

The core control logic includes two 8237A compatible DMA controllers providing seven DMA channels. The hardware and software implementation of these controllers, and the additional address generation logic included, are functionally identical to a standard AT. Table 4-4 shows how the Little Board/386SX-IIA uses the seven DMA channels.

CHANNEL	FUNCTION
0	Available for 8-bit transfers
1	Available for 8-bit transfers
2	Floppy controller (if present)
3	Onboard SCSI (if present)
4	Cascade for channels 0-3
5	Available for 16-bit transfers
6	Available for 16-bit transfers
7	Available for 16-bit transfers

Table 4-4. DMA Channel Assignment

As in all AT compatible computers, several distinctions exist between the features of DMA Channels 0-3 and Channels 5-7:

- **Channels 0-3** -- used for 8-bit transfers between 8-bit I/O adapters and both 8-bit and 16-bit system memory. For these channels, the 8237A compatible DMA controller generates addresses A0-A15. DMA

page registers generate addresses A16-A23. These channels can transfer data throughout the AT's 16M byte address space, with a maximum block transfer size of 64K bytes.

- **Channels 5-7** -- these three channels support 16-bit transfers, between 16-bit I/O adapters and 16-bit system memory. For these channels, the 8237A compatible DMA controller logic generates A1-A16. Page registers generate A17-A23. These channels can transfer data throughout the AT's 16M byte address space, with a maximum block transfer size of 128K bytes. Channels 5-7 do not support address bit A0, so they cannot transfer data on odd byte boundaries.

The DMA channels have these restrictions:

NOTE

During a DMA block transfer, addresses *cannot* automatically cross page boundaries. On Channels 0 to 3, the page boundaries are at 64K. Channels 5 to 7 have 128K boundaries. The ROM BIOS disk services handle boundary crossing automatically.

DMA Transfer Rate

The Little Board/386SX-IIA's DMA controller operates at 4 MHz with one wait-state. The single cycle DMA transfer rate is 4 MHz with 9 cycles per transfer. This results in a maximum transfer rate of 444K bytes/sec for 8-bit transfers and 888K bytes/sec for 16-bit transfers. The effective rate is lower due to interspersed CPU cycles.

4.3.7 Programmable Timers

The core control logic include an 8254 compatible timer/counter. This device is used as in a standard PC/AT. A 1.109 MHz clock, derived from a 14.318 MHz oscillator, drives each channel of the 8254. This oscillator can be internally divided down to provide a variety of frequencies.

Table 4-5 summarizes the standard use of this device's timers. You can also use timer 3 as a general purpose timer if you don't need the speaker function.

TIMER	FUNCTION
0	ROM BIOS clock tick (18.2 Hz)
1	DRAM refresh request timing (15 uSec)
2	Speaker tone generation time base

Table 4-5. Timer Assignment

4.3.8 Keyboard Interface

The board uses a standard AT keyboard controller. A four-wire cable, carrying +5 volts, ground, data and clock, connects the keyboard to the board at J5.

The system will operate without a keyboard. To prevent the POST (power-on-self-test) from stopping and issuing a Keyboard Error message, specify "No Keyboard Error Halt" on the first page of SETUP.

Besides generating the keyboard interface, the keyboard controller contains a digital I/O port used for other system functions:

- It operates the A20 Gate and 80386SX CPU reset associated with system protected mode control.

- It provides several control signals for onboard logic control, including: mono/color jumper; keyboard disable switch sensing; and power fail NMI status.

4.3.9 Speaker Interface

One of the core control logic devices includes logic for the speaker port. The speaker logic signal is buffered by a transistor amplifier, and provides about 100 milliwatts to an external 8 ohm speaker.

The audio output is based on two signals: the output of Timer 2; and the programming of two bits, 0 and 1, at I/O port 61h. Bit 1 of I/O port 61h is one term of a 2-input AND gate in U11. The other term is the output from Timer 2. Thus, setting bit 1 to a logic 1 enables the output of Timer 2 to the speaker, and a logic 0 disables it. If you disable Timer 2 by setting bit 0 of port 61h to a 0, then you can use bit 1 of port 61h to control the speaker directly.

4.3.10 Battery-Backed Clock

The AT compatible date/time clock includes a CMOS static RAM for Configuration Memory. This is standard in ATs. System configuration data is stored in the CMOS RAM as in most ATs. Unique to the Little Board/386SX-IIA is automatic back-up of this data in the Configuration Memory EEPROM by the SETUP function.

The board has a 1/2 AA lithium battery located near the power connector. The board can operate without the battery. As the CMOS RAM's contents are backed up in the configuration EEPROM, configuration data is not lost when the battery is removed. Should battery power be lost, the Ampro ROM BIOS detects that the CMOS RAM's data is invalid and loads the correct data from the configuration EEPROM.

4.3.11 AT Expansion Bus

The PC bus signals on P1A and P1B include an 8-bit bidirectional data bus, 20 address lines, 6 levels of interrupt, three DMA channel handshake lines, several other control lines, and power and ground for expansion cards. The first 62 pins of P1A, P1B (A1-31, B1-31) correspond to the standard signals on the 62-pin PC bus edgecard backplane; the last two pins of (A32, B32) are extra grounds to enhance system reliability. An independent 14.318 MHz oscillator made up of a crystal and U13 provides the bus OSC signal. The OSC signal is not synchronous to other expansion bus signals.

For compatibility with AT standards, wait states are in all expansion bus I/O and memory cycles. I/O cycles include 4 wait states. Memory cycles include 1 wait state. The bus operates at 8 MHz. With certain minor exceptions, it meets the IEEE P996 (draft) specifications for the ISA bus.

The AT bus signals on P2C, P2D include six high order address lines, the high order data byte, five additional interrupt requests (IRQs), four additional DMA channel handshake signal pairs (DRQ/DACKs), and several additional control signals. You can latch the upper six address lines (LA17-LA23) with BALE.

4.4 SUPER I/O CONTROLLER

The board's Super I/O controller a contains the equivalent of an entire AT controller card in a three chip set. The controller integrates the functions of a floppy disk controller, a serial controller, and a parallel controller:

4.4.1 Floppy Disk Controller

The Super I/O Controller integrates the following functions:

- Formatter/controller
- Digital data separation
- Digital write precompensation
- Data rate selection

- Clock generation
- Drive interface drivers and receivers
- Drive motor control
- AT compatible control registers

The 37C665 is compatible with the industry standard NEC765 floppy controller, and associated external devices, as in a standard AT. It uses data rates of 125, 250, 300, and 500K bits/Sec.

The system supports dual capacity drives, which allow a single drive to read both 360K byte and 1.2M byte diskettes. These are standard AT drives in which the data rate shifts between 250K and 500K bytes/Sec, but the drive rotational speed stays constant.

The 37C665 (equivalent) floppy controller contains a highly reliable 2nd order digital data separator. The device also generates write precompensation. Because both critical circuits are fully digital, the floppy drive interface is highly reliable and temperature independent.

The ROM BIOS configures the floppy interface based on the Configuration Memory in the battery-backed CMOS RAM in the clock chip, and backed up in the EEPROM Configuration Memory. You can use any combination of supported drives.

The floppy controller uses interrupt channel IRQ6, and DMA channel DRQ2 and DACK2. If you don't use floppies, these and the floppy controller's I/O port addresses are available. You could substitute a floppy controller card on the AT expansion, if you disable the floppy controller in SETUP and remove jumper W6. Refer to Chapter 2 for jumpering information and for the port's connector pinout.

4.4.2 Serial Controller

The Super I/O controller provides two AT-standard 16C550 compatible, RS232C serial ports as full duplex asynchronous communications channels. Many of their features are software selectable. These include: baud rate (up to 57.6K baud); word size (5-8 bits); and stop bits (1, 1.5, or 2). The RS-232 specification limits the drivers usable baud rate to 19.2 Kbaud as the maximum slew rate is 30 volts/uSec.

Each serial port has three output and 5 input signals with EIA compatible buffers. Onboard DC-to-DC converters generate the ±10 volts required by the RS232C drivers. You can disable either serial port with SETUP. When you disable a port, its I/O port addresses and system interrupt become available for other devices. Refer to Chapter 2 for the connector pinouts of these two ports.

4.4.3 Parallel Controller

The parallel printer port is functionally identical to a standard AT port with one exception: in a conventional AT, when you read the eight data lines and the four control lines, you read the data you just wrote to them. On the Little Board/486SLC-II, you can sense the state of the lines as they are influenced by an external device. Thus, you can use the parallel port as a *bidirectional* data port with up to 12 output lines and 17 input lines. This can be very valuable in custom applications. For example, you might use it to control an LCD display, scan keyboards, sense switches, or interface with optically isolated I/O modules. All data and interface control signals are TTL compatible.

In SETUP, you can configure it as either disabled, the primary parallel port or the secondary parallel port. These differ in the I/O port base address (378h or 278h). If you disable the port, its I/O port addresses and system interrupt become available for other devices. Any changes you make take effect the next time you boot the system.

The default mode of the port is AT-compatible, that is, output only. To use the port as a bidirectional data port, set it to *Enhanced Mode* with a BIOS call. Here is an example of code to do that.

```
MOV  AH,0CDh        ;  AMPRO command
```

```
MOV  AL,0Ch          ;  AMPRO function
MOV  BX,01h          ;  Enhanced mode
                     ;  (00 for output-only mode)
INT 13H
```

This code leaves the port in input mode. Once the port is in Enhanced Mode, you can directly access the control register without using the BIOS. The port address is 37Ah for LPT1 and 27Ah for LPT2. You can dynamically change the port between input and output modes by changing bit 5. A 1 in bit five sets the port to input only; a 0 sets it to output only. Here is a sample of code for dynamically changing the port direction *after* it is in Enhanced Mode.

```
MOV  DX,37Ah         ;  (27Ah for LPT2)
IN   AL,DX
OR   AL,0010 0000b   ;   set bit 5
OUT  DX,AL
      (or)
AND  AL,1101 1111b   ;   clear bit 5
OUT  DX,AL
```

Besides the eight data lines, you can use the four control lines (-STROBE, -AUTOFD, -INIT, and -SEL IN) as general purpose output lines. Similarly, you can use the five status lines (-ERROR, SEL OUT, PAPER EMPTY, -ACK, and BUSY) as general purpose input lines.

You can read the four control lines and use them as input lines. These lines have open collector drivers with 4.7K ohm pullups. To use a control line as an input line, you must first write to its corresponding bit in the control register. Refer to the polarity column in Table 4-7. If the line is non-inverting, write a 1. If the line is inverting, write a 0. This will cause the output to be set to a TTL logic 1 (as measured on the connector pin). The outputs must be high to be used as inputs. Table 4-6 is a summary of the uses of the parallel port lines.

SIGNAL TYPE	NUMBER OF LINES	FUNCTION
Data	8 lines	Read/Write
Control	4 lines	Read/Write
Status	5 lines	Read Only

Table 4-6. Parallel Port Use

Bit 4 in the control register (Table 4-7) enables the parallel port interrupt. If this bit is high (1), then a rising edge on the -ACK (IRQ) line will produce an interrupt on the interrupt selected by W5, either IRQ5 or IRQ7.

REGISTER	BIT	SIGNAL NAME OR FUNCTION	IN/ OUT	POLARITY	J3 PIN	DB25F PIN
DATA	0	Data 0	i/o	non-inv	3	2
(378h)	1	Data 1	i/o	non-inv	5	3
(278h)	2	Data 2	i/o	non-inv	7	4
	3	Data 3	i/o	non-inv	9	5
	4	Data 4	i/o	non-inv	11	6
	5	Data 5	i/o	non-inv	13	7
	6	Data 6	i/o	non-inv	15	8
	7	Data 7	i/o	non-inv	17	9
STATUS	0	1	---	---	---	---
(379h)	1	1	---	---	---	---
(279h)	2	1	---	---	---	---
	3	-ERROR	in	non-inv	4	15
	4	SEL OUT	in	non-inv	25	13
	5	PAPER OUT	in	non-inv	23	12
	6	-ACK (IRQ)	in	non-inv	19	10
	7	BUSY	in	inverted	21	11
CONTROL	0	-STROBE	out*	inverted	1	1
(37Ah)	1	-AUTOFD	out*	inverted	2	14
(27Ah)	2	-INIT	out*	non-inv	6	16
	3	-SEL IN	out*	inverted	8	17
	4	IRQ Enable	---	---	---	---
	5	-OUT Enable	---	---	---	---
	6	1	---	---	---	---
	7	1	---	---	---	---
*Can also be used as input (see text).						

Table 4-7. Parallel Port Register Bits

4.5 INTEGRATED DEVICE ELECTRONICS (IDE) INTERFACE

The module's IDE interface is for hard disk drives that contain an embedded AT hard disk controller. The advantage of using IDE drives is that you need no other hard disk controller because the controller is in the drive itself. From a software perspective, an IDE drive operates the same as a controller-drive combination on the AT bus.

The IDE interface provides bus signal buffering. You can expect reliable operation with ribbon cables up to 18 inches in length depending on system ambient noise level. You can attach up to two IDE drives to the interface. Each drive must be configured according to the manufacturer's instructions as Drive 1 or Drive 2. This may vary from one drive manufacturer to another.

You can use both IDE drives and SCSI devices in the system at the same time. Through SETUP, you can select a floppy drive, an IDE drive or SCSI drive as the system default boot device.

4.6 SMALL COMPUTER SYSTEM INTERFACE (SCSI)

A 53C80 SCSI controller comprises the SCSI interface. The device is ANSI X3.131 compatible with 48 mA bus drivers. It provides hardware support for bus arbitration, REQ/ACK handshaking, asynchronous SCSI data

transfer, and all required SCSI Initiator and Target functions. The 53C80 is an industry standard, produced by many manufacturers.

Refer to the 53C80 technical manual for additional technical details.

53C80 Technical Manual
NCR Corporation
Microelectronics Division
1635 Aeroplaza Drive
Colorado Springs, CO 80916

For more information on the SCSI interface, refer to the American National Standards Institute document, ANSI X3.131-1986, available from:

American National Standards Institute
1430 Broadway
New York, NY 10018

When the SCSI option is enabled, the 53C80's DMA request output signal connects to DMA channel 3. This channel provides an 8-bit DMA data path to system RAM memory on the Little Board/386SX-IIA. A jumper option (W25) allows you to connect the interrupt output of the 53C80 to the IRQ5 system interrupt. It is not currently used by the Ampro SCSI BIOS. Do not connect it.

The board includes sockets for 220/330 ohm SCSI bus termination. Short jumper W19 to supply power to the SCSI TERMPWR signal. External termination networks may require this signal. As recommended by the SCSI specification, a shottky diode on the board limits current flow from the SCSI TERMPWR line *to* the board. This prevents system damage from occurring in the event other devices on the SCSI bus are also supplying power to the TERMPWR line.

You can eliminate the SCSI function by disabling it in SETUP. Removing the jumper from W12 frees I/O port addresses 330-337h. Removing the jumpers from W23 and W24 frees DMA channel 3 for use by other system components.

4.6.1 SCSI Hard Disk Support

You can use SCSI drives instead of a conventional hard disk controller. Depending on the hard disk configuration you select in SETUP, the ROM BIOS automatically maps hard disk functions to the SCSI interface. It does this using the SCSI direct access device Common Command Set for compatibility with a variety of SCSI disk drives. Due to the use of the SCSI Common Command Set, you can use a variety of commercially available hard disks. Other direct access device options include: optical storage devices, certain types of tape drives, and SCSI solid state disk drives.

The ROM BIOS reads the SCSI Initiator ID from the configuration EEPROM. This ID is used in all SCSI transactions. You set the Initiator ID in SETUP. See Chapter 3. Typically, use the default Initiator ID of 7. The ROM BIOS performs a SCSI bus reset on powerup or system reset when you use this value.

4.6.2 Ampro SCSI BIOS

To make it easy to use SCSI devices and functions not supported by the standard Ampro drivers and utilities, the ROM BIOS includes the SCSI BIOS functions that allow use of the SCSI interface without direct hardware programming.

The SCSI BIOS adds an additional layer of standardization to SCSI. It provides a high level interface for software. The Ampro SCSI BIOS is accessed through an extension of the INT13 ROM BIOS support. SCSI drivers and utilities written around the Ampro SCSI BIOS INT13 extensions will run on any system in which the INT13 extensions are available. (This includes all Ampro's DOS compatible Little Board single board systems.)

If you plan to support SCSI devices using the SCSI BIOS, you should acquaint yourself with the SCSI bus and its protocols. You can obtain a copy of the ANSI SCSI specification, from the American National Standards

Institute. Additional detailed information on the SCSI BIOS is available in application note AAN-8804, available from Ampro.

4.7 BYTE-WIDE MEMORY SOCKETS

4.7.1 The Byte-Wide Sockets

The three byte-wide memory sockets at S0, S1, and S2 support a variety of 28- and 32-pin JEDEC pinout memory devices, including EPROM, Flash EPROM, and page-addressed EPROM. One socket, S0, also accepts SRAM and NOVRAM devices. Chapter 2 gives examples of the memory devices each socket will hold. Ampro's solid state disk (SSD) drive support in the ROM BIOS and optional SSD Support Software treat these sockets as up to three DOS disk devices, containing up to 1M byte of EPROM each. The PLCC sockets (S1 and S2) are wired to accept JEDEC devices up to 1M byte although currently 512K byte devices are the largest available. The DIP socket (S0) will hold currently available 1M byte EPROMs.

The BIOS accesses the byte-wide sockets as 8-bit devices, each with the same memory area, but only one byte-wide socket is enabled at a time. Using SETUP, select the starting address and size of each byte-wide socket used in your application. If you install smaller devices than specified in SETUP, or use page-addressed EPROM's, the devices are "mirrored" (that is, appear at multiple addresses) in the socket's address window.

The byte-wide sockets can be disabled by the ROM BIOS at powerup and boot time via options in the Configuration Memory. Additionally, the sockets can be enabled or disabled under software control, using a special ROM BIOS call provided for this purpose. When you disable a byte-wide socket (with SETUP or a BIOS call), its address space is available on the expansion bus. When you enable a socket, its address space is not available on the bus. When you select one of the byte-wide sockets, the logic automatically deselects the other two. Devices used in the byte-wide sockets must have access times of 250 nS or less.

4.7.2 Accessing Large Devices

For devices larger than 64K bytes, select the 64K byte window size in SETUP. Using a BIOS call, you can select which segment of the device you want to appear in that window. Do this with the upper nibble of the BH register. Table 4-8 gives the byte (in Hex) to write to the BH register to select each segment of a large device. Here is a simple assembly language routine that controls the byte-wide memory sockets. The segment byte is given in binary.

```
MOV  AH,0CDH      ;  AMPRO function call
MOV  AL,nn        ;  Use 03 for S0, 04 for S1, or 0A for S2
MOV  BL,nn        ;  Use 01 to turn ON or 00 to turn OFF
MOV  BH,xxxx0000b ;  The upper nibble of BH contains the segment
                  ;  number for devices larger than 64 K.
INT 13H
```

DEVICE SIZE	64 KB SEGMENTS	SEGMENT ADDRESS (UPPER NIBBLE OF BH)	
128 KB	2	LOWER UPPER	BH=00h BH=10h
256 KB	4	FIRST SECOND THIRD FOURTH	BH=00h BH=10h BH=20h BH=30h
512 KB	8	FIRST SECOND THIRD FOURTH FIFTH SIXTH SEVENTH EIGHTH	BH=00h BH=10h BH=20h BH=30h BH=40h BH=50h BH=60h BH=70h
1 MB	16	FIRST SECOND THIRD FOURTH FIFTH SIXTH SEVENTH EIGHTH NINTH TENTH ELEVENTH TWELFTH THIRTEENTH FOURTEENTH FIFTEENTH SIXTEENTH	BH=00h BH=10h BH=20h BH=30h BH=40h BH=50h BH=60h BH=70h BH=80h BH=90h BH=A0h BH=B0h BH=C0h BH=D0h BH=E0h BH=F0h

Table 4-8. Segment Addressing in Large Memory Devices

4.7.3 Byte-Wide Socket Signals

Jumper arrays W10, W11 and W7 (for S0), W8 (for S1) and W9 (for S2) configure the byte-wide sockets. Table 4-9 lists the signals that appear on the pins of the arrays.

W7 Pin	Signal	Description
1	--	No connection
2	Vpp	Programming power for 12V Flash devices
3	--	No connection
4	A18	Address A18 (static)
5	Pin 1	Connection to pin 1 of the byte-wide socket
6	A19	Address A19 (static)
7	Pin 31	Connection to pin 31 of the byte-wide socket
8	-SMEMR	Write strobe
9	Pin 29	Connection to pin 29 of the byte-wide socket
10	SA15	Address SA15 from the expansion bus
11	Pin 3	Connection to pin 3 of the byte-wide socket
12	SA14	Address SA14 from the expansion bus
13	A17	Address A17 (static)
14	Pin 30	Connection to pin 30 of the byte-wide socket
15	Vcc or backup battery	Connected to the center pin of W10. W10-1 connects to the backup battery; W10-3 connects to +5V. Also connects to pin 32 of byte-wide socket
*W11-1/2 - Vcc W11-2/3 = Vcco, backup battery power. DO NOT use Vcco for EPROMs See 2.2.2		

W8 Pin	Signal	Description
2	BA19	Buffered Address 19; BH register, bit 7
3	S1-1	Socket S1, pin 1
4	Vpp	Flash EPROM programming voltage (through W13)
5	-PMEMW	Memory Write; Write protect function controlled
6	S1-31	Socket S1, pin 31
7	BA18	Buffered Address 18; BH register, bit 6

W9 Pin	Signal	DescriptionN
2	BA19	Buffered Address 19; BH register, bit 7
3	S2-1	Socket S2, pin 1
4	Vpp	Flash EPROM programming voltage (through W13)
5	-PMEMW	Memory Write; Write protect function controlled
6	S2-31	Socket S2, pin 31
7	BA18	Buffered Address 18; BH register, bit 6

Table 4-9. Byte-Wide Jumper Pin Signals

4.7.4 Write Protection

If you have an SRAM in socket S0, or Flash EPROMs in any byte-wide socket(s), you can write protect them with software. You can do this dynamically with the following code.

```
MOV  AH,0CDh  ;  AMPRO function call
MOV  AL,0Eh   ;  Subfunction
MOV  BL,0     ;  Use 0 to disable write protect (enable writing)
MOV  BL,1     ;  Use 1 to enable write protect (disable writing)
INT 13H
```

4.7.5 Flash EPROM Programming

To program Flash EPROMs you need to supply +12 volts to the board, and jumper W13-1/2 to supply the power to the software controlled Vpp (programming voltage) switch, and turn the switch on at the appropriate time. The following code will turn the Vpp switch on and off.

```
MOV  AH,0CDh ;  AMPRO function call
MOV  AL,09h  ;  Subfunction
MOV  BL,0    ;  Use 0 to turn off +12 Flash EPROM programming voltage
MOV  BL,1    ;  Use 1 to turn on +12 Flash EPROM programming voltage
INT 13H
```

*Jumper W13 must be installed to program Flash EPROMs

4.8 CONFIGURATION EEPROM

System configuration is simpler and more flexible because of the Configuration Memory. The Configuration Memory is a 2,048 bit serial Electrically Erasable PROM (EEPROM). The Configuration Memory serves two purposes: part of it is for SETUP; the rest is for OEM data storage. The ROM BIOS configures the system from the data stored in the SETUP portion of the memory following powerup and reset.

You can store 512 bits of data in the OEM portion of the Configuration Memory. To use the OEM memory directly from programs, you will need to write special software routines to read and write the configuration EEPROM. The software required to read and write bits to this device is complex. To make it easier, the ROM BIOS includes functions for reading and writing the configuration EEPROM. For details, refer to application note AAN-8805, available from Ampro.

You can also use SETUP.COM to read from and write to the configuration EEPROM. First, save the current contents of the EEPROM to a file. Then with a text editor, change any values you want in the lines designated EEPROM40 through EEPROM70. *DO NOT* alter any other values. They are codes for the ROM BIOS setup parameters. After you have entered the data you wish, save the file and use SETUP.COM to load the altered file back to the configuration EEPROM.

Do not use the configuration EEPROM as DRAM. It is limited to 10,000 write cycles. Use the ROM BIOS routine for configuration EEPROM access. This routine automatically maintains a count of the number of times the EEPROM is written. It also maintains a checksum of the contents to insure data integrity.

4.9 SERIAL LOADER OPTION

The Ampro SERLOAD utility is included on the Common Utilities diskette furnished with the Development Kit or System. You can use it to serially download and execute a block of executable code prior to system boot. Data is transferred to the board on a three-wire RS232C cable to COM1 as the target. The host is a remote system sending the data. To use this function, you must enable it on the target board using SETUP.

The host may be any PC or AT compatible, running DOS, and having a standard RS232C serial port. The maximum file size is 64K bytes. The file must be a binary, executable file, with its origin at 0000h. First, run the SERLOAD program on the host system to convert the file to ASCII and add the required control characters and sequences. Then follow the instructions in the Common Utilities manual.

4.10 WATCHDOG TIMER

The purpose of the watchdog timer is to restart the system should some mishap occur. Possible problems include: a failure to boot properly; the application software losing control; temporary power supply problems including spikes, surges, or interference; the failure of an interface device; unexpected conditions on the bus; or other hardware or software malfunctions. Thus, the watchdog timer helps insure proper start-up from power on or reset, and it helps insure proper continued operation of the application software in use.

The Little Board/386SX-IIA ROM-BIOS supports the watchdog timer function in two ways:

There is an initial watchdog timer setting parameter specified using SETUP, which determines whether the watchdog timer should be started prior to system boot, and if so, how long the timeout is (30 seconds, 60 seconds, or 90 seconds).

There is a ROM-BIOS function for use by application software in starting, stopping, or retriggering the watchdog timer function.

The initial timeout (set using SETUP) should be set to be long enough to guarantee that the system can boot and pass control to the application. Then, the application must periodically retrigger the timer so that the timeout does not occur. If the timeout occurs, the system will respond in a way determined by how the watchdog timer jumper is set. See section 2.3.6.

The following example shows a simple assembly language routine that controls the watchdog timer:

```
MOV  AH,0C3h  ;  Watchdog Timer BIOS function
MOV  AL,nn    ;  Use "00" to disable, "01" to enable timer
MOV  BX,nn    ;  Time in seconds (00-FFh) (1-255 Seconds)
INT  15h
```