# CoreModule™ 730
# (Stackable Single Board Computer)
# Reference Manual

P/N 50-1Z019-1010

# Notice Page

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**REVISION HISTORY**

| Revision | Reason for Change | Date |
|---|---|---|
| 00 | Initial Release | July/09 |
| 1.1 | Revised currents in Table 2-5; changed revision of this manual from 00 to 1.1 | Nov/09 |
| 1010 | Added 1.1 GHz model; added JP10 jumper header; changed JP9 to 2 pins in Table 2-3; added BIOS Setup Menus to ch. 4; changed revision of this doc from 1.1 to 1010 | Dec/10 |
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# Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

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# Chapter 1 About This Manual

## Purpose of this Manual

This manual is for designers of systems based on the CoreModule™ 730 stackable Single Board Computer (SBC) module. This manual contains information that permits designers to create embedded systems based on specific design requirements.

**Information provided** in this reference manual includes:

- CoreModule 730 SBC Specifications
- Environmental requirements
- Major chips and features implemented
- CoreModule 730 SBC connector/pin numbers and definitions
- BIOS Setup information

**Information not provided** in this reference manual includes:

- Detailed chip specifications
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry standard busses and signals

## References

The following list of references may help you successfully complete your custom design.

**Specifications**

- SUMIT Specification Revision 1.0, April 4, 2008

  Web site: http://www.sff-sig.org/sumit_spec_v10.pdf
- ISM Specification Revision 1.0, August, 2009

  Web site: http://www.sff-sig.org/ism_spec_v10.pdf
- PCI Express Specification Revision 1.0a

  Web site: http://www.pcisig.com

**Major Integrated Circuit (IC) Specifications**

The following ICs are used in the CoreModule 730 SBC:

- Intel® Corporation and the Atom™ Z510 and Z530 processors (with integrated Northbridges)

  Web site: http://www.intel.com/products/processor/atom/techdocs.htm
- Intel Corporation and the US15W System Controller Hub (SCH)

  Web site: http://download.intel.com/design/chipsets/embedded/datashts/319537.pdf
- Analog Devices and the ADM1032ARMZ-1 CPU Temperature Monitor

  Web site: http://www.analog.com/static/imported-files/data_sheets/ADM1032.pdf
- Chrontel and the SDVO to RGB Converter

  Web site: http://www.chrontel.com/pdf/7317ds.pdf

- PLX and the PEX8505 PCIe to PCIe Switch

  Web site:

  http://www.plxtech.com/products/expresslane/pex8505

- Intel Corporation and the 82574IT Gigabit Ethernet controller

  Web site: http://download.intel.com/design/network/datashts/82574.pdf

- Renesas and the R4F2117R H8S Controller

  Web site: http://http://am.renesas.com/

| **NOTE** | If you are unable to locate the datasheets using the links provided, search the internet to find the manufacturer's web site and locate the documents you need. |
|---|---|

# Chapter 2 Product Overview

This introduction presents general information about the Stackable architecture and the CoreModule 730 Single Board Computer (SBC). After reading this chapter you should understand:

- Stackable architecture
- CoreModule 730 product description
- CoreModule 730 features
- Major components
- Header, Connector, Socket definitions
- Specifications

## Stackable Architecture

Stackable architecture affords a great deal of flexibility in system design. You can build a simple system using only a CoreModule SBC and a Compact Flash card in the Compact Flash socket. To expand a simple CoreModule system, simply add self-stacking ADLINK MiniModule products or 3rd party stackable expansion boards to provide additional capabilities, such as:

- Additional I/O ports
- Analog or digital I/O interfaces

Stackable expansion modules can be stacked with the CoreModule 730 avoiding the need for card cages and backplanes. The stackable expansion modules can be mounted directly to the SUMIT connector of the CoreModule 730. SUMIT-compliant modules can be stacked with an inter-board spacing of ~0.60" (15mm) so that a 3-module system fits in a 3.6" x 3.8" x 2.4" space. See Figure 2-1.

One or more MiniModule products or other stackable modules can be installed on the CoreModule expansion connectors. When installed on the SUMIT connectors, the expansion modules fit within the CoreModule outline dimensions. Most MiniModule products have stack-through connectors compatible with the SUMIT Version 1.0 specification. Several modules can be stacked on the CoreModule headers. Each additional module increases the thickness of the package by 0.60" (15mm). See Figure 2-1.

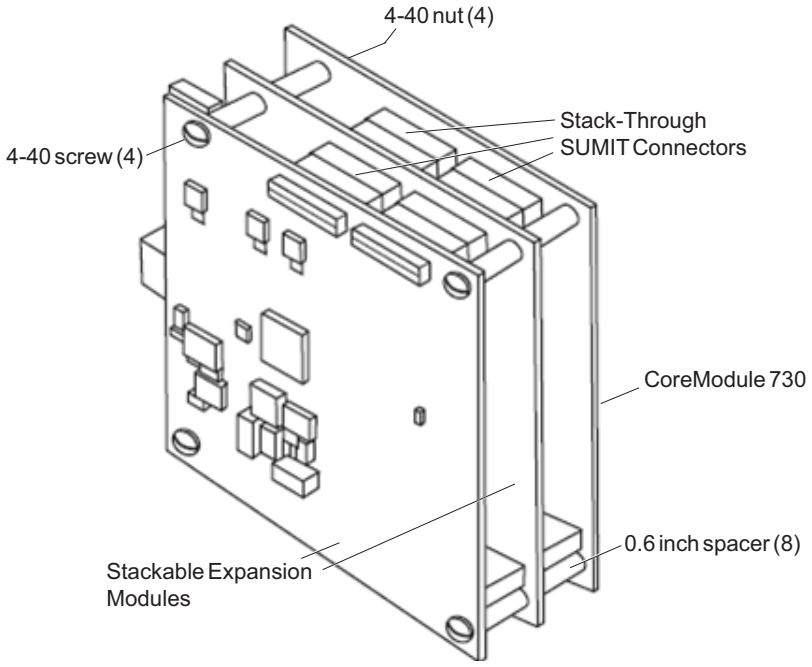


**Figure 2-1. Stacking Modules with the CoreModule 730**

# Product Description

The CoreModule 730 SBC is an exceptionally high integration, x86-based, PC compatible system in the ISM (Industry Standard Module) form factor. This rugged and high quality single-board system contains all the component subsystems of a PC/AT motherboard plus the equivalent of several PC/AT expansion boards.

The CoreModule 730 includes a comprehensive set of system extensions and enhancements that are specifically designed for embedded systems. These enhancements ensure fail-safe embedded system operation, such as a Watchdog Timer and a temperature monitor. This design meets the size, power consumption, temperature range, quality, and reliability demands of embedded applications and requires only a single +5V power source.

Embedded and portable applications benefit from the flexibility of the CoreModule 730, making system design quick and easy. The CoreModule 730 stacks with ADLINK MiniModule products or other SUMIT-compliant expansion boards or it can serve as the computing engine in a fully customized application.

## Module Features

- CPU
  - Provides x86-based Intel Atom Z510 (1.10GHz) or Z530 (1.60GHz) processors
  - Supports Front Side Buses (FSBs) of 100 MHz (for Z510) or 133 MHz (for Z530)
  - Supports IA 32-bit architecture
  - Provides 32kB Unified Instruction Cache and 24kB Write-Back Data Cache
  - Provides Low Power and System Management Modes
- SCH (System Controller Hub)
  - Provides integrated Northbridge and Southbridge
  - Provides CMOS Front Side Bus signaling
  - Integrates a DDR2 memory controller with a single 64-bit wide interface
  - Provides three UHCI USB 1.1 controllers
  - Provides one EHCI USB 2.0 controllers
- Memory
  - Provides one standard DDR2 SODIMM socket
  - Supports 533 MHz Clock Speed
  - Supports non-ECC, unbuffered memory
  - Supports +2.5V DDR2, 533MHz RAM up to 2GB DDR2 SODIMM
- SUMIT Interface
  - Provides up to two SUMIT connectors
  - Supports high-speed serial bus signals
- IDE Interface
  - Provides one IDE channel
  - Supports two enhanced IDE devices
  - Supports Ultra ATA
  - Supports ATAPI and DVD peripherals
  - Supports IDE native and ATA compatibility modes

- Compact Flash Socket
  - Provides Compact Flash socket (Type I or II)
  - Attached to Primary IDE bus
- Ethernet
  - Supports IEEE 802.3 10BaseTX/100Base/1000BaseT compatible physical layer
  - Supports Auto-negotiation for speed, duplex mode, and flow control
  - Supports full-duplex or half-duplex mode
    - Full-duplex mode supports transmit and receive frames simultaneously
    - Supports IEEE 802.3x Flow control in full-duplex mode
    - Half-duplex mode supports enhanced proprietary collision reduction mode
- Utility Interface
  - Supports standard external 8Ω “Beep” speaker interface
  - Supports external Reset switch
  - Supports external Power button
- USB Ports
  - Provide three root USB hubs
  - Provide seven USB ports
  - Support USB v2.0 EHCI and v1.1 UHCI
- Video (LCD/CRT) Display
  - Supports full hardware acceleration of H.264 video decode standard
  - Supports CRT (2048 x 1536) with up to 224MB UMA (Unified Memory Architecture)
  - Single channel 24-bit LVDS
- Miscellaneous
  - Provides Real Time Clock and CMOS RAM, with support for battery-free operation
  - Provides General Purpose I/O (GPIO) interface
  - Provides Ethernet External LED
  - Provides System Managment Bus (SMBus)
  - Supports Oops! Jumper (BIOS Recovery)
  - Supports Serial Console (Console Redirection)
  - Supports customizable Splash Screen
  - Supports Watchdog Timer (WDT)

## Block Diagram

Figure 2-2 shows the functional components of the CoreModule 730.

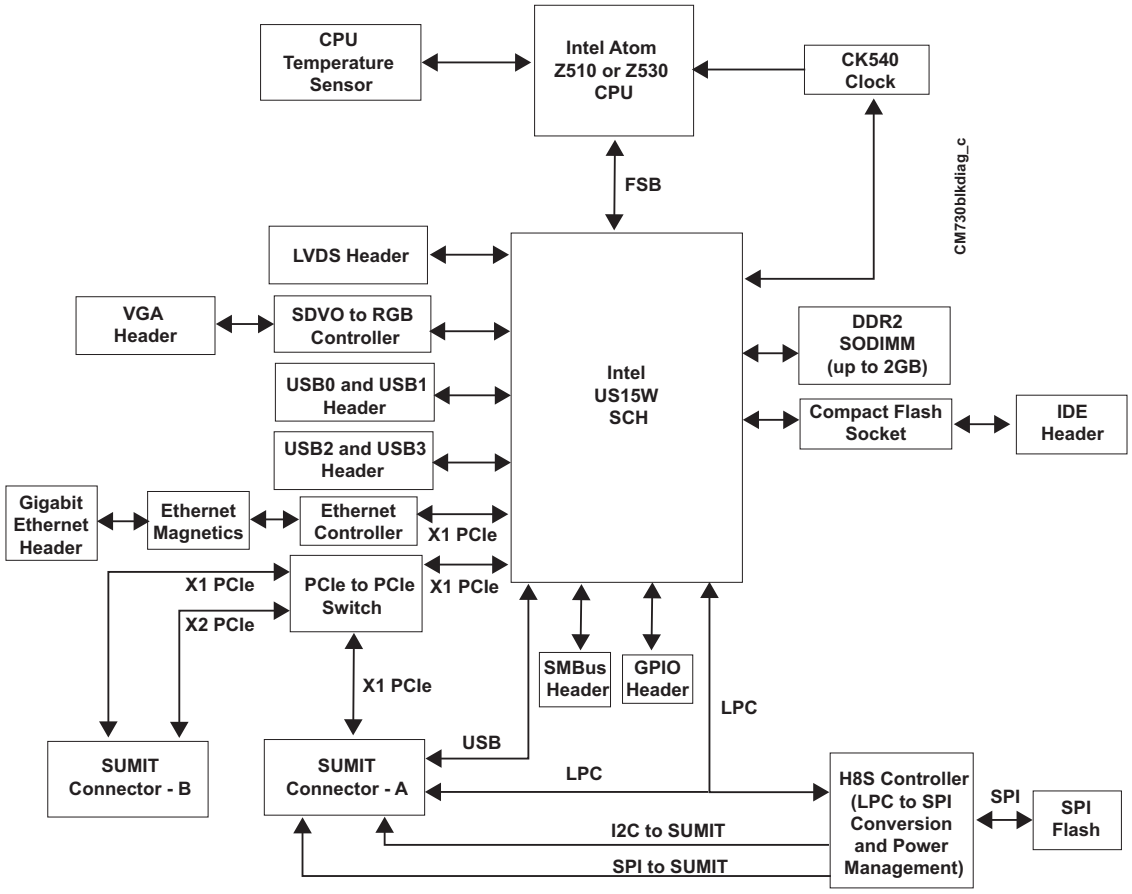


**Figure 2-2. Block Diagram**

# Major Components (ICs)

Table 2-1 lists the major ICs, including a brief description of each, on the CoreModule 730, and Figures 2-3 and 2-4 show the locations of the major ICs on the board.

**Table 2-1. Major Components (ICs) Descriptions and Functions**

| Chip Type | Mfg. | Model | Description | Function |
|---|---|---|---|---|
| CPU (U1) | Intel | Atom Z510 and Z530 | x86 32-bit processor offered at 1.1GHz (Z510) and 1.6GHz (Z530) | Embedded CPU |
| Sensor (U2) | Analog Devices | ADM1032ARMZ-1 | CPU Temperature Monitor | Temperature Monitor and Alarm |
| SCH (U3) | Intel | US15W | Graphics, Memory, and I/O Expansion controller | System Controller Hub |
| Converter (U4) | Chrontel | CH7317A | SDVO to RGB Display Controller | Digital to Analog Conversion |
| Switch (U10) | PLX | PEX8505 | PCIe to PCIe Switch | I/O Expansion Interconnect |
| Microcomputer (U27) - on bottom side; see Figure 2-4 on page 8 | Renesas | R4F2117R | H8S Controller | LPC to SPI Conversion and Power Management |
| Controller (U42) | Intel | WG82574IT | Ethernet Controller | Gigatbit Ethernet |
| Transformer (T1) - on bottom side; see Figure 2-4 on page 8 | Pulse | H5004NL | XFMR, 10/100/1000BaseT | Ethernet Magnetics |

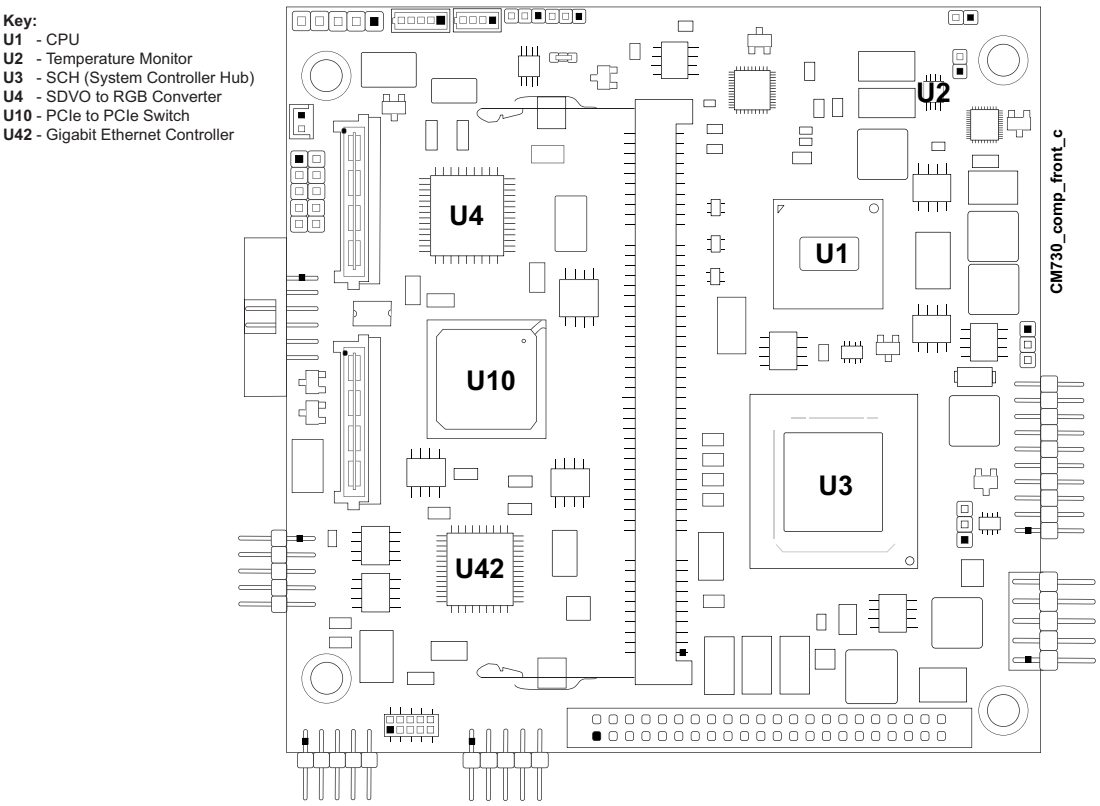


**Figure 2-3. Component Locations (Top Side)**

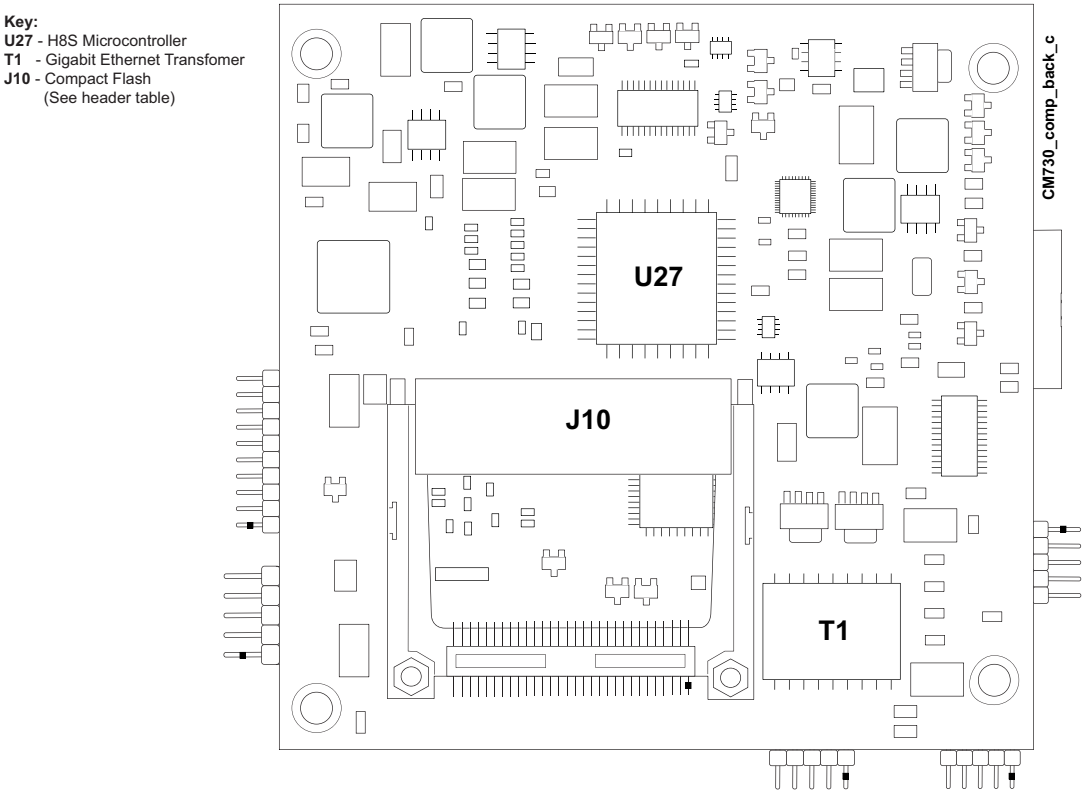


**Figure 2-4. Component Locations (Bottom Side)**

# Header, Connector, and Socket Definitions

Table 2-2 describes the headers, connectors, and sockets shown in Figure 2-6. All I/O interfaces use 0.100" (2.54mm) pitch unless otherwise indicated.

**Table 2-2. Header, Connector, and Socket Descriptions**

| Reference # | Access | Description |
|---|---|---|
| J2 – Memory | Front | 200-pin, 0.024" (0.60mm) socket for DDR2 SODIMM |
| J3 – Ethernet | Front | 10-pin, 0.079" (2mm), right-angle header for 10/100/1000BaseT Gigabit Ethernet port |
| J5 – SUMIT A (de-populated on one model) | Front | 52-pin, 0.025" (0.635mm) connector for out-going USB, PCIe, Power, ACPI, SMBus, I2C, SPI, LPC, Serial, Keyboard, Mouse, and Clock signals |
| J6 – SUMIT B (de-populated on certain models) | Front | 52-pin, 0.025" (0.635mm) connector for PCIe and Power |
| J7 – VGA | Front | 12-pin, 0.079" (2mm), right-angle, shrouded header for Video Out |
| J8 – LVDS | Front | 20-pin, 0.079" (2mm), right-angle header for Video Out |
| J9 – IDE | Front | 44-pin, standard header for primary IDE interface |
| J10 – Compact Flash (on bottom side; see Figure 2-4) | Back | 50-pin, 0.050" (1.27mm) socket for Type I or II Compact Flash cards |
| J12 – USB0 & USB1 | Front | 10-pin, 0.079" (2mm), right-angle header for USB0 and USB1 ports |
| J13 – USB2 & USB3 | Front | 10-pin, 0.079" (2mm), right-angle header for USB2 and USB3 ports |
| J17 – BATT | Front | 2-pin, 0.049" (1.24mm), shrouded header for power from external battery |
| J20 – GPIO | Front | 10-pin, 0.079" (2mm) header for General Purpose I/O |
| J21 – N/S | Front | Not Supported |
| J23 – Power In | Front | 10-pin, right-angle header for receiving external power |
| J25 – Utility | Front | 5-pin header for Power Button, Reset, and Speaker |
| J26 – Ethernet LED | Front | 4-pin, 0.049" (1.25mm) header for external Gigabit Ethernet LED |
| J27 – SMBus | Front | 5-pin, 0.049" (1.25mm) header for Clock, Data, and Power I/O |

**NOTE** The pinout tables in Chapter 3 of this manual identify pin sequence using the following methods: A 20-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as 20-pin, 2 rows, odd/even (1, 2). Alternately, a 20-pin connector using consecutive numbering, where pin 11 is directly across from pin 1, is noted in this way: 20-pin, 2 rows, consecutive (1, 11). The second number in the parenthesis is always directly across from pin 1. See Figure 2-5.

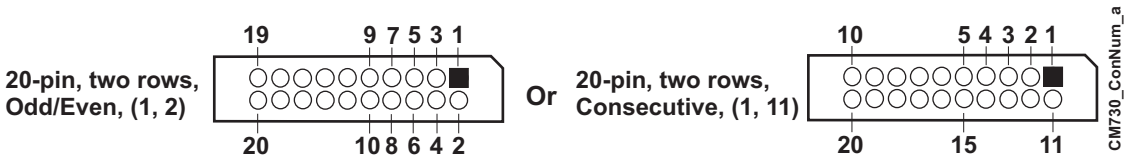


**Figure 2-5. Connector Pin Identifications**

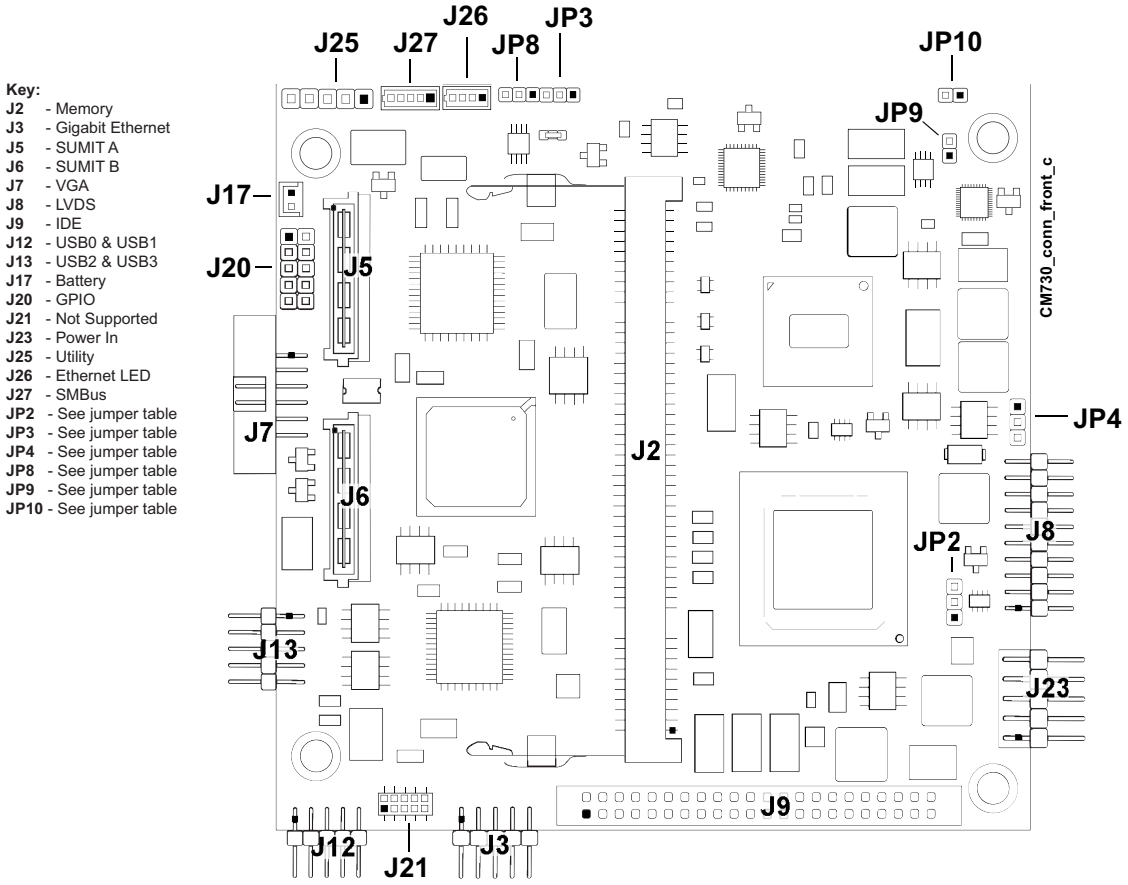


**Figure 2-6. Header, Connector, Socket Locations (Top Side)**

| **NOTE** | Pin 1 is shown as a black pin (square or round) on vertical headers in all illustrations. Black dots on right-angle headers indicate pin 2 in top-side views and pin 1 in bottom-side views. |
|---|---|

# Jumper Header Definitions

Table 2-3 describes the jumper headers shown in Figure 2-6.

**Table 2-3. Jumper Settings**

| Jumper # | Installed | Removed/Moved |
|---|---|---|
| JP2 – LVDS Voltage Select | +3.3 Volts (Pins 1-2) **Default** | +5 Volts (Pins 2-3) |
| JP3 – IDE Select | Enable HDD master, CF slave (Pins 1-2) **Default** | Enable HDD slave, CF master (Pins 2-3) |
| JP4 – Compact Flash Voltage Select | +5 Volts (Pins 1-2) | +3.3 Volts (Pins 2-3) **Default** |
| JP8 – N/S | Not Supported | Not Supported |
| JP9 – Clear CMOS | Clear CMOS Setup (pins 1-2) | Normal (Removed) **Default** |
| JP10 – N/S | Not Supported | Not Supported |

**Note:** All jumper headers use 0.079" (2mm) pitch.

# Specifications

## Physical Specifications

Table 2-4 shows the physical dimensions of the module, and Figure 2-7 shows the mounting dimensions.

**Table 2-4. Weight and Footprint Dimensions**

| Item | Dimension |
|---|---|
| Weight | 0.105 kg. (0.232 lbs.) |
| Height (upper surface) | 10.16mm (0.40") |
| Width | 90.170mm (3.550") |
| Length | 95.885mm (3.775") |

**NOTE** Height is measured from the upper board surface to the top of the highest permanent component (J25 Utility header) on the upper board surface. This does not include the heatsink. The height of the board with the heatsink installed is 0.433" (11mm). Component height should not exceed 0.435" (11.05mm) from the upper surface of the board and 0.100" (2.54mm) from the lower surface of the board.

## Mechanical Specifications

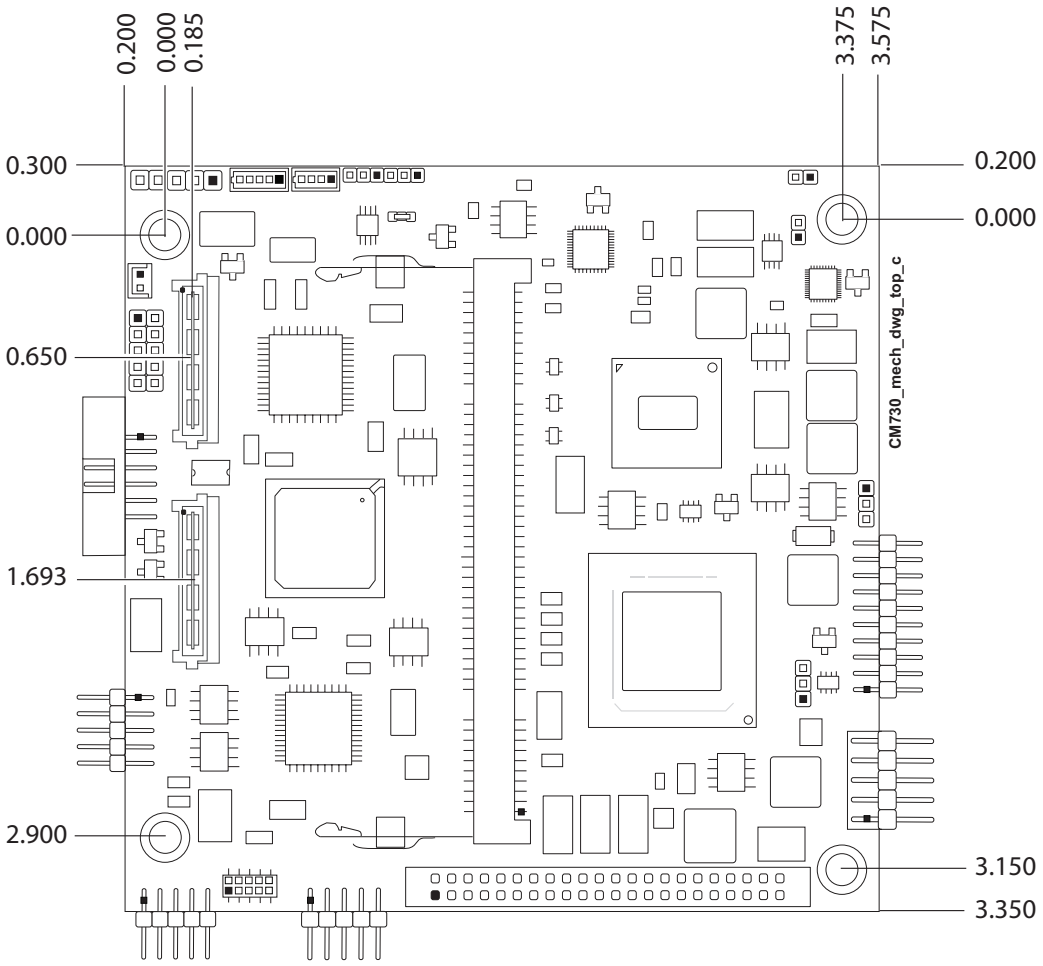


**Figure 2-7. Mechanical Dimensions (Top Side)**

| | |
|---|---|
| **NOTE** | All dimensions are given in inches. Pin 1 is shown as a black pin (square or round) on vertical headers. Black dots on right-angle headers indicate pin 2 in top-side views and pin 1 in bottom-side views. |

## Power Specifications

Table 2-5 provides the power requirements for the CoreModule 730.

**Table 2-5. Power Supply Requirements**

| Parameter | 1.1GHz Z510 CPU Characteristics (with only SUMIT A) | 1.6GHz Z530 CPU Characteristics (without SUMIT) | 1.6GHz Z530 CPU Characteristics (with SUMIT A and B) |
|---|---|---|---|
| Input Type | Regulated DC voltages | Regulated DC voltages | Regulated DC voltages |
| In-rush Current (Maximum) | 1.88A (9.40W) | 1.68A (8.40W) | 1.81A (9.05W) |
| Idle Power (Typical) | 0.91A (4.57W) | 0.93A (4.66W) | 1.00A (4.98W) |
| BIT Current (Typical) | 1.41A (7.06W) | 1.55A (7.74W) | 1.99A (9.94W) |

**Operating configurations:**

- In-rush operating configuration includes CRT video, MMSIO (only on SUMIT boards) and 1GB DDR2 RAM.
- Idle operating configuration includes the In-rush configuration as well as on-board 128MB Compact Flash, one IDE hard drive, one mouse (on MMSIO), and one keyboard (on MMSIO).
- BIT (Burn-In-Test) operating configuration includes Idle configuration as well as one USB Compact Flash reader with 64MB Compact Flash, one Ethernet connection, and one USB CD-ROM drive.

## Environmental Specifications

Table 2-6 provides the operating and storage condition ranges required for this module.

**Table 2-6. Environmental Requirements**

| Parameter | Conditions |
|---|---|
| Temperature | |
| Operating | –20° to +70° C (–4° to +158° F) |
| Extended (Optional) | –40° to +85° C (–40° to +185° F) |
| Storage | –55° to +85° C (–67° to +185° F) |
| Humidity | |
| Operating | 5% to 90% relative humidity, non-condensing |
| Non-operating | 5% to 95% relative humidity, non-condensing |

## Thermal/Cooling Requirements

The CPU is the primary source of heat on the board. The CoreModule 730 CPU is designed to operate at maximum speed and requires a heatsink (provided). The height of the heatsink is 0.433" (11mm).

# Chapter 3 Hardware

## Overview

This chapter discusses the ICs and headers of the module features in the following order:

- CPU
- Graphics
- Memory
- Interrupt Channel Assignments
- Memory Map
- I/O Address Map
- USB
- Ethernet
- Video
  - VGA
  - LVDS
- Utility
  - Power Button
  - Reset Switch
    - BIOS Recovery (Using Reset Switch)
  - Speaker
- Miscellaneous
  - Battery
  - Time of Day/RTC
  - User GPIO
  - SMBus
  - Ethernet LED
  - Oops! Jumper (BIOS Recovery)
  - Serial Console (Console Redirection)
  - Hot Cable
  - Watchdog Timer
- Power Interface

**NOTE** ADLINK Technology, Inc. only supports the features and options listed in this manual. The main components used on the CoreModule 730 may provide more features or options than are listed in this manual. Some of these features/options are not supported on the module and will not function as specified in the chip documentation.

The pinout tables only of non-standard headers and connectors are included in this chapter. This chapter does not include pinout tables for standard headers and connectors such as SUMIT, 44-pin IDE, and Compact Flash.

# CPU

The CoreModule 730 offers an embedded microprocessor—the Intel Atom Z510 and Z530—operating at 1.1 GHz and 1.6 GHz, respectively. This CPU provides a powerful x86 core and support for the SCH (System Controller Hub) US15W which integrates Northbridge and Southbridge functions.

# Graphics

The US15W SCH integrates a graphics controller which provides LVDS and SDVO ports that terminate to LVDS and VGA headers, respectively. The graphics controller achieves high 2D and 3D performance with a DDR2 memory interface (shared with the system controller) supporting a bandwith of up to 2 GB (DDR2 @ up to 533 MHz.)

# Memory

The CoreModule 730 provides one 200-pin DDR2 SODIMM of up to 2GB of memory, which is shared between the system memory controller and the graphics memory controller in the SCH.

# Interrupt Channel Assignments

The interrupt channel assignments are shown in Table 3-1.

**Table 3-1. Interrupt Channel Assignments**

| Device vs IRQ No. | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Timer | X | | | | | | | | | | | | | | | |
| Keyboard* | | X | | | | | | | | | | | | | | |
| Secondary Cascade | | | X | | | | | | | | | | | | | |
| COM1* | | | | O | D | | | | | | O | O | | | | |
| COM2* | | | | D | O | | | | | | O | O | | | | |
| COM3* | | | | O | O | | | | | | O | D | | | | |
| COM4* | | | | O | O | | | | | | D | O | | | | |
| Parallel* | | | | | | O | | D | | | | | | | O | O |
| RTC | | | | | | | | | X | | | | | | | |
| IDE | | | | | | | | | | | | | | | D | |
| Math Coprocessor | | | | | | | | | | | | | | X | | |
| PS/2 Mouse* | | | | | | | | | | | | | X | | | |
| PCI INTA* | Automatically Assigned | | | | | | | | | | | | | | | |
| PCI INTB* | Automatically Assigned | | | | | | | | | | | | | | | |
| PCI INTC* | Automatically Assigned | | | | | | | | | | | | | | | |
| PCI INTD* | Automatically Assigned | | | | | | | | | | | | | | | |
| PCI INTE | Automatically Assigned | | | | | | | | | | | | | | | |
| PCI INTF | Automatically Assigned | | | | | | | | | | | | | | | |
| PCI INTG | Automatically Assigned | | | | | | | | | | | | | | | |
| PCI INTH | Automatically Assigned | | | | | | | | | | | | | | | |

**Legend:** D = Default, O = Optional, X = Fixed, * = Located on the optional expansion module.

| **NOTE** | The PCI IRQs for the Ethernet, Video, and Internal Local Bus are automatically assigned by the BIOS Plug and Play logic. Local ISA IRQs assigned during initialization can not be used by external devices. |
|---|---|

# Memory Map

The following table provides the common PC/AT memory allocations. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management. Memory below 000500h is used by the BIOS.

**Table 3-2. Memory Map**

| Base Address | | | Function |
|---|---|---|---|
| 00000000h | - | 0009FFFFh | Conventional Memory |
| 000A0000h | - | 000AFFFFh | Graphics Memory |
| 000B0000h | - | 000B7FFFh | Mono Text Memory |
| 000B8000h | - | 000BFFFFh | Color Text Memory |
| 000C0000h | - | 000CFFFFh | Standard Video BIOS |
| 000D0000h | - | 000DFFFFh | Reserved for Extended BIOS |
| 000E0000h | - | 000EFFFFh | Extended System BIOS Area |
| 000F0000h | - | 000FFFFFh | System BIOS Area (Storage and RAM Shadowing) |
| Top 0, 1, 4, or 8MB of DRAM | | | Integrated Graphics Memory |
| FFE00000h | - | FFFFFFFFh | System Flash |

# I/O Address Map

Table 3-3 provides the I/O address map. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management.

**Table 3-3. I/O Address Map**

| Address (hex) | Subsystem |
|---|---|
| 0000-000F | System reserved |
| 0020-0021 | Master Interrupt Controller |
| 0040-0043 | Programmable Interrupt Timer (Clock/Timer) |
| 0060 | Keyboard Controller |
| 0061 | NMI, Speaker control |
| 0062 | Board Controller |
| 0063 | NMI Controller |
| 0064* | Keyboard Controller |
| 0065 | NMI Controller |
| 0066 | Board Controller |
| 0067 | NMI Controller |
| 0070-007F | CMOS RAM, NMI Mask Reg, RT Clock |
| 0080 | System reserved |
| 0081-0083 | System reserved |
| 0084-0086 | System reserved |
| 0087 | System reserved |
| 0088 | System reserved |
| 0089-008B | System reserved |
| 008C-008E | System reserved |
| 008F | System reserved |

**Table 3-3. I/O Address Map (Continued)**

| | |
|---|---|
| 0090-0091 | System reserved |
| 0092 | Fast A20 gate and CPU reset |
| 0093-009F | System reserved |
| 00A0-00A1 | Slave Interrupt Controller |
| 00A2-00BF | System reserved |
| 00C0-00DF | System reserved |
| 00E0-00EF | System reserved |
| 00F0-00FF | Math Coprocessor |
| 01F0-01F7 | IDE Hard Disk Controller |
| 0201 | Watchdog Timer (WDT) |
| 0205 | System reserved |
| 02E8-02EF* | Serial Port 4 (COM4) |
| 02F8-02FF* | Serial Port 2 (COM2) |
| 360 | Board Controller |
| 364 | Board Controller |
| 0378-037F* | Parallel Port (Standard and EPP) |
| 03B0-03BB | Video (monochrome) |
| 03C0-03DF | Video (VGA) |
| 03E8-03EF* | Serial Port 3 (COM3) |
| 03F6 | IDE Hard Disk Controller |
| 03F8-03FF* | Serial Port 1 (COM1) |
| 04D0-04D1 | Edge/Level Trigger PIC |
| 0778-077F* | Parallel Port (ECP Extensions) (Port 378+400) |
| 0CF8-0CFF | PC I Configuration Registers |
| 0CF9 | Reset Control Register |

* Located on the optional expansion module.

# USB Interfaces

The CoreModule 730 contains three root USB (Universal Serial Bus) hubs and seven functional USB ports. The SCH terminates four USB ports to two headers and routes three USB ports to the SUMIT Connector A. Each of these ports include the following features:

- USB EHCI v.2.0 and USB UHCI v.1.1
- Over-current detection
- Over-current protection
- High-speed data transfers up to 480 MB/sec on USB 2.0

Table 3-4 describes the pin signals of the USB0 and USB1 header which consists of 10 right-angle pins, in two rows, with odd/even (1, 2) pin sequence, and 0.079" (2mm) pitch.

**Table 3-4. USB0 and USB1 Interface Pin Signals (J12)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | USB-PWR_0 | USB0 Power – VCC (+5V +/-5%) power goes to the port through an on board fuse. Port is disabled if this input is low. |
| 2 | USB-PWR_1 | USB1 Power – VCC (+5V +/-5%) power goes to the port through an on board fuse. Port is disabled if this input is low. |
| 3 | CONN_USB0_N | USB0 Port Data Negative |
| 4 | CONN_USB1_N | USB1 Port Data Negative |
| 5 | CONN_USB0_P | USB0 Port Data Positive |
| 6 | CONN_USB1_P | USB1 Port Data Positive |
| 7 | USB_GND0 | USB0 Ground |
| 8 | USB_GND1 | USB1 Ground |
| 9 | USB_GND0 | USB0 Ground |
| 10 | USB_GND1 | USB1 Ground |

**Note:** The shaded areas denote power or ground.

Table 3-5 describes the pin signals of the USB2 and USB3 header which consists of 10 right-angle pins in two rows, with odd/even (1, 2) pin sequence, and 0.079" (2mm) pitch.

**Table 3-5. USB2 and USB3 Interface Pin Signals (J13)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | USB-PWR_2 | USB2 Power – VCC (+5V +/-5%) power goes to the port through an on board fuse. Port is disabled if this input is low. |
| 2 | USB-PWR_3 | USB3 Power – VCC (+5V +/-5%) power goes to the port through an on board fuse. Port is disabled if this input is low. |
| 3 | CONN_USB2_N | USB2 Port Data Negative |
| 4 | CONN_USB3_N | USB3 Port Data Negative |
| 5 | CONN_USB2_P | USB2 Port Data Positive |
| 6 | CONN_USB3_P | USB3 Port Data Positive |
| 7 | USB_GND2 | USB2 Ground |
| 8 | USB_GND3 | USB3 Ground |
| 9 | USB_GND2 | USB2 Ground |
| 10 | USB_GND3 | USB3 Ground |

**Note:** The shaded areas denote power or ground.

# Ethernet Interface

The Ethernet solution originates from the 82574IT Gigabit Ethernet controller and consists of both the Media Access Controller (MAC) and the Physical Layer (PHY) combined into a single component solution. The Gigabit Ethernet Control Unit is a 64-bit PCIe controller that features enhanced scatter-gather bus mastering capabilities, which enables the processor to perform high-speed data transfers over the internal PCIe bus. The bus master capabilities enable the component to process high-level commands and perform multiple operations, thereby off-loading communication tasks from the CPU. The Ethernet interface offers the following features:

- Full duplex or half duplex support at 10 Mbps, 100 Mbps, or 1000 Mbps
- In full duplex mode, the Ethernet controller adheres to the IEEE 802.3x Flow Control specification.
- In half duplex mode, performance is enhanced by a proprietary collision reduction mechanism.
- IEEE 802.3 compatible physical layer to wire transformer
- IEEE 802.3u Auto-Negotiation support
- Fast back-to-back transmission support with minimum interframe spacing (IFS).
- IEEE 802.3x auto-negotiation support for speed and duplex operation
- 3 kB transmit and 3 kB receive FIFOs (helps prevent data underflow and overflow)
- On-board magnetics (Ethernet isolation transformer)

Table 3-6 describes the pin signals of the Ethernet header which consists of 10 right-angle pins, two rows, odd/even (1,2) pin sequence, and 0.079" (2mm) pitch.

**Table 3-6. Ethernet Interface Pin/Signal Descriptions (J3)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | GND | Ground |
| 2 | GND | |
| 3 | MDI0+ | Media Dependent Interface 0 +/- |
| 4 | MDI0- | |
| 5 | MDI1+ | Media Dependent Interface 1 +/- |
| 6 | MDI1- | |
| 7 | MDI2+ | Media Dependent Interface 2 +/- |
| 8 | MDI2- | |
| 9 | MDI3+ | Media Dependent Interface 3 +/- |
| 10 | MDI3- | |

**Note:** The shaded areas denote power or ground.

**NOTE** The magnetics (isolation transformer, T1) for the Ethernet connector is included on the CoreModule 730.

# Video Interfaces

The SCH chip provides the graphics control and video signals to traditional glass CRT (VGA) monitors and LVDS flat panel displays, supporting full hardware acceleration of H.264 video decode. Other chip features are listed below:

*VGA* features:

- Support for an integrated 400-MHz, 24-bit RAMDAC to drive a progressive scan analog monitor and outputs to three, 8-bit DACs that provide the R, G, and B signals to the monitor
- Support for resolutions up to QXGA (2048x1536)
- Support for a maximum allowable video frame buffer size of 224MB UMA (Unified Memory Architecture)

*LVDS* features:

- Support for a single channel LFP Transmitter interface
- Support for LVDS LCD panel resolutions up to UXGA (1600X1200)
- Support for a maximum pixel format of 24 bpp with SSC supported frequency range from 25 MHz to 112 MHz (single channel)

## VGA Interface

Table 3-7 describes the pin signals of the VGA interface, which uses 12 right-angle pins, 2 rows, odd/even sequence (1, 2) with 0.079" (2mm) pitch.

**Table 3-7. VGA Interface Pin Signals (J7)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | RED | Red – This is the Red analog output signal to the CRT. |
| 2 | GND1 | Ground 1 (Red Return) |
| 3 | GREEN | Green – This is the Green analog output signal to the CRT. |
| 4 | GND2 | Ground 2 (Green Return) |
| 5 | BLUE | Blue – This is the Blue analog output signal to the CRT. |
| 6 | GND3 | Ground 3 (Blue Return) |
| 7 | HSYNC | Horizontal Sync – This signal is used for the digital horizontal sync output to the CRT. |
| 8 | GND4 | Ground 4 (VGA) |
| 9 | VSYNC | Vertical Sync – This signal is used for the digital vertical sync output to the CRT. |
| 10 | PWR | Power – Provided through fuse (F1) to +5 volts +/- 5%. F1 is next to J7 header on board. |
| 11 | DDC_DATA | Display Data Channel - Data |
| 12 | DDC_CLK | Display Data Channel - Clock |

**Note:** The shaded areas denote power or ground.

## LVDS Interface

Table 3-8 describes the pin signals of the LVDS interface, which uses a 20-pin, right-angle header with 2 rows, odd/even sequence (1, 2), and 0.079" (2mm) pitch.

**Table 3-8. LVDS Interface Pin/Signal Descriptions (J8)**

| Pin # | Signal | Description | Line |
|---|---|---|---|
| 1 | VCC_INTRV | +12V source | |
| 2 | VCC_LVDS_CONN | JP2 = +3.3 or +5V source | |
| 3 | GND | Ground | Gnd |
| 4 | GND | Ground | |
| 5 | LVDS_CLK+ | Clock Positive Output | Clk |
| 6 | LVDS_CLK- | Clock Negative Output | |
| 7 | LVDS_DAT3+ | Data 3 Positive Output | 3 |
| 8 | LVDS_DAT3- | Data 3 Negative Output | |
| 9 | LVDS_DAT2+ | Data 2 Positive Output | 2 |
| 10 | LVDS_DAT2- | Data 2 Negative Output | |
| 11 | LVDS_DAT1+ | Data 1 Positive Output | 1 |
| 12 | LVDS_DAT1- | Data 1 Negative Output | |
| 13 | LVDS_DAT0+ | Data 0 Positive Output | 0 |
| 14 | LVDS_DAT0- | Data 0 Negative Output | |
| 15 | LVDS_BKLT_CTRL | Backlight Control | |
| 16 | LVDS_VDD_EN | LCD Enable | |
| 17 | LVDS_DDC_CLK | Clock | |
| 18 | LVDS_DDC_DATA | Data | |
| 19 | LVDS_BKLT_EN | Backlight Enable | |
| 20 | NC | Not connected | |

**Note:** The shaded areas denote power or ground.

# Utility Interface

The Utility interface provides three utility and I/O signals on the module and consists of a 5-pin, 0.100" (2.54mm), single row header. The US15W SCH drives the signals on the Utility interface. Table 3-9 provides the signal definitions.

- Power Button
- Reset Switch
- Speaker

## Power Button

The Utility header provides a signal for an external Power button through pins 1 and 2. The Power button allows the user to turn Off the system.

## Reset Switch

Pins 2 and 3 on the Utility header provide the signal for an external reset button which allows the user to re-boot the system.

### BIOS Recovery (Using Reset Switch)

In the event you have selected BIOS settings that prevent you from booting the system, you can stop the current BIOS settings in the CMOS from being loaded by pressing and holding the Reset button for five seconds and then releasing the button. The system re-boots, and the BIOS loads the default settings.

## Speaker

The speaker signal provides sufficient signal strength to drive a 1W 8 Ω "Beep" speaker through the Utility interface at an audible level. The speaker signal is driven from an on-board amplifier and the SCH.

**Table 3-9. Utility Interface Pin Signals (J25)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | /PWR_BTN | External Power Button (Pins 1-2) |
| 2 | GND | Ground |
| 3 | /RESET SW* | External Reset Switch signal (Pins 2-3) |
| 4 | 5V | +5 Volts Power |
| 5 | SPKR_CONN | Speaker Output (Pins 4-5) |

**Note:** The shaded area denotes power or ground. The signals marked with * indicate active low.

# Miscellaneous

## Battery

An external battery connection is provided through the J17 header to support a backup battery for the CMOS RAM and the RTC (Real Time Clock).

## Real Time Clock (RTC)

The CoreModule 730 contains a Real Time Clock (RTC). The CMOS RAM can be backed up with a lithium battery. If the battery is not present, a battery-free boot option in the BIOS completes the boot process and resets the clock to the default date and time.

| **NOTE** | Some operating systems require a valid default date and time to function. |
|---|---|

## User GPIO Interface

The CoreModule 730 provides GPIO pins for customer use, and the signals are routed to header J20 which uses 10 pins with odd/even (1,2) pin sequence and 0.049" (2mm) pitch. An example of how to use the GPIO pins resides in the Miscellaneous Source Code Examples on the CoreModule 730 Support QuickDrive™.

**Table 3-10. User GPIO Interface Pin/Signal Descriptions (J20)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | H8S_GPI0 | User defined |
| 2 | H8S_GPO0 | User defined |
| 3 | H8S_GPI1 | User defined |
| 4 | H8S_GPO1 | User defined |
| 5 | H8S_GPI2 | User defined |
| 6 | H8S_GPO2 | User defined |
| 7 | H8S_GPI3 | User defined |
| 8 | H8S_GPO3 | User defined |
| 9 | GND | Ground |
| 10 | GND | Ground |

**Note:** The shaded areas denote ground.

## Oops! Jumper (BIOS Recovery)

The Oops! jumper is provided in the event you have selected BIOS settings that prevent you from booting the system. By using the Oops! jumper you can stop the current BIOS settings in the CMOS from being loaded, allowing you to proceed, using the default settings. Connect the DTR pin to the RI pin on Serial port 1 (COM 1 on the MiniModule board) prior to boot up to prevent the present BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper and go into the BIOS Setup Utility. Change the desired BIOS settings, or select the default settings, and save changes before rebooting the system.

To convert a standard DB9 connector to an Oops! jumper, short together the DTR (4) and RI (9) pins on the rear of the female connector or the front of the male connector as shown in Figure 3-1 on the Serial Port 1 DB9 connector.

To restore your BIOS setting changes without the errors, you must first select *Load Factory Default Settings*, which will automatically load and save the defaults and reboot the system. Then you can modify the default settings to your desired values. Ensure you save the changes before rebooting the system.

> **NOTE** Serial Port 1 (on the MiniModule) is a 10-pin header and uses pin 7 = DTR and pin 8 = RI for the Oops! Jumper. At Serial Port 1, short pin 7 to 8, as shown in Figure 3-1. Alternatively, you may short the equivalent pins (4 to 9) on the DB9 connector attached to Serial Port 1 as shown in Figure 3-1.

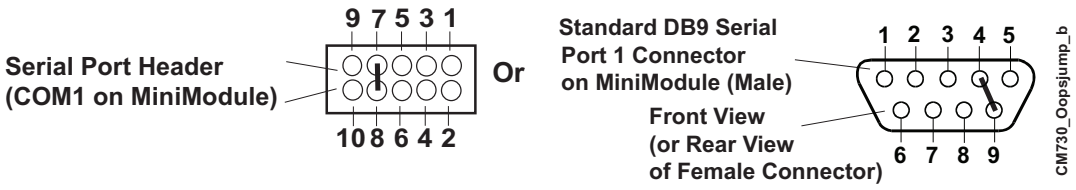


**Figure 3-1. Oops! Jumper**

## Serial Console

The CoreModule 730 BIOS supports the serial console (or console redirection) feature. These I/O functions are provided by an ANSI-compatible serial terminal, or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to keyboards and displays.

### Serial Console BIOS Setup

The serial console (console redirection) feature is implemented by connecting a standard null-modem cable or a modified serial cable (or "Hot Cable") between one of the serial ports, such as Serial 1 or 2 (from SUMIT connector A), and the serial terminal or a PC with communications software. The BIOS Setup Utility controls the serial console settings on the CoreModule 730. Refer to the BIOS Setup for the serial console option settings using a serial terminal or PC with communications software.

### Hot (Serial) Cable

To convert a standard serial cable to a Hot Cable, certain pins must be shorted together at the Serial port header or at the DB9 connector. Short together the RTS (4) and RI (8) pins on either serial port header (J3 or J9). As an alternate, you can short the equivalent pins 7 and 9 on the rear of the respective DB9 female connector or the front of the male connector as shown in Figure 3-2.

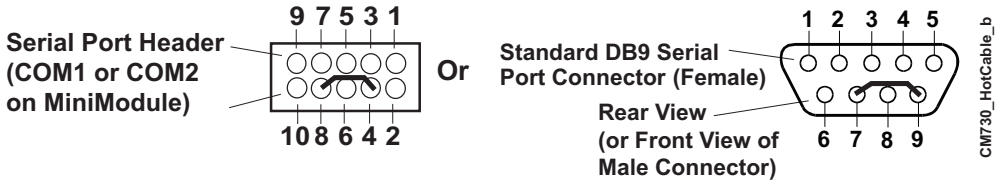


**Figure 3-2. Hot Cable Jumper**

## System Management Bus (SMBus)

The SCH chip contains a host SMBus port. The host port allows the CPU access to the SMBus slaves through header J27. The SMBus slaves include the SODIMM EPROM, CPU Temperature Sensor, Clock Buffer, and the Clock Generator. Table 3-11 lists the device names and corresponding reserved binary addresses on the SMBus. Table 3-12 lists the SMBus pin signals on 5 pins, 1 row, 0.049" (2 mm) pitch on the external SMBus header (J27).

**Table 3-11. SMBus Reserved Addresses**

| Component | Address Binary |
|---|---|
| SODIMM EPROM | $1010{,}000x_b$ |
| Clock Generator | $1101{,}001x_b$ |
| Clock Buffer | $1101{,}110x_b$ |
| CPU Temperature Sensor | $1001{,}100x_b$ |

**Table 3-12. SMBus Pin Signals (J27)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | SMB_CLK | SMBus Clock |
| 2 | GND | Ground |
| 3 | SMB_DATA | SMBus Data |
| 4 | VSM | +3.3V standby voltage |
| 5 | /SMB_ALERT* | SMBus Alert |

**Note:** The shaded areas denote power or ground. The signals marked with * indicate Active Low.

## Ethernet External LED

This header provides signals for an external LED that indicates Ethernet links and activity using a single row of 4 pins with 0.049" (1.25mm) pitch.

**Table 3-13. Ethernet External LED Pin Signals (J26)**

| Pin # | Signal | Description |
|---|---|---|
| 1 | V3.3_CONN | +3 volts – Provides +3 volts to external LED (Pins 1-2 for Green LED) |
| 2 | ETH_ACT_LED | Ethernet Activity |
| 3 | ETH_LINK100_LED | Fast Ethernet Link with +3 volts power (Pins 3-4 for Bi-Color LED) |
| 4 | ETH_LINK1000_LED | Gigabit Ethernet Link |

**Note:** The shaded area denotes power or ground.

## Watchdog Timer

The Watchdog Timer (WDT) restarts the system if an error or mishap occurs, allowing the system to recover from the mishap, even though the error condition may still exist. Possible problems include failure to boot properly, loss of control by the application software, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (Watchdog Timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the OS fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the *Watchdog Timer (sec)* field in the BIOS and Hardware Settings screen of BIOS Setup. Set the WDT for a time-out interval in seconds, between 1 and 255, in one second increments. Ensure you allow enough time for the operating system (OS) to boot. The OS or application must tickle (reset) the WDT before the timer expires. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. ADLINK Board Support Packages provide APIs to the WDT. The application must tickle (reset) the WDT before the timer expires or the system will be reset.

- Watchdog Code examples – ADLINK has provided source code examples on the CoreModule 730 Support Software QuickDrive illustrating how to control the WDT. The code examples can be easily copied to your development environment to compile and test the examples, or make any desired changes before compiling. Refer to the WDT Readme file in the Sample Code directory on the CoreModule 730 Support Software QuickDrive.

# Power Interface

The CoreModule 730 requires one +5 volt DC power source and uses a 10-pin header with odd/even (1, 2) pin sequence and 0.10" (2.54mm) pitch. If the +5VDC power drops below ~4.65V, a low voltage reset is triggered, resetting the system.

The power input header (J23) supplies the following voltages and ground directly to the module:

- 5.0VDC +/- 5%

**Table 3-14. Power Interface Pin/Signals (J23)**

| Pin | Signal | Descriptions |
|---|---|---|
| 1 | GND | Ground |
| 2 | +5V | +5 Volts |
| 3 | Key/GND | Key Pin on connector/Grounded on board |
| 4 | +12V | +12 volts routed to SUMIT A |
| 5 | GND | Ground |
| 6 | NC | Not connected |
| 7 | GND | Ground |
| 8 | +5V | +5 Volts |
| 9 | GND | Ground |
| 10 | +5V | +5 Volts |

**Note:** The shaded areas denote power or ground.

# Chapter 4 BIOS Setup

## Introduction

This section assumes the user is familiar with general BIOS Setup. Refer to the appropriate PC reference manuals for information about the on-board ROM-BIOS software interface.

### Entering BIOS Setup (VGA Display)

To access BIOS Setup using a VGA display for the CoreModule 730:

1. Turn on the VGA monitor and the power supply to the CoreModule 730.
2. Start Setup by pressing the [Del] key when the following message appears on the boot screen.

```
Press DEL to run Setup
```

> **NOTE** If the setting for *Quick Boot* is [Enabled], you may not see this prompt appear on screen. If this happens, press the <Del> key earlier in the boot sequence to enter BIOS Setup.

3. Follow the instructions on the right side of the screen to navigate through the selections and modify any settings.

### Entering BIOS Setup (Remote Access)

This section describes how to enable the Remote Access in VGA mode and enter the BIOS setup through a serial terminal or PC.

1. Turn on the power supply to the CoreModule 730 and enter the BIOS Setup Utility in VGA mode.
2. Set the BIOS feature *Serial Console Redirection* to [Enabled] under the **Advanced** menu.
3. Accept the default options or make your own selections for the balance of the Remote Access fields and record your settings.
4. Ensure you select the type of remote serial terminal you will be using and record your selection.
5. Select *Save Changes and Exit* and then shut down the CoreModule 730.
6. Connect the remote serial terminal (or the PC with communications software) to the COM port you selected and recorded earlier in the BIOS Setup Utility.
7. Turn on the remote serial terminal or PC and set it to the settings you selected in the BIOS Setup Utility.

   The default settings for the CoreModule 730 are:

   - COM1
   - 8 bits
   - 1 stop bit
   - no parity
8. Restore power to the CoreModule 730 and look for the screen prompt shown below.

```
Press <space bar> to update BIOS
```

9. Press the F4 key to enter Setup (early in the boot sequence if *Quick Boot* is set to [Enabled].)

   If *Quick Boot* is set to [Enabled], you may never see the screen prompt.

10. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen.

> **NOTE** The serial console port is not hardware protected. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

# OEM Logo Utility (Splash Screen)

The CoreModule 730 BIOS supports a graphical logo utility, which can be customized by the user and displayed when enabled through the BIOS Setup Utility. The graphical image can be a company logo or any custom image the user wants to display during the boot process. The custom image can be displayed as the first image displayed on screen during the boot process and remain there, depending on the options selected in BIOS Setup, while the OS boots.

## Logo Image Requirements

The user's image may be customized with any image editing tool, and the system will automatically convert the image into an acceptable format to the tools (files and utilities) provided by ADLINK. The CoreModule 730 OEM Logo utility supports the following image formats:

- Bitmap image
  - 16-Color, 640x480 pixels
  - 256-Color, 640x480 pixels
- JPG image
  - 16-Color, 640x480 pixels
- PCX image
  - 256-Color, 640x480 pixels
- A file size no larger than sample image

# BIOS Setup Menus

This section provides illustrations of the six main setup screens in the CoreModule 730 BIOS Setup Utility. Below each illustration is a bulleted list of the screen's submenus and setting selections. The setting selections are presented in brackets after each submenu or menu item and the default settings are presented in bold. Refer to right hand columns of your actual BIOS screens for descriptions of the selected settings.

**Table 4-1. BIOS Setup Menus**

| BIOS Setup Utility Menu | Item/Topic |
|---|---|
| Main | BIOS and Memory Information, System Date and Time |
| Advanced | Legacy OpROM Support, Launch PXE OpROM, PCI Subsystem Settings, CPU, IDE, Thermal, USB, Super IO, Serial Port Console Redirection |
| Chipset | North Bridge and South Bridge Configurations |
| Boot | Boot up Settings, Boot Order, Removable Drives |
| Security | Setting or changing Passwords |
| Save & Exit | Exiting with or without changing settings, Loading Optimal or Failsafe conditions |

## BIOS Main Setup Screen

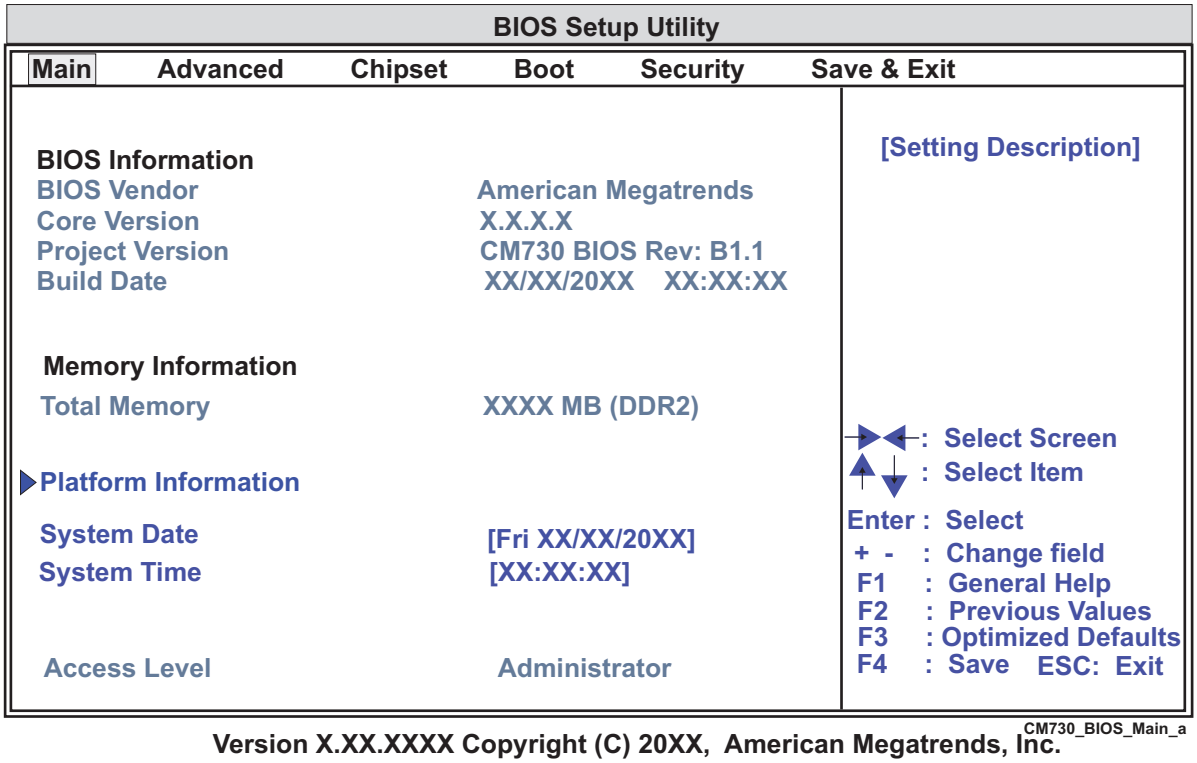


**Figure 4-1. BIOS Main Setup Screen**

- **Platform Information**
  - SCH Stepping D1
  - CMC Hi-Module 0D2.017X
  - CMC Lo-Module 0D2.025X
  - IGD VBIOS Version 0016

- PSlewRate LUT Rev XX/XX/XX
- NSlewRate LUT Rev XX/XX/XX

- **Date & Time**
  - System Date (day of week, mm:dd:yyyy) – This field requires the alpha-numeric entry of the day of week, day of the month, calendar month, and all 4 digits of the year, indicating the century plus year (*Fri XX/XX/20XX*).
  - System Time (hh:mm:ss) – This is a 24-hour clock setting in hours, minutes, and seconds.

## BIOS Advanced Setup Screen

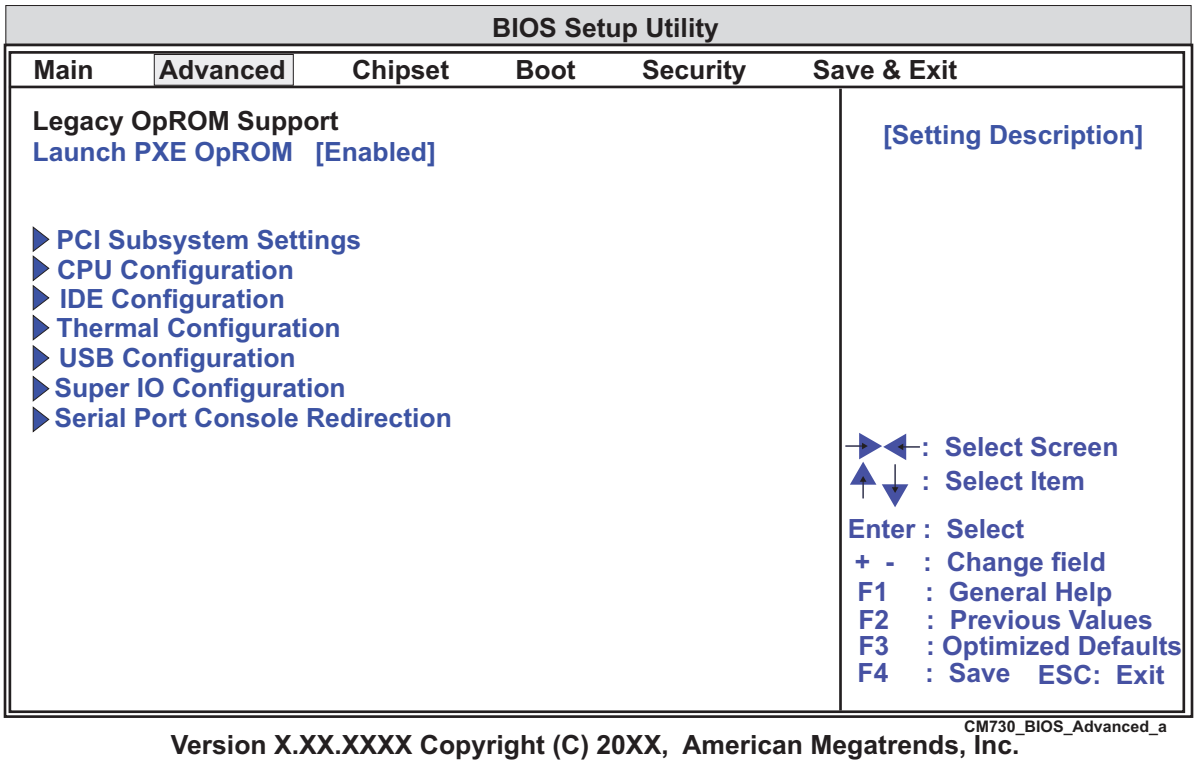


**Figure 4-2. BIOS Advanced Setup Screen**

- **Legacy OpROM Support**
  - Launch PXE OpROM [Disabled; **Enabled**]
- **PCI Subsystem Settings**
  - PCI Settings
    - PCI Latency Timer [**32 PCI Bus Clocks**; 64 PCI Bus Clocks; 96 PCI Bus Clocks; 128 PCI Bus Clocks; 160 PCI Bus Clocks; 192 PCI Bus Clocks; 224 PCI Bus Clocks; 248 PCI Bus Clocks]
  - PCI Express Device Settings
    - Relaxed Ordering [**Disabled**; Enabled]
    - Extended Tag [**Disabled**; Enabled]
    - No Snoop [Disabled; **Enabled**]
    - Maximum Payload [**Auto**; 128 Bytes; 256 Bytes; 512 Bytes; 1024 Bytes; 2048 Bytes; 4096 Bytes]

  - Maximum Read Request [**Auto**; 128 Bytes; 256 Bytes; 512 Bytes; 1024 Bytes; 2048 Bytes; 4096 Bytes]

- PCI Express Link Settings
  - Automatic ASPM [**Disabled**; Auto; Force L0]
    WARNING: Enabling ASPM may cause some PCI-E devices to fail
- IRQ Settings
  - IRQ3 [**Available**; Reserved]
  - IRQ4 [**Available**; Reserved]
  - IRQ5 [**Available**; Reserved]
  - IRQ7 [**Available**; Reserved]
  - IRQ9 [**Available**; Reserved]
  - IRQ10 [**Available**; Reserved]
  - IRQ11 [**Available**; Reserved]
  - IRQ14 [Available; **Reserved**]
  - IRQ15 [**Available**; Reserved]

- **CPU Configuration**
  - Processor Type Intel(R) Atom(TM) CPU XXXX
  - EMT64 Not Supported
  - Processor Speed XXXX MHz
  - System Bus Speed XXX MHz
  - Ratio Status XX
  - Actual Ratio XX
  - Processor Stepping XXXcX
  - Microcode Revision XXX
  - L1 Cache RAM XX k
  - L2 Cache RAM XXX k
  - Processor Core Single
  - Hyper-Threading Not Supported
  - Execute - Disable Bit [Disabled; **Enabled**]
  - Limit CPUID Maximum [**Disabled**; Enabled]
  - EMTTM [**Disabled**; Enabled]
  - Turbo Mode [**Disabled**; Enabled]
  - SpeedStep (tm) [Disabled; **Enabled**]
  - Boot Performance Mode [Max Performance; Max Battery; **Auto**]
  - C-States [Disabled; **Enabled**]
  - Enhanced C-States [Disabled; **Enabled**]
  - Max C-States [C1; C2; C3; C4; **C6**]
  - Hard C4E [Disabled; **Enabled**]
  - TM1 [Disabled; **Enabled**]
  - TM2 [Disabled; **Enabled**]

- Bi-directional PROCHDT# [Disabled; **Enabled**]
- ACPI 3.0 T-States [Disabled; **Enabled**]

- **IDE Configuration**
  - PATA Master Not Present
  - PATA Slave Not Present
- **Thermal Configuration**
  - Critical Trip Point [60C; 70C; 80C; 90C; 95C; 100C; 105C; **110C**]
  - Passive Trip Point [60C; 70C; 80C; 90C; **95C**; 100C; 105C; Disabled]
  - Throttling Ratio [87.5%; 75.0%; 62.5%; **50.0%**; 37.5%; 25.0%; 12.5%]
- **USB Configuration**
  - USB Devices
    - 1 Keyboard
  - Legacy USB Support [**Enabled**; Disabled; Auto]
  - EHCI Hand-Off [Disabled; **Enabled**]
  - Device Reset Timeout [10 sec; **20 sec**; 30 sec; 40 sec]
- **Super IO Configuration**
  - Serial Port 1 Configuration
    - Serial Port [Disabled; **Enabled**]
    - RS485 Mode [**Disabled**; Enabled]
    - Device Settings IO=3F8h; IRQ=4
    - Change Settings [**IO=3F8h; IRQ=4**<br>IO=2F8h; IRQ=3<br>IO=3E8h; IRQ=11<br>IO=2E8h; IRQ=10]
  - Serial Port 2 Configuration
    - Serial Port [Disabled; **Enabled**]
    - RS485 Mode [**Disabled**; Enabled]
    - Device Settings IO=2F8h; IRQ=3
    - Change Settings [**IO=2F8h; IRQ=3**<br>IO=3F8h; IRQ=4<br>IO=3E8h; IRQ=11<br>IO=2E8h; IRQ=10]
  - Serial Port 3 Configuration
    - Serial Port [Disabled; **Enabled**]
    - RS485 Mode [**Disabled**; Enabled]
    - Device Settings IO=3E8h; IRQ=11
    - Change Settings [**IO=3E8h; IRQ=7**<br>IO=3F8h; IRQ=4<br>IO=2F8h; IRQ=3<br>IO=2E8h; IRQ=10]

- Serial Port 4 Configuration
  - Serial Port [Disabled; **Enabled**]
  - RS485 Mode [**Disabled**; Enabled]
  - Device Settings IO=2E8h; IRQ=10
  - Change Settings [**IO=2E8h; IRQ=7**
    IO=3F8h; IRQ=4
    IO=2F8h; IRQ=3
    IO=3E8h; IRQ=11]
- Parallel Port Configuration
  - Parallel Port [Disabled; **Enabled**]
  - Device Settings IO=378h; IRQ=7
  - Change Settings [**IO=378h; IRQ=7**
    IO=378h; IRQ=5
    IO=278h; IRQ=7
    IO=278h; IRQ=5
    IO=3BCh; IRQ=7
    IO=3BCh; IRQ=5]
- Device Mode [**Printer Mode**; SPP Mode]

- **Serial Port Console Redirection**
  - COM1
    - Console Redirection [**Disabled**; Enabled]
    - Console Redirection Settings
  - COM2
    - Console Redirection [**Disabled**; Enabled]
    - Console Redirection Settings
  - Serial Port for Out-of-Band Management/
    Windows Emergency Management Services (EMS)
    - Out-of-Band Mgmt Port [**COM1**; COM2]
    - Data Bits 8
    - Parity None
    - Stop Bits 1
    - Terminal Type [VT-UTF8]

## BIOS Chipset Setup Screen

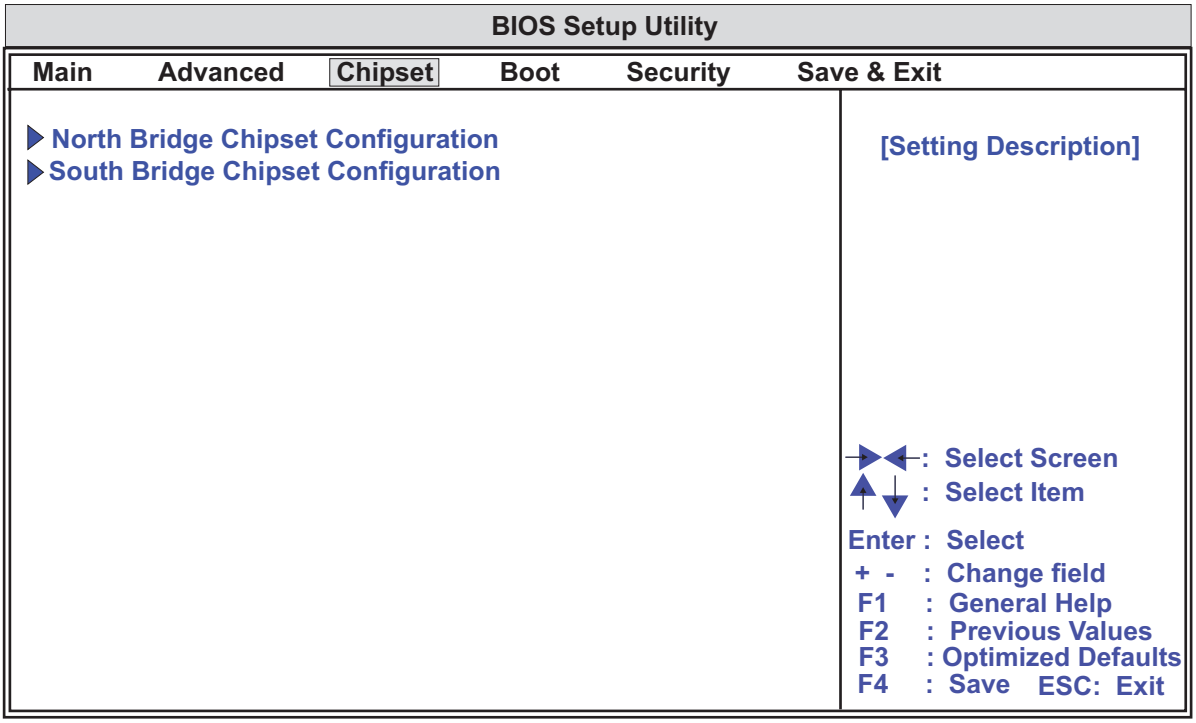


**Figure 4-3. BIOS Chipset Setup Screen**

- **North Bridge Chipset Configuration**
  - Memory Information
    - Total Memory XXXX MB (DDR2)
  - IGD Mode Select [Disabled;
    Enabled, 1MB;
    Enabled, 4MB;
    **Enabled, 8MB**]
  - Boot Display Configuration
    - Boot Display Device [**Auto**; CRT; LFP]
    - Flat Panel Scaling [**Auto**; Forced; Disabled]
    - Flat Panel Type [640x480 18bpp (generic)
      800x600 18bpp (generic)
      **1024x768 18bpp (generic)**
      640x480 18bpp (NEC 8.4" NL6448BC26-08D)
      800x480 18bpp (NEC 9" NL8048BC24-01)
      1024x600 18bpp (TMD 5.61" LTD056ET0S)
      1024x600 18bpp (Samsung 4.8" LTS480WS-C01)
      1024x768 18bpp (Samsung 15" LTX150XG-L01)
      1024x768 24bpp (AUO 15" M150XN07 V.2)
      1280x768 18bpp (Sharp 7.2" LQ072K1LAXX)
      1280x800 24bpp (Samsung 15.4" LTN154X5-L01)
      1366x768 18bpp (TMD 11.1" LTD111EXDA)]

- **South Bridge Chipset Configuration**
  - SMBUS Controller [**Enabled**; Disabled]
  - High Precision Timer [Disabled; **Enabled**]
  - USB Controllers
    - UHCI Controller #1 [Disabled; **Enabled**]
    - UHCI Controller #2 [Disabled; **Enabled**]
    - UHCI Controller #3 [Disabled; **Enabled**]
    - USB Client Controller [**Disabled**; Enabled]
  - PCI Ports Configuration
    - PCI Express Root Port 1 [Disabled; **Enabled**]
      - -VCI Enable [**Disabled**; Auto]
      - -ASPM [Disabled; **Enabled**]
      - -Automatic ASPM [Manual; **Auto**]
      - -URR [**Disabled**; Enabled]
      - -FER [**Disabled**; Enabled]
      - -NFER [**Disabled**; Enabled]
      - -CER [**Disabled**; Enabled]
      - -CTO [**Disabled**; Enabled]
      - -SEFE [**Disabled**; Enabled]
      - -SENFE [**Disabled**; Enabled]
      - -SECE [**Disabled**; Enabled]
      - -PME Interrupt [**Disabled**; Enabled]
      - -PME SCI [**Disabled**; Enabled]
      - -Hot Plug SCI [**Disabled**; Enabled]
      - -Extra Bus Reserved 0
      - -Reserved Memory 10
      - -Reserved I/O 4

- PCI Express Root Port 2 [Disabled; **Enabled**]
  - -VCI Enable [**Disabled**; Auto]
  - -ASPM [Disabled; **Enabled**]
  - -Automatic ASPM [Manual; **Auto**]
  - -URR [**Disabled**; Enabled]
  - -FER [**Disabled**; Enabled]
  - -NFER [**Disabled**; Enabled]
  - -CER [**Disabled**; Enabled]
  - -CTO [**Disabled**; Enabled]
  - -SEFE [**Disabled**; Enabled]
  - -SENFE [**Disabled**; Enabled]
  - -SECE [**Disabled**; Enabled]
  - -PME Interrupt [**Disabled**; Enabled]
  - -PME SCI [**Disabled**; Enabled]
  - -Hot Plug SCI [**Disabled**; Enabled]
  - -Extra Bus Reserved 0
  - -Reserved Memory 10
  - -Reserved I/O 4
- PCI-to-PCI Bridge
  - -Extra Bus Reserved 0

♦ PPM Configuration

- C-State POPUP [Disabled; **Enabled**]

## BIOS Boot Setup Screen

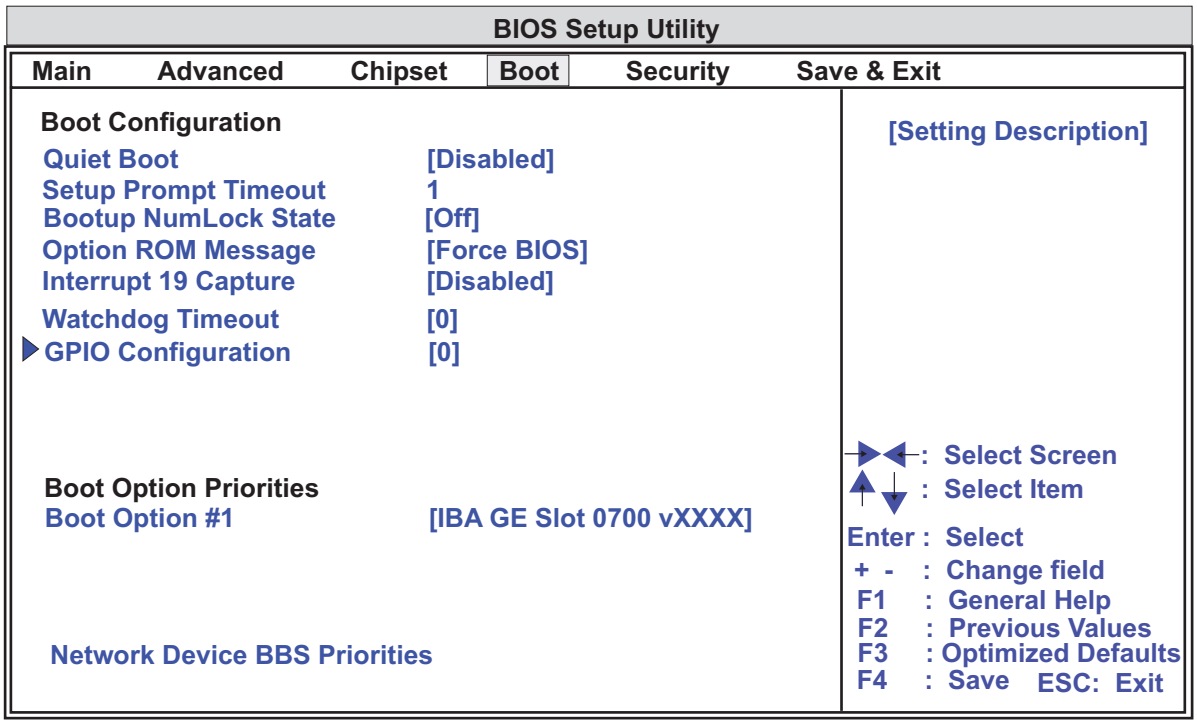


**Figure 4-4. BIOS Boot Setup Screen**

- **Boot Configuration**
  - Quiet Boot [**Disabled**; Enabled]
  - Setup Prompt Timeout 1
  - Bootup Num-Lock [On; **Off**]
  - Option ROM Messages [**Force BIOS**; Keep Current]
  - Interrupt 19 Capture [**Disabled**; Enabled]
  - Watchdog Timeout 0
  - GPIO Configuration
    - GPIO Configuration [Disabled; **Enabled**]
    - GPIO 1 Direction [Input; **Output**]
    - GPIO 2 Direction [Input; **Output**]
    - GPIO 3 Direction [Input; **Output**]
    - GPIO 4 Direction [Input; **Output**]
    - GPIO 5 Direction [**Input**; Output]
    - GPIO 6 Direction [**Input**; Output]
    - GPIO 7 Direction [**Input**; Output]
    - GPIO 8 Direction [**Input**; Output]
    - GPIO 1 Output Level [**0**; 1]
    - GPIO 2 Output Level [**0**; 1]

- GPIO 3 Output Level [**0**; 1]
- GPIO 4 Output Level [**0**; 1]

- **Boot Option Priorities**
  - Boot Option #1 [**IBA GE Slot 0700 vXXXX**; Disabled]
  - Network Device BBS Priorities
    - Boot Option #1 [IBA GE Slot 0700 vXXXX]

## BIOS Security Setup Screen

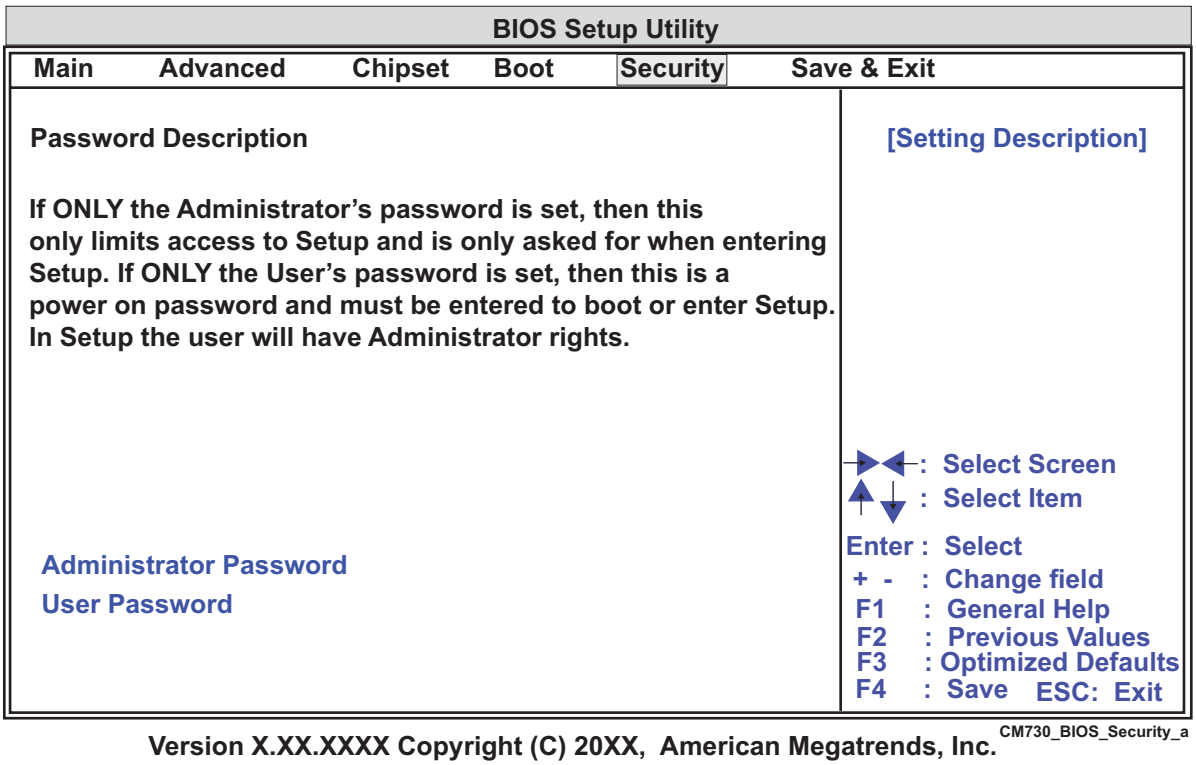


**Figure 4-5. BIOS Security Setup Screen**

- **Administrator Password** [Create New Password]
- **User Password** [Create New Password]

## BIOS Save & Exit Setup Screen

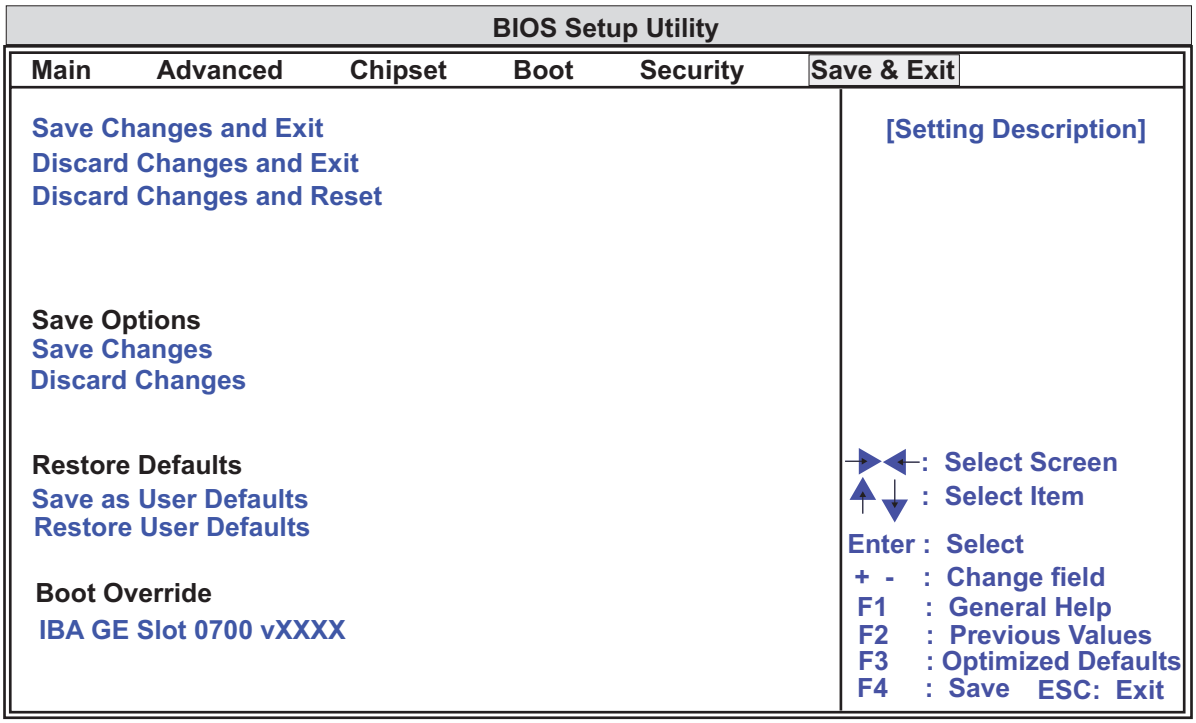


**Figure 4-6. BIOS Save & Exit Setup Screen**

- Save Changes and Exit
  - Save Configuration and Exit? [**Yes**; No]
- Discard Changes and Exit
  - Quit without Saving? [**Yes**; No]
- Save Changes and Reset
  - Save Configuration and Reset? [**Yes**; No]
- Discard Changes and Reset
  - Reset without Saving? [**Yes**; No]

- **Save Options**
  - Save Changes
    - Save Configuration [**Yes**; No]
  - Discard Changes
    - Load Previous Values [**Yes**; No]
  - Restore Defaults
    - Load Optimized Defaults [**Yes**; No]
- **Restore Defaults**
  - Save as User Defaults
    - Save Configuration [**Yes**; No]

- Restore User Defaults
  - Restore User Defaults? [**Yes**; No]

- **Boot Override**
  - IBA GE Slot 0700 vXXXX
    - Save Configuration and Reset? [**Yes**; No]

# Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in the Table A-1 below. Requests for support through the Ask an Expert are given the highest priority, and usually will be addressed within one working day.

- ADLINK's Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the Ampro By ADLINK web page at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

  ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called "My ADLINK" unique to you with access to exclusive services and account information

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to My Stuff area where you can check status, update your request, and access other features.

- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

**Table A-1. Technical Support Contact Information**

| Method | Contact Information |
|---|---|
| Ask an Expert | http://www.adlinktech.com/AAE/ |
| Web Site | http://www.adlinktech.com |
| Standard Mail | Contact us should you require any service or assistance.<br><br>**ADLINK Technology, Inc.**<br>Address: 9F, No.166 Jian Yi Road, Chungho City,<br>Taipei County 235, Taiwan<br>台北縣中和市建一路 166 號 9 樓<br>Tel: +886-2-8226-5877<br>Fax: +886-2-8226-5717<br>Email: service@adlinktech.com<br><br>**Ampro ADLINK Technology, Inc.**<br>Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA<br>Tel: +1-408-360-0200<br>Toll Free: +1-800-966-5200 (USA only)<br>Fax: +1-408-360-0222<br>Email: info@adlinktech.com<br><br>**ADLINK Technology (China) Co., Ltd.**<br>Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203)<br>300 Fang Chun Rd., Zhangjiang Hi-Tech Park,<br>Pudong New Area, Shanghai, 201203 China<br>Tel: +86-21-5132-8988<br>Fax: +86-21-5132-3588<br>Email: market@adlinktech.com |

**Table A-1. Technical Support Contact Information**

**ADLINK Technology Beijing**
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1, B/D
Shang Di East Rd., Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8625
Email: market@adlinktech.com

**ADLINK Technology Shenzhen**
Address: 深圳市南山区科技园南区高新南七道 数字技术园
A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7,
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

**ADLINK Technology (Europe) GmbH**
Address: Nord Carree 3, 40477 Duesseldorf, Germany
Tel: +49-211-495-5552
Fax: +49-211-495-5557
Email: emea@adlinktech.com

**ADLINK Technology, Inc. (French Liaison Office)**
Address: 15 rue Emile Baudot, 91300 Massy CEDEX, France
Tel: +33 (0) 1 60 12 35 66
Fax: +33 (0) 1 60 12 35 66
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**ADLINK Technology Japan Corporation**
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KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
Chiyoda-ku, Tokyo 101-0045, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5209-6013
Email: japan@adlinktech.com

**ADLINK Technology, Inc. (Korean Liaison Office)**
Address: 서울시 서초구 서초동 1506-25 한도 B/D 2 층
2F, Hando B/D, 1506-25, Seocho-Dong, Seocho-Gu,
Seoul 137-070, Korea
Tel: +82-2-2057-0565
Fax: +82-2-2057-0563
Email: korea@adlinktech.com

**ADLINK Technology Singapore Pte. Ltd.**
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Singapore 349584
Tel: +65-6844-2261
Fax: +65-6844-2263
Email: singapore@adlinktech.com

**ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)**
Address: No. 1357, "Anupama", Sri Aurobindo Marg, 9th Cross,
JP Nagar Phase I, Bangalore - 560078, India
Tel: +91-80-65605817
Fax: +91-80-22443548
Email: india@adlinktech.com

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