UMC 80486 System Board

User's Manual

(4SLUD-1.0)

Mainboard

ISA BUS
EISA BUS
LOCAL BUS

UMC 80486 System Board

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Table of Content

Chapter 1

INTRODUCTION

The UMC 486 system board is a high performance main-board that offers outstanding features and performance for advanced personal computer. It contains INTEL 80486 Micro-Processor, Direct Mapping Write Back Cache Controller.
It provides tremendous flexibility in configuration for on-board memory, from 1MBytes to 32Mbytes of memory configuration.

1.1 FEATURES

The UMC 486 system board comes with the following features:

* INTEL 80486 Microprocessor with standard 32-bit architecture.
* Two stage cache memory system for fast caching
* Second level cache with Direct-Mapped organization with Write-Back operation with 64KB/128KB or 256KB cache subsystem.
* Tremendous flexibility for on-board memory, either using 256KB, 1MB and 4MB types of RAM module separately or those types of RAM module combination.
* Up to 32MB DRAM memory support with FAST page Mode
* Socket for PGA packing 486SX(P23),486DX,486DX2(P24), P23T(P23 overdriver) 80487SX.
* PQFP packing 80486SX.
* BIOS Shadow RAM:System BIOS, Video BIOS and Adapter BIOS can remap 256KBytes of memory to the top of system memory
* CMOS RAM with rechargeable battery backup
* Real time clock.
* 7 DMA channels.
* 15 interrupt levels.
* 3 programmable timer
* Operates with PC-DOS, MS-DOS, OS/2, UNIX, XENIX, WINDOW 3.0, NOVELL.
* Half size with 4-layers PC board.
* UMC 82C481 & 82C482 chip sets supports.

Chapter 2

HARDWARE CONFIGURATION

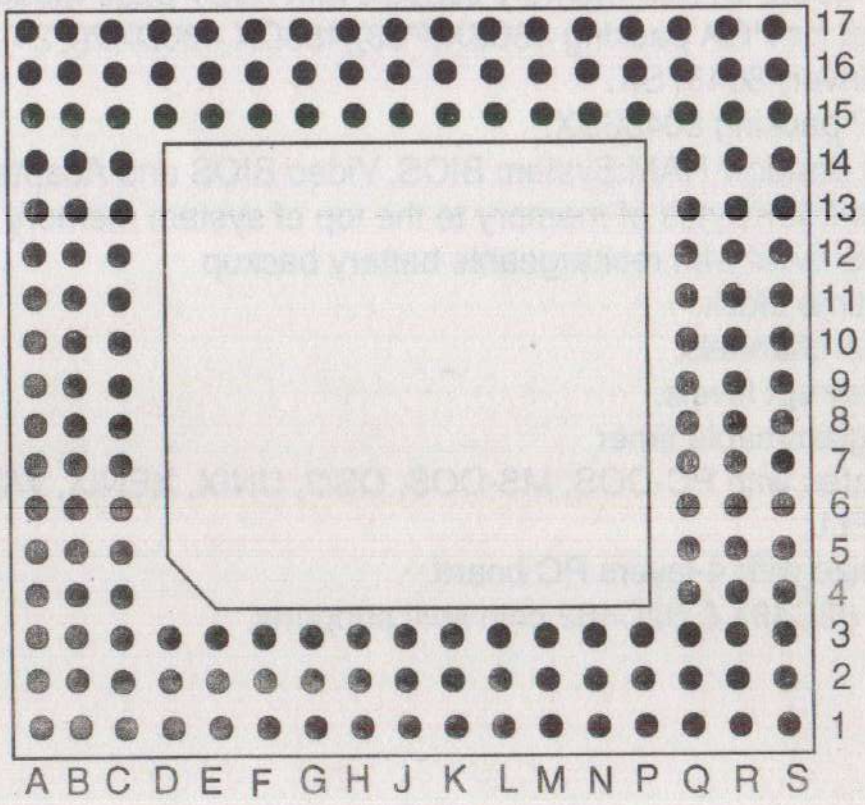
2.1 General

The UMC 486 system board is a 80486 based motherboard, it is designed to have wide range of memory configuration, from 1MBytes upto 32MBytes of memory on board. In addition, it allows to install either 64KBytes, 128KBytes or 256KBytes Secondary Level Cache Memory Subsystem to increase the system performance.

2.2 80486 CPU

INTEL 80486 use an 80486 microprocessor that runs at a clock speed of 25/33/50/66MHz. The Intel 80486 chip basically is an 80386 microprocessor integrated with the 80387 math coprocessor, a paging and memory management unit, and an 8KByte data and instruction cache by integration all these components on one chip, the Intel company has created a microprocessor capable of operating two times faster than the 80386DX CPU.

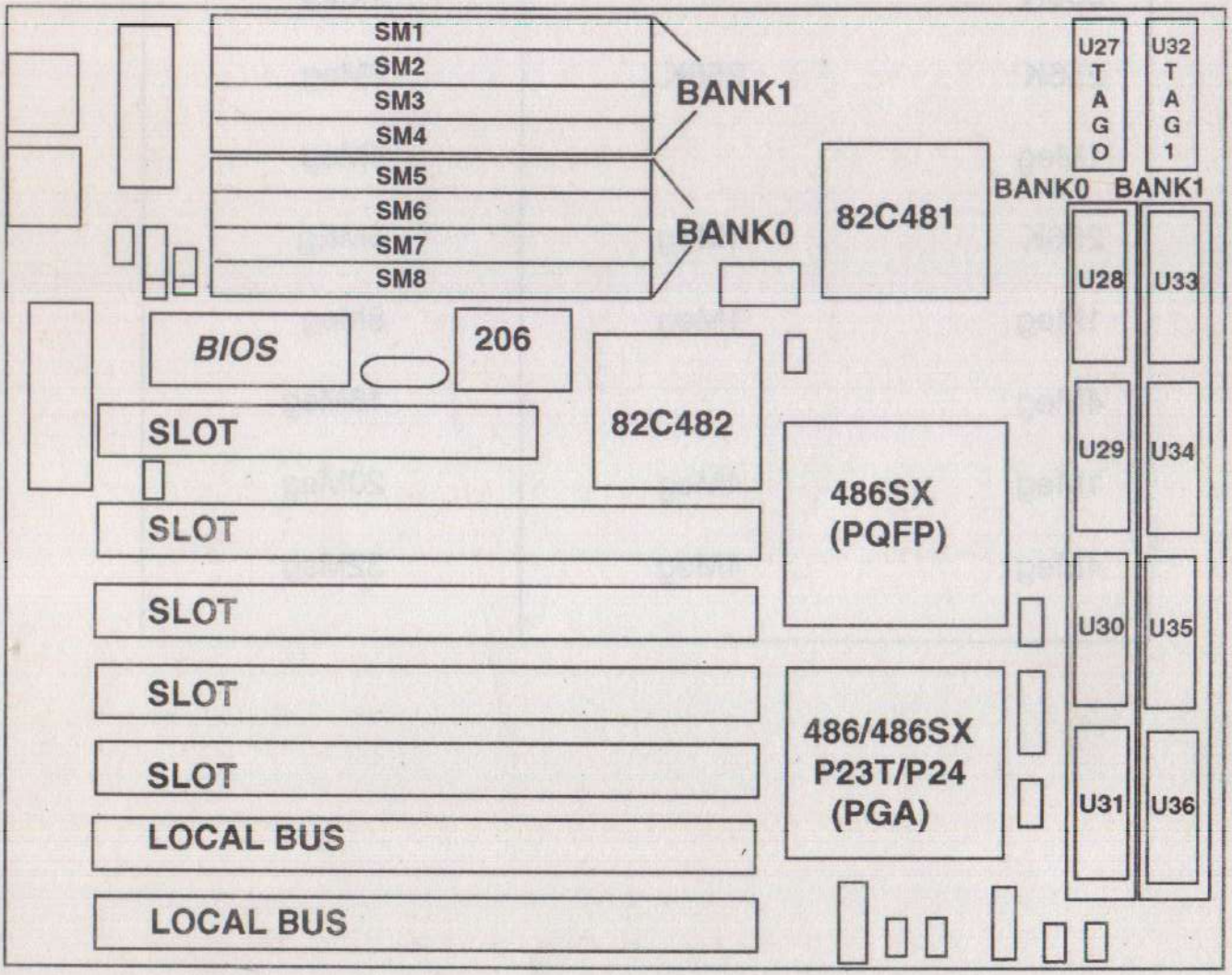
Figure 2.1 80486 pin configuration



2.3 Cache Memory

The primary memory is the 8Kbyte 4-way associated cache inside the 80486 chip itself. To take the fullest advantage of the speed of the CPU there is a secondary cache: the direct map LOOK-THROUGH, no WRITE buffered, write-back cache controller on board. The function of cache memory is to provide fast local storgae for frequently accessed code and data. The cache system intercepts memory from the 486 and checks if the required data is already stored in the cache. If it is, this referred to as a "hit". When ever "hit" occurs, the data is transferred to the 486 without incurring a wait state.

If the required data is not in the cache ,the memory reference is returned to the system and the data is retrieved from the main memory.



2.4 System Memory

The UMC 486 mother board provides tremendous flexibility in configuration for on-board memory. The local DRAM system is no limitation on the configuration of DRAM as long as no previous banks are empty. The DRAM banks have to be filled in the following order: BANK0 included SM5,SM6,SM7,and SM8. BANK1 included SM1,SM2,SM3 and SM4 .Table 2.2 is a listing of possible memory configuration.

BANK0	BANK1	TOTAL SIZE
256K		1Meg
256K	256K	2Meg
1Meg		4Meg
256K	1Meg	5MEg
1Meg	1Meg	8Meg
4Meg		16Meg
1Meg	4Meg	20Meg
4Meg	4Meg	32Meg

In order to work with different types of DRAM speed.
DRAM controller is designed to be very robust to accommodate different manufacturer's DRAM specifications. Yet it is sophisticated to support:

-Fast or Standard page mode DRAM.
-Programmable Wait states: 0, 1, 2.
-Burst mode directly if CPU is 80486.
-256KB or 384KB (A to F segments of the first 1 Meg) relocation to the top of DRAM memory.
-Write Protected Shadow RAM for BIOS (C, D, E, F segments of the first 1 Meg.)
-Automatic Memory Size Detection.
-Two banks of DRAM with memory size up to 32Meg.
-HIDDEN DRAM refresh is automatically performed when cache is enable to improve system performance.

2.5 Shadow RAM and Memory Remapping

The UMC 486 system board provides shadow RAM capability, since access to local memory RAM is much faster than access to BIOS ROM. The function of shadow RAM is to copy the system BIOS program into the memory RAM so called memory remapping, for direct access. Besides, it also supports for different shadowing-- video BIOS and adapter BIOS.

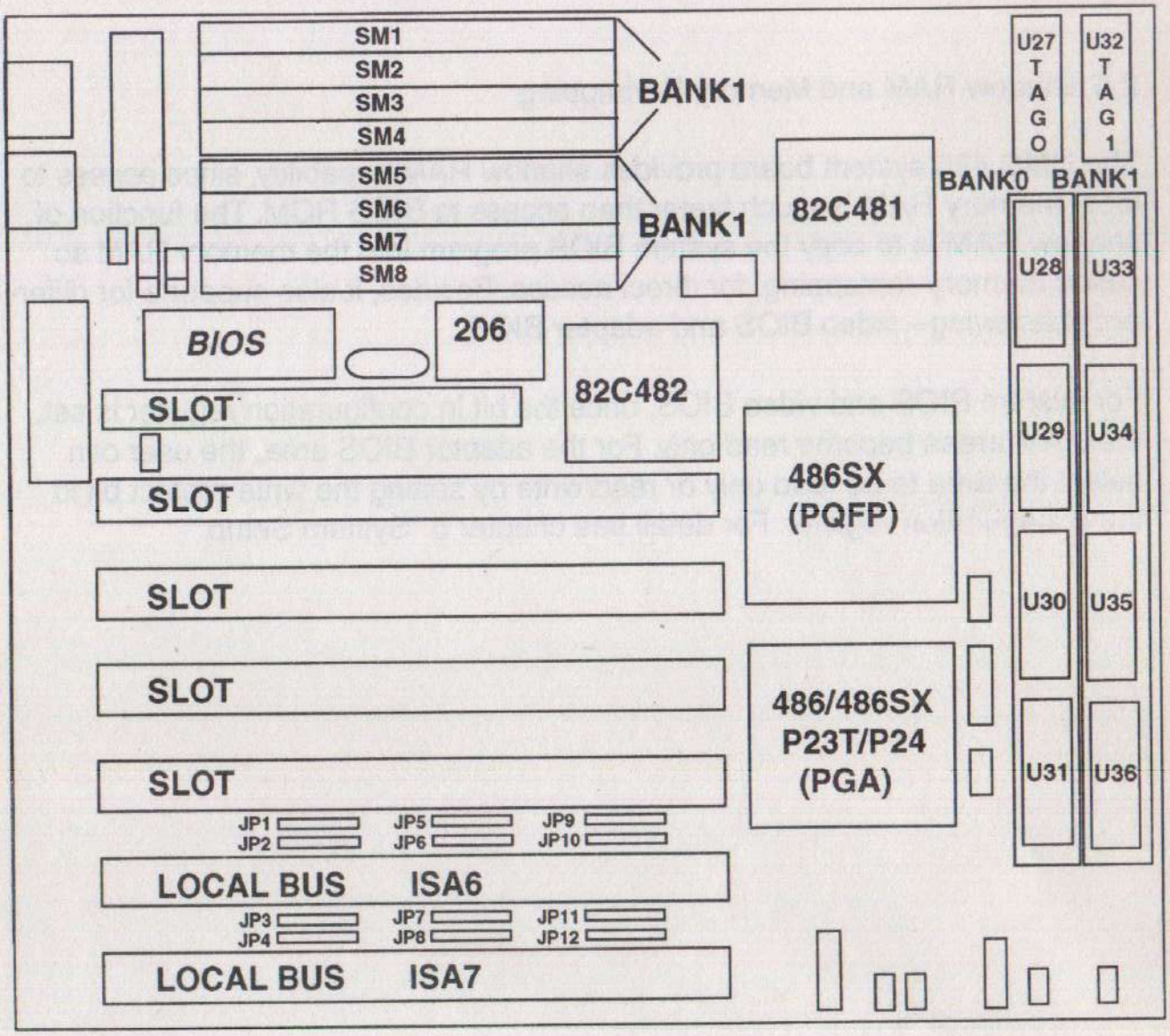
For system BIOS and video BIOS, once the bit in configuration register is set, the RAM areas become read only. For the adaptor BIOS area, the user can select the area to be read only or read/write by setting the write protect bit in the configuration register. For detail see chapter 5 "System Setup."

2.6 Expansion Bus

2.6.1 ISA Bus Slots

Industry Stardand Architecture (ISA) bus is used for UMC 486 system board. Therefore, most of the add-on-cards available on the market are suitable to be used together with the Cache 486 system board. In addition, the bus consists of six 16-bit expansion slots and one 8-Bit slot.(Two local bus slots can be changed to two ISA slots independently.)

The speed of the I/O bus depends on the BIOS setting, it can be selected as divided by 2,3,4,5,6 & 8 for the Cache 486 system board. In order to avoid the compatibility problem, make sure the speed of the add-on-card which is compatible with the speed as mention above.

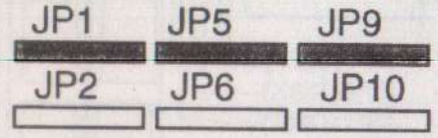


2.6.2 Local Bus Slots

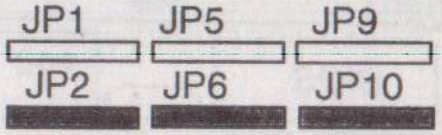
UMC system board can change the slot 6 and slot 7 from ISA slots to the type of EISA slots then going to the local bus function.

UMC system board include two version of the OPTi local bus defination. The detail pin defination as next page. In the first version of OPTi local bus defination is compatible with the ISA bus ,its mean you also can use the ISA card in the local bus slot. But in the second version of OPTi loacl bus defination this is not allowed. Please check your add on cards suppliers in detail for local bus add on cards.

ISA 6

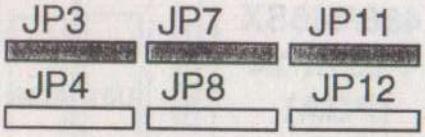


The second version of OPTi local bus defination.

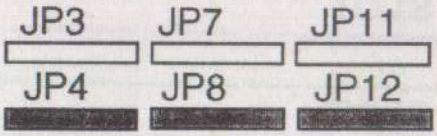


The first version of OPTi local bus defination.
(ISA compatible)

ISA 7



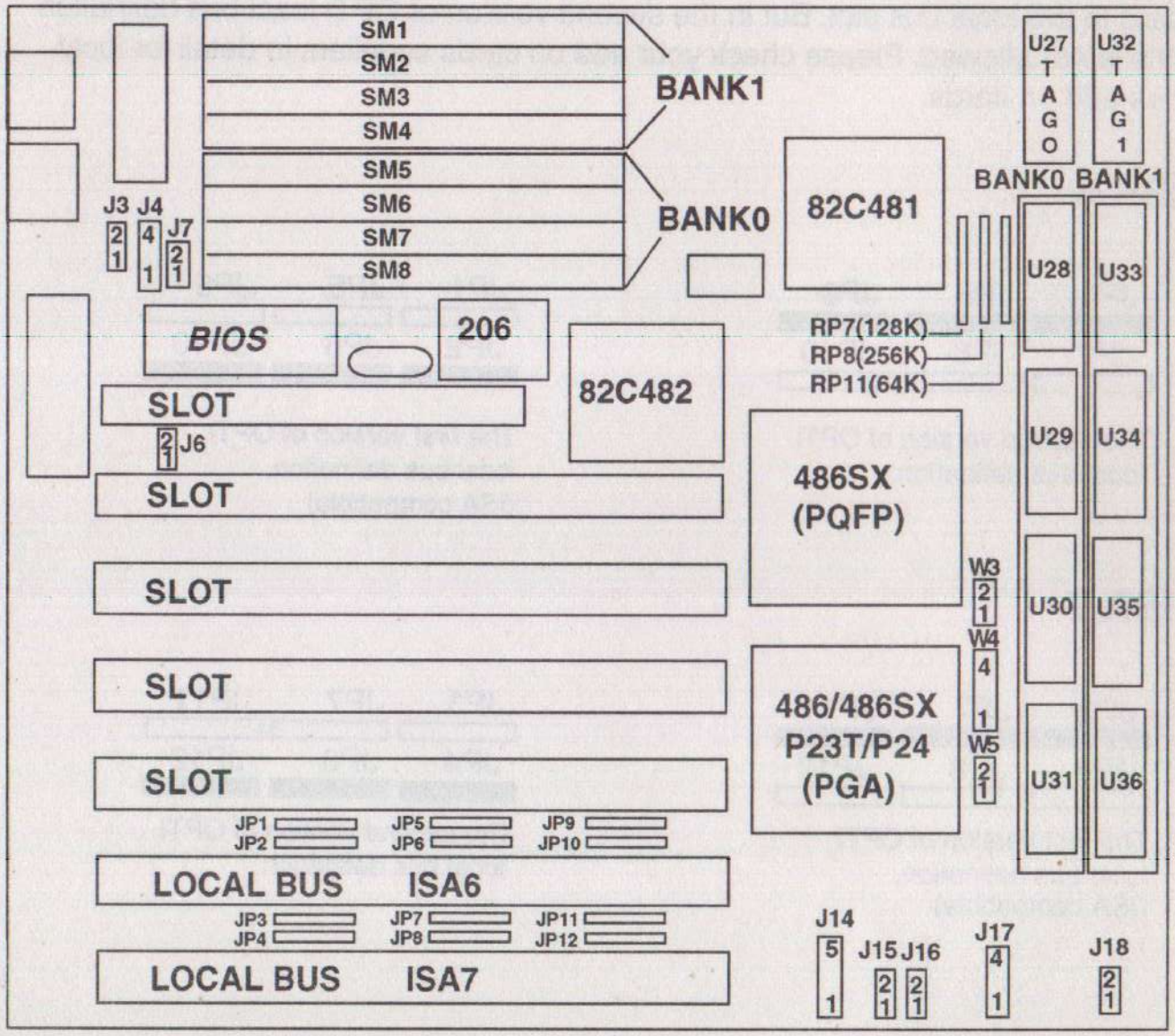
The first version of OPTi local bus defination.
(ISA compatible)



The second version of OPTi local bus defination.

2.7 LAYOUT OF UMC 486 SYSTEM BOARD

The layout diagram of the UMC 486 system board indicated the location of main components and Memory Bank.



2.8 The UMC Chip-Set

The UMC 486 system board consists of the following chipset:
82C481-----Integrated Memory Controller (IMC)
82C482-----Integrated System Controller (ISC)
82C206------Integrated Peripherals Controller(IPC)

With these combination, the chip-set support the UMC 486 system board with Direct Mapped organization with Write-Back cache subsystem.

* 100% IBM PC/AT compatible
* Support 80486 CPU running at 25/33/50/66 MHz in 1X clock
* Support PQFP 80486SX.
* Built-in cache controller:
  -Direct-mapped organization with write-back operation
  -0 wait state for cache hit
  -Flexible cache size: 64/128/256 KB
  -Hidden DRAM refresh to boost system performance
  -Built-in registers to support three independent non-cacheable regions
  -Support Automatic Memory Size Detection
  -Support cache line filled with the same as well as 80486 burst mode
* Sophisticated DRAM controller:
  -Support Fast/Standard page mode
  -Support 2 banks DRAM with memory size up to 32MB
  -Support mixable 256K, 1M, 4M DRAM modules
  -Programmable DRAM wait states
  -Support 256KB or 384KB (A to F segments for first 1MB) relocation to the top of DRAM memory
* Support sophisticated Shadow RAM for video and system BIOS (C,D,E,F segments)
* Support fast GATE A20 and fast CPU reset to optimize OS/2 operations.
* Synchronous AT bus clock with programmable clock (devided by 2,3,4,5,6)
* Programmable CPU clock (divided by 1,2,3,4)
* Support 512KB EPROM with single EPROM BIOS configuration
* Support parity generation and checking

2.9 ROM BIOS

Basic Input Output System (BIOS) is used for booting up the system whenever power is on. It is permanently recorded in Read Only Memory (ROM) chips, if the battery maintain the power. For UMC 486 system board, AMI BIOS, be installed on the UMC 486 system board.

In addition, AMI BIOS provides CMOS and XCMOS configuration registers for different system configuration setup. Details of the setup procedure see Chapter 5 for detail explaination.

2.10 Peripheral Connections

Peripheral connections designed on UMC 486 system board include: keyboard & powersupply connection port, and the standard on-board connector that commonly mounted on the front panel, such as--reset connector, Turbo LED display connector, Turbo mode connector, speaker connector, external battery connector, keylock and power LED connector.

2.11 Real Time Clock Battery

Real time clock battery is a nickel cadmiun battery. Its function is to maintain the system configuration information in the CMOS RAM. If your system will be not in use for long time, the system configuration information may lost, result in on-board battery lost of its charge.

Chapter 3

Hardware Setup Guide

This Setup Guide helps the user to setup the function as designed on UMC 486 system board, or others. Each jumper setting explained clearly at the following section.

3.1 Jumpers

The UMC 486 system board has been designed with different jumpers. It has to be setup before boot up to configure various functions of the system. A jumper is two or more gold pin which may or may not be covered by a plastic connector plug.

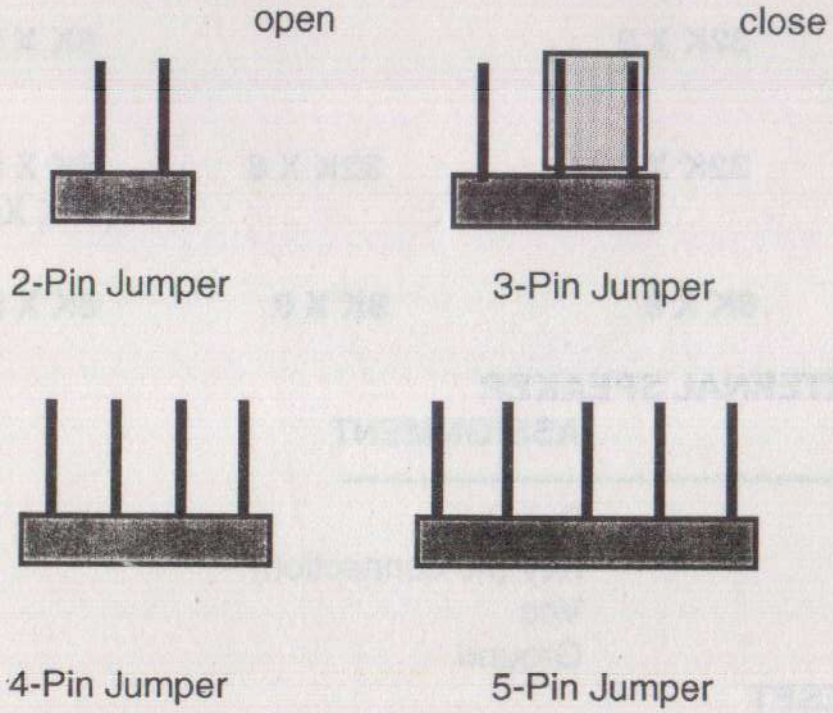


Figure 3.1 jumper

3.2 UMC 486 System Board Jumpers Setting

J4: EXTERNAL 6 VOLT BATTERY

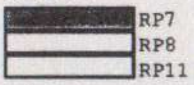
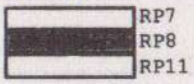
PIN#	ASSIGNMENT
1	Battery Positive
2	Key (no connection)
3	Ground
4	Ground

J4 is a 4-pin Battery connector. It is used to supply power to CMOS real time clock, in order to maintain previous configuration setup, while the system power is off.

J6: TYPE OF DISPLAY

PIN#	ASSIGNMENT
1-2	Color
No Jumper	Monochrome

RP7,RP8,RP9 CACHE SELECT

	U28,U29,U30,U31	U33,U34,U35,U36	U27	U32
128K 	**32K X 8**		**8K X 8**	
256K 	**32K X 8**	**32K X 8**	**8K X 8 (32K X 8)**	**8K X 8**
64K 	**8K X 8**	**8K X 8**	**8K X 8**	

J17: EXTERNAL SPEAKER

PIN#	ASSIGNMENT
1	Speaker
2	Key (no connection)
3	Vcc
4	Ground

J18: RESET

PIN#	ASSIGNMENT
1	Reset
2	Ground

J14: KEYLOCK & POWER LED

PIN#	ASSIGNMENT
1	Power Good
2	Key(no connection)
3	Ground
4	Keylock
5	Ground

J15: TURBO SWITCH

PIN#	ASSIGNMENT
1	Ground
2	Turbo

J16: TURBO LED

PIN#	ASSIGNMENT
1	Negative End of Turbo LED
2	Postive End of Turbo LED

W3,W4,W5 CPU TYPE SELECT

PQFP TYPE CPU CONTROL

W3 :OPEN 80486SX(PQFP) ENABLED
W3 :CLOSE 80486SX(PQFP) DISABLED

PGA TYPE CPU CONTROL

	W5	W4	W3
486	1-2	1-2,3-4	CLOSED
486DX2(P24)	1-2	1-2,3-4	CLOSED
486SX(P23)	OPEN	2-3	CLOSED
P23T	2-3	1-2,3-4	DON'T CARE
487SX(P23N)	2-3	1-2,3-4	DON'T CARE

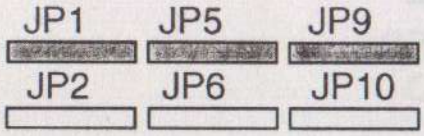
J3: Battery Select

PIN#	ASSIGNMENT
OPEN	External Battery
CLOSE	Internal Battery

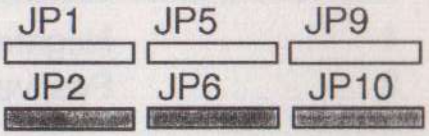
J7: CMOS Discharge

PIN#	ASSIGNMENT
1-2	Normal
2-3	CMOS Reset

LOCAL BUS STANDARD SELECT (ISA6)

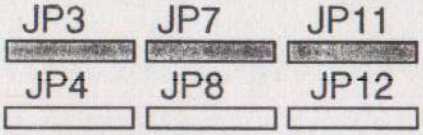


The second version of OPTi local bus defination.

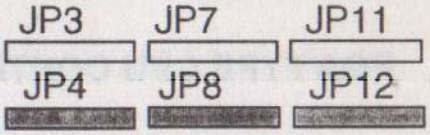


The first version of OPTi local bus defination. (ISA compatible)

LOCAL BUS STANDARD SELECT (ISA7)



The first version of OPTi local bus defination. (ISA compatible)



The second version of OPTi local bus defination.

Chapter 4

INSTALLATION

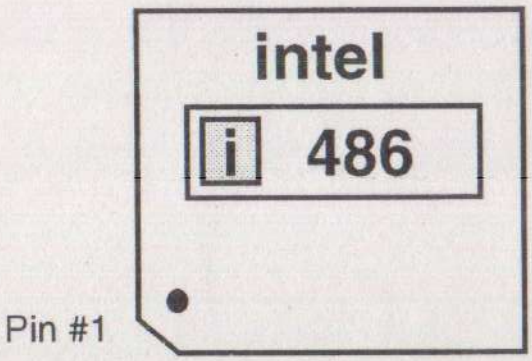
4.1 Micro-Processor Installation

The mainboard is used with 80486DX CPU, and the CPU speed must match with the frequency value of the OSC component. It will cause system hanging up if the OSC's frequency value is higher than CPU's.The CPU is a sensitive electric component and it can be easily damaged bystaticelectricity,so users must keep it away from metal surface when the CPU is installed onto mainboard.When the user installs the CPU on socket,please notice the pin 1 of CPU is in the same corner as the pin 1 of socket.Before the CPU isinstalled, the mainboard must be placed on a flat plane in order to avoid being broken by the pressure of CPU installation.

Installing the Micro-Processor:

* Look for the CPU and the PGA socket pin# 1 location
* Place the CPU # 1 pin on the PGA socket #1 pin (printed on the PCB)
* Press the CPU gently

The pin location of CPU is shown as follow:



Chapter 5

AMI BIOS SETUP PROGRAM

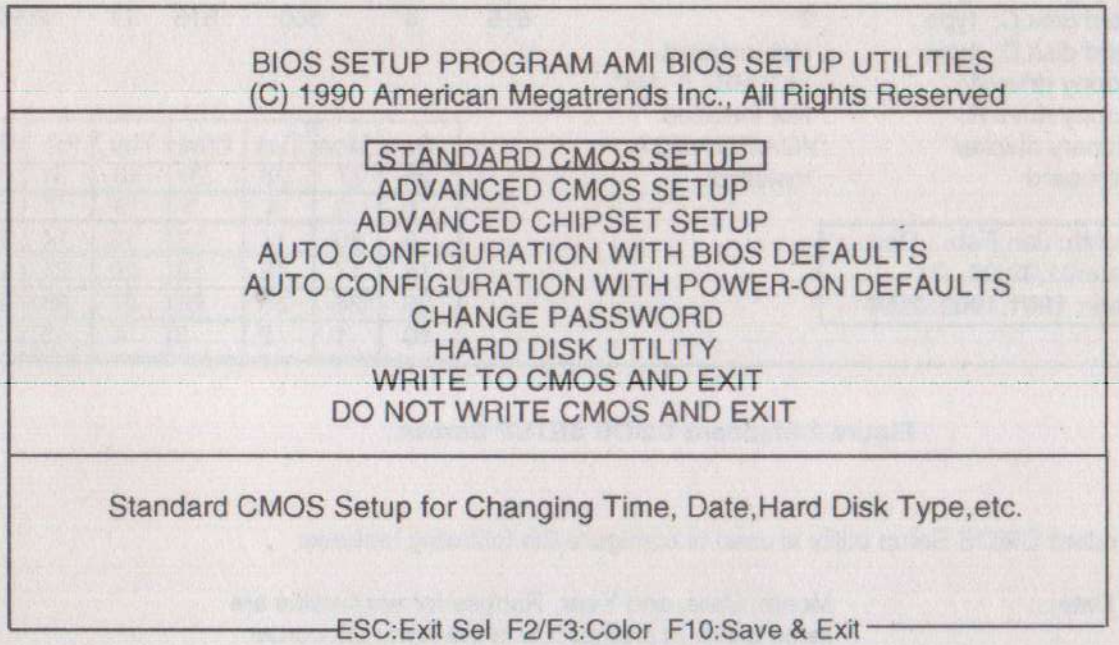
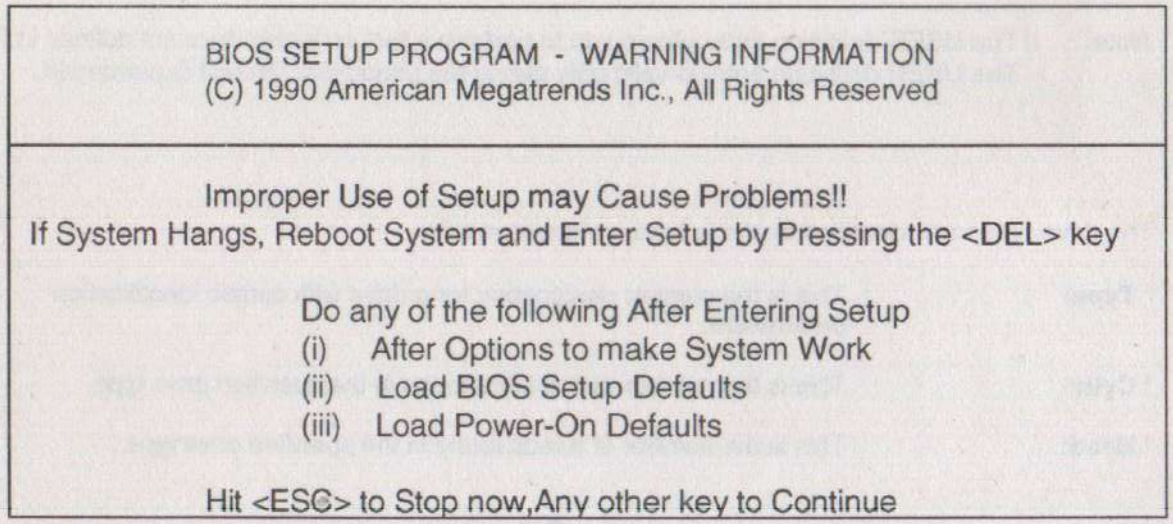


Figure 1

The generic menu options of the BIOS SETUP Program are shown in Figure 1

A warning message, shown in below is displayed each time one of the first three options (Standard CMOS Setup, Adveanced CMOS Setup, and Advanced Chips Set Setup) is selected, before any changes are shown to any of the setup parameters.



BIOS SETUP PROGRAM-STANDARD CMOS SETUP
(C) 1990 American Megatrends Inc., All Rights Reserved

Date (mn/date/year) : Sun, Feb,2,1992
TIME (hour/min/sec) : 15 : 01 : 16
Daylight saving : Disabled
Hard disk C: type : 2
Hard disk D: type : Not Installed
Floppy drive A: : 1.2 MB, 5 1/4"
Floppy drive B: : Not Installed
Primary display : VGA/PGA/EGA
Keyboard : Installed

Base memory: 640 KB
Ext. memory: 1408 KB

Cyln	Head	WPcom	LZone	Sect	Size
615	4	300	615	17	20MB

Month: Jan,Feb....Dec
Date:01,02,03...31
Year: 1901,1902..2099

Sun	Mon	Tue	Wed	Thu	Fri	Sat
26	27	28	29	30	31	1
2	3	4	5	6	7	8
9	10	11	12	13	14	15
16	17	18	19	20	21	22
23	24	25	26	27	28	29
30	1	2	3	4	5	6

Figure 2 Standard CMOS SETUP Screen

The Standard CMOS Setup utility is used to configure the following features:

* **Date:** Month, Date, and Year, Ranges for each value are listed below in prompt box in the lower left corner of the CMOS Setup Screen (Figure 2).

***Time:** Hour, Minute, and Second. Uses 24 hour clock format, i.e., for PM numbers, add 12 to the hour. You would enter 4:30 P.M. as 16:30:00.

* **Daylight Saving:** Disabled or Enabled.

* **Hard Disk C:**
* **Hard Disk D:** Hard disk types from 1 to 46 are standard ones: and type 47 is user definable. The user must enter the hard disk parameters for each drive.

Note: The USER definition entry allows you to perform a test on a disk drive not defined in ROM. The USER definition entry is valid only during the period that the test is performed.

The drive types are identified by the following characteristics:

* **Type:** This is the number designation for a drive with certain identification parameters.

* **Cyln:** This is the number of cylinders found in the specified drive type.

* **Head:** This is the number of heads found in the specified drive type.

* **WPcom:** WPcom is the read delay circuitry which takes into account the timing differences between the inner and outer edges of the surface of the disk platter .

* **L-zone:** L-zone is the landing zone of the heads. This number determines the cylinder location where the heads will normally park when the system is shut down.

* **Capacity:** This is the formatted capacity of the drive based on the following formula: (# of heads) x (#of cylinders) x (17 secs/cyl) x (512 bytes/sec)

Listed below are the attributes for disk types 1 through 46.

Type	Cyln	Head	WPcom	LZone	Sect	Size
1	306	4	128	305	17	10MB
2	615	4	300	615	17	20MB
3	615	6	300	615	17	31MB
4	940	8	512	940	17	62MB
5	940	6	512	940	17	47MB
6	615	4	65535	615	17	20MB
7	462	8	256	511	17	31MB
8	733	5	65535	733	17	30MB
9	900	15	65535	901	17	112MB
10	820	3	65535	820	17	20MB
11	855	5	65535	855	17	35MB
12	855	7	65535	855	17	50MB
13	306	8	128	319	17	20MB
14	733	7	65535	733	17	43MB
16	612	4	0	663	17	20MB
17	977	5	300	977	17	41MB
18	977	7	65535	977	17	57MB
19	1024	7	512	1023	17	60MB
20	733	5	300	732	17	30MB
21	733	7	300	732	17	43MB
22	733	5	300	733	17	30MB
23	306	4	0	336	17	10MB
24	925	7	0	925	17	54MB
25	925	9	65535	925	17	69MB
26	754	7	754	754	17	44MB
27	754	11	65535	754	17	69MB
28	699	7	256	699	17	41MB
29	823	10	65535	823	17	68MB
30	918	7	918	918	17	53MB
31	1024	11	65535	1024	17	94MB
32	1024	15	65535	1024	17	128MB
33	1024	5	1024	1024	17	43MB
34	612	2	128	612	17	10MB
35	1024	9	65535	1024	17	77MB
36	1024	8	512	1024	17	68MB

37	615	8	128	615	17	41MB
38	987	3	987	987	17	25MB
39	987	7	987	987	17	57MB
40	820	6	820	820	17	41MB
41	977	5	977	977	17	41MB
42	981	5	981	981	17	41MB
43	830	7	512	830	17	48MB
44	830	10	65535	830	17	69MB
45	917	15	65535	918	17	114MB
46	1224	15	65535	1223	17	152MB

"Not Installed" is available for use as an option.
This option could be used for diskless workstations and SCSI hard disks. Type 47 may be used for both hard disks C: and D:.
The parameters for type 47 under Hard Disk C:and Hard Disk D: may be different, which effectively allows 2 different user-definable hard disk types

* Floppy Drive A and Floppy Drive B: The options are 360 KB 5 1/4," ,1.2 MB 5 1/4",720KB 31/2",1.44MB 3 1/2", and Not installed. Not installed could be used as an option for diskless workstations.
* Primary Display: Options are Monochrome,Color 40 x 25, VGA/PGA/EGA,Color 80 x 25, and Not Installed. The Not installed option could be used for network file servers.
* Keyboard: Options are installed or Not installed.

ADVANCED CMOS SETUP

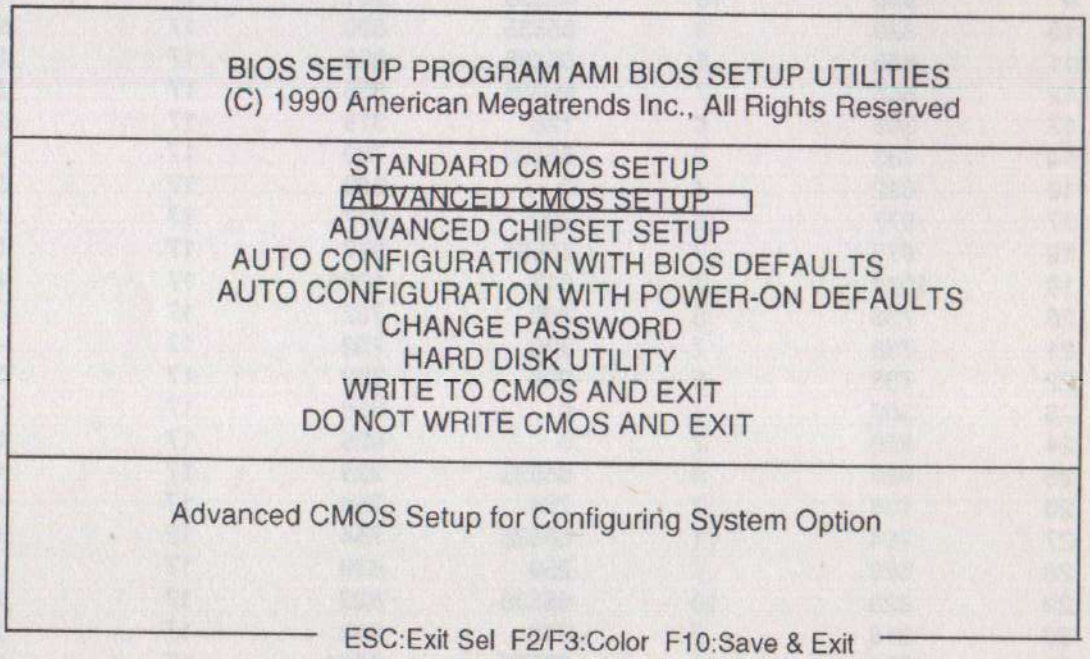


Figure 3

Typematic Rate Programming
Extended Momory Test
Memory Test Tick Sound
Memory Parity Error Check
Hit<DEL>Message Display
Wait for<F1>If Any Error
Internal/External Cache Memory
(486) of Cache Memory (386)
* Fast Gate A20 Option
* Video of Adapter ROM Shadow
* GA20 Line After System Boot
The options for the following featuers of the Advancde CMOS setup are either "Present" or "Absent:"
Numeric Processor
Weitek Processor
The options for Power-On Up Num Lock are "On" or "Off."
The options for system boot Up Speed are "High" or "Low."

BIOS SETUP PROGRAM - ADVANCED CMOS SETUP
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Typematic Rate Programming	: Disabled	Video ROM Shadow C400,16K	: Enabled
Typematic Rate Delay (msec)	: 500	Adaptor ROM Shadow C800,16K	: Disable
Typematic Rate (Chars/Sec)	: 15	Adaptor ROM Shadow CC00,16K	: Disabled
Above 1 MB Memory Test	: Disabled	Adartor ROM Shadow D000,16K	: Disabled
Memory Test Tick Sound	: Enabled	Adaptor ROM Shadow D400,16K	: Disabled
Memoty Parity Error Check	: Enabled	Adaptor ROM Shadow D800,16K	: Disabled
Hit <DEL> Message Display	: Enabled	Adaptor ROM Shadow DC00,16K	: Disabled
Hard Disk Type 47 RAM Area	: 0:300	Adaptor ROM Shadow E400, 16K	: Disabled
Wait For <F1> If Any Error	: Enabled	Adaptor ROM Shadow E800, 16K	: Disabled
System Boot Up Num Lock	: On	Adaptor ROM Shadow EC00, 16K	: Disabled
Weitek Processor	: Absent	System ROM Shadow F000, 64K	: Enabled
Floppy Driver Seek At Boot	: Disabled		
System Boot Up Sequence	: A: , C:		
System Boot Up CPU Speed	: High		
Cache Memory	: Both		
Gate A20 Emulation	: Enabled		
Password Checking Option	:Disabled		
Video ROM Shadow C000,16K	:Enabled		

Figure 4

A short description follows for each of the options on the Advanced CMOS Setup Screen.

Typematic Rate Programming :

By enabling this option, the user can adjust the rate at which a keystroke is repeated. The options "Typematic Rate Delay" and "Typematic Rate" affect this rate. When a key is pressed and held down,the character appears on the screen and after a delay set by the Typematic Rate Delay, it keeps on repeating at a rate set by the Typematic Rate value. When two or more keys are pressed and held down simultaneously, only the last key pressed will be repeated at the typematic

. rate. This stops when the last key pressed is released, even if other keys are depressed.

Extended Memory Test:

This feature, when enabled, will invoke the POST memory routines on the RAM above 1 MB (if present on the system). If disabled, the BIOS will only check the first 1MB of RAM.

Memory Test Tick Sound:

This option will enable (turn on) or disable (turn off) the "ticking" sound during the memory test.

Memory Parity Error Check:

If the system board does not have parity RAM, the user may disable the memory parity error checking routines in the BIOS. The user should check with the manufacturer regarding the proper setting of this option.

Hit <DEL> Message Display :

Disabling this option, will prevent the message:

"Hit <DEL> if you want to run SETUP"

From appearing on the screen when the system boots-up.

Hard Disk Type 47 Data Area :

the AMI BIOS SETUP features two user-definable hard disk types.

Normally, the data for these disk types are stored at 0:300 in lower system RAM. If a problem occurs with other software, this data can be located at the upper limit of the DOS shell (640KB). If the option is set to "DOS 1 KB," the DOS Shell is shortened to 639 KB, and the top KB is used for the hard disk data storage. Please refer to Figure 4 for this option.

Wait for <F1> If Any Error :

Before the system boots-up, the BIOS will execute the POST routines, a series of system diagnostic routines. If any of these tests fail, but a non-fatal error has occurred and the system can still function, the BIOS will respond with an appropriate error message followed by the following statement:

"Press <F1> to continue."

If this option is disabled, any non-fatal error which occurs will not generate the above statement, but the BIOS will still display the appropriate error message. This will eliminate the need for any user response to a non-fatal error condition message..

System Boot Up Num Lock :

The user may turn off the "numlock" option on his Enhanced Keyboard when the system is powered on. This will allow him to use the arrow keys on the numeric keypad instead of using the other set of arrow keys on the Enhanced Keyboard. The BIOS will default to turning the "num lock" on.

Weitek Processor :

These options allow the user to mark the Weitek numeric coprocessor (WTL4167) as present or absent.

Floppy Drive Seek At Boot :

The default for this option is "Disabled" to allow a fast boot and to decrease the possibility of damage to the heads.

System Boot Up CPU Speed :

The speed at which the system will boot up is determined with this option. Choices for this option are "high" or "low". The default speed is "low".

System Boot Up Sequence :

The AMI BIOS will normally attempt to boot from floppy drive A: (if present), and if unsuccessful, it will attempt to boot from hard disk C: This sequence can be switched using this option if the option is set to "C: ,A:," the system will attempt to boot from the hard drive C: and then A: If the option is set to "A:, C:," the sequence is reversed. Please refer to Figure 4 for this option.

Password Check Option :

The password feature can be used to prevent unauthorized system boot-up or unauthorized use of BIOS SETUP. The option in the BIOS SETUP only allows the user to enable the password check option every time the system boots or upon entering SETUP only. A third option is to disable the password option entirely.

The default option is **"Disabled."** The prompt for the password will not appear when the system is rebooted.

If the **"Always"** option is chosen at Setup.each time the system is turned on, i.e. "booted,"the prompt for user password will appear.

If the **"Setup"** option is chosen at Setup. The password prompt will not appear when the system is turned on, but will appear if the user attempts to enter the Setup program.
The program allows three attempts to key in the correct password. After each incorrect attempt, the prompt to enter the current password will appear, followed by an "X." After the third incorrect attempt, the system will lock and it will be necessary to reboot. The screen will not display the characters entered.

Cache Memory:

With this option, the user may enable or disable the cache.

Gate A20 Emulation:

This option uses the fast gate A20 line supported in some chip sets, to access any memory above 1 MB. Normally, all RAM access above 1 MB is handled through the keyboard controller chip. Using this option will make the access faster than the normal method. This option is very useful in networking operating systems.

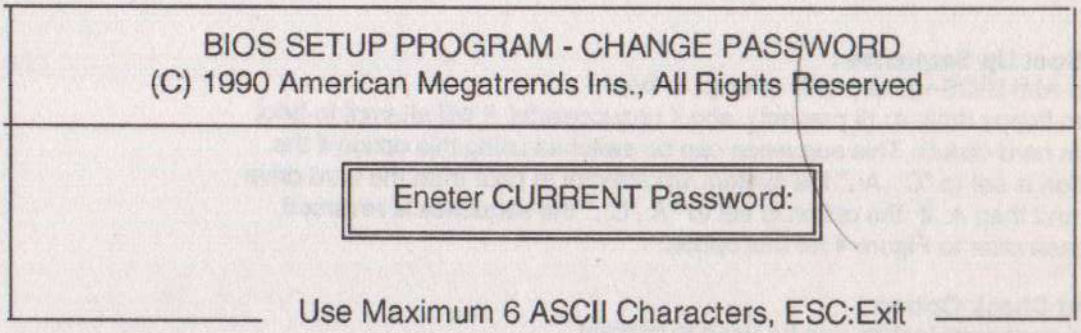
1.Normal : Gate A20 controlled by the 8042.
2.Fast gate A20 : Gate A20 controlled by programming the Bit o, 1 of I/O port 92h.
3.Chipset : This method is to emulate 8742 for fast gate A20 generation
4.Both : Both 2. and 3. method.

Video or Adaptor ROM Shadow :

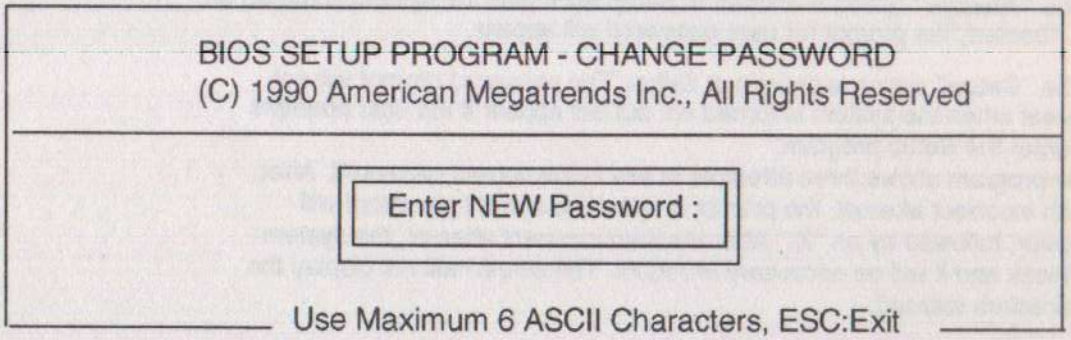
ROM shadow is a procedure in which BIOS code is copied from slower ROM to faster RAM. The BIOS is then executed from the RAM. These options are chip set specific and are dependent on the system hardware. They may or may not appear on the BIOS screen. Each option, when it does appear, allows for a segment of 16 KB to be shadowed from ROM to RAM. If one of these options is enabled , and BIOS will be shadowed.

System ROM shadow :

The same concept applies here as above, except that in this case, the system BIOS (64 KB in length) is shadowed.

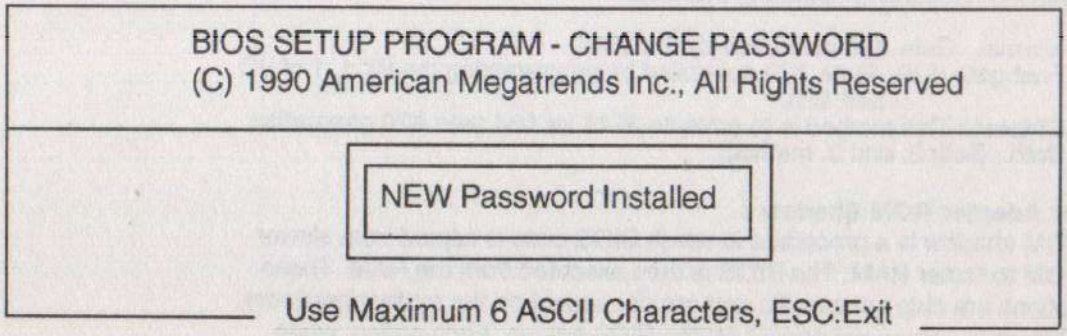


The first time you select this option, enter the default password AMI, or the default password specified in your system documentation, then press <Enter> to complete your selection. The screen will not display the characters entered. After the current password has been correctly entered, the screen in following Figure will appear, prompting you for the new password.



After the new password is entered, the prompt in above figure will appear. Rekey the new password and press <Enter>.

If the new password confirmation is entered without error, the screen in following.will appear. Perss <ESC> to return to the Main Setup menu.



Once Setup is completed and the changed values have been stored in the CMOS, when the system next boots. The user will be prompted for the password if the password function is present and has been enabled.

When and if the prompt appears is dependent upon the options chosen in Advanced CMOS Setup :

If the "Always" option was chosen in Advanced CMOS Setup. the prompt will appear each time the system is powered on.

If the "Setup" option was chosen in Advanced CMOS Setup, the prompt will not appear when the system is powered on, but will appear each time an attempt is made to enter the Setup program.

If the "Disabled" option was chosen in Advancde CMOS Setup, the password prompt will never appear.

When the password prompt appears, the new password, which is now stored in the CMOS, should be entered and the <Enter> key pressed. If the CMOS is corrupted,e.g., the batteries fall out or are loosened, the default ROM password mentioned above should be used instead.

NOTE: When the password is change, however, it is important that a record of the change be kept in a safe place. In the event the password check has been enabled in Setup and the user forgets or loses the new password, the default password stored in the ROM cannot be used unless the CMOS is disabled. A relatively safe way to do this would be to disconnect the CMOS batteries.

ADVANCED CHIPSET SETUP

BIOS SETUP PROGRAM AMI BIOS SETUP UTILITIES
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STANDARD CMOS SETUP
ADVANCED CMOS SETUP
ADVANCED CHIPSET SETUP
AUTO CONFIGURATION WITH BIOS DEFAULTS
AUTO CONFIGURATION WITH POWER-ON DEFAULTS
CHANGE PASSWORD
HARD DISK UTILITY
WRITE TO CMOS AND EXIT
DO NOT WRITE CMOS AND EXIT

Advanced CHIPSET Setup for Configuring the CHIPSET Registers

ESC:Exit Sel F2/F3:Color F10:Save & Exit

BIOS SETUP PROGRAM - ADVANCED CHIPSET SETUP
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Auto-Configuration	:Enabled	Co-processor Ready# Delay	:Enabled
AT Bus Clock	:CPUCLK/6	Check ELBA# Signal	:T2
Keyboard Clock selection	:7.2MHZ	Local Bus Ready Delay	:Enabled
I/O Recovery Time Delay	:4 BCLK		
Cache Read Hit Burst	:3-2-2-2		
Cache Write Hit Wait State	:2WS		
DRAM Page Mode	:Disabled		
DRAM Read WS Option	:3WS		
DRAM Write WS Option	:1WS		
Memory Remapping	:Enabled		
E0000 ROM Belongs to ATBUS	:No		
Memory Above 16 MB Cache Enabled	:Disabled		
Non-Cacheable Block1 Enable	:Disabled		
Non-Cacheable Block-1 Size	:1MB		
Non-Cacheable Block-1 Base	:0KB		
Non-Cacheable Block2 Enable	:Disabled		
Non-Cacheable Block-2 Size	:16MB		
Non-Cacheable Block-2 Base	:0KB		

Automatic Configuration: If this option is enable. The BIOS use the setup default values as follow: 1.Bus clock 2.Fast cache write hit 3.Fast cache read hit 4.Fast Page Mode DRAM 5.DRAM Wait State 6.DMA CAS Timing Delay.(Set on "Enable" for 50MHz and 45MHz)

AT Bus Clock: The AT BUS clock is divided from CPU clock between 2 and 6. (50MHz and 45MHz set on divided 6.)

Keyboard Clock Selection: This setting is for the keyboard clock.

I/O Recovery Time Delay: This setting can Extend the I/O command cycle to suit some I/O card.

Cache Read Hit Burst: This setting is for CPU reading policy.(For DX2 or P23T,Set in 2-1-1-1)

Cache Write Hit Wait State: This setting is for cache write hit wait state.(For DX2 or P23T, set in 1WS)

DRAM Page Mode: Fast or stand page mode DRAM.

DRAM Read WS Options: DRAM Read waite state.(For DX2 or P23T,set in 1WS)

DRAM Write WS Options: DRAM write wait state.(For DX2 or P23T,set in 0WS)

Memory Remapping: Normally main memory in the 384K region at he top of the first 1 Mega byte (000FFFFFH-000A0000H) will be lost because it is decoded as ROM region. If this region is not used for anything else (Shodow RAM or expanded memory), it can be remapped for extra memroy.
-Remapping 256Kbyte (A,B,D, and E segments) only and leaving C and F segments unchanged (normally used for shadow RAM)..
-Or remapping all 384Kbytes (A to F segments) for maximum extra memroy Note that remapped segments cannot be accessed by old address (for example logical address 000A0000H does not exist any longer if A segment is remapped).

E0000 ROM Belongs to ATBUS: No,E0000 ROM belonge to system board.
Yes,E0000 ROM belongs to ATBUS.

Memory above 16MB Cacheable: This option is to set memory above 16MB is cachable.

Non-Cacheable Block Enabled: defined by user.

Non-Cacheable Size: defined by user.

Non-Cacheable Base: defined by user.

Co-processor Ready# Delay: Delay the math coprocessor ready signal by 1 T-cycle.

Check ELBA# pin: This option is to check local bus device at T1 or T2 cycle. (T1 has better performance,but the interface card must be suitted.)

Local Bus Ready# Delay: Delay the local bus ready signal.