HIPPO II
486

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REVISION: 1.0

RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

* *Reorient the receiving antenna.*
* *Relocate the computer away from the receiver.*
* *Move the computer away from the receiver.*
* *Plug the computer into a different outlet so that computer and receiver are on different branch circuits.*
* *Ensure that card slot covers are in place when no card is installed.*
* *Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.*
* *If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.*

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

Note

1. Electronic components are sensitive to dust and dirt. Do inspect and clean the computer system regularly.

2. Turn off the power whenever you install or remove any connector, memory module and add-on card. Before turning on the power, make sure that all the connectors, memory modules and add-on cards are secured.

3. After power is on, wait for a minute. The system BIOS are going through a self-test during this period and nothing is shown on the screen. After the self-test, the system BIOS will initialize the display adaptor and show messages.

4. The SIMM sockets are fragile device. Do not force the SIMM modules into the sockets. It may break the locking latches.

Preface

The manual provides information about the installation and maintenance of OCTEK HIPPO II motherboard. In-depth explanations of the functions of this motherboard are provided. In the appendix, the system BIOS setup is explained.

The content in this manual is only for reference and is intended to provide the basic information for the general users. There are also technical information for hardware and software engineers.

In this manual, there are 4 chapters. Chapter 1 contains a brief introduction and specification of OCTEK HIPPO II motherboard. In the Chapter 2, the functions of HIPPO II are explained. It also outlines many advanced features of the CPU and the system architecture. Chapter 3 explains the installation of coprocessor, DRAM modules and jumpers. Technical information is provided in the Chapter 4.

System BIOS and the system setup are described in the appendix A. All setup procedures are explained. Appendix B contains the information about the memory expansion board. The optional secondary cache memory card is described in appendix C. Additional information is given in the Appendix D, E, F, G and H for maintenance purpose.

Table of Content

Chapter 1
Introduction

OCTEK HIPPO II is designed to be a powerful platform for sophisticated software available now and in the future. It contains the most powerful microprocessor 80486 which combines CPU, numeric coprocessor and internal cache memory on a single chip. Incorporated with a highly integrated chipset which consists of an advanced cache controller, OCTEK HIPPO II fully takes advantage of the power of 80486 and provides high performance, reliability and compatibility to the user.

OCTEK HIPPO II supports a large secondary cache memory with a write-back cache controller. Cache size can be 64KB or 256KB. Access to the cache memory can be carried out in the 80486 unique burst mode. Therefore HIPPO II is a perfect choice for CAD/CAM application, file server and other advanced 32-bit computing applications and operating systems. Improved design makes the memory controller more efficient. On board memory can be added up to 32MB.

Fast A20 gate and fast reset generation are incorporated to improve the performance of advanced operation system and expanded memory managers.

Compatibility and reliability are important issues. I/O channel is compatible to standard AT bus and any peripheral may be used. On board POWERGOOD generator is essential to ensure the reliability of the system and is well-designed to work with all power supplies.

Chapter 2
General Features

SPECIFICATION

Processor :

Intel 80486 CPU
with optional WEITEK 4167 Co-processor

Speed :

Turbo/normal speed

I/O Slot :

Compatible to standard AT bus
Eight 16-bit slots

Secondary Cache Memory :

64KB or 256KB Direct mapped
Write-back cache memory

GENERAL FEATURES

Memory :

Shadow RAM for system and video BIOS
Page mode and hidden refresh
Flexible configuration
SIMM sockets for 1MB or 4MB modules
Maximun 32MB on board

System Support Functions :

- *8-Channel DMA (Direct Memory Access)*
- *16-level interrupt*
- *3 programmable timers*
- *CMOS RAM for system configuration*
- *Real time clock with battery back-up*
- *Fast A20 gate and fast reset*

Other Features :

- *On board POWERGOOD generation*
- *External battery connector*

PROCESSOR

The power of HIPPO II comes from 80486. 80486 is the state-of-art microprocessor which merges many innovative features on a single chip for advanced applications and operation systems. Fabricating with the 1um process, this CPU consists of more than one million transistors. With such high density, this CPU incorporates as many as new features to make itself the most powerful microprocessor.

80486 is a 32-bit microprocessor with 32-bit external data bus and 32-bit external address bus. It not only contain a central processing unit, but also integates a numeric processor and a four-way set associate cache memory. It is fully binary compatible with 80386 and 80387. All existing software for PC XT/AT can be used on OCTEK HIPPO II. However, due to the new internal architecture, the performance of 80486 is two to four times of 80386.

Cache memory can improve the overall performance of a computer system. Nevertheless, if the cache memory is separated from CPU, CPU still needs to fetch code and data through external bus. That means the data transfer rate should not be too fast so that the external devices are able to keep pace with the CPU. In 80486, the cache controller and cache memory are integrated into the chip. Most of the operations can be carried out inside the CPU, which reduces the bus operations on external data and address bus and thus speeds up the internal execution.

The cache memory is a 8K bytes, 16 bytes line size, four-way set associative configuration. The hit rate of this configuration is much better than 32K bytes two-way set associative external cache because a four-way set associative architecture provides better performance in a multitasking and multi-processor environment.

Bus snooping feature keeps the cache memory consistent with the main memory. When an external processor overwrites the content in the main memory, the corresponding data in the internal cache memory will be invalidated and will be fetched from main memory when CPU reads this data.

If a read miss occurs, the CPU will initiate a burst mode read operation. In burst mode read operation, CPU performs four successive read operations each of which takes only one cycle. Total 128 bits data are fetched into the CPU's internal cache. Since burst mode read operation is very fast, the traffic of the CPU bus is greatly reduced and the bus is available to other bus masters, such as DMA controller.

Reading 128 bits data into CPU will take some times. In order to reduce the delay, the internal cache controller works parallel with CPU. It fetches the data needed by CPU for the present operation and the CPU read cycle is terminated. Then the other data are read into the internal cache memory while CPU is doing something else. This arrangement permits the CPU to run at zero wait state.

By eliminating the access to external bus, operations with the internal cache can be completed in a single cycle. 80386 at least needs two cycles for an operation. To further increase the rate of data transfer inside the CPU, the internal bus of the cache memory is increased to 128 bits, which is four times of the external bus. Since, in most of the time, the CPU is using the internal cache, the large bus size substantially improves the overall performance.

When the CPU writes data to the main memory, the data is first stored in a write buffer. There are four write buffers. When the external bus is idle, data will be sent to the main memory. If all buffers are filled, it can start write operation in burst mode. Since the internal cache is updated immediately, the CPU need not suspend its operation and there is no need to wait for the external device to update the main memory.

Many often-used instructions are executed in a clock cycle and some instructions are modified to take fewer cycles than in 80386. On the contrary, 80386 may take two to three more cycles for the same instruction. The CPU contains an advanced instruction pipeline structure and a 32-byte code queue to speed up the execution.

80486 includes all the functions of 80386 and is able to support sophisticated software and operation systems which are widely employed now. It is able to operate in real mode, protected mode and virtual 8086 mode.

Internal memory management unit provides a flexible addressing scheme for the next generation operation system. Multitasking, concurrent operation and manipulating huge data base can be accomplished with excellent performance. Paging mechanism is employed to allow powerful operating system to implement virtual memory. Each segment is divided into several pages which are 4K bytes per page. Page mechanism is transparent to software and allows software to address 64 terabytes. Furthermore, the 64KB segment boundary which is an barrier of 8088 and 80286 is removed and the segment length can be increased up to 4GB.

The demand for sophisticated, number-crunching scientific and business applications has rapidly increased in recent years. In the past, microprocessor features an integer Arithmetic Logic Unit which only handles simple integer operations such as addition and multiplication. Floating-point operations which are actually utilized by applications must be accomplished through software routines.

To meet the demand of floating-point calculation, a numeric coprocessor is necessary. However, an external coprocessor has been found to be the bottleneck of data transfer. 80486 integrates the coprocessor on chip and thus the data transfer to external bus is eliminated. The on-chip coprocessor is compatible with 80387. It works parallel with other units in the CPU, which results in a better performance of numeric process.

SECONDARY CACHE MEMORY

Although there is 8K bytes internal cache memory inside the CPU, a secondary cache memory is still necessary under some circumstances, such as when running multi-user or multitasking opration systems, or installing several devices with bus master capibility.

In a single user system, when only DOS is used and few megabytes memory is installed, the internal cache memory is adequate and the performance is still very high.

In a multi-user or multitasking environment, CPU has to switch from one process to another, which involves a large mount of data transfer. The performance to a great extent depends on the data transfer rate. In a 80486 system, a large portion of the internal cache memory has to be updated to the main memory and then the data for another process is retrieved into the cache memory. The low speed main memory will substantially slow down the system.

In order to shorten the time required for switching between processes, a secondary cache memory is needed as a buffer between the slow speed main memory and the internal cache memory of 80486. Wait state is thus eliminated when the CPU reads external data from the secondary cache memory. Furthermore, the secondary cache memory can support the burst mode of 80486. The CPU is able to run at full speed.

Since there is already a 8K bytes cache memory in 80486, a small cache memory, such as 32K bytes, can not substantially improved the performance. On the other hand, the secondary cache should be able to contain a copy of the internal cache memory or more, which means data of different processes can coexist in the secondary cache memory. So, an optimal size is 128K or 256K bytes and this size is adequate for over 8M bytes main memory.

The secondary cache also helps to reduce the main memory bus utilization. In a system with several devices using bus master for data transfer, the main memory bus will be very bus but all the devices have to share a single mamoey bus. So, the less the CPU accesses the main memory, the more the extenal devices is able to use the memory bus.

In HIPPO II, the secondary cache controller is incorporated in the chipset. There is no need to install an external cache controller. A write-back direct-mapped scheme is implemented in HIPPO II. In a direct-mapped cache memory, the cache memory is treated as a buffer for the main memory. The main memory is logically divided into pages which has the size equal to the cache memory size. Each location in the cache memory is directly mapped into the same location in each page of main memory.

Advanced features are incorporated to further improve the overall performance and to support sophisticated 32-bit softwsare. Firstly, the cache controller is able to work in the unique 80486 burst read mode, which results in true zero wait state operation at high speed.

The write policy of the HIPPO II cache controller is write-back. In a cache-based system, the performance is downgraded when there is a lot
of write operations because the CPU has to update both cache memory and main memory simultane-ously. In many cache designs, the write operation is buffered,

which is called 'post-write'. But it can only buffer a single write operation and wait state is still needed in case of multiple write operations. In 80486 system, since there is already a 8KB cache inside, the external bus operation will be mostly write operation.

In a write-back cache system, the amount of write operations to main memory is minimized. The CPU writes the data to the cache memory if the data on the same location is already in the cache memory. The main memory is not updated yet and the operation completes in a single cycle. So, it implies that writing to the same location need not initiate a main memory write operation. The main memory is only needed to be updated when the data from main memory has to replace the same location in the cache memory.

The advantage of the write-back scheme is that the main memory bus utilization is substantially reduced and hence the main memory bus can be available to other bus master devices in the system. It is very important for high-end computer systems in which several devices have to access the main memory for data transfer.

Two non-cacheable address ranges can be speicfied. It allows you to protect some partitions of program or the BIOS on the add-on cards. The video BIOS may be individually selected to be cacheable or not. The setup of the non-cachebale address ranges can be easily done in the BIOS setup.

MEMORY SYSTEM

Two banks of DRAMs can be installed on board. 1MB and 4MB DRAM SIMM modules are supported. The DRAM should be fast-page mode DRAM with CAS#-before-RAS# refresh capability.

The memory system provides a flexible memory configuration. Both 1MB and 4MB DRAM can be used together. Several combinations of DRAM types are allowed. The DRAM type and the memory size is automatically detected by the system BIOS. So, you may easily change the configuration of the system.

The memory system supports page mode. The memory is divided into pages. Successive memory accesses within the same page need not require wait state. Furhtermore, a burst line fill mode is implemented. In case of a read miss of cache memory, 16 bytes data will be fetched from main memory to cache memory. Using page mode operation will speed up the line fill operation. To enhance the system performance, shadow RAM mode is supported. In shadow RAM mode, system BIOS and video BIOS contained in low speed memory such as EPROM and ROM are copied into DRAM. Improvement is significant because access to DRAM is mush faster than ROM.

The memory refresh logic is redesigned to improve the system performance and power consumption. In the original PC/AT design, the memory refresh operation will suspend the CPU operation because it has to access the main memory. In a high speed system like HIPPO II, the CPU indeed can process a large amount of operations in the memory refresh period.

By implementing hidden refresh method, the refresh operations for expansion card on the AT bus and for the main memory are separated. To be compatible, the refresh operation for AT bus will not be changed. But the refresh operation for main memory will be carried

out individually and will be done when there is no access to main memory. Furhtermore, the frequency of the main memory refresh operation may be set to 'normal' or 'slow'. All types of DRAM can be used in `normal' mode. When 'slow' mode is selected, the availability of main memory is increased but the refresh period of DRAM should be longer. Since the refresh period of DRAM from different manufacturers may vary, consult your dealer for detail.

8042 EMULATION

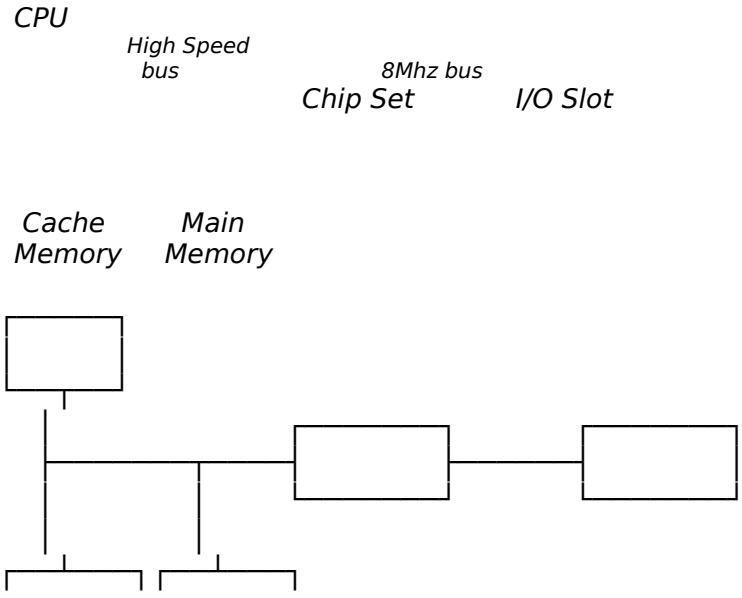
Now, there are many PC designs with a special feature for OS/2 optimization. It is intended to speed up the protected mode switching operation which is done by the slow speed keyboard controller in the original PC design. However, this feature often causes compatibility problem because they use different hardware logic design to bypass the keyboard controller. Thus, the BIOS is needed to be modified to take advantage of it. An application without modification may cause problem.

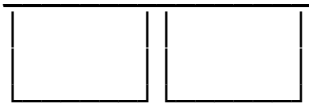
In HIPPO II, there are some logic designs in the chipset to emulate the keyboard conntoller. An application can work in the usual way to send commands to keyboard controller, but these commands are in fact interpreted by the chipset. The protected mode switching operation is much faster. There will be no potential problem since modification of software is not needed.

DUAL BUS DESIGN

It is very important that a high speed system should be compatible with existing peripherals without lowering the performance. To be compatible, the I/O slot should run at 8MHz or slower. On the other hand, the rest of the system are running at full speed.

In HIPPO II, a dual bus design is employed. A high speed bus links the CPU, coprocessor, cache memory and main memory. This bus is synchronous with clock of the CPU and the data transfer is 32 bits. Whenever there is a request for transferring data to or from I/O slot, the chipset is responsible for handling the conversion between the bus. The clock rate of the high speed bus will not be reduced, which eliminates many compatibility problem.





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Chapter 3
Configuring The System

Important Note : Turn off the power before installing or replacing any component.

INSTALLING MATH COPROCESSOR

Math coprocessor WEITEK 4167 is a PGA devices. Beside the CPU, there is a 144-pin PGA socket. To install Math Coprocessor, be sure to line up pin 1 of the Math coprocessor with pin 1 of the socket as shown below.

Before installing the Math coprocessor, make sure that all the pins are straight. The pins are very fragile. Once these pins are bent, the coprocessor may be damaged.

The Math coprocessor is automatically detected by the system and the applications. No jumper is needed to be set.

CONFIGURATION OF CACHE MEMORY

Note : if you have any question about the configuration of the cache memory, consult your local dealer. Improper configuration will cause the system malfuction.

The external cahce memory is either 64KB or 256KB. Eight pieces of SRAM should be installed on U47 to U55. JP8, JP9 and JP11 are used for setting up the cache memory. Place mini-jumpers on all of them for 256KB cache memory. No mini jumper is needed for 64KB cache memory.

Cache Size	*JP8*	*JP9*	*JP11*
64KB	*OPEN*	*OPEN*	*OPEN*
256KB	*CLOSE*	*CLOSE*	*CLOSE*

I/O Speed Control

JP3 is used to select the I/O speed.

JP3	*OPEN*	*CLOSE*
I/O Speed	*8MHz*	*6MHz*

Most add-on cards should work at 8MHz I/O Speed. If you have a slow add-on card which fails at 8MHz, changes to 6MHz.

INSTALLING RAM MODULES

OCTEK HIPPO II has eight sockets for SIMM modules. Whenever you add memory to the motherboard, install four modules at the same time. Also make sure that the chips on the modules face towards CPU. The modules should be locked by the sockets. Please check carefully before turning on the power. Otherwise, the system will not work properly.

To install a module, the module edge is angled into the socket's contact and then the module is pivoted into position, where the locking latches will secure it. If the module edge is not completely inserted into the socket, it cannot be pivoted to be in vertical position and should be dragged out and re-inserted again. Do not force the module into the SIMM socket. It will damage the locking latches.

The modules should be locked by the locking latches of the sockets firmly. Please check carefully before turning on the power. Otherwise, the system will not work properly.

If the BIOS reports an memory error or parity error, drag out the modules and insert them again. If the locking latches are damaged, contact your dealer to replace the socket.

CONFIGURATION OF MEMORY

The configuration of the memory is very flexible. There are several combinations of DRAM types you may consider. Either 1MB or 4MB SIMM are acceptable. So, a basic system can be equipped with fewer memory and later more memory can be installed when upgrading the system. There are totally two banks of DRAM on the motherboard. The memory size is detected automatically by system BIOS and indicated during memory test after reset. No jumper is needed to be set for the memory size and DRAM type.

To determine what DRAM speed rating should be used depends on the system speed and wait state. The highest performance is accomplished by using zero wait state, but high speed DRAM has to be used. If zero wait state is selected, fast page mode DRAM is needed.

The wait state setting is applied to all banks of memory. Therefore make sure to install DRAM with the same speed rating, or accom-modate the wait state setting to the slow DRAM type.

Because of the shadow RAM fuction, the 386KB memory between 640KB to 1MB can not accessed. So, the memory size found by the system BIOS is not equal to the actual memory size. For example, when there is 4MB on board, the BIOS will show 3712KB.

DRAM CONFIGURATION

	Bank 0	*Bank 1*	*Total Memory*
1	*1M*	*--*	*4M*
2	*1M*	*1M*	*8M*
3	*1M*	*4M*	*20M*
4	*4M*	*1M*	*20M*
5	*4M*	*--*	*16M*
6	*4M*	*4M*	*32M*

CONTROL OF SYSTEM SPEED

System speed can be controlled by keyboard. To change the speed by keyboard, use **`-'** *and* **`+'** *of the numeric keypad. Press* **`Ctrl' `Alt'** *and* **`-'** *for slow speed and press* **`Ctrl' `Alt'** *and* **`+'** *for fast speed.*

The turbo LED connector is plugged into JP12.

RESET CMOS SETUP INFORMATION

Sometimes, the improper setting of system setup may make the system malfunction. In this case, turn off the power and set JP2 to 1-2 for a while. The internal CMOS status register is reset. Then set the jumper to 2-3 and turn on the power. The BIOS finds the CMOS status register is reset and regards the setup information is invalid. so it will prompt you to correct the information.

If you just want the BIOS to discard the register settings, you select the XCMOS SETUP, press `INS' on the keyboard for a few seconds after power up. The BIOS will detect the key stroke and use the default setting for booting.

SYSTEM BOARD JUMPER SETTING

There are several options which allows user to select by hardware switches.

Display Selection

JP1	
ON	*CGA, EGA, VGA*
OFF	*Monochrome display **

*Note : * factory setting*
JP4,JP5,JP6, JP7 and JP10 are reserved jumpers.

SYSTEM BOARD CONNECTORS

Under typical conditions, these connectors should be connected to the indicators and switches of the system unit. The functions of connectors on the motherboard (version 1.0) are listed below.

Connector	*Function*
SW1	*Hardware reset connector*
J24	*Speaker connector*
J23	*Power LED & Ext-lock connector*
J11, J12	*Power supply connector*
J10	*External battery connector*
J1	*Keyboard connector*

Pin assignment of the connector are illustrated as follows:

SW 1 - Hardware Reset Connector

Pin	*Assignment*
1	*Selection Pin*
2	*Ground*

J 10 - External Battery Connector

Pin	*Assignment*
1	*+ Vdc*
2	*not used*
3	*Ground*
4	*Ground*

J 1 - Keyboard Connector

Pin	*Assignment*
1	*Keyboard clock*
2	*Keyboard data*
3	*Spare*
4	*Ground*
5	*+5 Vdc*

J 24 - Speaker Connector

Pin	*Assignment*
1	*Data out*
2	*+5 Vdc*
3	*Ground*
4	*+5 Vdc*

J 23 - Power LED & Ext-Lock Connector

Pin	*Assignment*
1	*+5 Vdc*
2	*Key*
3	*Ground*
4	*Keyboard inhibit*
5	*Ground*

J 11, J 12 - Power Supply Connector

Pin	*Assignment*
1	*POWERGOOD*
2	*+5 Vdc*
3	*+12 Vdc*
4	*-12 Vdc*
5	*Ground*
6	*Ground*

Pin	*Assignment*
1	*Ground*
2	*Ground*
3	*-5 Vdc*
4	*+5 Vdc*
5	*+5 Vdc*

6	*+5 Vdc*

Chapter 4
Technical Information

This section provides technical information about OCTEK HIPPO II and is intended for advanced users interested in the basic design and operation of OCTEK HIPPO II.

MEMORY MAPPING

Address	*Range*	*Function*
000000-7FFFFF	*000K-512K*	*System Board Memory (512K)*
080000-09FFFF	*512K-640K*	*System Board Memory (128K)*
0A0000-0BFFFF	*640K-768K*	*Display Buffer (128K)*
0C0000-0DFFFF	*768K-896K*	*Adaptor ROM / Shadow RAM (128K)*
0E0000-0EFFFF	*896K-960K*	*System ROM / Shadow RAM (64K)*
0F0000-0FFFFF	*960K-1024K*	*System BIOS ROM / Shadow RAM (64K)*
100000-7FFFFF	*1024K-8192K*	*System Memory*
800000-FFFFFF	*8192K-16318K*	*System Memory*

I/O ADDRESS MAP

I/O Address Map on System Board

I/O address hex 000 to 0FF are reserved for the system board I/O.

ADDRESS (HEX)	*DEVICE*
000-01F	*DMA Controller 1, 8237*
020-03F	*Interrupt Controller 1, 8259, Master*
040-05F	*Timer, 8254*
060-06F	*Keyboard Controller*
070-07F	*Real Time Clock, NMI (non-maskable interrupt) mask*
080-09F	*DMA Page Register, 74LS612*
0A0-0BF	*Interrupt Controller 2, 8259*
0C0-0DF	*DMA Controller 2, 8237*
0F0	*Clear Math Coprocessor Busy*
0F1	*Reset Math Coprocessor*
0F8-0FF	*Math Coprocessor Port*

I/O address hex 100 to 3FF are available on the I/O channel.

ADDRESS (HEX)	*DEVICE*
1F0-1F8	*Fixed Disk*
200-207	*Game I/O*
278-27F	*Parallel Printer Port 2*
2F8-2FF	*Serial Port 2*
300-31F	*Prototype Card*
360-36F	*Reserved*
378-37F	*Parallel Printer Port 1*
380-38F	*SDLC, bisynchronous 2*
3A0-3AF	*Bisynchronous 1*
3B0-3BF	*Monochrome Display and Printer Adapter*
3C0-3CF	*Reserved*
3D0-3DF	*Color Graphics Monitor Adapter*
3F0-3F7	*Diskette Controller*
3F8-3FF	*Serial Port 1*

SYSTEM TIMERS

OCTEK HIPPO II has three programmable timer/counters controlled by 82C206 and they are defined as channels 0 through 2:

Channel 0	*System Timer*
Gate 0	*Tied on*
Clk in 0	*1.190 Mhz OSC*
Clk out 0	*8259 IRQ 0*

Channel 1	*Refresh Request Generator*
Gate 1	*Tied on*
Clk in 1	*1.190 Mhz OSC*
Clk out 1	*Request Refresh Cycle*

Channel 2	*Tone Generation of Speaker*
Gate 2	*Controlled by bit 0 of port hex 61 PPI bit*
Clk in 2	*1.190 Mhz OSC*
Clk out 2	*Used to drive the speaker*

Note : Channel 1 is programmed to generate a 15-micro-second period signal.

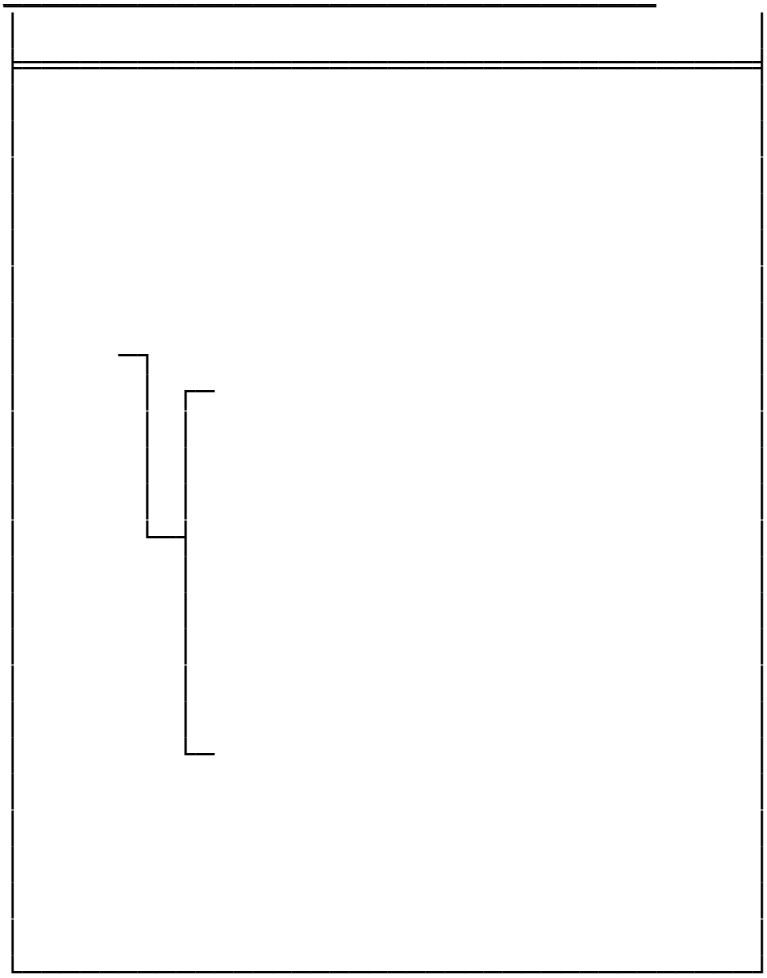
The 8254 Timer/Counters are treated by system programs as an arrangement of four programmable external I/O ports. Three are treated as counters and the fourth is a control register for mode programming.

SYSTEM INTERRUPTS

Sixteen levels of system interrupts are provided on OCTEK HIPPO II. The following shows the interrupt-level assignments in decreasing priority.

Level		Function
Microprocessor NMI		*Parity or I/O Channel Check*
Interrupt Controllers		
CTLR 1	*CTLR 2*	
IRQ0		*Timer Output 0*
IRQ1		*Keyboard (Output Buffer Full)*
IRQ2		*Interrupt from CTLR 2*
	IRQ8	*Real-time Clock Interrupt*
	IRQ9	*Software Redirected to INT 0AH (IRQ2)*
	IRQ10	*Reserved*
	IRQ11	*Reserved*
	IRQ12	*Reserved*
	IRQ13	*Coprocessor*
	IRQ14	*Fixed Disk Controller*
	IRQ15	*Reserved*
IRQ3		*Serial Port 2*
IRQ4		*Serial Port 1*
IRQ5		*Parallel Port 2*
IRQ6		*Diskette Controller*
IRQ7		*Parallel Port 1*

TECHNICAL INFORMATION



DIRECT MEMORY ACCESS (DMA)

OCTEK HIPPO II supports seven DMA channels.

Channel	*Function*
0	*Spare (8 bit transfer)*
1	*SDLC (8 bit transfer)*
2	*Floppy Disk (8 bit transfer)*
3	*Spare (8 bit transfer)*
4	*Cascade for DMA Controller 1*
5	*Spare (16 bit transfer)*
6	*Spare (16 bit transfer)*
7	*Spare (16 bit transfer)*

The following shows the addresses for the page register.

Page Register	*I/O Address (HEX)*
DMA Channel 0	*0087*
DMA Channel 1	*0083*
DMA Channel 2	*0081*
DMA Channel 3	*0082*
DMA Channel 5	*008B*
DMA Channel 6	*0089*
DMA Channel 7	*008A*
Refresh	*008F*

REAL TIME CLOCK AND CMOS RAM

Real time clock and CMOS RAM are contained on board. Real time clock provides the system date and time. CMOS RAM stores system information. Both are backed up by battery and will not lose information after power off. The following page shows the CMOS RAM Address Map.

CMOS RAM ADDRESS MAP

Addresses	*Description*
00-0D	** Real-time clock information*
0E	** Diagnostic status byte*
0F	** Shutdown status byte*
10	*Diskette drive type byte - drives A and B*
11	*Reserved*
12	*Fixed disk type byte - drives C and D*
13	*Reserved*
14	*Equipment byte*
15	*Low base memory byte*
16	*High base memory byte*
17	*Low expansion memory byte*
18	*High expansion memory byte*
19-2D	*Reserved*
2E-2F	*2-byte CMOS checksum*
30	** Low expansion memory byte*
31	** High expansion memory byte*
32	** Date century byte*
33	** Information flags (set during power on)*
34-3F	*Reserved*

REAL TIME CLOCK INFORMATION

The following table describes real-time clock bytes and specifies their addresses.

Byte	*Function*	*Address*
0	*Seconds*	*00*
1	*Second alarm*	*01*
2	*Minutes*	*02*
3	*Minute alarm*	*03*
4	*Hours*	*04*
5	*Hour alarm*	*05*
6	*Day of week*	*06*
7	*Date of month*	*07*
8	*Month*	*08*
9	*Year*	*09*
10	*Status Register A*	*0A*
11	*Status Register B*	*0B*
12	*Status Register C*	*0C*
13	*Status Register D*	*0D*

SYSTEM EXPANSION BUS

OCTEK HIPPO II provides eight 16-bit slots.

The I/O channel supports:

* *I/O address space from hex 100 to hex 3FF*
* *Selection of data access (either 8 or 16 bit)*
* *24 bit memory addresses (16MB)*
* *Interrupts*
* *DMA channels*
* *Memory refresh signal*

The following figure shows the pin numbering for I/O channel connectors (A-side and B-side).

The following figure shows the pin numbering for I/O channel connectors (C-side and D-side).

The following tables summarize pin assignments for the I/O channel connectors.

I/O Channel (A-Side)

I/O Pin	*Signal Name*	*I/O*
A1	*-I/O CH CK*	*I*
A2	*SD7*	*I/O*
A3	*SD6*	*I/O*
A4	*SD5*	*I/O*
A5	*SD4*	*I/O*
A6	*SD3*	*I/O*
A7	*SD2*	*I/O*
A8	*SD1*	*I/O*
A9	*SD0*	*I/O*
A10	*-I/O CH RDY*	*I*
A11	*AEN*	*O*
A12	*SA19*	*I/O*
A13	*SA18*	*I/O*
A14	*SA17*	*I/O*
A15	*SA16*	*I/O*
A16	*SA15*	*I/O*
A17	*SA14*	*I/O*
A18	*SA13*	*I/O*
A19	*SA12*	*I/O*
A20	*SA11*	*I/O*
A21	*SA10*	*I/O*
A22	*SA9*	*I/O*

A23	*SA8*	*I/O*
A24	*SA7*	*I/O*
A25	*SA6*	*I/O*
A26	*SA5*	*I/O*
A27	*SA4*	*I/O*
A28	*SA3*	*I/O*
A29	*SA2*	*I/O*
A30	*SA1*	*I/O*
A31	*SA0*	*I/O*

I/O Channel (B-Side)

I/O Pin	*Signal Name*	*I/O*
B1	*GND*	*Ground*
B2	*RESET DRV*	*I*
B3	*+5 Vdc*	*Power*
B4	*IRQ9*	*I*
B5	*-5 Vdc*	*Power*
B6	*DRQ2*	*I*
B7	*-12 Vdc*	*Power*
B8	*0WS*	*I*
B9	*+12 Vdc*	*Power*
B10	*GND*	*Ground*
B11	*-SMEMW*	*O*
B12	*-SMEMR*	*O*
B13	*-IOW*	*I/O*
B14	*-IOR*	*I/O*
B15	*-DACK3*	*I*
B16	*DRQ3*	*O*
B17	*-DACK1*	*I*
B18	*DRQ1*	*O*
B19	*-Refresh*	*I/O*
B20	*CLK*	*O*
B21	*IRQ7*	*I*
B22	*IRQ6*	*I*
B23	*IRQ5*	*I*
B24	*IRQ4*	*I*

B25	*IRQ3*	*I*
B26	*-DACK2*	*O*
B27	*T/C*	*O*
B28	*BALE*	*O*
B29	*+5 Vdc*	*Power*
B30	*OSC*	*O*
B31	*GND*	*Ground*

I/O Channel (C-Side)

I/O Pin	*Signal Name*	*I/O*
C1	*SBHE*	*I/O*
C2	*LA23*	*I/O*
C3	*LA22*	*I/O*
C4	*LA21*	*I/O*
C5	*LA20*	*I/O*
C6	*LA19*	*I/O*
C7	*LA18*	*I/O*
C8	*LA17*	*I/O*
C9	*-MEMR*	*I/O*
C10	*-MEMW*	*I/O*
C11	*SD8*	*I/O*
C12	*SD9*	*I/O*
C13	*SD10*	*I/O*
C14	*SD11*	*I/O*
C15	*SD12*	*I/O*
C16	*SD13*	*I/O*
C17	*SD14*	*I/O*
C18	*SD15*	*I/O*

I/O Channel (D-Side)

I/O Pin	*Signal Name*	*I/O*
D1	*-MEM CS16*	*I*
D2	*-I/O CS16*	*I*
D3	*IRQ10*	*I*
D4	*IRQ11*	*I*
D5	*IRQ12*	*I*
D6	*IRQ15*	*I*
D7	*IRQ14*	*I*
D8	*-DACK0*	*O*
D9	*DRQ0*	*I*
D10	*-DACK5*	*O*
D11	*DRQ5*	*I*
D12	*-DACK6*	*O*
D13	*DRQ6*	*I*
D14	*-DACK7*	*O*
D15	*DRQ7*	*I*
D16	*+5 Vdc*	*Power*
D17	*-MASTER*	*I*
D18	*GND*	*Ground*

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Appendix A
System BIOS

The system BIOS in HIPPO II provides an interface for operating systems and applications to access the hardware. It is fully compatible with standard AT BIOS and works flawlessly in the network system. It also performs self-test after reset and includes a setup program to setup the system.

SELF-TEST

To ensure that the computer hardware is functional, the system BIOS will carry out a self-test upon reset. The test is very intensive and covers all parts of hardware. It takes a while before some messages are shown on the screen. It does not mean that the system is not working when the screen is blank. So wait for a while after turning on the power and listen carefully to the speaker. Some errors are reported by a number of beep sounds. After completing the self-test, the BIOS will display some messages on the screen.

In case of serious errors, the BIOS will suspend the test. If the display is not initialized, the BIOS will report the error through a sequence of beep sounds. Otherwise, error message will be shown on the screen.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list below correspond to the number of beeps for the corresponding error. All errors listed, with the exception of #8, are fatal errors.

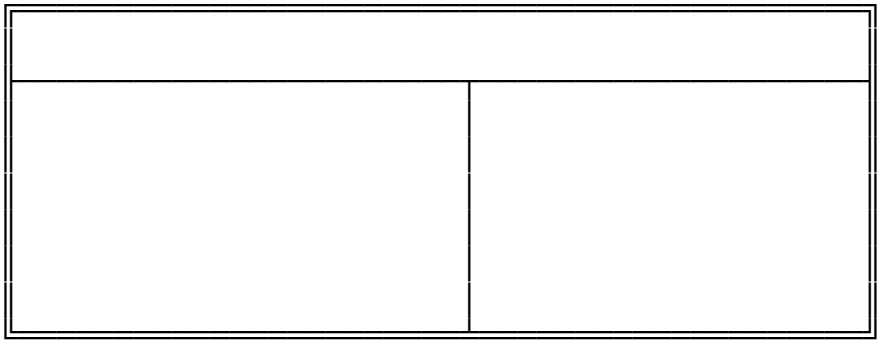
No. of Beeps	*Error Message*
1	*DRAM Refresh Failure*
2	*Base 64KB Memory Parity Error*
3	*Base 64KB Memory Failure*
4	*System Time Failure*
5	*Processor Error*
6	*Keyboard Controller Gate A20 Failure*
7	*Processor Exception Interrupt Error*
8	*Display Memory Read / Write Error (Video Adapter)*
9	*ROM Checksum Error*
10	*CMOS Shutdown Register Read/Write Error*

If no error is found during self-test, the system BIOS will proceed to boot from floppy disk or hard disk. The system BIOS will list the system configuration on the screen shown in next page.

SYSTEM BIOS

System Configuration (C) Copyright 1985-1990, American Megatrends Inc.,

Main Processor	*:*	*80486*	*Base Memory Size*	*:*	*640 KB*
Numeric Processor	*:*	*Present*	*Ext. Memory Size*	*:*	*3072 KB*
Floppy Drive A:	*:*	*1.2 MB, 5¼"*	*Hard Disk C: Type*	*:*	*2*
Floppy Drive B:	*:*	*1.44MB, 3½"*	*Hard Disk D: Type*	*:*	*None*
Display Type	*:*	*VGA or EGA*	*Serial Port(s)*	*:*	*None*
ROM-BIOS Date	*:*	*04/15/91*	*Parallel Port(s)*	*:*	*3BC*



Do check the list to make sure that the configuration is correct. Sometimes, problems arise because of the incorrect information of the configuration. For example, if you forget to modify the setup after changing the floppy disk drive from one type to another, it can not boot from floppy disk or may not work properly. If you check the list, you can find the cause of the problem.

SYSTEM SETUP

The BIOS incorporates four setup sections:

(1) Standard CMOS Setup
(2) Advanced CMOS Setup
(3) Auto Configuration with BIOS Defaults
(4) Hard Disk Utilities

It is important that all the setup procedures should be completed before operating the system. Otherwise, the system may not run properly with the incorrect setup information. Run the setup again if the configuration is changed.

To enter the setup section, press 'DEL' when the following message is shown during memory test :

Hit <DEL> if you want to run SETUP

Whenever the system BIOS finds that the configuration of the system is altered, a message will be shown and you may press 'F1' to run setup. Then the following messages are shown on the screen.

BIOS SETUP PROGRAM - AMI BIOS SETUP UTILITIES
<C> 1990 American Megatrends, Inc. All Rights Reserved
STANDARD CMOS SETUP
ADVANCED CMOS SETUP
AUTO CONFIGURATION WITH BIOS DEFAULTS
HARD DISK UTILITY
WRITE TO CMOS AND EXIT
DO NOT WRITE TO CMOS AND EXIT
Configure system with Power On Default Values for Chipset and Advanced CMOS

(1) CMOS SETUP

The memory size and the numeric processor are detected by the BIOS. So you are only required to set those options on the left side of the screen. The system configuration information are shown as follows:

BIOS SETUP PROGRAM - STANDARD CMOS SETUP
(C) 1990 American Megatrends Inc., All Rights Reserved

Date (mn/date/year) : Sun, Jul 01, 1990
Time (hour/min/sec) : 12 : 05 : 30
Daylight Saving : Disabled
Hard Disk C: type : Not Installed
Hard Disk D: type : Not Installed
Floppy Drive A: : 1.2 MB, 5¼
Floppy Drive B: : 1.44 MB, 3½
Primary Display : VGA or EGA
Keyboard : Installed

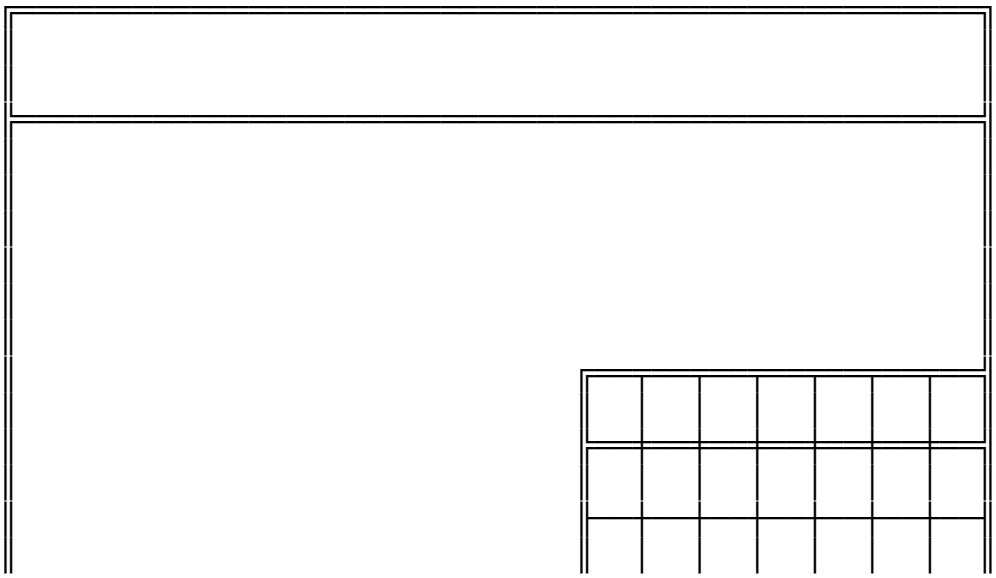
Base memory size : 640 KB
Ext. memory size : 3072 KB

Cyln Head WPcom LZone Sect Size

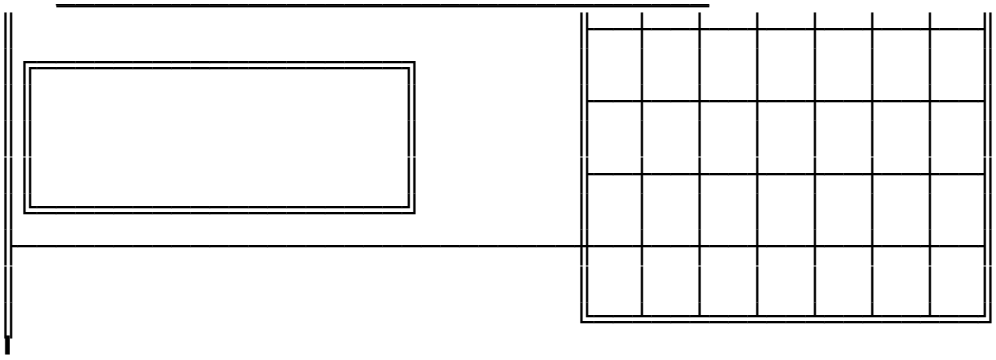
Month : Jan, Feb, ... Dec
Date : 01, 02, 03, ...
28
Year : 1901, 1902, ...

Sun	*Mon*	*Tue*	*Wed*	*Thu*	*Fri*	*Sat*
1	*2*	*3*	*4*	*5*	*6*	*7*
8	*9*	*10*	*11*	*12*	*13*	*14*
15	*16*	*17*	*18*	*19*	*20*	*21*
31	*22*	*23*	*24*	*25*	*26*	*27*
2099						
29	*30*	*31*	*1*	*2*	*3*	*4*
5	*6*	*7*	*8*	*9*	*10*	*11*

ESC:Exit,↓→↑←:Select F2/F3:Color,PgUp/PgDn:Modify



SYSTEM BIOS



OPTION 1 TIME AND DATE

Use PgUp and PgDn keys to change the value. The date and time cannot be entered directly. An calender is displayed on the lower right corner of the screen for your reference.

OPTION 2 FIXED DISK DRIVE

There are 47 types of fixed disks supported by the BIOS. Consult your fixed disk manual to determine its correct type. The parameters such as cylinder number, head number, sector number and pre-compensation must match your fixed disk's parameters.

Use PgUp and PgDn keys to change the fixed disk type. If the type of your fixed disk is not included in the hard disk list, define a new type as type 47. Use left and right arrow keys to move between the parameter fields and enter the parameters. The parameters will be stored in the CMOS RAM and your fixed disk can be used afterwards. Each hard disk can be assigned a different type 47 hard disk. So two hard disks which are not included in the list can be used together in your system.

If the type of fixed disk is wrong, it takes a while before the BIOS can identify the error. After setting the fixed disk type, if the system halts after reboot, please wait for a while. It is most likely that the setting of fixed disk type is incorrect.

When you install a new hard disk, make sure whether it is already formatted. If not, the BIOS has to check for a while before reporting the hard disk error. In fact, the error arises only because the hard disk is not formatted. If the hard disk is formatted, you can run DOS FDISK and DOS FORMAT.

Some fixed disks are specially handled and must be set to 'Not Installed'. Consult the fixed disk manual for details.

OPTION 3 FLOPPY DISK DRIVE

Four types of floppy disk drives are supported:

1. *5-¼ inch standard drive (360K)*
2. *5-¼ inch high-density drive (1.2M)*
3. *3-½ inch standard drive (720K)*
4. *3-½ inch high-density drive (1.44M)*

The system BIOS supports two floppy disk drives and they are recognized as drive A and B. Select the correct types. Otherwise the drives cannot work properly. If one of them is not installed, select 'Not Installed' for that drive.

The BIOS is able to detect the type of the drives automatically. But remember to check the settings before exit.

OPTION 4 DISPLAY

Four types of display are supported:

1. *CGA 80 column mode*
2. *CGA 40 column mode*
3. *EGA and VGA*
4. *Monochrome*

If the type of display is incorrect, the BIOS will prompt you and ask you to set up again. But the BIOS is still able to display messages on the display attached to the system. Thus you can enter the setup program.

The jumper JP8 must be set according to this setting. Otherwise, the BIOS will report error after self-test.

OPTION 5 KEYBOARD

If a keyboard is attached to the system, select 'Installed'. The BIOS will test the keyboard during self-test.

(2) ADVANCED CMOS SETUP

All the registers of the chipsets are set to default values by the system BIOS. Usually, there is no need to modify these registers unless the configuration is changed. Since improper settings of these registers may cause the system malfunction, check your settings carefully before exit.

In ADVANCED CMOS SETUP, the main menu is shown as below:

BIOS SETUP PRGRAM - ADVANCED CMOS SETUP
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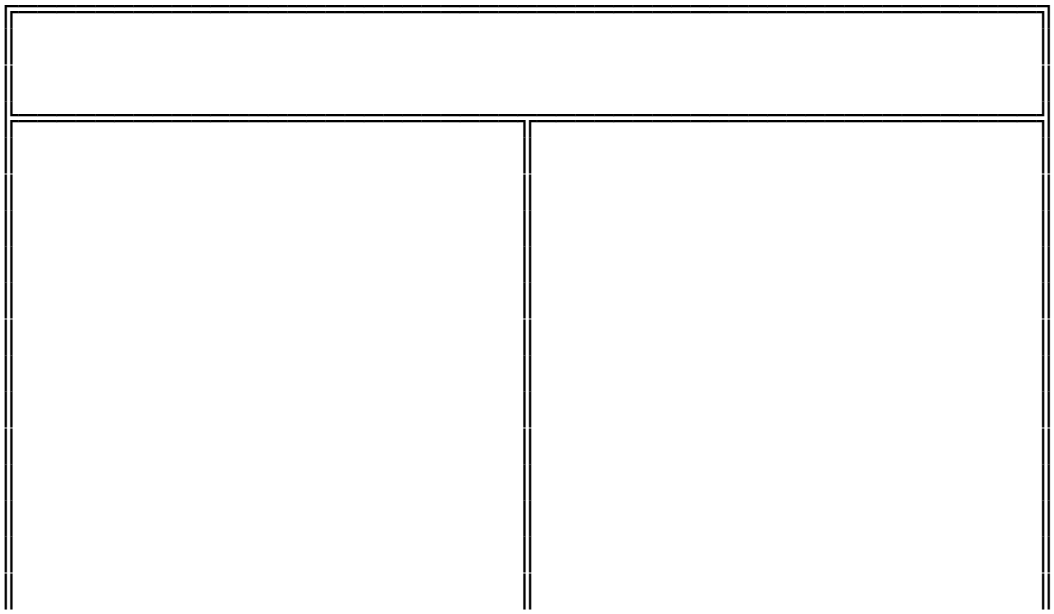
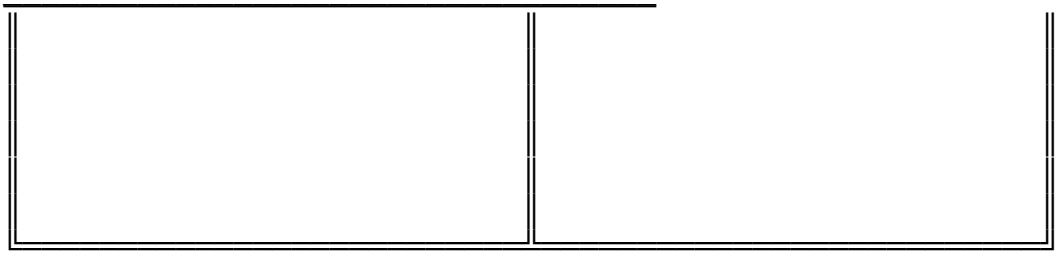
Typematic Rate Pgrogamming	*: Enabled*	*Adapter ROM Shadow CC00,16K*	*: Disabled*	
Typematic Rate Delay (Msec)	*: 500*	*Adapter ROM Shadow D000,16K*	*: Disabled*	
Typematic Rate (Chars/Sec)	*: 15*	*Adapter ROM Shadow D400,16K*	*: Disabled*	
Extended Memory Test	*: Disabled*	*Adapter ROM Shadow D800,16K*	*: Disabled*	
Memory Test Tick Sound	*: Enabled*	*Adapter ROM Shadow DC00,16K*	*: Disabled*	
Memory Parity Error Check	*: Enabled*	*Adapter ROM Shadow E000,16K*	*: Disabled*	
Hit <DEL> Message Display	*: Enabled*	*Adapter ROM Shadow E800,16K*	*:*	*Disabled*
Wait for <F1> if Any Error	*: Enabled*	*Adapter ROM Shadow EC00,16K*	*: Disabled*	
Hard Disk Type 47 RAM Area	*: 0:300*	*Adapter ROM Shadow E000,16K*	*: Disabled*	
System Boot Up Num Lock	*: On*	*System ROM Shadow F000,16K*	*: Enabled*	
Weitek Processor	*: Absent*			
Floppy Drive Seek At Boot	*: Enabled*			
System Boot Up Sequence	*: A:, C:*			
External Cache memeory	*: Enabled*			
Internal Cache memeory	*: Enabled*			
Video Rom Shadow C000,16K	*: Disabled*			
Video ROM shadow C400,16K	*: Disabled*			
Adapter ROM Shadow C800,16K	*: Disabled*			





After changing the registers' settings, test your system first to make sure that the settings are correct. It is likely that your system becomes unstable and you need to setup the registers again.

In this section, you simply use the up and down arrow keys to move between options and press PgUp/PgDn to scroll bit value. After you finish the Setup, press `Esc' to return to main menu. The BIOS will set the registers accordingly.

A short description follows for each of the options on the Advanced CMOS Setup Screen. If any problem in some options, press the <F1> Help Key.

Typematic Rate Programming :

By enabling this option, the user can adjust the rate at which a keystroke is repeated. The options "Typematic Rate Delay" and "Typematic Rate" also affect this rate. When a key is pressed and held down, the character appears on the screen and, after a delay set by the Typematic Rate Delay, it keeps on repeating at a rate set by the Typematic Rate Value. When two or more keys are pressed and held down simultaneously, only the last key pressed will be repeated at the typematic rate. This stops when the last key pressed is released, even if other keys are depressed.

Extended Memory Test :

If the option is enabled, the memory above 1MB will be tested.

Memory Test Tick Sound :

This option will turn on or turn off the "ticking" sound during the memory test.

Memory Parity Error Check :

If the system board does not have parity RAM, the memory parity error checking routines may be disabled in the BIOS. You should check with the dealer regarding the proper setting of this option.

Hit <Esc> Message Display :

If enabled, the following message will be shown after memory test :

"Hit <Esc> if you want to run SETUP"

It allows you to enter Setup section.

Hard Disk Type 47 Data Area :

The AMI BIOS SETUP features two user-definable hard disk types. Normally, the data for these disk types are stored at 0:300 in lower system RAM. However, if a problem occurs with some software regarding hard disk, try setting to `DOS 1 KB'. 1KB in the main memory will be allocated for hard disk type storage and the main memory is reduced to 639 KB.

Wait for F1 if Any Error :

If the BIOS finds some errors in the system, but it is a non-fatal error and the system can still function, the BIOS will respond with an error message followed by the following statement :

"Press <F1> to continue."

If this option is disabled, the BIOS will only display the error message and proceeds to other operations.

System Boot Up Num Lock :

The "num lock" option on the keyboard is usually turned on after power on. This option allows you to turn the "num lock" off after power on. So you can use the arrow keys on the numeric keypad without pressing the "num lock" key.

Numeric/Weitek Processor(s) :

These options allow the user to mark the numeric processor (Intel 80387 or compatible) or the Weitek numeric processor (WTL4167) as present or absent.

Floppy Drive Seek At Boot :

The default for this option is "Enabled". If disabled, it allows a fast boot.

System Boot Up Sequence :

This option allows you to choose which drive the system will boot from first. The default setting is `A:, C:'. It allows you to boot from device A if necessary. However, it will directly boot from hard disk when selecting `C:, A:'. The BIOS will not read the floppy disk A unless there is no drive C: installed. Thus it takes less time for boot up.

External Cache Memory :

This option controls the secondary cache memory. If the secondary cache memory is installed, select "enable".

Internal Cache Memory :

This option controls the internal cache memory of 80486. Normally, the internal cache memory is enabled.

Video,Adapter and System ROM shadow :

There are two options of shadow RAM for video adapter, ten options of shadow RAM for add-on card and one for the system BIOS. For the option System ROM, the content of the system at F000H segment BIOS is copied to the on board memory. For the option Video ROM, the video ROM at C0000H segment or C4000H segment are copied to memory. If you install an add-on card which ROM BIOS is locate at one of the Adapter ROM shadow options, you may select corresponding option to shadow this ROM. If there is any problem after enabling the shadow memory on the add-on card, it recommends to enable the shadow RAM function for system BIOS only.

(3) ADVANCED CHIPSET SETUP

Hidden Refresh :

If enabled, the refresh operation of main memory will not suspend the CPU operation and the overall performance is better.

Slow Refresh :

If enabled, the period of the refresh is four times slower. But since some DRAM from various manufacturers can only work with the ordinary refresh period, consult your dealer whether this option may be enabled. Normally, disables this option.

Single ALE Enable :

During bus conversion in AT bus cycle, such as I/O operation to add-on cards, the system logic will generate multiple ALE signal for add-on cards to latch the address bus status. A few add-on cards may not work properly with multiple ALE signals. In this case, select "Enable" to solve the problem. Should you have any question, please contact your local dealer.

Keyboard Reset Control :

When enabled, the system logic will generate reset control signal with a shorter delay and thus the switching between real mode and protected mode is faster. But some software may not work with this feature. So check your software carefully before enabling this feature.

Master Byte Mode Swap :

An add-on card with bus master capability should handle the data swapping on 8-bit operation correctly and this option need not be enabled normally. However, some bus masters add-on cards is not fully compatible with the ISA bus standard. By enabling this option, the system logic will instead perform the data swapping.

At Cycle Wait State :

If you set it to "Enable", an extra wait state will be inserted to every operation to ISA bus. It is useful when you find that some slow add-on cards are unable to work on HIPPO II. Normally, select "Disable" for maximum performance.

DRAM Read/Write Wait State :

Select 0 wait state with 80ns DRAM or faster and 1 wait state for 100ns DRAM.

Check carefully whether your DRAM is suitable for the number of wait states you want to select. Improper setting can make the system unstable. Since the specification of DRAM from different manufacturers may vary, you would better consult your local dealer for the detail information.

Cache Write W/S :

This options sets the wait state for cache memory. Normally, set to 0 wait state for maximum performance. For 64KB cache size, select "0, 8KX8". For 256KB cache size, set it to "0, 32KX8".

Non-cacheable Block Size and Non-cacheable Block Base

Two non-cacheable block, block-1 and block-2, can be defined. You need to specify the size and base address. The block size may be 64KB, 128KB, 256KB and 512KB. The base address is where the non-cacheable block will start in the main memory. Press 'PgDn' and 'PgUp' keys to change the address value to an appropriate value.

Video BIOS Area Cacheable :

The video BIOS starts from the location 768K (C0000 hexadecimal) and the size is 32KB. This option lets you set the address range to be non-cacheable easily without concerning about the base address and the size. The default is "Disable". If the Video BIOS area is cacheable, the performance of the video BIOS is better, but it is likely that the BIOS may be overwritten by other software.

(4) AUTO CONFIGURATION WITH BIOS DEFAULTS

The Auto configuration with BIOS default is used to set the internal registers of the system in optimum performance with high reliability. Once the Auto Configuration is applied, the user need not enter the ADVANCED CMOS SETUP. You will still need to set those options in the STANDARD CMOS SETUP after the Auto Configuration is used.

(5) HARD DISK UTILITY

Hard Disk Diagnostics option is taken by pressing <Enter> at the Main Setup Menu, the screen is shown as below :

BIOS SETUP PROGRAM - HARD DISK UTILITY
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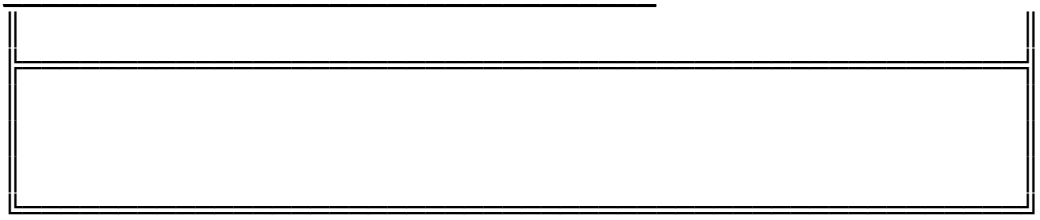
		Cylin	Head	WPcom	LZone	Sect	Size (MB)
Hard Disk C:	Type : 47 USER TYPE	1314	7	1314	1314	17	76
Hard Disk D:	Type : Not Installed						

Hard Disk Type can be changed from the STANDARD CMOS SETUP option in Main Menu

Hard Disk Format
Auto Interleave
Media Analysis



There are three options in the hard disk utility : Hard Disk Format, Auto Interleave, and Media Analysis.

For a new hard disk (drive), the manufacturer of the hard drive usually provides a list of "bad tracks" with the hard drive. Your hard disk manual might also include the optimum interleave factor.

In this case, assuming that you have a list of bad tracks and know the interleave factor, it will not be necessary to take the auto interleave and media analysis options. Simply follow the instructions in the Hard Disk Format. If you have a bad track list but have not been provided with the optimum interleave factor, follow the instructions in the Auto Interleave Section.

BIOS SETUP PROGRAM - HARD DISK UTILITY
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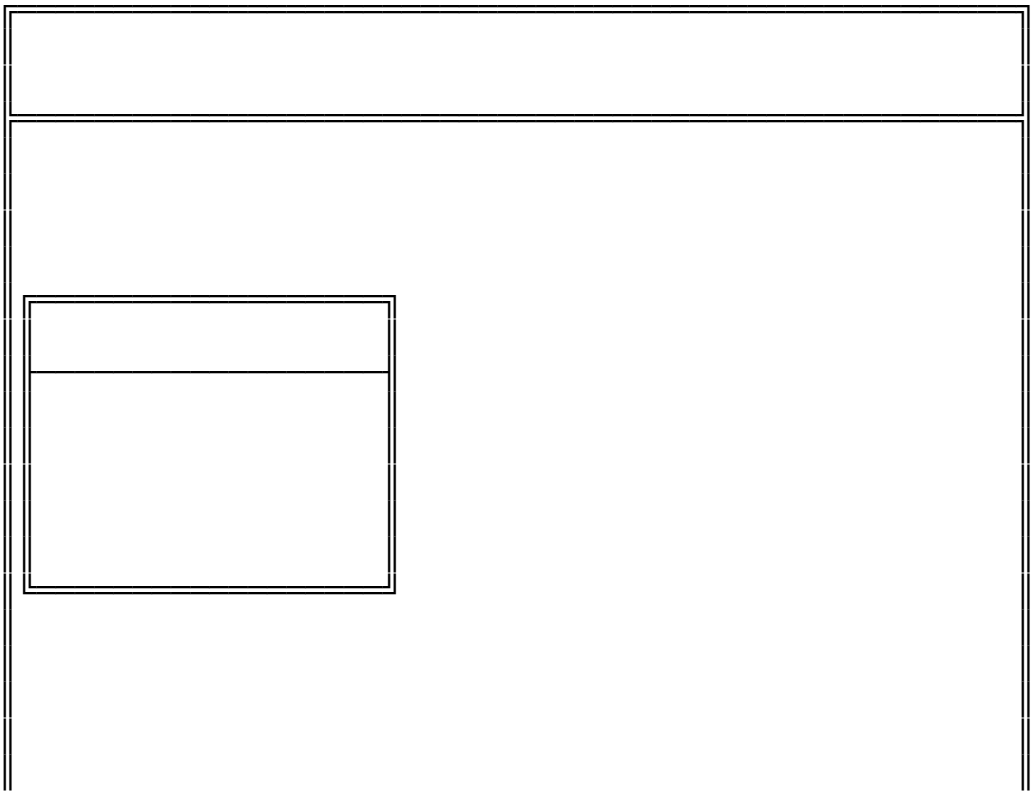
	Cylin	Head	WPcom	LZone	Sect	Size (MB)
Hard Disk C:Type :47 USER TYPE	1314	7	1314	1314	17	76
Hard Disk D: Type :Not Installed						

Hard Disk Format

Disk Drive (C/D) ? C
Disk Drive Type ? 47
Interleave (1-16) ? 3
Mark Bad Tracks (Y/N) ?
Proceed (Y/N) ?



OPTION 1 HARD DISK FORMAT UTILITY

Use the Hard Disk Format option to integrate a new hard disk to the system, or to reformat a used hard disk which has developed some bad tracks. To find these bad tracks on a used drive, select the Media Analysis option.

The value for Disk Drive is C for a C: Drive or D for a D: Drive. If two disk drives have been previously entered at the Standard CMOS Setup Scree, then the ID (C/D) will appear to the right of the question mark following the Disk Drive field. Choose which drive you wish to format by selecting the appropriate letter and pressing <ENTER>. If only one drive was selected at the Standard CMOS Setup Screen, the cursor will automatically be placed at the interleave prompt.

The Disk Drive Type is read from the CMOS. The

interleave factor can be selected manually, or can be determined with the Auto Interleave feature of the SETUP program.

The hard drive usually provides a list of bad tracks. These tracks should be entered with this option, and they will then be marked as "bad" in order to prevent data from being stored there.

The default for the Proceed prompt is <N> to prevent accidental formatting of the hard drive and subsequent loss of data. **Once this prompt is changed to <Y> and the <ENTER> key pressed, andy data residing on the hard disk will be irrevocably lost.**

Make sure that your hard disk is allowed to be formatted. Some hard disks are formatted in the factory and will be malfunctioned if reformatted. Check your hard disk manual for more information.

OPTION 2 AUTO INTERLEAVE UTILITY

The Auto Interleave Utility determines the optimum interleave value by measuring the transfer rate for four different interleave values. The cylinders, heads and sectors formatted for each value will be displayed in the actively box on the screen.

BIOS SETUP PROGRAM - HARD DISK UTILITY
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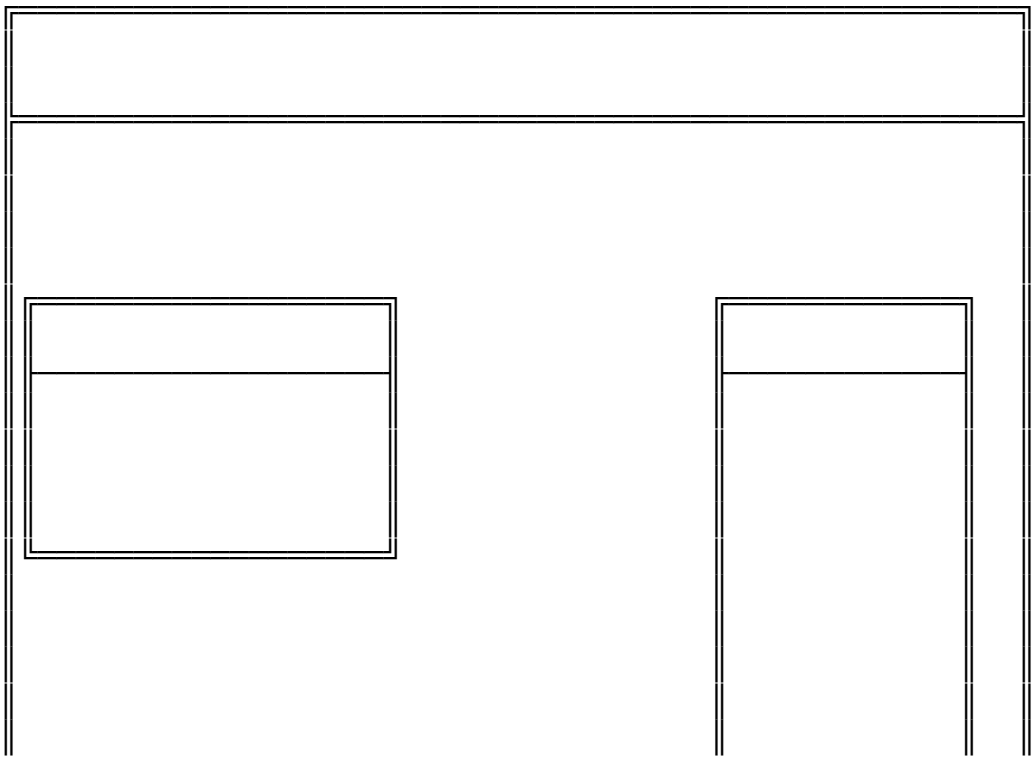
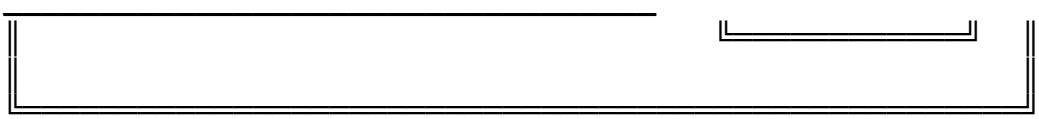
	Cylin	Head	WPcom	LZone	Sect	Size (MB)
Hard Disk C:Type :47 USER TYPE	1314	7	1314	1314	17	76
Hard Disk D: Type :Not Installed						

Auto Interleave *Bad Track %*

Disk Drive (C/D)	?	C
Disk Drive Type	?	47
Mark Bad Tracks (Y/N)	?	N
Proceed (Y/N)	?	

Ms. Cyln. Head





OPTION 3 MEDIA ANALYSIS UTILITY

The Media Analysis Utility performs a series of tests to locate bad tracks on the hard disk. All bad tracks on the hard disk will be listed in the Bad Track List Box. Since this test writes to all cylinders and heads on the hard disk to verify andy bad tacks, the test may require several minutes to complete.

BIOS SETUP PROGRAM - HARD DISK UTILITY
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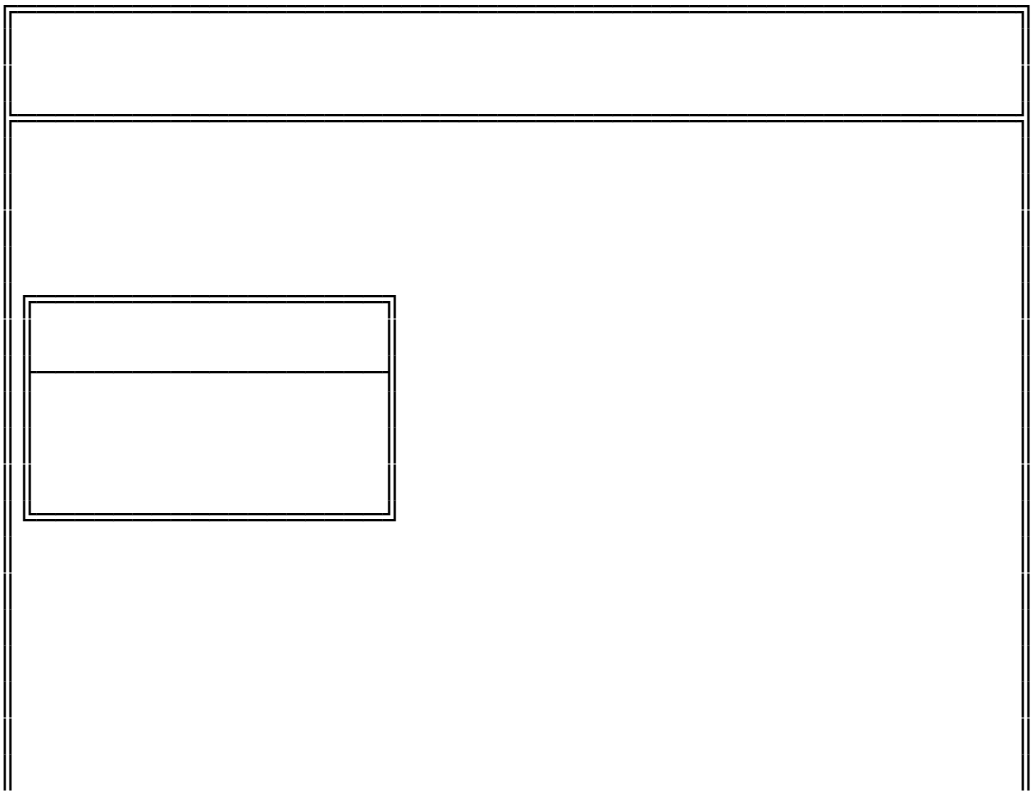
	Cylin	Head	WPcom	LZone	Sect	Size (MB)
Hard Disk C:Type :47 USER TYPE	1314	7	1314	1314	17	76
Hard Disk D: Type :Not Installed						

Media Analysis

Disk Drive (C/D) ? C
Disk Drive Type ? 47
Proceed (Y/N) ?



Appendix B
Operation and Maintenance

STATIC ELECTRICITY

When installing or removing any add-on card, DRAM module or coprocessor, you should discharge the static electricity on your body. Static electricity is dangerous to electronic device and can build-up on your body. When you touch the add-on card or motherboard, it is likely to damage the device. To discharge the static electricity, touch the metal of your computer. When handling the add-on card, don't contact the components on the cards or their "golden finger". Hold the cards by their edges.

KEEPING THE SYSTEM COOL

The motherboard contains many high-speed components and they will generate heat during operation. Other add-on cards and hard disk drive can also produce a lot of heat. The temperature inside the computer system may be very high. In order to keep the system running stably, the temperature must be kept at a low level. A easy way to do this is to keep the cool air circulating inside the case. The power supply contains a fan to blow air out of the case. If you find that the temperature is still very high, it would be better to install another fan inside the case. Using a larger case is recommended if there are a number of add-on cards and disk drives in the system.

CLEANING THE "GOLDEN FINGER"

Whenever inserting an add-on card to the motherboard, make sure that there is no dirt on the "golden finger" of the add-on card. If not, the contact between the "golden finger" and the slot may be poor and thus the add-on card may not work properly. Use a pencil eraser to clean the "golden finger" if dirt is found.

CLEANING THE MOTHERBOARD

The computer system should be kept clean. Dust and dirt is harmful to electronic devices. To prevent dust from accumulating on the mother-board, installing all mounting plates on the rear of the case. Regularly examine your system, and if necessary, vacuum the interior of the system with a miniature vacuum.

Appendix C
Troubleshooting

MAIN MEMORY ERROR

After power up, the monitor remains blank, and there are beep sounds indicating a main memory failure. In this case, turn off the power and remove all SIMM modules. Carefully place the modules back to the sockets and make sure that all the modules are locked by the locking latches firmly.

In some other cases, the total memory found by the BIOS is different from the actual amount of memory on board. (Note that 128K bytes memory is reserved for the shadow RAM function and will not be counted by the BIOS). It is also a memory failure and you can follow the instruction above.

CACHE MEMORY FAILURE

If the system hangs after memory test, it is likely that the cache memory has some problems when the secondary cache memory card is installed. Maybe some of the SRAMs are damaged or the contact of the IC pins is poor. Try to press the SRAM to make sure that the SRAMs are inserted in the sockets, or examine the SRAM to see whether any pins are bent under or out. If the bent pins are found, remove the SRAM, straighten the pin and place the SRAM again. You may also check the BIOS setup of the cache configuration. If the cache controller is enabled, you should select chipset's cache controller. Otherwise, the system will fail.

IMPROPER SETTING OF WAIT STATE

If the system hangs after memory test, another possible cause is the improper setting of the wait state for memory operation. The number of wait state must match the speed of the DRAM. Reset the CMOS RAM and set up the wait state. Try to increase the number of wait state.

Appendix D
System Board Layout