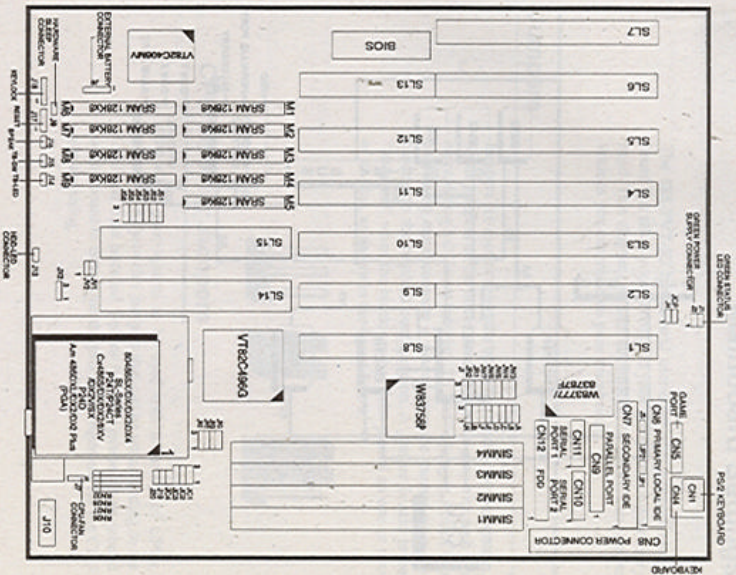


- 72-pin SIMM sockets supports up to 128MB DRAM, provides page mode DRAM operation.
- Supports system and video BIOS cacheable and shadow.
- Supports decoupled DRAM refresh.
- Optional regulator board for various SI-series CPUs.
- Supports six 16-bit and one 8-bit ISA expansion slots.
- Supports two VESA bus expansion slots.
- Optional enhanced IDE support allows for up to four host interface devices.
- Built-in internal real time clock/calendar.
- Provides built-in power management features.
- Winbond W83777/87F™ and W83758 Power I/O™ chipset.

→ **NOTE :** The 486-PVT-10 provides a socket for CPU chipset. To plug your CPU into the PGA socket, please observe proper alignment and position.

486-PVT-10

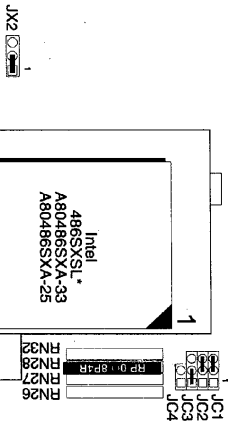
Mainboard Layout



486-PVT-10

→ **CAUTION :** When using a low-voltage CPU, a regulator board may be needed. Some mainboards install a low-voltage regulator chipset onboard. If the onboard low-voltage regulator is not present, the low-voltage daughter board should be installed, please refer to page 2-8 for the regulator board installation.

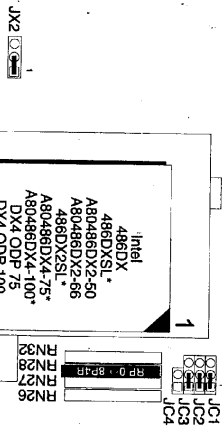
Intel 486SX/SXSL



* A regulator board may be needed when using this CPUs. Please refer to page 2-8 for its installation.

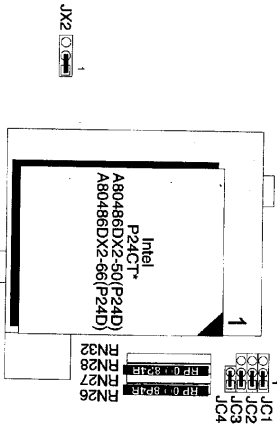
→ **NOTE :** Users are not encouraged to change the jumper settings not listed in this manual. Changing the jumper settings improperly may adversely affect system performance.

Intel 486DX/SL-Series/DX2/DX4/DX4 OVERDRIVE



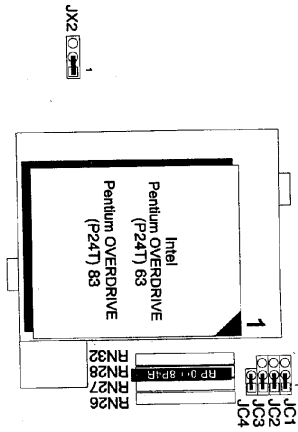
* A regulator board may be needed when using this CPUs. Please refer to page 2-8 for its installation.

Intel P24CT/P24D

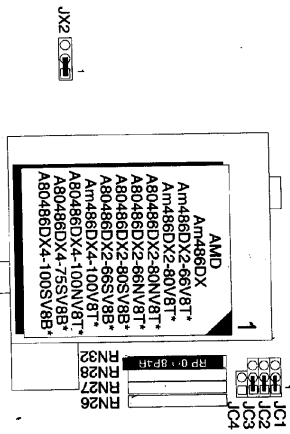


* A regulator board may be needed when using this CPUs. Please refer to page 2-8 for its installation.

Intel P24T

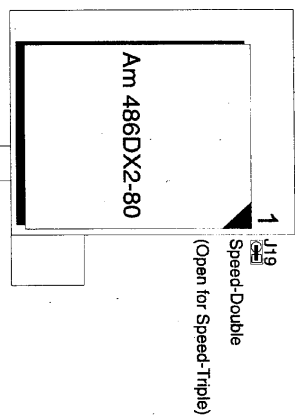


AMD 486DX/DX2/DX4

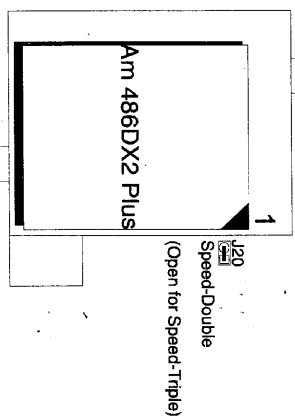


* A regulator board may be needed when using this CPU's. Please refer to page 2-8 for its installation.

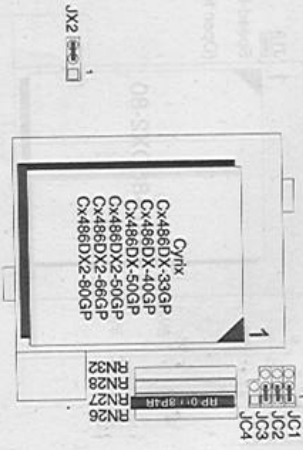
Check Selection for AMD CPU only



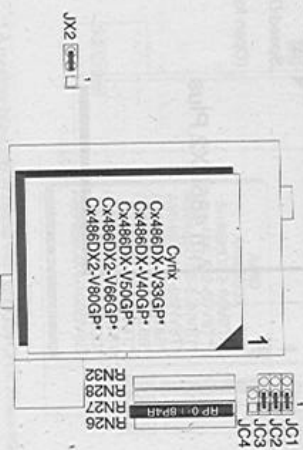
or



Cyrix 486DX/DX2

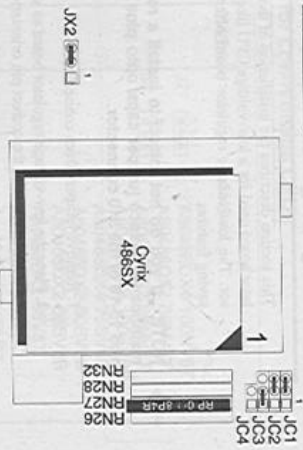


Cyrix 486DX-V/DX2-V



* A regulator board may be needed when using this CPU's. Please refer to page 2-8 for its installation.

Cyrix 486SX



CPU Clock Jumper JK1-JK4

	50 MHz DX50	40 MHz DX40 DX2-80	33.3 MHz (Default) SX33 DX33 DX4-100	25 MHz SX25 DX25 DX2-50 DX4-75
JK1	3 2 1	3 2 1	3 2 1	3 2 1
JK2	3 2 1	3 2 1	3 2 1	3 2 1
JK3	3 2 1	3 2 1	3 2 1	3 2 1
JK4	3 2 1	3 2 1	3 2 1	3 2 1

Low-Voltage Regulator Board Installation

This section describes the installation of the low-voltage regulator board used for a low-voltage CPU like Intel DX4 processor. The low-voltage regulator board offers advanced power saving features.

→ **NOTE : If you do not intend to install a regulator on the mainboard, replace jumper caps onto pins 1-2, 3-4, 13-14 and 15-16 of the J10 connector.**

1. Remove jumpers from connector J10.
2. Place the low-voltage regulator board as shown on the figure below with the correct pin orientation.

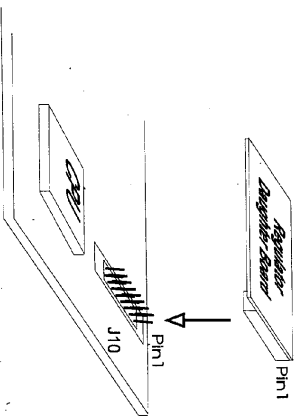








Figure 2.2. Low-Voltage Regulator Board Installation

Jumper Setting on Regulator Board for Low-Voltage CPUs

3.45V	J2 	AMD - A80486DX4-100NV/8T A80486DX2-80NV/8T A80486DX2-66NV/8T A80486DX4-100SV/8B A80486DX4-75SV/8B A80486DX2-80SV/8B A80486DX2-66SV/8B Am486DX2-66V/8T Am486DX2-80V/8T Am486DX4-100V/8T
	J3 	INTEL 486 - A80486DX4-100 A80486DX4-75
3.6V	J2 	Cyrix - CX486DX-V33GP CX486DX-V40GP CX486DX-V50GP CX486DX-V66GP
	J3 	
4.0V	J2 	Cyrix - CX486DX2-V80GP
	J3 	

Jumper Setting for ISA IDE

J3	Onboard IDE Controller <input type="checkbox"/> Disable <input checked="" type="checkbox"/> Enable (Default)
J5	Local IDE Connector Jumper Select <input checked="" type="checkbox"/> IDE connector pin28 linked to BALE signal <input type="checkbox"/> IDE connector pin28 open (Default)
Jp1	ISA IDE Connector Jumper Select <input checked="" type="checkbox"/> ISA IDE connector pin27 linked to IOCHRDY signal <input type="checkbox"/> ISA IDE connector pin27 open (Default)
Jp2	ISA IDE Connector Jumper Select <input checked="" type="checkbox"/> ISA IDE connector pin28 linked to BALE signal <input type="checkbox"/> ISA IDE connector pin28 open (Default)

Jumper Setting for VESA Bus

JV1	High Speed Write Select <input checked="" type="checkbox"/> One wait write <input type="checkbox"/> Zero wait write (Default)
JV2	CPU Speed Select <input checked="" type="checkbox"/> Greater than 33 MHz <input type="checkbox"/> Less than or equal to 33 MHz (Default)

Jumper Setting for System I/O (Continued)

JCP	Password Clear Select <input type="checkbox"/> Clear password <input checked="" type="checkbox"/> (Default)
J4	Display Type Select <input type="checkbox"/> Mono/EGM/GA (Default) <input checked="" type="checkbox"/> CGA
JW7	Game Port Select <input checked="" type="checkbox"/> Disable game port <input type="checkbox"/> Enable game port (Default)
JR1	IDE Hard Disk RW Signals From... <input checked="" type="checkbox"/> W83758 <input type="checkbox"/> VT82C496G (Default)
JR2	Same as JR1
JH	Onboard FDC <input checked="" type="checkbox"/> Disable <input type="checkbox"/> Enable (Default)

Jumper Setting for System I/O

COM 1 I/O Address Setting

	Disable	3E8H	2E8H	3F8H (Default)
J/A	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
J/B	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>

COM 2 I/O Address Setting

	Disable	2E8H	3E8H	2F8H (Default)
J/C	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
J/D	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>

LPT I/O Address Setting

	Disable	27BH	3BCH	37BH (Default)
J/E	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
J/F	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>

LPT Output Enhanced Control Setting

J/I	Data Direction Control	
	<input checked="" type="checkbox"/>	Parallel port as output port only
	<input type="checkbox"/>	Parallel port as input/output port (Default)

Jumper Setting for Printer Mode

	Print (Default)	EPP/SPP	EPP/ECP	EXT2FDD
J/W3	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
J/W4	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>

Jumper Setting for ECP Mode DMA Channel

	DMA 1 (Default)	DMA 3
J/W5	<input checked="" type="checkbox"/>	<input type="checkbox"/>
J/W6	<input type="checkbox"/>	<input checked="" type="checkbox"/>



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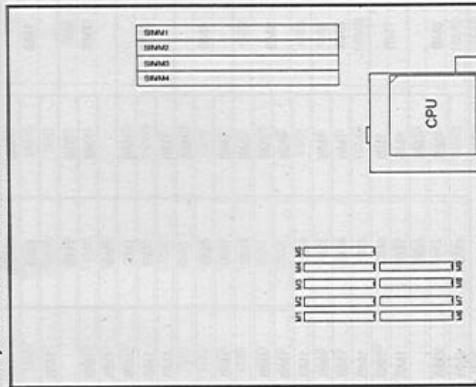
Chapter 3

Memory Subsystem

The 486-PVT-IO is equipped with the memory necessary for running all your applications. Memory comes in the form of DRAM (SIMMs) and cache SRAM. This chapter describes these two kinds of memory and gives instructions on how to install each kind on the mainboard.

Memory Locations

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:



Installing DRAM

SIMM Banks

The 486-PVT-IO accommodates onboard memory from 1 to 128MB using SIMMs (Single-In-Line Memory Modules). The mainboard has four memory banks that accept either a 1, 4, 16 or 32MB on each SIMM socket.

DRAM Configuration

Memory can be installed in a variety of configurations, as shown in the next table:

TOTAL MEMORY	SIMM 1 (72-PIN)	SIMM 2 (72-PIN)	SIMM 3 (72-PIN)	SIMM 4 (72-PIN)
1MB	1MB	1MB	1MB	
2MB	1MB	1MB	1MB	
3MB	1MB	1MB	1MB	1MB
4MB	1MB	1MB	1MB	1MB
5MB	1MB	4MB	4MB	
6MB	1MB	1MB	1MB	1MB
7MB	1MB	4MB	1MB	1MB
8MB	4MB	4MB	4MB	

486-PVT-IO

TOTAL MEMORY	SIMM 1 (72-PIN)	SIMM 2 (72-PIN)	SIMM 3 (72-PIN)	SIMM 4 (72-PIN)
9MB	1MB	4MB	4MB	4MB
10MB	1MB	1MB	4MB	4MB
12MB	4MB	4MB	4MB	4MB
13MB	4MB	4MB	4MB	4MB
16MB	4MB	16MB	16MB	4MB
17MB	1MB	16MB	16MB	1MB
18MB	1MB	16MB	16MB	1MB
20MB	4MB	16MB	16MB	1MB
21MB	1MB	16MB	4MB	4MB
22MB	4MB	16MB	4MB	1MB
24MB	4MB	16MB	4MB	4MB
25MB	1MB	16MB	4MB	4MB
28MB	4MB	16MB	4MB	4MB
32MB	32MB	32MB	16MB	16MB
33MB	1MB	16MB	16MB	16MB

486-PVT-IO

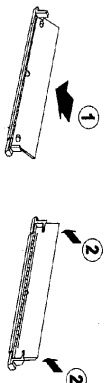
TOTAL MEMORY	SIMM 1 (227N)	SIMM 2 (173N)	SIMM 3 (173N)	SIMM 4 (227N)
34MB	1MB	1MB	16MB	16MB
36MB	4MB	16MB	16MB	16MB
37MB	4MB	4MB	16MB	16MB
40MB	4MB	1MB	16MB	16MB
48MB	1MB	16MB	16MB	16MB
49MB	4MB	16MB	16MB	16MB
52MB	4MB	16MB	16MB	16MB
64MB	1MB	32MB	32MB	
65MB	1MB	32MB	32MB	
66MB	1MB	1MB	32MB	32MB
68MB	1MB	32MB	1MB	32MB
	4MB	32MB	32MB	1MB
	4MB	32MB	32MB	32MB
	4MB	4MB	32MB	32MB
69MB	1MB	32MB	4MB	32MB
	4MB	1MB	32MB	32MB
	4MB	32MB	1MB	32MB
72MB	4MB	4MB	32MB	32MB
	32MB	32MB	4MB	4MB
80MB	32MB	16MB	32MB	32MB
81MB	1MB	16MB	32MB	32MB
84MB	4MB	16MB	32MB	32MB
96MB	16MB	4MB	32MB	32MB
97MB	32MB	32MB	32MB	1MB
128MB	32MB	32MB	32MB	32MB

→ NOTE : All memory banks accept double-RAS SIMM.

Installation Instructions

→ NOTE : Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.

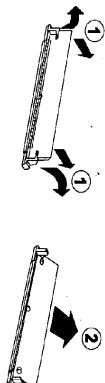
1. Locate the SIMM banks on the mainboard. Determine your desired configuration to be installed.
2. Swing each SIMM into its upright, locked position. When locking a SIMM in place, push on each end of the SIMM, don't push in the middle.



→ NOTE : The SIMMs will only fit in one direction.

When adding RAM memory modules (SIMMs), it may be necessary to remove the existing SIMMs so you have enough room to install additional SIMMs.

- Complete the following steps to remove a SIMM:
1. Carefully push out on the brackets securing each end of the SIMMs, while pushing out on the SIMM until it rests at a 45 degree angle. It is sometimes necessary to unlock an adjacent SIMM to allow enough working space.
 2. Once the SIMM is unlocked and in its 45 degree position, lift the SIMM from it's socket.



Cache Memory

The 486-PVT-IO accepts cache memory of 128KB, 256KB, 512KB or 1MB.

Installing Cache Memory

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the beginning of this manual.**

If you do not have the confidence to make the installation, better consult a service technician for assistance.

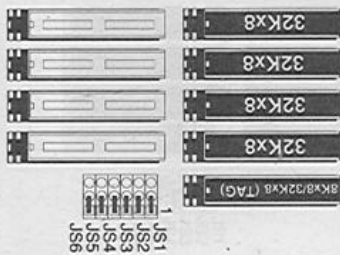
1. Locate the cache memory on the mainboard.
2. Be guided by the Cache SRAM settings depending on your desired SRAM configuration.
3. Correct orientation of the chips is necessary for the cache to operate properly. Normally, the chips have either a curved notch or a dot. This marker on the chip must be matched to the marker on the socket for correct alignment.

Install the chips individually as follows:

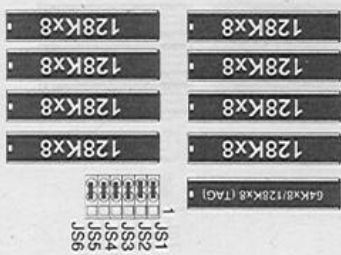
1. Align the chip with the marker on the socket. Press the chip onto the socket, ensuring that the pins on the chip are aligned with the corresponding connections on the socket.
2. Carefully apply enough pressure to partially seat the chip into the socket.
3. Ensure that all pins are properly aligned with the connectors and that there are no bent pins. If there are any bent pins, remove the chip, straighten the pin and repeat the process.
4. Press the chip completely into the socket so that the pins are properly seated.

Cache SRAM Specifications and Settings

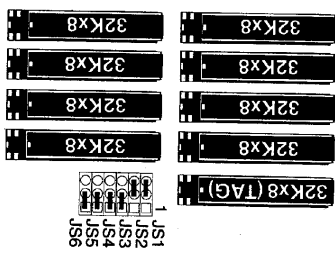
128K Cache SRAM



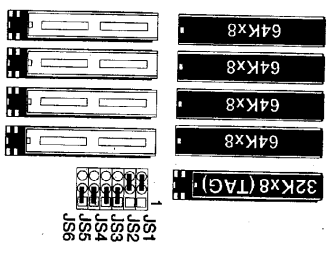
1M Cache SRAM



256K Cache SRAM

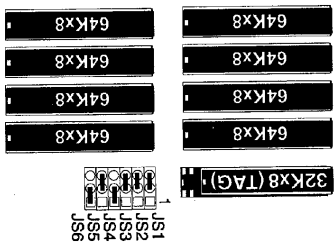


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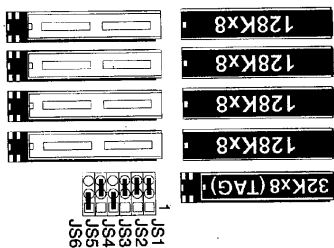


486-PVT-I/O

512K Cache SRAM



OR



486-PVT-I/O