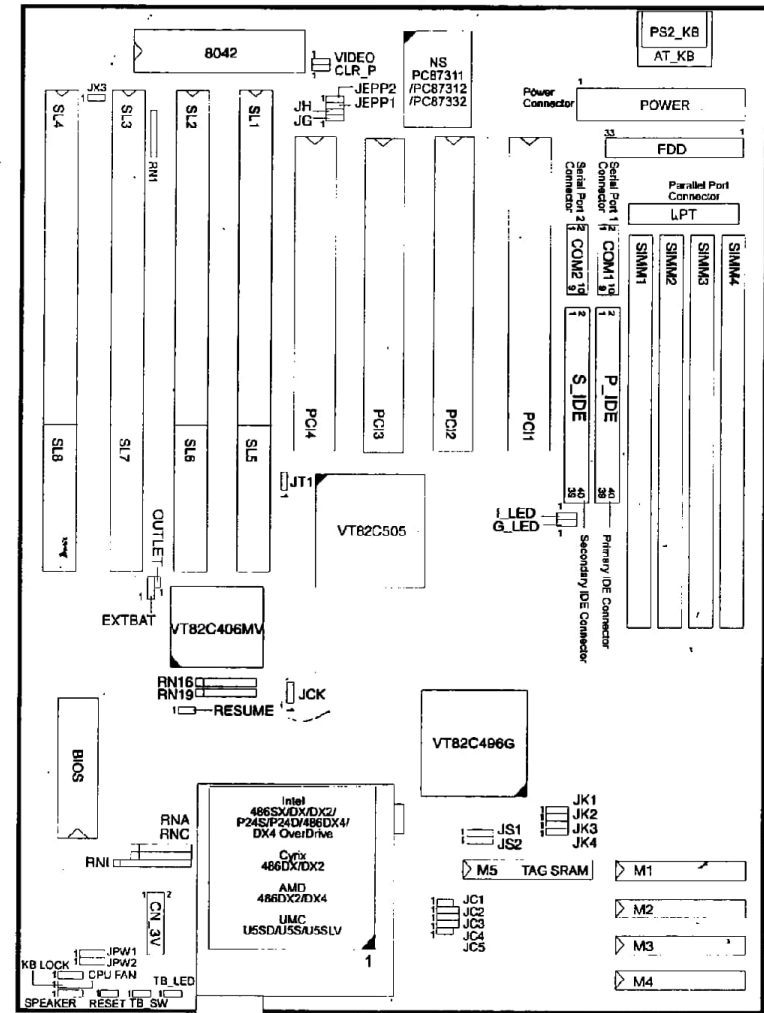


- Optional Flash ROM.
- Award BIOS.
- Supports 128K/256K/512K direct-mapped write-back/write-through cache memory.
- 72-pin SIMM sockets supports up to 128MB DRAM, provides page mode DRAM operation.
- Supports system and video BIOS cacheable, also video BIOS shadow.
- Supports decoupled DRAM refresh.
- Optional built-in ZIF socket that accepts Intel's OverDrive™ processors namely - P24D, P24T.
- Supports onboard regulator for low-voltage processors.
- Supports four 16-bit ISA expansion slots.
- Supports four PCI bus expansion slots.
- Built-in internal real time clock/calendar.
- Provides built-in power management features necessary for Green PCs.
- Enhanced IDE support allows for up to four host interface devices.
- Built-in IDE HDD/FDD controllers.
- NS PC87311/312™ or NS PC87332™ chipset for two serial/one parallel port.
- Supports ECP/EPP Protocol (NS PC87332™ only).

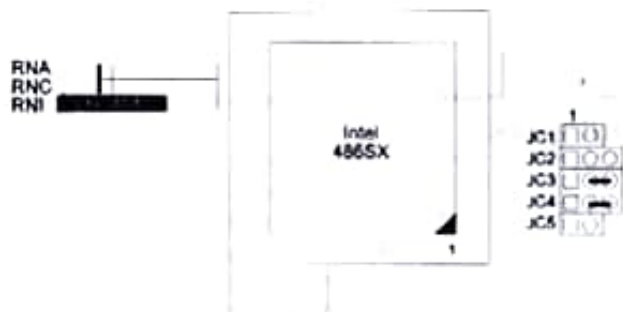
## Mainboard Layout



→ **NOTE :** The 486-PIO-2 provides a socket for the processor chipset. When plugging your new processor into the PGA socket, please observe proper alignment and position.

→ **CAUTION** : When using a low-voltage processor, please refer to page 2-11 for jumper setting modifications.

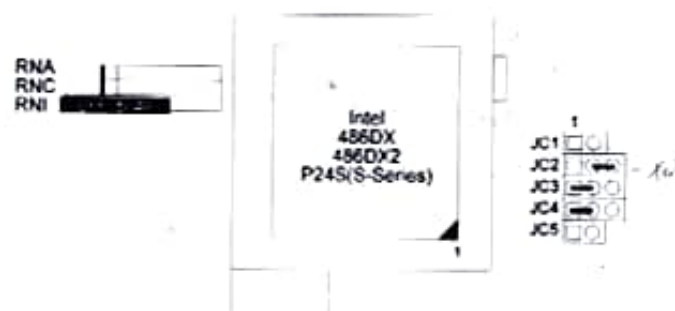
### Intel 486SX



→ **NOTE** : Users are not encouraged to change the jumper settings not listed in this manual. Changing the jumper settings improperly may adversely affect system performance.

### Intel 486DX/DX2/P24S (S-Series)

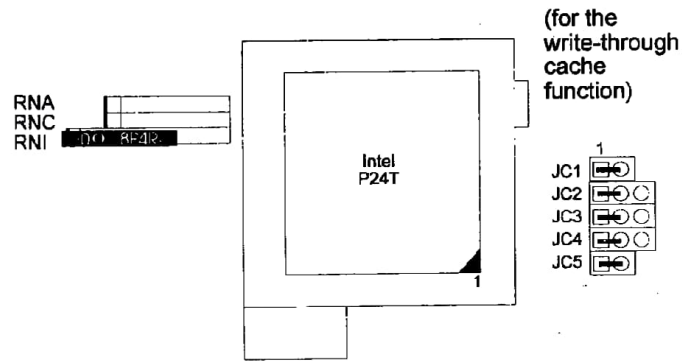
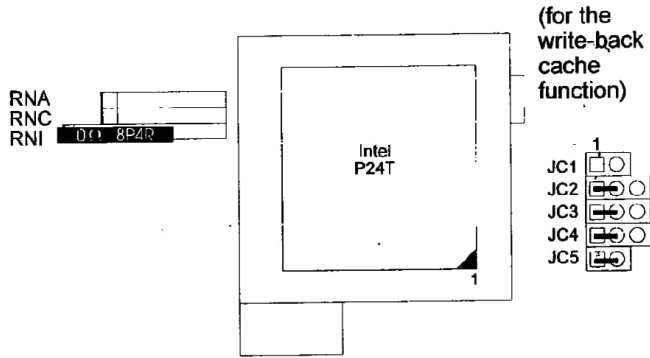
Enhanced A11D-X5



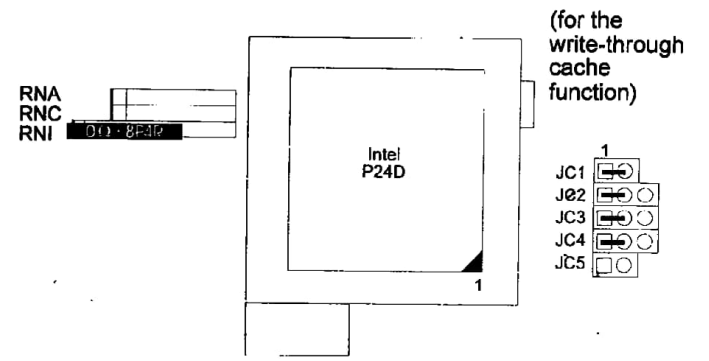
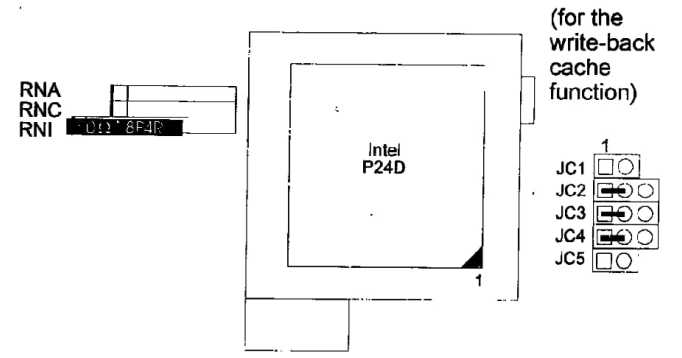
### IntelDX4 ODP (DX4 OverDrive)



**Intel P24T**



**Intel P24D**



**IntelDX4****Double-Speed**

\* When using this processor, please refer to page 2-11 for more information about jumper setting.

**Triple-Speed**

\* When using this processor, please refer to page 2-11 for more information about jumper setting.

**UMC U5SD****UMC U5S/U5SLV**

\* When using this processor, please refer to page 2-11 for more information about jumper setting.

**Cyrix Cx486DX/DX2**

\* When using this processor, please refer to page 2-11 for more information about jumper setting.

**AMD 486DX2**

\* When using this processor, please refer to page 2-11 for more information about jumper setting.

**AMD 486DX4**

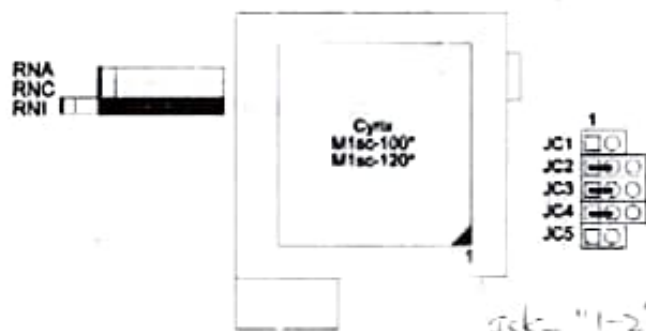
\* When using this processor, please refer to page 2-11 for more information about jumper setting.

**Enhanced AMD 486DX2**

\* When using this processor, please refer to page 2-11 for more information about jumper setting.

**Enhanced AMD 486DX4**

\* When using this processor, please refer to page 2-11 for more information about jumper setting.

**Cyrix M1sc**

\* When using this processor, please refer to page 2-11 for more information about jumper setting.

**Low-Voltage Processor Jumper Setting**

Processor Voltage Type	Jumper Setting	Processor Model
3.3V	JPW1 JPW2	UMC - USSLV-SUPER25 USSLV-SUEPR33
3.45V	JPW1 JPW2	AMD - A80486DX4-100NV8T A80486DX2-80NV8T A80486DX2-66NV8T A80486DX4-100SV8B A80486DX4-75SV8B A80486DX2-80SV8B A80486DX2-66SV8B Am486DX2-66V8T Am486DX2-80V8T Am486DX4-100V8T  INTEL 486 - A80486DX4-100 A80486DX4-75  Cyrix - M1sc-100 M1sc-120
3.6V	JPW1 JPW2	Cyrix - Cx486DX-V33GP Cx486DX-V40GP Cx486DX2-50GP Cx486DX2-66GP
4.0V	JPW1 JPW2	Cyrix - Cx486DX2-V80GP
CN_3V	 	For 3.3V, 3.45V, 3.6V and 4.0V processors  For 5V processors (Default)



**Processor Clock Jumper Setting**

	60 MHz DX-50	40 MHz DX-40 DX2-80	33.3 MHz (Default) SX-33 DX-33 DX2-66 DX4-100	25 MHz SX-25 DX-25 SX2-50 DX2-50 DX4-75
JK1				
JK2				
JK3				
JK4				

**System Jumper Setting**

JT1, JCK		<b>PCI Bus Clock Select</b> (When the processor clock is less than or equal to 33 MHz.) PCI Bus Clock = Processor Clock (Default)
		(When the processor clock is greater than 33 MHz.) PCI Bus Clock = Processor Clock / 2





misc Jck - 1-2

**I/O Jumper Setting**

CLR_P		<b>Password Clear Select</b> (Default)
		Clear password
VIDEO		<b>Display Type Select</b> Mono/EGA/VGA (Default)
		CGA
JK3		<b>Internal/External Keyboard Select</b> Internal keyboard controller (Default)
		External keyboard controller
		<b>Internal/External Keyboard Select</b> Internal keyboard controller (Default)
		External keyboard controller






## DMA Channel Jumper Setting

### NS87332 ECP Mode



	DMA 1 (Default)	DMA 3
JEPP2		
JEPP1		

## Printer Port Jumper Setting

### NS87311/312 Printer Port Direction

	OUTPUT (Default)	INPUT	BIDIRECTION
JH			
JG			NA

### NS87332 Printer Port Direction

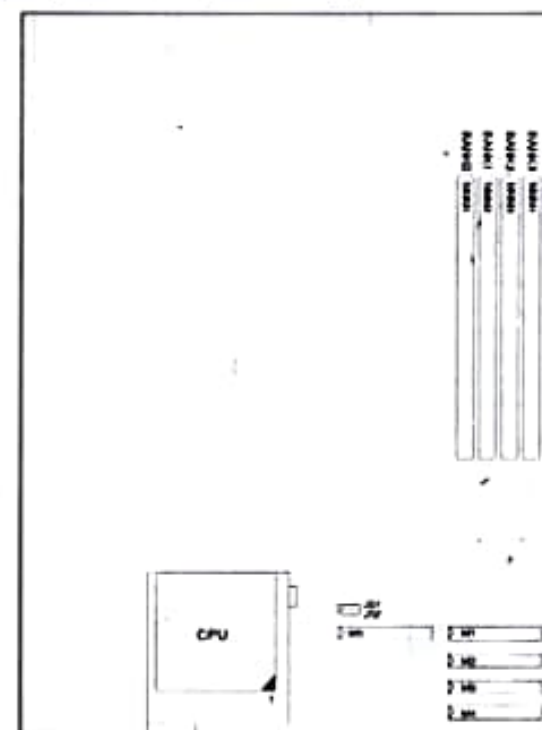
	OUTPUT
JH	
JG	

## Memory Subsystem

The 486-PIO-2 is equipped with the memory necessary for running all your applications. Memory comes in the form of DRAM (SIMMs) and cache SRAM. This chapter describes these two kinds of memory and gives instructions on how to install each kind on the mainboard.

## Memory Locations

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:





## Installing DRAM

### SIMM Banks

The 486-PIO-2 can accommodate on-board memory from 1 to 128MB using SIMMs (Single-In-Line Memory Modules). The mainboard has four memory banks — Bank 0, 1, 2, 3. Bank 0, 1, 2 and 3 can accept either a 1MB, 4MB, 16MB or 32MB SIMM in each socket.

### DRAM Configuration

Memory can be installed in a variety of configurations, as shown in the next table:

TOTAL MEMORY	BANK 0 (72-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)	BANK 3 (72-PIN)
1MB	1MB			
		1MB		
			1MB	
2MB	1MB	1MB		
	1MB		1MB	
			1MB	1MB
		1MB	1MB	
3MB	1MB	1MB	1MB	
		1MB	1MB	1MB
	1MB		1MB	1MB
4MB	4MB			
		4MB		
			4MB	
	1MB	1MB	1MB	1MB
5MB	1MB	4MB		
	1MB		4MB	
	4MB	1MB		
	4MB		1MB	
		1MB	4MB	
		4MB	1MB	
6MB	1MB	1MB	4MB	
	1MB	4MB	1MB	
	4MB	1MB	1MB	
		4MB	1MB	1MB
7MB	1MB	4MB	1MB	1MB
	4MB	1MB	1MB	1MB

TOTAL MEMORY	BANK 0 (72-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)	BANK 3 (72-PIN)
8MB	4MB	4MB		
	4MB		4MB	
			4MB	4MB
9MB		4MB	4MB	
	1MB	4MB	4MB	
	4MB	1MB	4MB	
	4MB	4MB	1MB	
		1MB	4MB	4MB
10MB	1MB	1MB	4MB	4MB
	4MB	4MB	1MB	1MB
12MB	4MB	4MB	4MB	
		4MB	4MB	4MB
	4MB		4MB	4MB
13MB	1MB	4MB	4MB	4MB
	4MB	1MB	4MB	4MB
16MB		16MB		
			16MB	
	4MB	4MB	4MB	4MB
17MB	1MB	16MB		
	1MB		16MB	
		1MB	16MB	
		16MB	1MB	
18MB	1MB	1MB	16MB	
	1MB	16MB	1MB	
		16MB	1MB	1MB
19MB	1MB	16MB	1MB	1MB
	4MB	16MB		
20MB	4MB		16MB	
		4MB	16MB	
		16MB	4MB	
21MB	1MB	4MB	16MB	
	1MB	16MB	4MB	
	4MB	1MB	16MB	
	4MB	16MB	1MB	
22MB	4MB	16MB	1MB	1MB
	4MB	4MB	16MB	
24MB	4MB	16MB	4MB	
		16MB	4MB	4MB
25MB	1MB	16MB	4MB	4MB
28MB	4MB	16MB	4MB	4MB
33MB	1MB	16MB	16MB	
		1MB	16MB	16MB
34MB	1MB		16MB	16MB
	1MB	1MB	16MB	16MB

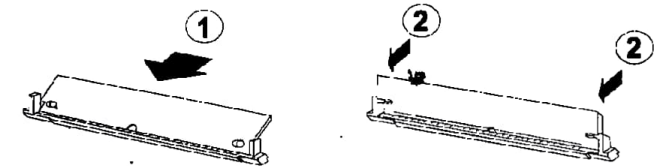
TOTAL MEMORY	BANK 0 (72-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)	BANK 3 (72-PIN)
36MB	4MB	16MB	16MB	
		4MB	16MB	16MB
37MB	1MB	4MB	16MB	16MB
	4MB	1MB	16MB	16MB
40MB	4MB	4MB	16MB	16MB
48MB		16MB	16MB	16MB
49MB	1MB	16MB	16MB	16MB
52MB	4MB	16MB	16MB	16MB
64MB		32MB	32MB	
65MB	1MB	64MB		
	1MB	32MB	32MB	
66MB	1MB	1MB	32MB	32MB
	1MB	32MB	1MB	32MB
	32MB	32MB	1MB	1MB
68MB	4MB	32MB	32MB	
		4MB	32MB	32MB
69MB	32MB	32MB	4MB	
	1MB	4MB	32MB	32MB
	1MB	32MB	4MB	32MB
	4MB	1MB	32MB	32MB
72MB	4MB	32MB	1MB	32MB
	4MB	4MB	32MB	32MB
	32MB	32MB	4MB	4MB
80MB	32MB	16MB	32MB	
	32MB	32MB	16MB	
81MB	1MB	16MB	32MB	32MB
	1MB	32MB	16MB	32MB
84MB	4MB	16MB	32MB	32MB
	4MB	32MB	16MB	32MB
96MB	32MB	32MB	32MB	
97MB	1MB	32MB	32MB	32MB
128MB	32MB	32MB	32MB	32MB

→ NOTE : All banks accept double-RAS SIMM.

## Installation Instructions

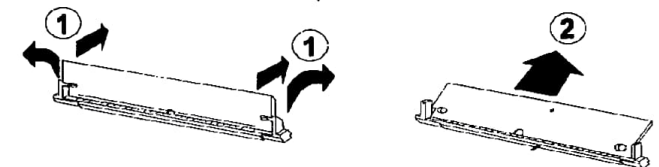
→ NOTE : Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.

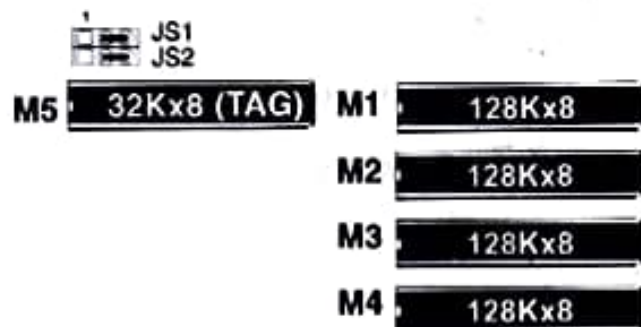
1. Locate the SIMM banks on the mainboard.
2. Insert the SIMM edge connector at a 90-degree angle onto the socket.



3. Carefully push the SIMM down and back into the socket until the retaining clips of the socket snap, holding the SIMM in place. The holes in the SIMM should match the pins on the socket's retaining clips.

To remove the SIMM/s, pull the retaining latch on both ends of the socket and reverse the procedure above.



**512K Cache SRAM****Award BIOS Setup**

The 486-PIO-2 comes with the Award BIOS chip that contains the ROM Setup information of your system. This chip serves as an interface between the processor and the rest of the mainboard's components. This chapter explains the information contained in the Setup program and tells you how to modify the settings according to your system configuration.

**CMOS Setup Utility**

ROM PC15A BIOS (2441870A) CMOS SETUP UTILITY AWARD SOFTWARE, INC.	
STANDARD CMOS SETUP	SUPERVISOR PASSWORD
BIOS FEATURES SETUP	USER PASSWORD
CHIPSET FEATURES SETUP	IDE HDD AUTO DETECTION
POWER MANAGEMENT SETUP	SAVE & EXIT SETUP
PCI CONFIGURATION SETUP	EXIT WITHOUT SAVING
LOAD BIOS DEFAULTS	
LOAD SETUP DEFAULTS	
Esc : Quit	F1 -> : Select Item
F10 : Save & Exit Setup	(Shift) F2 : Change Color
Time, Date, Hard Disk Type	

A Setup program, built into the system BIOS, is stored in the CMOS RAM. This Setup utility program allows changes to the mainboard configuration settings. It is executed when the user changes system configuration; user changes system backup battery; or the system detects a configuration error and asks the user to run the Setup program. After power-on RAM testing, the message "Press DEL to enter SETUP." appears. Use the arrow keys to select and press <Enter> to run the selected program.

**PCI IRQ Activated By**

We suggest that you set this to its default configuration unless you are a qualified technician.

The options are: Level (Default), Edge

**PCI IDE IRQ Map To**

Set "PCI-AUTO" to allow the system BIOS to automatically detect the add-on PCI IDE card interrupt used by the PCI hard disk drive.

The options are: PCI-AUTO (Default), PCI-SLOT1, PCI-SLOT2, PCI-SLOT3, PCI-SLOT4, ISA

**CPU to PCI Write Buffer**

When enabled, allows data and address access to the internal buffer of VT82C505 so that the processor can be released from the wait state.

The options are: Enabled (Default), Disabled

**PCI Master Write Buffer**

When enabled, allows the PCI write operation by informing the processor of pending data from the PCI device. Processor is released from waiting state by a signal from the master card.

The options are: Enabled (Default), Disabled

**PCI Master Prefetch**

When enabled, allows the data and address to be saved in the internal buffer of VT82C505 to reduce master drive access time.

The options are: Enabled (Default), Disabled

**PCI Master 1WS Write**

When enabled, allows one more wait state cycle delays when the PCI master drive writes data to DRAM.

The options are: Enabled, Disabled (Default)

**Interrupt Assignments of PCI Slots**

SLOT	INT OF SLOT	INT OF VT82C505
PCI Slot 1	A	A
	B	B
	C	C
	D	D
PCI Slot 2	A	B
	B	C
	C	D
	D	A
PCI Slot 3	A	C
	B	D
	C	A
	D	B
PCI Slot 4	A	D
	B	A
	C	B
	D	C

**Load BIOS Defaults**

BIOS defaults contain the most appropriate values of the system parameters that allow minimum system performance. The OEM manufacturer may change the defaults through MODBIN before the binary image burns into the ROM.

**Load Setup Defaults**

Selecting this field loads the factory defaults for BIOS and Chipset Features which the system automatically detects.