# 486-GVT

# MAIN BOARD MANUAL

# 486-GVT

## MAIN BOARD
## User's Guide

DOC No. : 13009
Revision : A2
Date : December 1993

**SEAGATE**

| MODEL | CAPACITY | CYLINDER | HEAD | SECTOR |
|---|---|---|---|---|
| ST3144A | 125MB | 1001 | 15 | 17 |
| ST3283A | 245MB | 978 | 14 | 35 |

**WESTERN DIGITAL**

| MODEL | CAPACITY | CYLINDER | HEAD | SECTOR |
|---|---|---|---|---|
| AC2120 | 125MB | 872 | 8 | 35 |
| AC2200 | 200MB | 989 | 12 | 35 |
| AC2250 | 255MB | 1010 | 9 | 55 |
| AC2340 | 341MB | 1010 | 12 | 55 |

**PRIAM**

| MODEL | CAPACITY | CYLINDER | HEAD | SECTOR |
|---|---|---|---|---|
| S19 | 152MB | 1024 | 15 | 17 |



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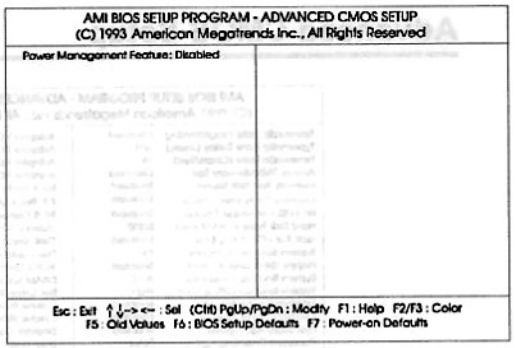
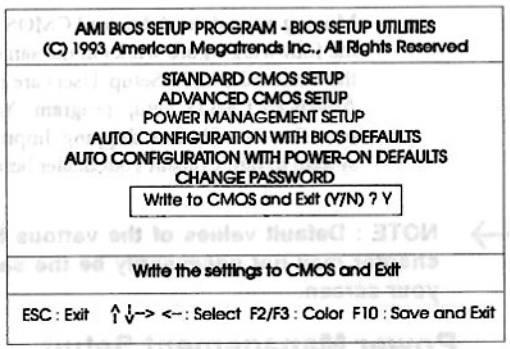
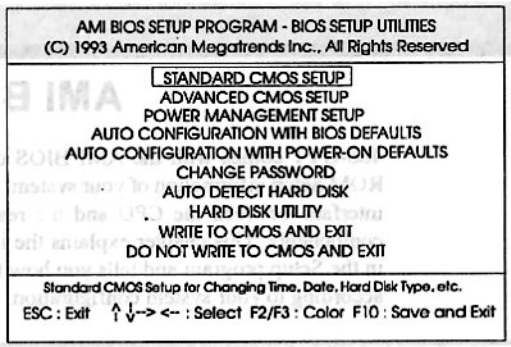



## Write to CMOS and Exit

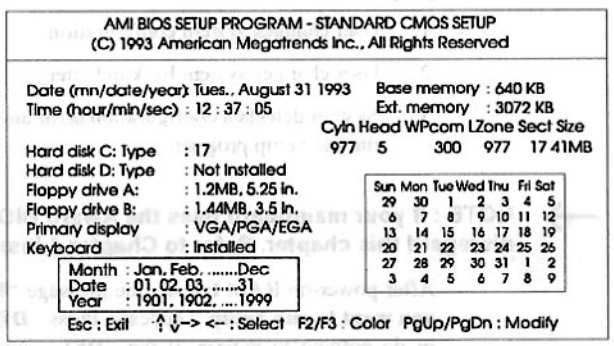



After making the necessary changes under Setup, press "**Esc**" to return to the main menu. Move cursor to "**Write to CMOS and Exit**", and press "**Y**" to change the CMOS Setup. If no changes are made, press "**Esc**" again and press "**Y**" to retain the CMOS settings.




Use the arrow keys to select and press "**Enter**" to run the selected program.

## Standard CMOS Setup




The Setup program is completely menu driven. Use the arrow keys to select an entry; "**PgUp/PgDn**" keys to change an entry; and "**Esc**" key to exit. Help messages are displayed in a window on the screen when "**Alt+F1**" keys are pressed. The Standard CMOS Setup screen is shown above. System BIOS automatically detects memory size, thus no changes are necessary. After the changes are made, press "**Esc**" to exit.





# Overview

Based on an ISA/VL-bus, the 486-GVT mainboard empowers any high-end system to exploit a wide-range of hardware and software capabilities and applications. This chapter gives you a brief overview of this mainboard, providing basic information on its major parts and components.

## Specifications

The 486-GVT mainboard comes with the following features:

- Intel 80486SX/DX/DX2/P24T/80486S-series/ CX486S™ dual CPU microprocessor in PQFP and PGA packages.
- VIA VT82C486 80486/80386 PC/AT chipset includes built-in 8042 keyboard controller.
- Supports 64/128/256K direct-mapped write-back/write-through cache memory.
- DuPont 30 and 72-pin SIMM sockets supports 1 up to 96MB DRAM for 486 system, provides page mode DRAM operation.
- Supports system and video BIOS cacheable and shadow.
- Supports decoupled DRAM refresh.
- Provides built-in power management features ideal for Green PCs.
- Optional built-in ZIF socket that accepts Intel's OverDrive™ processors or Pentium™ OverDrive™ processor.
- 64KB BIOS.
- One 8-bit and six 16-bit ISA expansion slots.
- Supports two VESA bus slots for Local bus master or slave.
- Real time clock/calendar.

This message indicates that the password is cleared. Remove Jumper J7 and reset the system. At this point, you will not be asked for the password to enter Setup.

## Exiting Setup

| ROM ISA BIOS (VIA00000)<br>CMOS SETUP UTILITY<br>AWARD SOFTWARE, INC. | |
|---|---|
| STANDARD CMOS SETUP | PASSWORD SETTING |
| BIOS FEATURES SETUP | IDE HDD AUTO DETECTION |
| CHIPSET FEATURES SETUP | HDD LOW LEVEL FORMAT |
| POWER MANAGEMENT SETUP | SAVE AND EXIT SETUP |
| LOAD BIOS DEFAULTS | EXIT WITHOUT SAVING |
| LOAD SETUP | SAVE to CMOS and EXIT (Y/N)? Y |
| ESC : Quit | ↑↓-> <- : Select Item |
| F10 : Save and Exit | (Shift) F2 : Color |
| Time, Date, Hard Disk Type | |

After you have made changes under Setup, press "**Esc**" to return to the main menu. Move cursor to "**Save and Exit Setup**" or press "**F10**" and then press "**Y**" to change the CMOS Setup. If you did not change anything, press "**Esc**" again or move cursor to "**Exit Without Saving**" and press "**Y**" to retain the Setup settings.

→ **NOTE : Default values of the various Setup items on this chapter may not necessarily be the same ones shown on your screen.**





## System Block Diagram

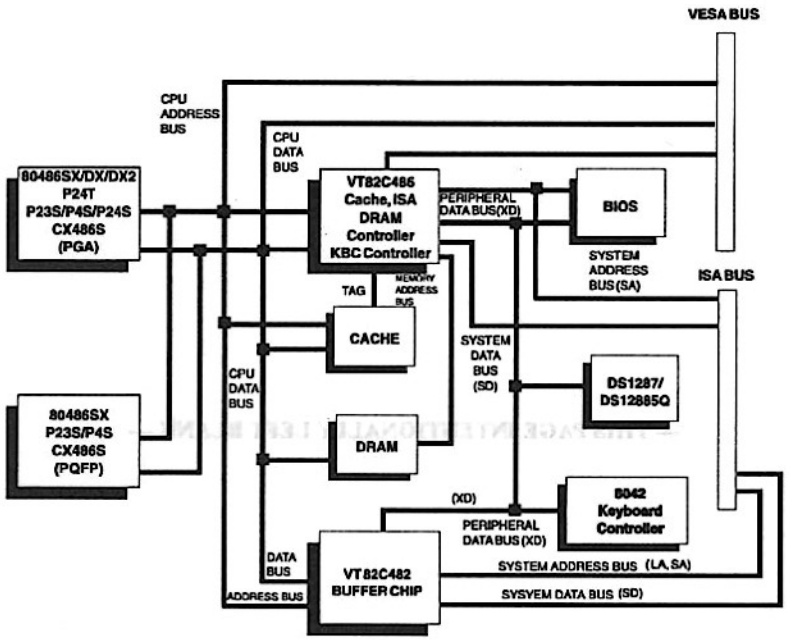



*Figure 1-2. System Block Diagram*

ROM ISA BIOS (VIA00000)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

| | |
|---|---|
| Decoupled Refresh | : Enabled |
| Relocate 256K/384K | : Disabled |
| Video BIOS Cacheable | : Enabled |
| System BIOS Cacheable | : Enabled |
| External Cache Scheme | : Write Back |
| Cache Timing Control | : Turbo |
| DRAM Timing Control | : Fast |
| Fast DRAM Write | : Enabled |
| Burst Write | : Disabled |
| CPU Write Back Cache | : Disabled |

Esc : Quit
F1 : Help
F5 : Old Values
F6 : Load BIOS Defaults
F7 : Load Setup Defaults
↑↓–> <– : Select Item
PgUp/PgDn/+/- : Modify
(Shift) F2 : Change Color

## Power Management Setup

ROM ISA BIOS (VIA00000)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.

| | |
|---|---|
| Power Management | : Disabled |

Esc : Quit
F1 : Help
F5 : Old Values
F6 : Load BIOS Defaults
F7 : Load Setup Defaults
↑↓–> <– : Select Item
PgUp/PgDn/+/- : Modify
(Shift) F2 : Change Color

→ **NOTE : Pressing "Ctrl+Alt+8" will invoke the Power Management Feature when "Enabled" while pressing "Ctrl+Alt+Backspace" will restore the system with normal display.**





# Mainboard Settings

486-GVT has several user-adjustable jumpers and connectors on the board that allow you to configure your system to suit your every need. This chapter contains information on the various jumper and connector settings you can make on your mainboard.

## Jumpers

Jumpers are used to select the operation modes for your system. Each jumper on the board has three metal pins with each pin representing a different function. To "set" a jumper, a black cap containing metal contacts is placed over the jumper pin/s according to the required configuration. A jumper is said to be "shorted" when the black cap has been placed on one or two of its pins, as shown in the figure below:

*Figure 2 - 1 Jumper with Pins Shorted*

### CPU Selector Jumpers

To allow your system to be used with a variety of CPU's, 486-GVT provides ten jumpers that can be set according to the CPU you want installed. Follow the diagrams found in the lower-middle area of the board to determine the proper arrangement for the CPU you are using.

The next two table summarizes the settings of the CPU Selector jumpers.

| ROM ISA BIOS (VIA00000)<br>CMOS SETUP UTILITY<br>AWARD SOFTWARE, INC. | |
|---|---|
| STANDARD CMOS SETUP | PASSWORD SETTING |
| BIOS FEATURES SETUP | IDE HDD AUTO DETECTION |
| CHIPSET FEATURES SETUP | HDD LOW LEVEL FORMAT |
| POWER MANAGEMENT SETUP | SAVE AND EXIT SETUP |
| LOAD BIOS DEFAULTS | EXIT WITHOUT SAVING |
| LOAD SETUP DEFAULTS | |
| ESC : Quit | ↑↓--> <-- : Select Item |
| F10 : Save and Exit | (Shift) F2 : Color |
| Time, Date, Hard Disk Type | |

Use the arrow keys to select and press "**ENTER**" to run the selected program.

## Standard CMOS Setup

The Standard CMOS Setup has ten items for setting. Each item may have one or more option settings. Use the arrow keys to highlight the item and then use the **<PgUp>**, or **<PgDn>** keys to select the value you want in each item.

ROM ISA BIOS (VIA00000)
STANDARD CMOS SETUP
AWARD SOFTWARE, INC.

Date (mm: dd: yy) : Tues., August 31 1993
Time (hh: mm: ss) : 12 : 37 : 05
DAYLIGHT SAVING : Disabled

| | CYLS. | HEADS | PRECOMP | LANDZONE | SECTORS |
|---|---|---|---|---|---|
| Drive C: User (81MB) : | 611 | 16 | 0 | 0 | 17 |
| Drive D: None ( 0MB) : | 0 | 0 | 0 | 0 | 0 |

Drive A : 1.2MB, 5.25 in.
Drive B : 1.44MB, 3.5 in.
Video : EGA/VGA

| | |
|---|---|
| Base Memory | : 640K |
| Extended Memory | : 7168K |
| Expanded Memory | : 0K |
| Other Memory | : 384K |
| Total Memory | : 8192K |

Halt on : All Errors

Esc : Quit ↑↓--> <-- : Select Item PgUp/PgDn/+/- : Modify
F1 : Help (Shift) F2 : Change Color F3 : Toggle Calendar





| JUMPER | PIN DEFINITION |
|---|---|
| J2 | External, Internal Battery Select<br>1-2 External battery<br>2-3 Internal battery |
| J4 | Display Type Select<br>Open Mono/EGA/VGA (default)<br>Close Color |
| J7 | Password Clear (Award/AMI BIOS Select)<br>1-2 Award BIOS<br>2-3 AMI BIOS |
| JC6 | 80486SX/P23S/P4S/CX486S PQFP Select<br>Short Disable on-board<br>Open Enable |
| JCX1 | CPU Type Select<br>Short CX486S<br>Open Intel S-series CPU |
| JKB1, JKB2, JKB3, JKB4, JX3 | Internal/External Keyboard Select<br>1-2 External keyboard<br>2-3 Internal keyboard |
| JX1 | CPU Clock Select<br>1-2 1 X<br>2-3 2 X |
| JX2, J8 | 1-2 IRQ15<br>2-3 -SMI |

*Table 2-2. Jumper Definitions*

### 256K Cache SRAM


The cache size is jumper selectable. M1 - M4 are assigned as Bank 0 and M6 - M9 are assigned as Bank 1.

| | 64K | 128K | 256K |
|---|---|---|---|
| Bank 0 | 8K x 8 | 32K x 8 | 32K x 8 |
| Bank 1 | 8K x 8 | Empty | 32K x 8 |
| Tag RAM (M5) | 8K x 8 | 8K x 8 | 32K x 8 |
| JS1 (Jumper) | 1-2 | 1-2 | 2-3 |
| JS2 (Jumper) | 1-2 | 2-3 | 2-3 |
| JS3 (Jumper) | 1-2 | 2-3 | 1-2 |

*Table 3-2. Cache Configuration Size*





## Connectors

The connectors allow the mainboard to connect electronically with other parts of the system. Some connectors have two pins, others have four or five pins. The next table gives the functions of each connector. Some malfunction problems encountered with your system may be caused by loose or improper connection. Ensure that the all connections are in place and firmly attached.

| CONNECTOR | PIN OUTS | SIGNAL NAME |
|---|---|---|
| CN1<br>Keyboard Connector | 1<br>2<br>3<br>4<br>5 | Keyboard clock<br>Keyboard data<br>NC<br>Ground<br>+5V |
| CN2<br>Power Connector | 1<br>2, 10, 11, 12<br>3<br>4<br>5, 6, 7, 8<br>9 | Power good<br>+5V<br>+12V<br>–12V<br>Ground<br>–5V |
| J1<br>External Battery Connector | 1<br>2, 3<br>4 | Anode+<br>NC<br>Cathode – |
| J9<br>Turbo LED | 1<br>2 | VCC<br>LED |
| J10<br>Turbo Switch | 1<br>2 | Turbo Signal<br>Ground |
| J11<br>Hardware Reset | 1<br>2 | Ground<br>Reset signal |
| J12<br>Speaker Connector | 1<br>2<br>3<br>4 | Speaker signal<br>NC<br>Ground<br>+5V |

*Table 2-5. Connector Pin Definitions (Continued)*

3. Carefully push the SIMM down and back into the socket until the retaining clips of the socket snap, holding the SIMM in place. The holes in the SIMM should match the pins on the socket's retaining clips.

To remove the SIMM/s, pull the retaining latch on both ends of the socket and reverse the procedure above.

## Cache Memory

The 486-GVT can accept cache memory of 64, 128 or 256KB.

→ **NOTE : Be sure to use the correct chips for the amount of cache memory you want to add. You must install both the correct Cache and Tag SRAM.**
**Alter RAM type is always the same as Tag RAM.**

## Installing Cache Memory

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the beginning of this manual.**

If you do not have the confidence to make the installation, better consult a service technician for assistance.

1. Locate the cache memory on the mainboard. See Figure 3-1 again.
2. Be guided by the Cache SRAM settings depending on your desired SRAM configuration:

Correct orientation of the chips is necessary for the cache to operate properly. Normally, the chips have either a curved notch or a dot. This marker on the chip must be matched to the marker on the socket for correct alignment.

Install the chips individually as follows:

3. Align the chip with the marker on the socket. Press the chip onto the socket, ensuring that the pins on the chip are aligned with the corresponding connections on the socket.





| CONNECTOR | SIDE A - PINS AND PIN OUTS | | SIDE B - PINS AND PIN OUTS | |
|---|---|---|---|---|
| SL14 — Local Bus | 01 | DAT01 | 01 | DAT00 |
| | 02 | DAT03 | 02 | DAT02 |
| | 03, 10, 17, 24, 35, 43, 51 | Ground | 03 | DAT04 |
| | 04 | DAT05 | 04 | DAT06 |
| | 05 | DAT07 | 05 | DAT08 |
| | 06 | DAT09 | 06, 14, 22, 29, 38, 49, 55 | Ground |
| | 07 | DAT11 | 07 | DAT10 |
| | 08 | DAT13 | 08 | DAT12 |
| | 09 | DAT15 | 09, 20, 32, 57 | VCC |
| | 11 | DAT17 | 10 | DAT14 |
| | 12, 27, 40, 53 | VCC | 11 | DAT16 |
| | 13 | DAT19 | 12 | DAT18 |
| | 14 | DAT21 | 13 | DAT20 |
| | 15 | DAT23 | 15 | DAT22 |
| | 16 | DAT25 | 16 | DAT24 |
| | 18 | DAT27 | 17 | DAT26 |
| | 19 | DAT29 | 18 | DAT28 |
| | 20 | DAT31 | 19 | DAT30 |
| | 21 | ADR30 | 21 | ADR31 |
| | 22 | ADR28 | 23 | ADR29 |
| | 23 | ADR26 | 24 | ADR27 |
| | 25 | ADR24 | 25 | ADR25 |
| | 26 | ADR22 | 26 | ADR23 |
| | 28 | ADR20 | 27 | ADR21 |
| | 29 | ADR18 | 28 | ADR19 |
| | 30 | ADR16 | 30 | ADR17 |
| | 31 | ADR14 | 31 | ADR15 |
| | 32 | ADR12 | 33 | ADR13 |
| | 33 | ADR10 | 34 | ADR11 |
| | 34 | ADR08 | 35 | ADR09 |
| | 36 | ADR06 | 36 | ADR07 |
| | 37 | ADR04 | 37 | ADR05 |
| | 38 | WBACK# | 39 | ADR03 |
| | 39 | BE0# | 40 | ADR02 |
| | 41 | BE1# | 41 | NC |
| | 42 | BE2# | 42 | RESET# |
| | 44 | BE3# | 43 | D/C# |
| | 45 | ADS# | 44 | M/IO# |
| | 48 | LRDY# | 45 | W/R# |
| | 49 | LDEV1# | 48 | RDYRTN# |
| | 50 | LREQ# | 50 | IRQ9 |
| | 52 | LGNT# | 51 | BRDY# |
| | 54, 55, 56 | ID2, 3, 4 | 52 | BLAST# |
| | 57 | LKEN# | 53, 54 | ID0, 1 |
| | 58 | LEADS# | 56 | LCLK1 |
| | | | 58 | LBS16# |

*Table 2-6. Local Bus Connector Pin Assignment (Continued)*

| TOTAL MEMORY | BANK 0 (30-PIN) | BANK 1 (72-PIN) | BANK 2 (72-PIN) |
|---|---|---|---|
| 21MB | 256K x 4 | 4M x 1 | 16M x 1 |
| | 256K x 4 | 16M x 1 | 4M x 1 |
| | 1M x 4 | 1M x 1 | 16M x 1 |
| | 1M x 4 | 16M x 1 | 1M x 1 |
| | 4M x 4 | 1M x 1 | 4M x 1 |
| | 4M x 4 | 4M x 1 | 1M x 1 |
| 24MB | 1M x 4 | 4M x 1 | 16M x 1 |
| | 1M x 4 | 16M x 1 | 4M x 1 |
| | 4M x 4 | 4M x 1 | 4M x 1 |
| 32MB | 4M x 4 | 16M x 1 | |
| | 4M x 4 | | 16M x 1 |
| | | 16M x 1 | 16M x 1 |
| 33MB | 256K x 4 | 16M x 1 | 16M x 1 |
| | 4M x 4 | 1M x 1 | 16M x 1 |
| | 4M x 4 | 16M x 1 | 1M x 1 |
| 36MB | 1M x 4 | 16M x 1 | 16M x 1 |
| | 4M x 4 | 4M x 1 | 16M x 1 |
| | 4M x 4 | 16M x 1 | 4M x 1 |
| 48MB | 4M x 4 | 16M x 1 | 16M x 1 |
| 64MB | 16M x 4 | | |
| 65MB | 16M x 4 | 1M x 1 | |
| | 16M x 4 | | 1M x 1 |
| 66MB | 16M x 4 | 1M x 1 | 1M x 1 |
| 68MB | 16M x 4 | 4M x 1 | |
| | 16M x 4 | | 4M x 1 |
| 69MB | 16M x 4 | 1M x 1 | 4M x 1 |
| | 16M x 4 | 4M x 1 | 1M x 1 |
| 72MB | 16M x 4 | 4M x 1 | 4M x 1 |
| 80MB | 16M x 4 | 16M x 1 | |
| | 16M x 4 | | 16M x 1 |

*Table 3-1. DRAM Configurations (Continued)*



Chapter 3

# Memory Subsystem

486-GVT can be equipped with the memory necessary for running all your applications. Memory comes in the form of DRAM (SIMMs) and cache SRAM. This chapter describes these two kinds of memory and gives instructions on how to install each kind on the mainboard.

## Memory Locations

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:

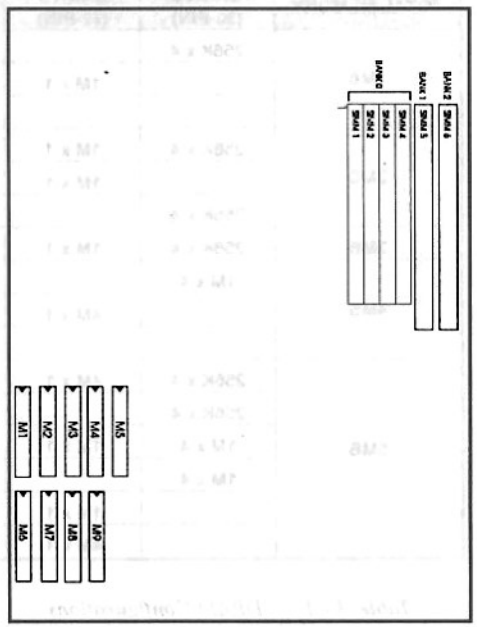



*Figure 3-1. Cache and Memory Locations*

# HANDLING PRECAUTIONS

→ **Static electricity may cause damage to the integrated circuits on the mainboard. Before handling any mainboard outside of its protective packaging, ensure that there is no static electric charge in your body.**

Observe any or all of these basic precautions when handling the mainboard or other computer components:

- Wear a static wrist strap which fits around your wrist and is connected to a natural earth ground.
- Touch a grounded or anti-static surface or a metal fixture such as a water pipe.
- Avoid contact with the components on add-on cards, boards and modules and with the "golden finger" connectors plugged into the expansion slot. It is best to handle system components by their mounting bracket.

Above methods either prevent static build-up or cause it to be discharged properly.

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# Hard Disk Specifications

This appendix contains some technical information about the different IDE hard disk drives which can be installed with your 486-GVT mainboard.

**CONNER**

| MODEL | CAPACITY | CYLINDER | HEAD | SECTOR |
|---|---|---|---|---|
| CP-30104 | 120MB | 762 | 8 | 39 |
| CP-30174 | 170MB | 903 | 8 | 46 |
| CP-30204 | 203MB | 684 | 16 | 38 |
| CP-30254 | 251MB | 895 | 10 | 55 |
| CP-30344 | 343MB | 904 | 16 | 46 |
| CP-30364 | 360MB | 702 | 16 | 63 |
| CP-30544 | 544MB | 1024 | 16 | 63 |

**MAXTOR**

| MODEL | CAPACITY | CYLINDER | HEAD | SECTOR |
|---|---|---|---|---|
| 7120A | 120MB | 1023 | 14 | 17 |
| 2190 | 152MB | 1024 | 15 | 17 |
| 7170A | 170MB | 984 | 10 | 34 |
| 7213A | 213MB | 683 | 16 | 38 |
| 7245A | 245MB | 967 | 16 | 31 |
| 7345A | 345MB | 790 | 15 | 57 |

**QUANTUM**

| MODEL | CAPACITY | CYLINDER | HEAD | SECTOR |
|---|---|---|---|---|
| LPS120AT | 120MB | 901 | 5 | 53 |
| LPS240AT | 240MB | 723 | 13 | 51 |
| ELS127AT | 127MB | 919 | 16 | 17 |
| ELS170AT | 170MB | 1011 | 15 | 22 |

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## Advanced CMOS Setup

AMI BIOS SETUP PROGRAM - ADVANCED CMOS SETUP
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| | | | |
|---|---|---|---|
| Typematic Rate Programming | : Disabled | Adaptor ROM Shadow C800, 32K | : Disabled |
| Typematic Rate Delay (msec) | : 500 | Adaptor ROM Shadow D000, 32K | : Disabled |
| Typematic Rate (Chars/Sec) | : 15 | Adaptor ROM Shadow D800, 32K | : Disabled |
| Above 1MB Memory Test | : Disabled | Adaptor ROM Shadow E000, 64K | : Disabled |
| Memory Test Tick Sound | : Enabled | Boot Sector Virus Protection | : Enabled |
| Memory Parity Error Check | : Enabled | IDE Block Mode Transfer | : Disabled |
| Hit <DEL> Message Display | : Enabled | BIOS Cacheable Option | : Enabled |
| Hard Disk Type 47 RAM Area | : D.300 | Video Cacheable Option | : Enabled |
| Wait For <F1> If Any Error | : Enabled | 256K Relocate Option | : Disabled |
| System Boot Up NumLock | : On | Decouple Refresh | : Enabled |
| Floppy Drive Seek At Boot | : Enabled | AUTO Config Option | : Enabled |
| System Boot Up Sequence | : A: C: | DRAM Speed Select | : 0 W/S |
| System Boot Up CPU Speed | : High | Bus Clock Rate Select | : CLK2/1.5 |
| External Cache Memory | : Enabled | Cache Read Cycle Select | : 0 W/S |
| Internal Cache Memory | : Enabled | Cache Write Cycle Select | : 0 W/S |
| Fast Gate A20 Option | : Enabled | External Cache Scheme | : W/BACK |
| Password Checking Option | : Setup | Burst Write | : Disabled |
| Video ROM Shadow C000, 32K | : Enabled | CPU Write Back Cache | : Disabled |

Esc : Exit ↑↓→← : Sel (Ctrl) PgUp/PgDn : Modify F1 : Help F2/F3 : Color
F5 : Old Values F6 : BIOS Setup Defaults F7 : Power-on Defaults

Moving around the Advanced CMOS Setup program shown in the following figure works in the same way as moving around the Standard CMOS Setup. Users are not encouraged to run the Advanced CMOS Setup program. Your system should have been fine-tuned before shipping. Improper Setup may cause the system to fail. Consult your dealer before making any changes.

→ **NOTE : Default values of the various Setup items on this chapter may not necessarily be the same ones shown on your screen.**

## Power Management Setup

→ **NOTE : Pressing "Ctrl+Alt+8" will invoke the Power Management Feature when "Enabled" while pressing "Ctrl+Alt+Backspace" will restore the system with normal display.**

## Mainboard Layout

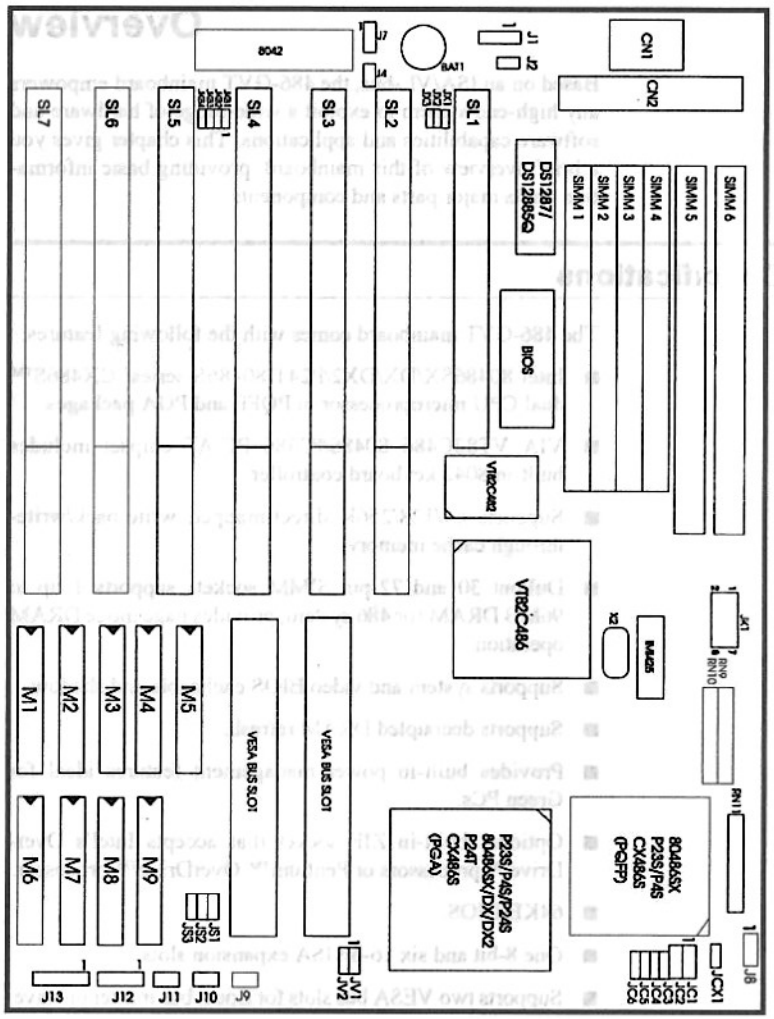



*Figure 1-1. Mainboard Layout*



Chapter 5

# AMI BIOS Setup

486-GVT comes with the AMI BIOS chip that contains the ROM Setup information of your system. This chip serves as an interface between the CPU and the rest of the mainboard's components. This chapter explains the information contained in the Setup program and tells you how to modify the settings according to your system configuration.

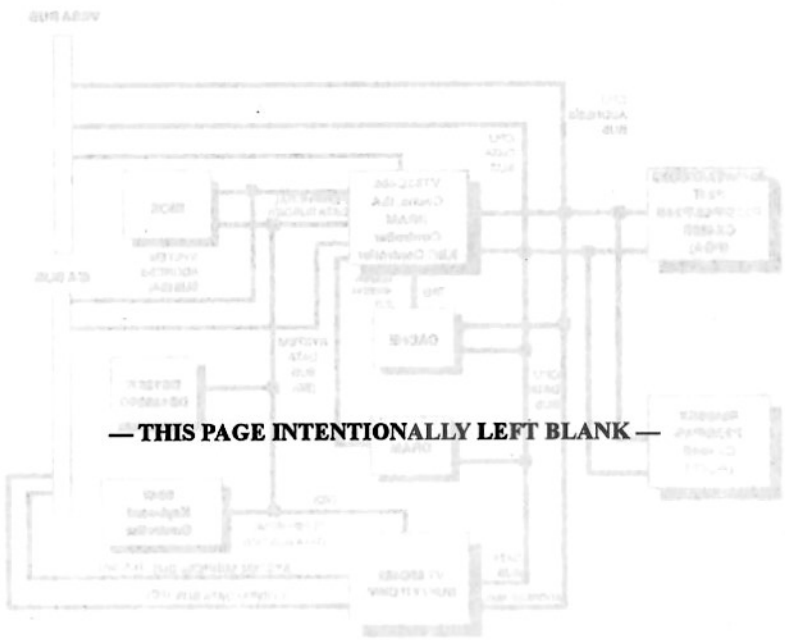
## System Setup

A Setup program has been built into the system BIOS so that configurations stored in the CMOS RAM can be changed. This program is executed when:

1. User changes system configuration.
2. User changes system backup battery.
3. System detects a configuration error and asks the user to run the Setup program.

→ **NOTE : If your mainboard uses the Award BIOS chip, disregard this chapter. Refer to Chapter 4 instead.**

After power-on RAM testing, the message **"Press <DEL> if you want to run Setup."** appears. Press "**DEL**" to run setup or do nothing to bypass. If the "**DEL**" key is pressed, the following screen is displayed:



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## Load BIOS Default

BIOS defaults contain the most appropriate values of the system parameters that allow minimum system performance. The OEM manufacturer may change the defaults through MODBIN before the binary image burns into the ROM.

## Load Setup Default

Selecting this field loads the factory defaults for BIOS and Chipset Features which the system automatically detects.

## Password Setting

When you select this function, you can create a password. Type your password up to eight characters and press **<Enter>**. You will be asked to confirm the password. Type the password again and press **<Enter>**. You may also press **<Esc>** to abort the selection and not enter a password. To disable password, press **<Enter>** when you are prompted to enter password. A message appears, confirming the password is disabled. When the password is disabled, the system boot and you can enter Setup freely.

### Security Option

If you select **System** under this field, you will be prompted for the password every time system is rebooted or any time you try to enter Setup. If you select Setup, you will be prompted only when you try to enter Setup.

### Clear Password

If you forget your password, turn off the system power first and remove the system unit cover. Locate Jumper J7 and cap it. Turn the system power back on and screen will display the message below:

**PASSWORD IS SET DISABLED**
**PLEASE REMOVE JUMPER (J7) BEFORE**
**SETTING UP NEW PASSWORD**

| JUMPER | 486SX/P23S (PGA) | P24S/P4S/ 486DX/DX2 (PGA) | P24T (PGA) | CX486S (M6) (PGA) | CX486DX (M7) CX486S+CX487S (M6+C6) (PGA) |
|---|---|---|---|---|---|
| JC1 | 2-3 short | 1-2 short | 1-2 short | 2-3 short | 1-2 short |
| JC2 | 2-3 short | 1-2 short | 1-2 short | 2-3 short | 1-2 short |
| JC3 | open | short | open | short | short |
| JC4 | open | open | short | open | open |
| JC5 | short | short | open | open | open |

| JUMPER | P23S/P4S/P24S (PGA) | 486DX/DX2/SX (PGA) | CX486S CX486S+CX487S CX486DX (M6, M6+C6, M7) (PGA) | P23S/P4S/ CX486S (PQFP) |
|---|---|---|---|---|
| RN9 (10p5R 0 ohm) | empty | empty | inserted | empty |
| RN10 (10p5R 0 ohm) | inserted | empty | empty | empty |
| RN11 (8p4R 0 ohm) | empty | empty | empty | inserted |

*Table 2-1. Jumper Settings for CPU Selector*

→ **NOTE : Users are not encouraged to change the non-specified jumper settings as they are considered factory defaults which may adversely affect system performance.**





The Standard CMOS Setup screen is displayed above. System BIOS automatically detects memory size, thus no changes are necessary. Press "**F3**" function key to show the calendar.

### Daylight Saving

When enabled, this field allows user to set the clock one hour in advance. When disabled, it subtracts one hour when standard time begins. After the changes are made, press "**Esc**" to return to main menu.

## BIOS Features Setup

```
                    ROM ISA BIOS (VIA00000)
                  BIOS FEATURES SETUP
                AWARD SOFTWARE, INC.

Virus Warning                : Enabled     System BIOS Shadow     : Enabled
CPU Internal Cache           : Enabled     Video BIOS Shadow      : Enabled
External Cache               : Enabled     C8000-CBFFF Shadow     : Disabled
Quick Power-On Self-Test     : Disabled    CC000-CFFFF Shadow     : Disabled
Boot Sequence                : A:, C:      D000-D3FFF Shadow      : Disabled
Boot Up Floppy Seek          : Enabled     D4000-D7FFF Shadow     : Disabled
Boot Up Numlock Status       : On          D8000-DBFFF Shadow     : Disabled
Boot Up System Speed         : High        DC000-DFFFF Shadow     : Disabled
IDE HDD Block Mode           : Disabled    E0000-E3FFF Shadow     : Disabled
Gate A20 Option              : Fast        E4000-E7FFF Shadow     : Disabled
Memory Parity Check          : Enabled     E8000-EBFFF Shadow     : Disabled
Typematic Rate Setting       : Disabled    EC000-EFFFF Shadow     : Disabled
Typematic Rate (Chars/Sec)   : 6
Typematic Delay (Msec)       : 250         Esc : Quit             ↑↓--> <--: Select Item
Security Option              : Setup       F1 : Help              PgUp/PgDn/+/- : Modify
                                           F5 : Old Values        (Shift) F2 : Change Color
                                           F6 : Load BIOS Defaults
                                           F7 : Load Setup Defaults
```

## Chipset Features Setup

Moving around the BIOS and Chipset Features Setup programs shown above works the same way as moving around the Standard CMOS Setup program. Users are not encouraged to run the BIOS and Chipset Features Setup programs. Your system should have been fine-tuned before shipping. Improper Setup may cause the system to fail, consult your dealer before making any changes.

## IMISC425 (OSC2) CPU Clock (JK1)

| CLK | 1-2 | 3-4 | 5-6 | 7-8 |
|---|---|---|---|---|
| 80 MHz | Short | Short | Open | Short |
| 66.6 MHz | Open | Short | Open | Short |
| | Short | Open | Open | Short |
| 50 MHz | Open | Open | Short | Short |
| | Open | Short | Open | Open |
| 40 MHz | Short | Open | Short | Short |
| | Short | Short | Open | Open |
| 33.3 MHz | Short | Open | Open | Open |
| 25 MHz | Open | Open | Short | Open |

*Table 2-3. IMISC425 CPU Clock Jumper Selection (JK1)*

## VIA VT 8225 (OSC2) CPU Clock (JK1)

| CLK | 1-2 | 3-4 | 5-6 | 7-8 |
|---|---|---|---|---|
| 100 MHz | Open | Short | Open | Short |
| 80 MHz | Open | Open | Short | Short |
| 66.6 MHz | Short | Short | Open | Short |
| 50 MHz | Short | Open | Short | Short |
| | Open | Short | Open | Open |
| 40 MHz | Open | Open | Short | Open |
| | Open | Short | Short | Short |
| 33.3 MHz | Short | Short | Open | Open |
| 25 MHz | Short | Open | Short | Open |

*Table 2-4. VIA VT 8225 CPU Clock Jumper Selection (JK1)*





# Award BIOS Setup

486-GVT comes with the Award BIOS chip that contains the ROM Setup information of your system. This chip serves as an interface between the CPU and the rest of the mainboard's components. This chapter explains the information contained in the Setup program and tells you how to modify the settings according to your system configuration.

## System Setup

A Setup program, built into the system BIOS, is stored in the CMOS RAM that allows the configuration settings to be changed. This program is executed when:

1. User changes system configuration.
2. User changes system backup battery.
3. System detects a configuration error and asks the user to run the Setup program.

→ **NOTE : If your mainboard uses the AMI BIOS chip, disregard this chapter. Refer to Chapter 5 instead.**

After power-on RAM testing, the message **"TO ENTER SETUP BEFORE BOOT, PRESS CTRL-ALT-ESC"** or **<DEL>** key appears. The following screen appears:

| CONNECTOR | PIN OUTS | SIGNAL NAME |
|---|---|---|
| J13<br>Keylock and Power LED<br>Connector | 1<br>2<br>3, 5<br>4 | Power signal<br>Spare<br>Ground<br>Keylock |

*Table 2-5. Connector Pin Definitions*

## VESA Bus Connector

The cache system board provides two high-performance VESA bus connectors, SL14 and SL15, for use with VESA peripherals. These connectors can be utilized for Local bus (SL14) and (SL15).

→ **NOTE : The two VESA Local Bus slot can accommodate either one VESA Master with one VESA Slave or two VESA Slaves.**

The following tables give the pin assignments for SL14 and SL15. Side A of the connector are pin outs on the board's component side while Side B are pin outs on the board's solder side. Jumpers JV1 and JV2 give more information on settings on the mainboard and the VL-bus controller.

| JUMPER | PIN DEFINITION |
|---|---|
| JV1 | CPU Speed Select<br>1-2 Greater than 33 MHz<br>2-3 Less than or equal to 33 MHz |
| JV2 | High Speed Write<br>1-2 One wait write<br>2-3 Zero wait write (default) |





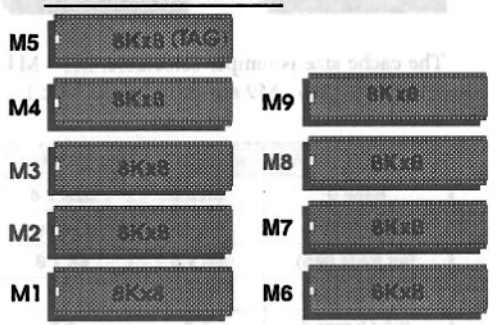
4. Carefully apply enough pressure to partially seat the chip into the socket.

Ensure that all pins are properly aligned with the connectors and that there are no bent pins. If there are any bent pins, remove the chip, straighten the pin and repeat the process.

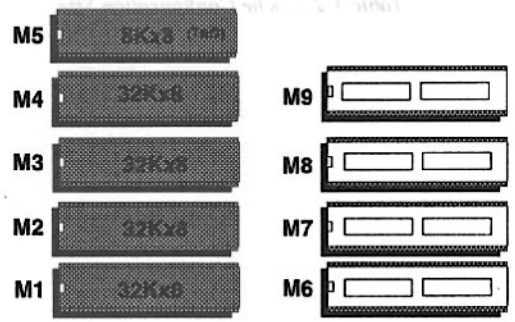
5. Press the chip completely into the socket so that the pins are properly seated.

## Cache SRAM Specifications and Settings

### 64K Cache SRAM




### 128K Cache SRAM



| CONNECTOR | SIDE A - PINS AND PIN OUTS | | SIDE B - PINS AND PIN OUTS | |
|---|---|---|---|---|
| SL15 — Local Bus | 01 | DAT01 | 01 | DAT00 |
| | 02 | DAT03 | 02 | DAT02 |
| | 03, 10, 17, 24, 35, 43, 51 | Ground | 03 | DAT04 |
| | 04 | DAT05 | 04 | DAT06 |
| | 05 | DAT07 | 05 | DAT08 |
| | 06 | DAT09 | 06, 14, 22, 29, 38, 49, 55 | Ground |
| | 07 | DAT11 | 07 | DAT10 |
| | 08 | DAT13 | 08 | DAT12 |
| | 09 | DAT15 | 09, 20, 32, 57 | VCC |
| | 11 | DAT17 | 10 | DAT14 |
| | 12, 27, 40, 53 | VCC | 11 | DAT16 |
| | 13 | DAT19 | 12 | DAT18 |
| | 14 | DAT21 | 13 | DAT20 |
| | 15 | DAT23 | 15 | DAT22 |
| | 16 | DAT25 | 16 | DAT24 |
| | 18 | DAT27 | 17 | DAT26 |
| | 19 | DAT29 | 18 | DAT28 |
| | 20 | DAT31 | 19 | DAT30 |
| | 21 | ADR30 | 21 | ADR31 |
| | 22 | ADR28 | 23 | ADR29 |
| | 23 | ADR26 | 24 | ADR27 |
| | 25 | ADR24 | 25 | ADR25 |
| | 26 | ADR22 | 26 | ADR23 |
| | 28 | ADR20 | 27 | ADR21 |
| | 29 | ADR18 | 28 | ADR19 |
| | 30 | ADR16 | 30 | ADR17 |
| | 31 | ADR14 | 31 | ADR15 |
| | 32 | ADR12 | 33 | ADR13 |
| | 33 | ADR10 | 34 | ADR11 |
| | 34 | ADR08 | 35 | ADR09 |
| | 36 | ADR06 | 36 | ADR07 |
| | 37 | ADR04 | 37 | ADR05 |
| | 38 | WBACK# | 39 | ADR03 |
| | 39 | BE0# | 40 | ADR02 |
| | 41 | BE1# | 41 | NC |
| | 42 | BE2# | 42 | RESET# |
| | 44 | BE3# | 43 | D/C# |
| | 45 | ADS# | 44 | M/IO# |
| | 48 | LRDY# | 45 | W/R# |
| | 49 | LDEV0# | 48 | RDYRTN# |
| | 50 | LREQ# | 50 | IRQ9 |
| | 52 | LGNT# | 51 | BRDY# |
| | 54, 55, 56 | ID2, 3, 4 | 52 | BLAST# |
| | 57 | LKEN# | 53, 54 | ID0, 1 |
| | 58 | LEADS# | 56 | LCLK0 |
| | | | 58 | LBS16# |

*Table 2-6. Local Bus Connector Pin Assignment*





| TOTAL MEMORY | BANK 0 (30-PIN) | BANK 1 (72-PIN) | BANK 2 (72-PIN) |
|---|---|---|---|
| 81MB | 16M x 4 | 1M x 1 | 16M x 1 |
| | 16M x 4 | 16M x 1 | 1M x 1 |
| 84MB | 16M x 4 | 4M x 1 | 16M x 1 |
| | 16M x 4 | 16M x 1 | 4M x 1 |
| 96MB | 16M x 4 | 16M x 1 | 16M x 1 |

*Table 3-1. DRAM Configurations*

## Installation Instructions

**NOTE : Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.**

Assuming the 486-GVT has been mounted on your computer system unit, follow the instructions below:

1. Locate the SIMM banks on the mainboard. Determine your desired configuration to be installed.
2. Insert the SIMM edge connector at a 75 degree angle onto the socket.

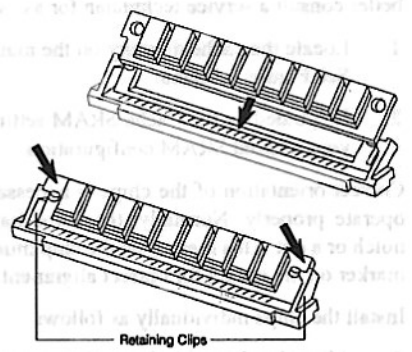



*Figure 3-2. Installing SIMMs*

# Installing DRAM

## SIMM Banks

486-GVT can accommodate on-board memory from 1 to 96MB using SIMMs (Single-In-Line Memory Modules). The mainboard has three memory banks — Bank 0, 1, 2. Each bank can accept either a 256KB, 1MB, 4MB, or 16MB SIMM in each socket.

## DRAM Configuration

Memory can be installed in a variety of configurations, as shown in the next table:

| TOTAL MEMORY | BANK 0 (30-PIN) | BANK 1 (72-PIN) | BANK 2 (72-PIN) |
|---|---|---|---|
| 1MB | 256K x 4 | | |
| | | 1M x 1 | |
| | | | 1M x 1 |
| 2MB | 256K x 4 | 1M x 1 | |
| | | 1M x 1 | 1M x 1 |
| | 256K x 4 | | 1M x 1 |
| 3MB | 256K x 4 | 1M x 1 | 1M x 1 |
| 4MB | 1M x 4 | | |
| | | 4M x 1 | |
| | | | 4M x 1 |
| 5MB | 256K x 4 | 4M x 1 | |
| | 256K x 4 | | 4M x 1 |
| | 1M x 4 | 1M x 1 | |
| | 1M x 4 | | 1M x 1 |
| | | 1M x 1 | 4M x 1 |
| | | 4M x 1 | 1M x 1 |

*Table 3 - 1 DRAM Configurations*





| TOTAL MEMORY | BANK 0 (30-PIN) | BANK 1 (72-PIN) | BANK 2 (72-PIN) |
|---|---|---|---|
| 6MB | 256K x 4 | 4M x 1 | 1M x 1 |
| | 256K x 4 | 1M x 1 | 4M x 1 |
| | 1M x 4 | 1M x 1 | 1M x 1 |
| 8MB | 1M x 4 | 4M x 1 | |
| | 1M x 4 | | 4M x 1 |
| | | 4M x 1 | 4M x 1 |
| 9MB | 256K x 4 | 4M x 1 | 4M x 1 |
| | 1M x 4 | 1M x 1 | 4M x 1 |
| | 1M x 4 | 4M x 1 | 1M x 1 |
| 12MB | 1M x 4 | 4M x 1 | 4M x 1 |
| 16MB | 4M x 4 | | |
| | | 16M x 1 | |
| | | | 16M x 1 |
| 17MB | 256K x 4 | 16M x 1 | |
| | 256K x 4 | | 16M x 1 |
| | | 1M x 1 | 16M x 1 |
| | | 16M x 1 | 1M x 1 |
| | 4M x 4 | 1M x 1 | |
| | 4M x 4 | | 1M x 1 |
| 18MB | 256K x 4 | 1M x 1 | 16M x 1 |
| | 256K x 4 | 16M x 1 | 1M x 1 |
| | 4M x 4 | 1M x 1 | 1M x 1 |
| 20MB | 1M x 4 | 16M x 1 | |
| | 1M x 4 | | 16M x 1 |
| | 4M x 4 | 4M x 1 | |
| | 4M x 4 | | 4M x 1 |
| | | 4M x 1 | 16M x 1 |
| | | 16M x 1 | 4M x 1 |

*Table 3-1. DRAM Configurations (Continued)*