486-GVT

MAIN BOARD
USER'S GUIDE

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Specifications

The 486-GVT mainboard comes with the following features:

- Intel 80486SX/DX/DX2/P24T/80486S-series/ CX486S™ dual CPU microprocessor in PQFP and PGA packages.
- VIA GMC VT82C486 80486/80386 PC/AT chipset includes built-in 8042 keyboard controller.
- Award or AMI BIOS.
- Supports 64/128/256K direct-mapped write-back/write-through cache memory.
- DuPont 30 and 72-pin SIMM sockets supports 1 up to 96MB DRAM for 486 system, provides page mode DRAM operation.
- Supports system and video BIOS cacheable and shadow.
- Supports decoupled DRAM refresh.
- Provides built-in power management features ideal for Green PCs. *
- Optional built-in ZIF socket that accepts Intel's OverDrive™ processors or Pentium™ OverDrive™ processor.
- One 8-bit and six 16-bit ISA expansion slots.
- Supports two VESA bus slots for Local bus master or slave.
- Dallas DS12885Q real time clock/calendar.

* The power management features will be available in Q4, '93.

Mainboard Layout

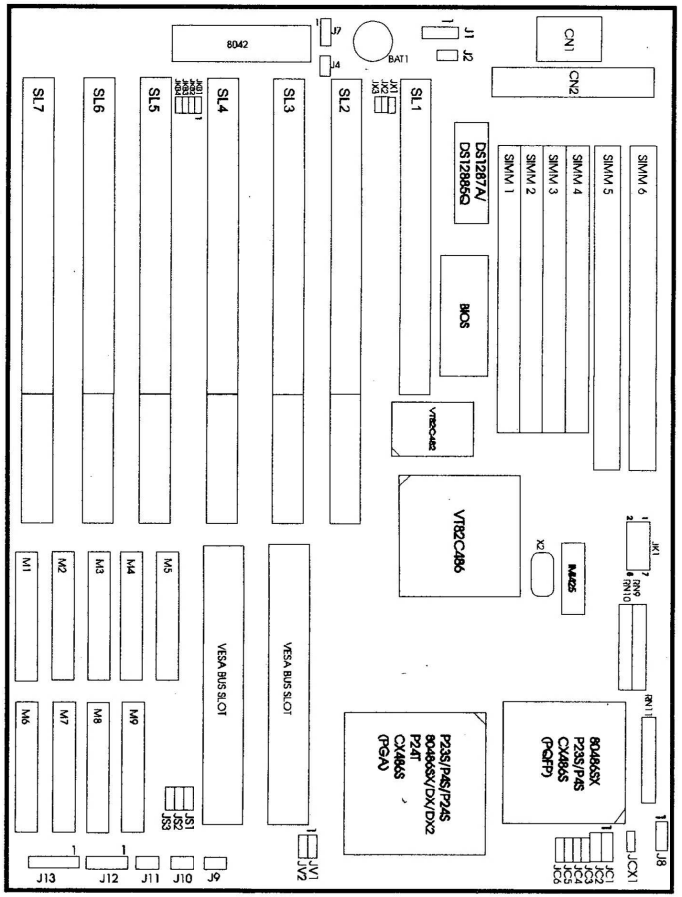


Figure 1-1. Mainboard Layout

System Block Diagram

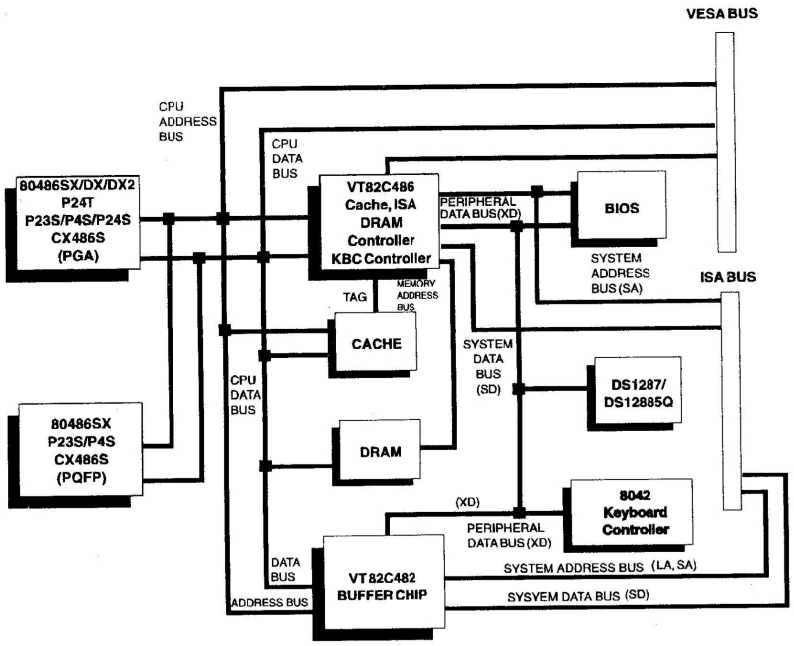


Figure 1-2. System Block Diagram

Chapter 2

Mainboard Settings

486-GVT has several user-adjustable jumpers and connectors on the board that allow you to configure your system to suit your every need.

This chapter contains information on the various jumper and connector settings you can make on your mainboard.

Jumper and Connector Locations

Figure II-1 below shows the jumper and connector locations on the mainboard.

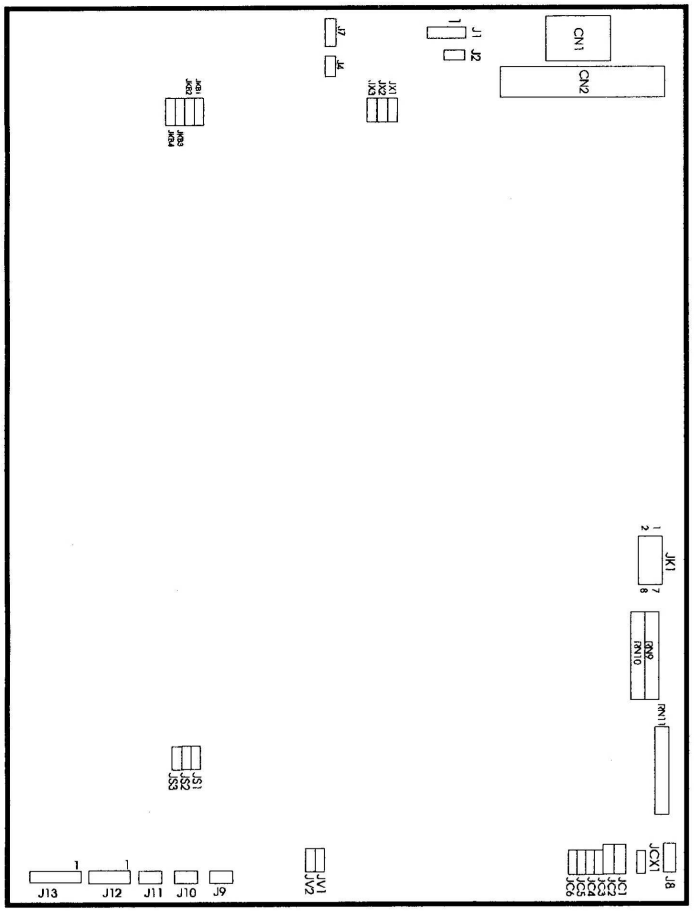


Figure II - 1 Jumper and Connector Positions

Jumpers

Jumpers are used to select the operation modes for your system. Each jumper on the board has three metal pins with each pin representing a different function. To "set" a jumper, a black cap containing metal contacts is placed over the jumper pin/s according to the required configuration. A jumper is said to be "shorted" when the black cap has been placed on one or two of its pins, as shown in the figure below:

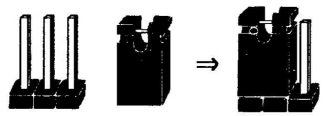


Figure II - 2 Jumper with Pins Shorted

Functions of these jumpers are summarized in the table below:

Jumper	Function
J2	External/Internal battery
J4	Mono/EGA/VGA display type
J7	Password clear (Award/AMI BIOS)
JK1, JX1	CPU clock
JKB1, JKB2, JKB3, JKB4, JX3	External/Internal keyboard
JC1, JC2, JC3, JC4, JC5, JC6, RN9, RN10, RN11	To select the CPU type
JCX1	CX486S/Intel S-series CPU
JV1	CPU speed
JV2	High speed write
JX2, J8	IRQ15, -SMI
JS1, JS2, JS3	Cache Size

Table II - 1 Jumper Functions

Setting the Jumpers

If your system has a 80486SX CPU and you want to add an 80486DX CPU, install the new CPU to the vacant upgrade socket and adjust the jumpers accordingly.

CPU Selector Jumpers

To allow your system to be used with a variety of CPU's, 486-GVT provides ten jumpers that can be set according to the CPU you want installed. These jumpers are: JC1, JC2, JC3, JC4, JC5, JC6, JCX1, RN9, RN10, and RN11. Follow the diagrams found in the lower-middle area of the board to determine the proper arrangement for the CPU you are using.

The next two table summarizes the settings of the CPU Selector jumpers.

Jumper	486SX/P23S (PGA)	P24S/P4S/486DX/ 486DX2 (PGA)	P24T (PGA)	CX486S (PGA)
JC1	2-3 shorted	1-2 shorted	1-2 shorted	2-3 shorted
JC2	2-3 shorted	1-2 shorted	1-2 shorted	2-3 shorted
JC3	open	shorted	open	shorted
JC4	open	open	shorted	open
JC5	shorted	shorted	open	open

Jumper	P23S/P4S/ P24S (PGA)	486DX/486DX2/ 486SX (PGA)	CX486S (PGA)	P23S/P4S/ CX486S (PQFP)
RN9	open	open	shorted	open
RN10	shorted	open	open	open
RN11	open	open	open	shorted

Table II - 2 Jumper Settings for CPU Selector

Jumper	Pin Definition
J2	External, Internal Battery Select 1-2 External battery 2-3 Internal battery
J4	Display Type Select Open Mono/EGA/VGA (default) Close Color
J7	Password Clear (Award/AMI BIOS Select) 1-2 Award BIOS 2-3 AMI BIOS
JC6	80486SX/P23S/P4S/CX486S PQFP Select Short Disable on-board Open Enable
JCX1	CPU Type Select Short CX486S Open Intel S-series CPU
JKB1, JKB2, JKB3, JKB4, JX3	Internal/External Keyboard Select 1-2 External keyboard 2-3 Internal keyboard
JX1	CPU Clock Select 1-2 1 X 2-3 2 X
JX2, J8	1-2 IRQ15 2-3 -SMI

Table II-3. Jumper Definitions

Change the default to "High Speed Write" value if the installed VL-bus controller needs high speed zero wait state write transfers. The CPU speed jumper settings follow the maximum clock speed of the CPU in use. Adjust the setting according to your CPU clock speed.

CPU Clock (JK1)

CLK 2	1-2	3-4	5-6	7-8
40 MHz	Short	Open	Short	Short
50 MHz	Open	Open	Short	Short
80 MHz	Short	Short	Open	Short
66.6 MHz	Open	Short	Open	Short
66.6 MHz	Short	Open	Open	Short
Test	Open	Open	Open	Short
25 MHz	Open	Open	Short	Open
40 MHz	Short	Short	Open	Open
50 MHz	Open	Short	Open	Open
33.3 MHz	Short	Open	Open	Open
Power Down	Short	Short	Short	Short

Table II-4. CPU Clock Jumper Selection (JK1)

Connectors

The connectors allow the mainboard to connect electronically with other parts of the system. Some connectors have two pins, others have four or five pins. The next table gives the functions of each connector.

Connector	Function
CN1	Keyboard
CN2	Power
J1	External Battery Connector
J9	Turbo LED
J10	Turbo Switch
J11	Hardware Reset
J12	Speaker
J13	Keylock and Power LED

Table II-5. Connector Definitions

Some malfunction problems encountered with your system may be caused by loose or improper connection. Ensure that the all connections are in place and firmly attached.

Connector	Pin Outs	Signal Name
CN1 Keyboard Connector	1 2 3 4 5	Keyboard clock Keyboard data No connection Ground +5V
CN2 Power Connector	1 2 3 4 5, 6, 7, 8 9 10, 11, 12	Power good +5V +12V -12V Ground -5V +5V
J1 External Battery Connector	1 2, 3 4	Anode+ NC Cathode -
J9 Turbo LED	1 2	VCC LED
J10 Turbo Switch	1 2	Turbo Signal Ground
J11 Hardware Reset	1 2	Ground Reset signal
J12 Speaker Connector	1 2 3 4	Speaker signal NC Ground +5V
J13 Keylock and Power LED Connector	1 2 3, 5 4	Power signal Spare Ground Keylock

Table II-6. Connector Pin Definitions

VESA Bus Connector

The cache system board provides two high-performance VESA bus connectors, SL14 and SL15, for use with VESA peripherals. These connectors can be utilized for one Local Bus Master and one Local Bus Slave, either (SL14) or (SL15).

The following tables give the pin assignments for SL14 and SL15. Side A of the connector are pin outs on the board's component side while Side B are pin outs on the board's solder side. Jumpers JV1 and JV2 give more information on settings on the mainboard and the VL-bus controller.

Jumper	Pin Definition
JV1	CPU Speed Select 1-2 Greater than 33 MHz 2-3 Less than or equal to 33 MHz
JV2	High Speed Write 1-2 One wait write 2-3 Zero wait write (default)

Memory Locations

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:

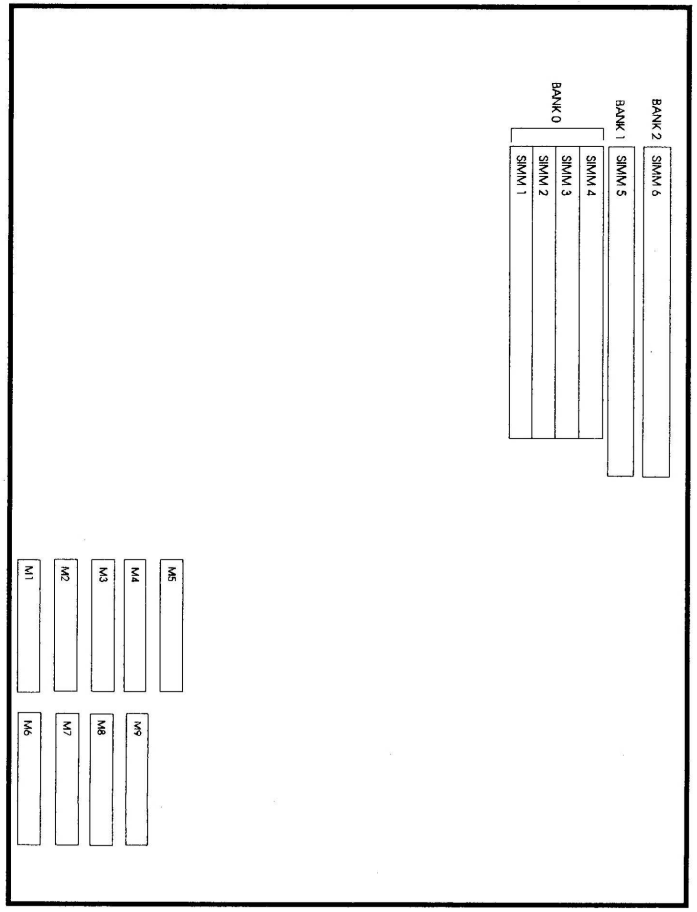


Figure III-1 Memory Locations

Installing DRAM

SIMM banks

486-GVT can accommodate on-board memory from 1 to 128MB using SIMMs (Single-In-Line Memory Modules). The mainboard has three memory banks — Bank 0, 1, 2. Each bank can accept either a 256KB, lMB, 4MB, or 16MB SIMM in each socket.

DRAM Configuration

Memory can be installed in a variety of configurations, as shown in the next table.

Total Memory	Bank 0 (30-pin)	Bank 1 (72-pin)	Bank 2 (72-pin)
1MB	256K x 4		
		1M x 1	
			1M x 1
2MB	256K x 4	1M x 1	
		1M x 1	1M x 1
	256K x 4		1M x 1
3MB	256K x 4	1M x 1	1M x 1
4MB	1M x 4		
		4M x 1	
			4M x 1
5MB	256K x 4	4M x 1	
	256K x 4		4M x 1
	1M x 4	1M x 1	
	1M x 4		1M x 1
		1M x 1	4M x 1
		4M x 1	1M x 1

Table III - 1 DRAM Configurations

Total Memory	Bank 0 (30-pin)	Bank 1 (72-pin)	Bank 2 (72-pin)
6MB	256K x 4	4M x 1	1M x 1
	256K x 4	1M x 1	4M x 1
	1M x 4	1M x 1	1M x 1
8MB	1M x 4	4M x 1	
	1M x 4		4M x 1
		4M x 1	4M x 1
9MB	256K x 4	4M x 1	4M x 1
	1M x 4	1M x 1	4M x 1
	1M x 4	4M x 1	1M x 1
12MB	1M x 4	4M x 1	4M x 1
16MB	4M x 4		
		16M x 1	
			16M x 1
17MB	256K x 4	16M x 1	
	256K x 4		16M x 1
		1M x 1	16M x 1
		16M x 1	1M x 1
	4M x 4	1M x 1	
	4M x 4		1M x 1
18MB	256K x 4	1M x 1	16M x 1
	256K x 4	16M x 1	1M x 1
	4M x 4	1M x 1	1M x 1
20MB	1M x 4	16M x 1	
	1M x 4		16M x 1
	4M x 4	4M x 1	
	4M x 4		4M x 1
		4M x 1	16M x 1
		16M x 1	4M x 1

Table III-1. DRAM Configurations (Continued)

Total Memory	Bank 0 (30-pin)	Bank 1 (72-pin)	Bank 2 (72-pin)
21MB	256K x 4	4M x 1	16M x 1
	256K x 4	16M x 1	4M x 1
	1M x 4	1M x 1	16M x 1
	1M x 4	16M x 1	1M x 1
	4M x 4	1M x 1	4M x 1
	4M x 4	4M x 1	1M x 1
24MB	1M x 4	4M x 1	16M x 1
	1M x 4	16M x 1	4M x 1
	4M x 4	4M x 1	4M x 1
32MB	4M x 4	16M x 1	
	4M x 4		16M x 1
		16M x 1	16M x 1
33MB	256K x 4	16M x 1	16M x 1
	4M x 4	1M x 1	16M x 1
	4M x 4	16M x 1	1M x 1
36MB	1M x 4	16M x 1	16M x 1
	4M x 4	4M x 1	16M x 1
	4M x 4	16M x 1	4M x 1
48MB	4M x 4	16M x 1	16M x 1
64MB	16M x 4		
65MB	16M x 4	1M x 1	
	16M x 4		1M x 1
66MB	16M x 4	1M x 1	1M x 1
68MB	16M x 4	4M x 1	
	16M x 4		4M x 1
69MB	16M x 4	1M x 1	4M x 1
	16M x 4	4M x 1	1M x 1
72MB	16M x 4	4M x 1	4M x 1
80MB	16M x 4	16M x 1	
	16M x 4		16M x 1

Table III-1. DRAM Configurations (Continued)

Total Memory	Bank 0 (30-pin)	Bank 1 (72-pin)	Bank 2 (72-pin)
81MB	16M x 4	1M x 1	16M x 1
	16M x 4	16M x 1	1M x 1
84MB	16M x 4	4M x 1	16M x 1
	16M x 4	16M x 1	4M x 1
96MB	16M x 4	16M x 1	16M x 1

Table III-1. DRAM Configurations (Continued)

Installation Instructions

→ **NOTE:**
Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.

Assuming the 486-GVT has been mounted on your computer system unit, follow the instructions below:

1. Turn off the computer.
2. Disconnect all connections to the system unit and unplug the power cord.
3. Open the system unit cover.
4. Locate the SIMM banks on the mainboard. Determine your desired configuration to be installed.
5. Insert the SIMM edge connector at a 75 degree angle onto the socket.
6. Carefully push the SIMM down and back into the socket until the retaining clips of the socket snap, holding the SIMM in place. The holes in the SIMM should match the pins on the socket's retaining clips.

To remove the SIMM/s, pull the retaining latch on both ends of the socket and reverse the procedure above.

Cache Memory

The 486-GVT can accept cache memory of 64, 128 or 256KB.

→ **NOTE:**
Be sure to use the correct chips for the amount of cache memory you want to add. You must install both the correct Cache and Tag SRAM.

Tag SRAM stores the address of the data in the cache memory. The CPU searches the Tag RAM to check if the required memory addresses are already in the cache memory. If it is, this is called a "hit." If the addresses are not found in the Tag, the Alter RAM of the write-back cache system is used. Every time the CPU wants to write data to the external memory, if the location in SRAM is a "hit", it writes this data to the cache RAM directory, not to the DRAM. At the same time, Alter RAM will be set.

Data in cache RAM is written to DRAM when the following two conditions are met:

1. When the CPU reads a "miss" in SRAM, it reads data from DRAM and places it in the cache RAM. (If the cache RAM location has data in it, the previous data is overwritten.) Before the "read" action, the system first writes-back data to DRAM, then places the second data in cache RAM, overlapping previous data.
2. When the CPU writes data to the same cache RAM location for the second time, the first set of data in the cache RAM is first written back to DRAM; then the new set of data is written to cache RAM. Each time the CPU rewrites the data from cache RAM to DRAM, the Alter RAM is reset.

→ **NOTE:**
Alter RAM type is always the same as Tag RAM.

Installing Cache Memory

NOTE:
Always observe static electricity precautions. See "Handling Precautions" at the beginning of this manual.

To install cache memory, it may be necessary to remove the board from the system, depending on your case design and arrangement of internal components. Read your computer's manual for instructions on how to remove the mainboard from the case. If you do not have the confidence to make the installation, better consult a service technician for assistance.

1. Turn off the computer.
2. Disconnect all connections to the system unit and unplug the power cord.
3. Open the system unit cover.
4. Following the instructions on your computer manual, remove the mainboard from the system unit (if necessary).
5. Locate the cache memory on the mainboard. See Figure III - 1 again.
6. Be guided by the Cache SRAM settings depending on your desired SRAM configuration:

Correct orientation of the chips is necessary for the cache to operate properly. Normally, the chips have either a curved notch or a dot. This marker on the chip must be matched to the marker on the socket for correct alignment.

Install the chips individually as follows:

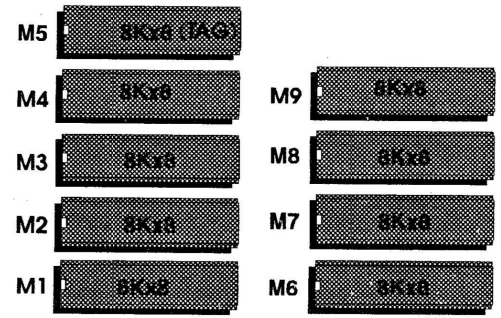
7. Align the chip with the marker on the socket. Press the chip onto the socket, ensuring that the pins on the chip are aligned with the corresponding connections on the socket.
8. Carefully apply enough pressure to partially seat the chip into the socket.

Ensure that all pins are properly aligned with the connectors and that there are no bent pins. If there are any bent pins, remove the chip, straighten the pin and repeat the process.

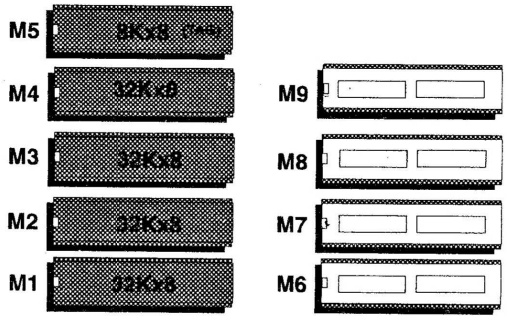
9. Press the chip completely into the socket so that the pins are properly seated.

Cache SRAM Specifications and Settings

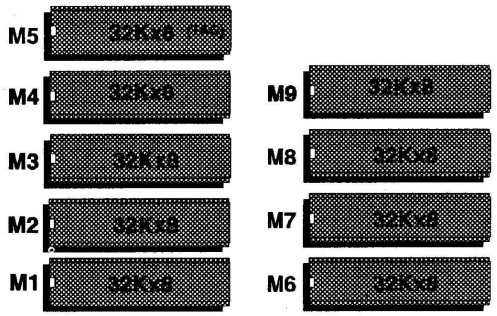
64K Cache SRAM



128K Cache SRAM



256K Cache SRAM



The cache size is jumper selectable. M1 - M4 are assigned as Bank 0 and M6 - M9 are assigned as Bank 1.

	64K	128K	256K
Bank 0	8K x 8	32K x 8	32K x 8
Bank 1	8K x 8	Empty	32K x 8
Tag RAM (M5)	8K x 8	8K x 8	32K x 8
JS1 (Jumper)	1-2	1-2	2-3
JS2 (Jumper)	1-2	2-3	2-3
JS3 (Jumper)	1-2	2-3	1-2

Table III-2. Cache Configuration Size

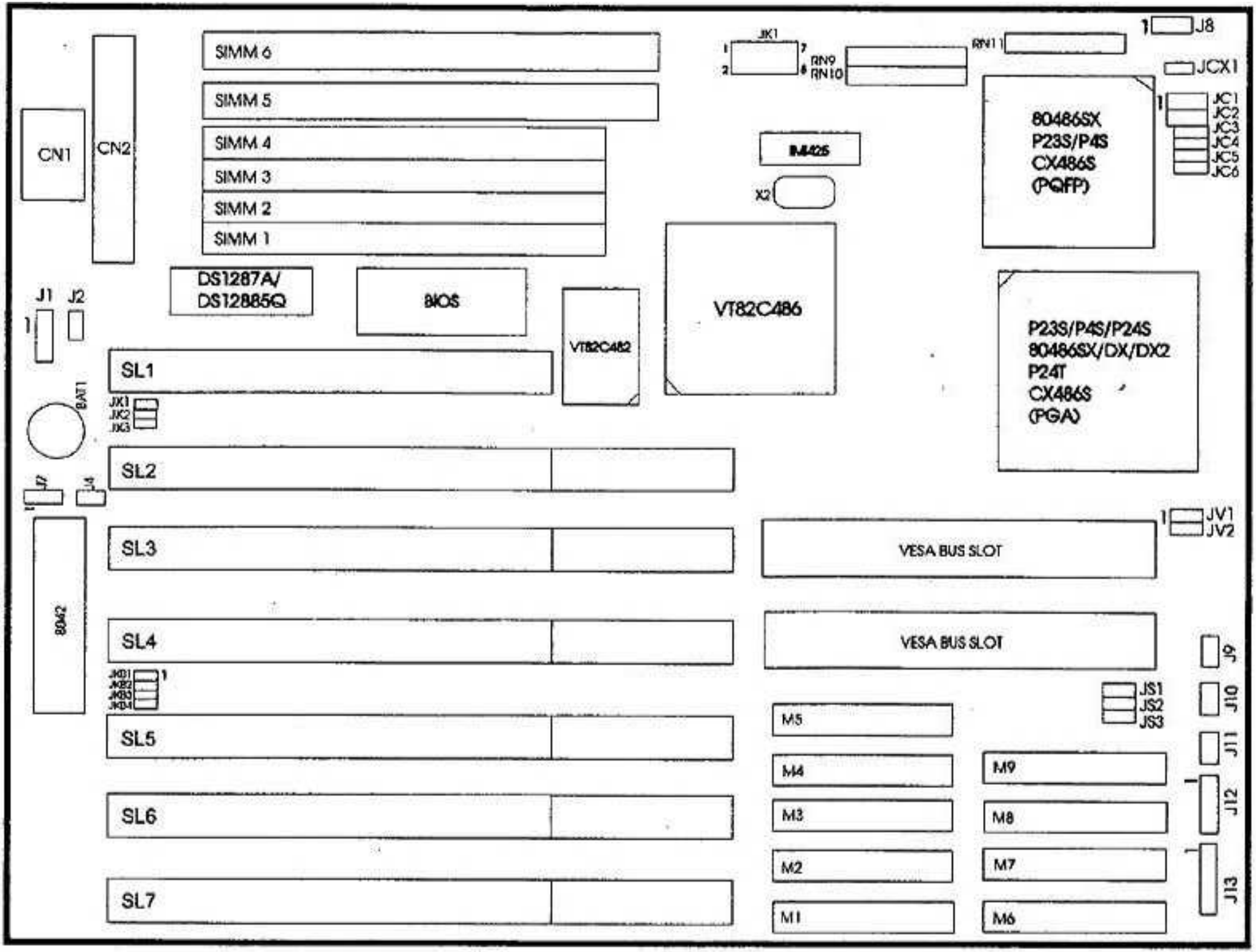
Chapter 4

Award BIOS Setup

*486-GVT comes with the Award BIOS * chip that contains the ROM Setup information of your system. This chip serves as an interface between the CPU and the rest of the mainboard's components.*

This chapter explains the information contained in the Setup program and tells you how to modify the settings according to your system configuration.

* If your mainboard uses the AMI BIOS chip, disregard this chapter. Refer to Chapter 5 instead.


SIMM 6
SIMM 5
SIMM 4
SIMM 3
SIMM 2
SIMM 1
CN1
CN2
JK1
RN9
RN10
RN11
J8
JCX1
JC1
JC2
JC3
JC4
JC5
JC6
80486SX
P23S/P4S
CX486S
(PQFP)
X2
DS1287A/
DS12885Q
BIOS
VT82C482
VT82C486
P23S/P4S/P24S
80486SX/DX/DX2
P24T
CX486S
(PGA)
J1
J2
BAT1
JK1
JK2
JK3
SL1
SL2
SL3
SL4
SL5
SL6
SL7
8042
JV1
JV2
VESA BUS SLOT
VESA BUS SLOT
JS1
JS2
JS3
J9
J10
J11
J12
J13
M5
M4
M3
M2
M1
M9
M8
M7
M6