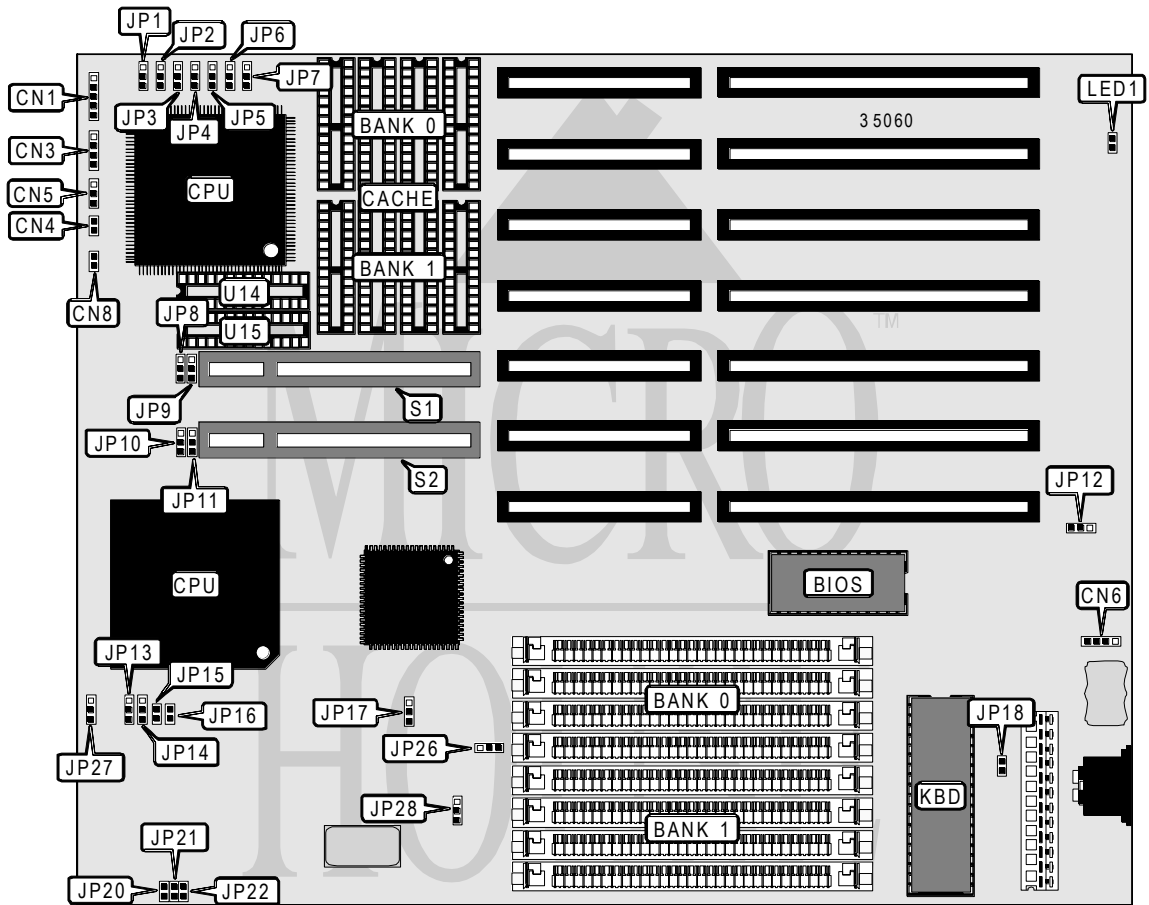


ABIT COMPUTER CORPORATION AV4 VL-BUS MAIN BOARD

Processor	80486SX/80487SX/80486DX/80486DX2
Processor Speed	20/25/33/50(internal)/50/66(internal)MHz
Chip Set	SIS
Max. Onboard DRAM	32MB
SRAM Cache	64/128/256KB
BIOS	AMI
Dimensions	220mm x 254mm
I/O Options	32-bit VESA card slot (2)
NPU Options	None



CONNECTIONS			
Purpose	Location	Purpose	Location
Keylock	CN1	External battery	CN6
Speaker	CN3	Reset	CN8
Turbo LED	CN4	Power LED	LED1
Turbo switch	CN5/pins 2 & 3	32-bit VESA card (2)	S1 & S2

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AV4 VL-BUS MAIN BOARD

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í VESA bus speed select 20/25/33MHz	JP8 and JP10	pins 1 & 2 closed
VESA bus speed select 50MHz	JP8 and JP10	pins 2 & 3 closed
í VESA bus wait state select 1	JP9 and JP11	pins 1 & 2 closed
VESA bus wait states select 0	JP9 and JP11	pins 2 & 3 closed
í CMOS memory normal operation	JP12	pins 1 & 2 closed
CMOS memory clear	JP12	pins 2 & 3 closed
í Fast gate A20 select enabled	JP17	pins 1 & 2 closed
Fast gate A20 select disabled	JP17	pins 2 & 3 closed
í Monitor type select color	JP18	closed
Monitor type select monochrome	JP18	open
í Factory configured - do not alter ¹	JP23	See note
í Factory configured - do not alter ¹	JP24	See note
í Factory configured - do not alter ¹	JP25	See note
í Factory configured - do not alter ¹	JP26	pins 2 & 3 closed
í Factory configured - do not alter	JP27	pins 2 & 3 closed
í Factory configured - do not alter ¹	JP28	See note
Note: The locations of JP23, JP24, and JP25 are unknown		
Note ¹ : JP23 through JP28 are set at the factory depending on whether the R1 or R2 Model is shipped.		

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
32MB	(4) 4M x 9	(4) 4M x 9

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SRAM CONFIGURATION				
Size	Cache SRAM	Location	TAG(U14)	TAG(U15)
64KB	(8) 8K x 8	Banks 0 & 1	(1) 8K x 8	(1) 8K x 8
128KB	(4) 32K x 8	Bank 0	(1) 8K x 8	(1) 8K x 8
256KB	(8) 32K x 8	Banks 0 & 1	(1) 32K x 8	(1) 32K x 8
Note: If SRAM is installed at U15 then write-back caching is enabled. If SRAM is installed at U14 and U15 then write-back or write-through caching can be enabled.				

SRAM JUMPER CONFIGURATION			
Jumper	64KB	128KB	256KB
JP1	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed
JP2	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
JP3	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed
JP4	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
JP5	pins 2 & 3 closed	pins 1 & 2 closed	pins 2 & 3 closed
JP6	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
JP7	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed

CPU JUMPER CONFIGURATION				
CPU	Jumper JP13	Jumper JP14	Jumper JP15	Jumper JP16
80486DX/80486DX2	pins 1 & 2 closed	pins 1 & 2 closed	closed	closed
80487SX	pins 2 & 3 closed	pins 1 & 2 closed	closed	closed
80486SX (PGA)	open	pins 2 & 3 closed	open	closed
80486SX (PQFP)	open	pins 2 & 3 closed	open	open

CPU SPEED CONFIGURATION			
Speed	Jumper JP20	Jumper JP21	Jumper JP22
20MHz	closed	closed	open
25MHz	closed	open	closed
33MHz	open	closed	closed
50MHz	open	closed	open