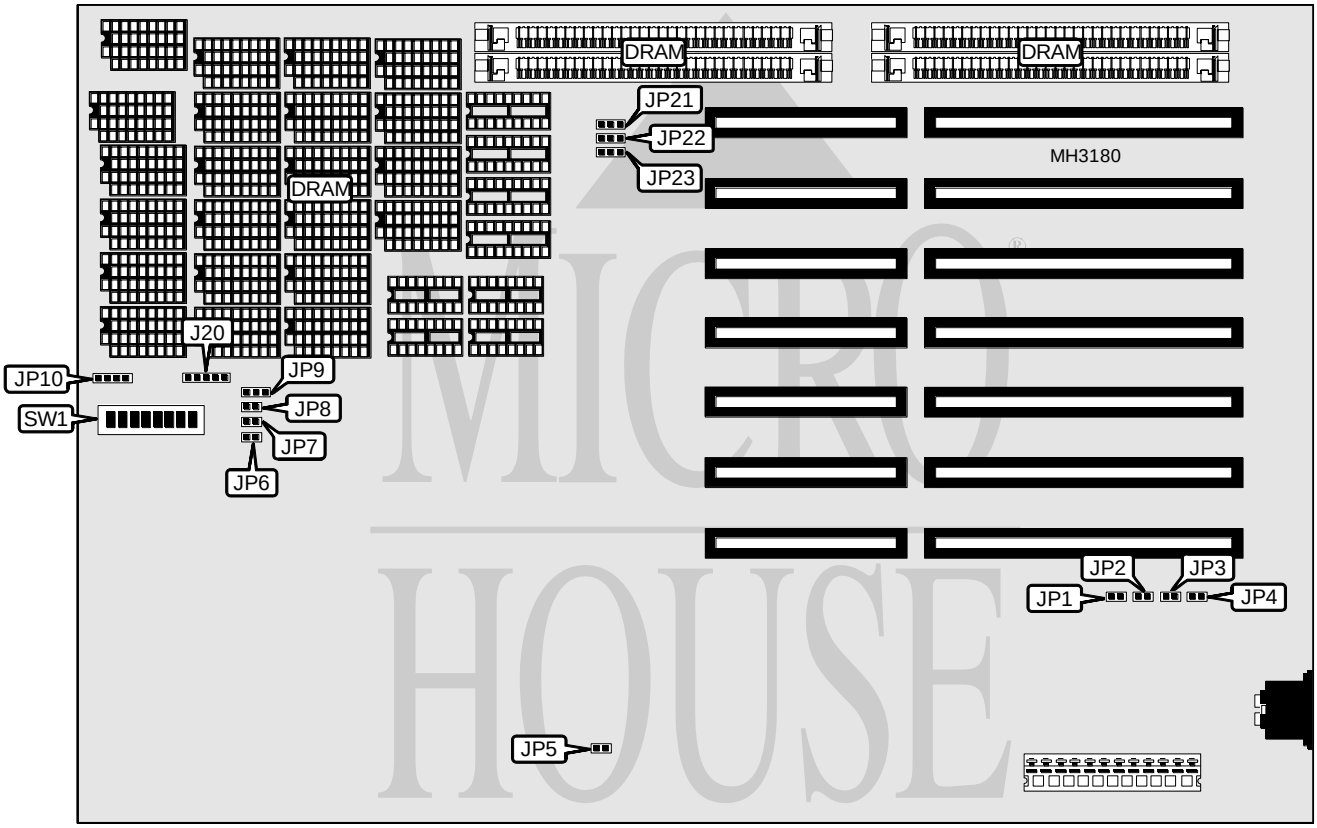
UNIDENTIFIED
J S - 1 6 8 A

Processor	80286 (exact location unidentified)
Processor Speed	12MHz
Chip Set	Unidentified
Max. Onboard DRAM	4MB
Cache	None
BIOS	AMI/Award/ERSO/Phoenix
Dimensions	330mm x 218mm
I/O Options	None
NPU Options	80287 (exact location unidentified)



CONNECTIONS			
Purpose	Location	Purpose	Location
Power LED & keylock	J20	Turbo LED	JP8
Reset switch	JP6	Speaker	JP10
Turbo switch	JP7		

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UNIDENTIFIED
J S - 1 6 8 A

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USER CONFIGURABLE SETTINGS		
Function	Jumper/Switch	Position
Wait state select 0 wait states	JP5	Closed
Wait state select 1 wait state	JP5	Open
Turbo select keyboard control	JP9	pins 1 & 2 closed
Turbo select controlled by SW1/1	JP9	pins 2 & 3 closed
CPU speed select low	SW1/1	On
CPU speed select high	SW1/1	Off
Monitor type select color	SW1/2	On
Monitor type select monochrome	SW1/2	Off
Parity enabled	SW1/3	On
Parity disabled	SW1/3	Off
EMS port address select 0E8H	SW1/4	On
EMS port address select 098H	SW1/4	Off
BIOS type select 27128	SW1/5	On
BIOS type select 27256	SW1/5	Off

DRAM CONFIGURATION			
Size	Bank A	Bank B	Bank B/0
512KB (A)	(18) 41256	NONE	NONE
512KB (B)	NONE	NONE	(4) 44256 & (2) 41256
512KB (C)	NONE	NONE	NONE
640KB(A)	(18) 4164	NONE	(4) 44256 & (2) 41256
640KB(B)	(18) 4164	NONE	NONE
640KB (C)	NONE	NONE	(4) 44256 & (2) 41256 & (4) 4464 & (2) 4164
1MB (A)	NONE	NONE	(8) 44256 & (4) 41256
1MB (B)	NONE	NONE	NONE
1MB (C)	(18) 41256	NONE	(4) 44256 & (2) 41256
1MB (D)	(18) 41256	NONE	NONE
1MB (E)	(18) 41256	NONE	NONE
1MB (F)	(18) 41256	NONE	NONE
2MB (A)	(18) IBM DRAM	NONE	NONE
2MB (B)	NONE	NONE	NONE
4MB (A)	NONE	NONE	NONE
4MB (B)	(18) 41256	NONE	NONE
4MB (C)	(18) 41256	NONE	NONE
Note: The orientation of the DRAM banks is unidentified.			

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UNIDENTIFIED
J S - 1 6 8 A

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DRAM CONFIGURATION (CON'T)				
Size	Bank B/1	Bank C	Bank C/SIM 0	Bank C/SIM 1
512KB (A)	NONE	NONE	NONE	NONE
512KB (B)	NONE	NONE	NONE	NONE
512KB (C)	NONE	NONE	(2) 256K x 9	NONE
640KB(A)	NONE	NONE	NONE	NONE
640KB(B)	NONE	NONE	(2) 256K x 9	NONE
640KB (C)	NONE	NONE	NONE	NONE
1MB (A)	NONE	NONE	NONE	NONE
1MB (B)	NONE	NONE	(2) 256K x 9	(2) 256K x 9
1MB (C)	NONE	NONE	NONE	NONE
1MB (D)	(4) 44256 & (2) 41256	NONE	NONE	NONE
1MB (E)	NONE	NONE	(2) 256K x 9	NONE
1MB (F)	NONE	NONE	NONE	(2) 256K x 9
2MB (A)	NONE	NONE	NONE	NONE
2MB (B)	NONE	NONE	(2) 1M x 9	NONE
4MB (A)	NONE	NONE	(2) 1M x 9	(2) 1M x 9
4MB (B)	NONE	NONE	(2) 1M x 9	NONE
4MB (C)	NONE	NONE	NONE	(2) 1M x 9
Note: The orientation of the DRAM banks is unidentified.				

DRAM JUMPER CONFIGURATION			
Size	JP21	JP22	JP23
512KB (A)	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed
512KB (B)	N/A	N/A	N/A
512KB (C)	N/A	N/A	N/A
640KB (A)	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed
640KB (B)	pins 2 & 3 closed	pins 1 & 2 closed	pins 1 & 2 closed
640KB (C)	N/A	N/A	N/A
1MB (A)	N/A	N/A	N/A
1MB (B)	N/A	N/A	N/A
1MB (C)	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed
1MB (D)	pins 2 & 3 closed	pins 1 & 2 closed	pins 1 & 2 closed
1MB (E)	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed
1MB (F)	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed
2MB (A)	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed
2MB (B)	N/A	N/A	N/A
4MB (A)	N/A	N/A	N/A
4MB (B)	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed
4MB (C)	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed

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UNIDENTIFIED
J S - 1 6 8 A

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DRAM SWITCH CONFIGURATION			
Size	SW1/6	SW1/7	SW1/8
512KB	On	On	On
640KB	On	On	Off
640KB + 384KB	On	Off	On
640KB + 384KB (EMS)	On	Off	Off
640KB + 1408KB	Off	On	On
640KB + 1408KB (EMS)	Off	On	Off
640KB + 3456KB	Off	Off	On
640KB + 3456KB (EMS)	Off	Off	Off

KEYBOARD BIOS PIN CONFIGURATION				
Pin	JP1	JP2	JP3	JP4
23	Open	Open	Closed	Open
27	Open	Closed	Open	Open
30	Open	Open	Open	Closed
32	Closed	Open	Open	Open

MISCELLANEOUS TECHNICAL NOTE
Note: The location of pin 1 is unidentified.