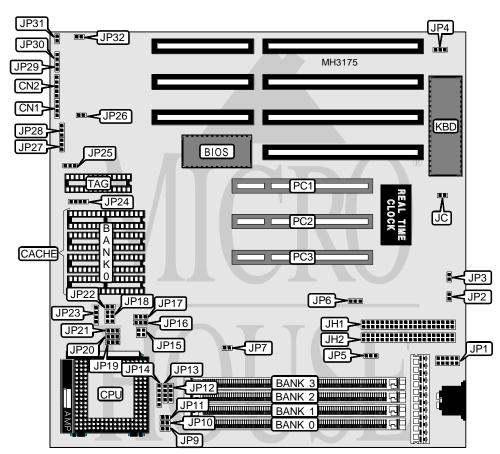
#### Processor

Processor Speed
Chip Set
Max. Onboard DRAM
Cache
BIOS
Dimensions
I/O Options
NPU Options

CX4865X/804865X/SL804865X/SL804865X2/CX486DX/AM486DX/UMCU55/ SL80486DX/CX486DX2/AM486DX2/SL80486DX2/AM486DX4/80486DX4 25/33/40/50(internal)/50/66(internal)/75(internal)/100(internal)MHz UMC 128MB 128/256/512KB Unidentified 220mm x 220mm 32-bit PCI slots (3), green PC connector, IDE interfaces (2) None



CONNECTIONS					
Purpose Location Purpose Locatio					
Speaker	CN1	Turbo switch	JP29		
Power LED & keylock	CN2	Turbo LED	JP30		
IDE interface	JH1	Reset switch	JP31		
IDE interface	JH2	IDE interface LED	JP32		
Green PC connector	JP26	32-bit PCI slots	PC1 - PC3		

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USER CONFIGURABLE SETTINGS				
Function	Jumper	Position		
í CMOS memory normal operation	JC	Closed		
CMOS memory clear	JC	Open		
IDE interface enabled	JP2	Open		
IDE interface disabled	JP2	Closed		
í Port address fixed	JP3	Closed		
Port address relocatable	JP3	Open		
í Factory configured - do not alter	JP10	Open		
í Factory configured - do not alter	JP15	pins 1 & 2 closed		

		DRAM CONFIGURATION	N	
Size	Bank 0	Bank 1	Bank 2	Bank 3
2MB	(1) 256K x 36	(1) 256K x 36	NONE	NONE
4MB	(1) 1M x 36	NONE	NONE	NONE
4MB	NONE	(1) 1M x 36	NONE	NONE
8MB	(1) 1M x 36	(1) 1M x 36	NONE	NONE
8MB	NONE	NONE	(1) 2M x 36	NONE
12MB	(1) 1M x 36	(1) 1M x 36	(1) 1M x 36	NONE
16MB	(1) 1M x 36	(1) 1M x 36	(1) 1M x 36	(1) 1M x 36
16MB	(1) 2M x 36	(1) 2M x 36	NONE	NONE
16MB	(1) 4M x 36	NONE	NONE	NONE
32MB	(1) 4M x 36	(1) 4M x 36	NONE	NONE
32MB	NONE	NONE	(1) 4M x 36	(1) 4M x 36
32MB	(1) 8M x 36	NONE	NONE	NONE
48MB	(1) 4M x 36	(1) 4M x 36	(1) 4M x 36	NONE
64MB	(1) 8M x 36	(1) 8M x 36	NONE	NONE
128MB	(1) 8M x 36	(1) 8M x 36	(1) 8M x 36	(1) 8M x 36

	CACHE CONFIGURATION	
Size	Bank 0	TAG
128KB	(4) 32K x 8	(1) 8K x 8
256KB	(4) 64K x 8	(1) 32K x 8
512KB	(4) 128K x 8	(1) 32K x 8

CACHE JUMPER CONFIGURATION						
Size JP22 JP23 pins 1 & 2 JP23 pins 3 & 4 JP25						
128KB	Open	Closed	Open	pins 1 & 2 closed		
256KB	Open	Closed	Closed	pins 2 & 3 closed		
512KB	Closed	Closed	Closed	pins 2 & 3 closed		

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CPU TYPE CONFIGURATION					
Туре	JP7	JP11	JP12	JP13	JP14
CX486SX	Open	1&2	Open	2 & 3	1 & 2, 3 & 4
80486SX	Closed	Open	Open	2 & 3	Open
SL80486SX	Closed	Open	Open	2 & 3	2&3,4&5
SL80486SX2	Closed	Open	Open	2 & 3	2&3,4&5
CX486DX	Open	1 & 2	3 & 4	1 & 2, 3 & 4	1 & 2, 3 & 4
AM486DX	Closed	Open	3 & 4	1&2,3&4	Open
UMCU5S	Closed	Open	1&2	2 & 3	Open
SL80486DX	Closed	Open	3 & 4	1&2,3&4	2 & 3, 4 & 5
CX486DX2	Open	1 & 2	3 & 4	1 & 2, 3 & 4	1 & 2, 3 & 4
AM486DX2	Closed	Open	3 & 4	1&2,3&4	Open
SL80486DX2	Closed	Open	3 & 4	1&2,3&4	2 & 3, 4 & 5
AM486DX4	Closed	Open	3 & 4	1&2,3&4	Open
80486DX4	Closed	Open	3 & 4	1 & 2, 3 & 4	2 & 3, 4 & 5
Note: Pins desig	nated should be in t	he closed position.			

CPU TYPE CONFIGURATION (CON'T)						
Туре	JP16	JP17	JP19	JP20	JP21	JP24
CX486SX	2 & 3	1&2	2&3	1&2	2&3	2&3
80486SX	1 & 2	1&2	Open	Open	Open	Open
SL80486SX	1 & 2	1&2	Open	1&2	1&2	Open
SL80486SX2	1 & 2	1&2	Open	1&2	1&2	Open
CX486DX	2 & 3	1&2	2&3	1&2	2&3	2&3
AM486DX	1 & 2	1&2	Open	Open	Open	Open
UMCU5S	1 & 2	2&3	Open	2&3	Open	3&4
SL80486DX	1 & 2	1&2	Open	1&2	1&2	Open
CX486DX2	2 & 3	1&2	2&3	1&2	2&3	2&3
AM486DX2	1 & 2	1&2	Open	Open	Open	Open
SL80486DX2	1 & 2	1&2	Open	1&2	1&2	Open
AM486DX4	1 & 2	1&2	Open	Open	Open	Open
80486DX4	1 & 2	1&2	Open	1 & 2	1&2	Open
Note: Pins des	ignated should be	e in the closed p	osition.		1	

CPU SPEED CONFIGURATION					
Speed	JP18 pins 1 & 2	JP18 pins 3 & 4	JP18 pins 5 & 6		
25MHz	Open	Open	Open		
33MHz	Closed	Closed	Open		
40MHz	Open	Closed	Open		
50iMHz	Open	Open	Open		
50MHz	Closed	Open	Open		
66iMHz	Closed	Closed	Open		
75iMHz	Open	Open	Open		
100iMHz	Closed	Closed	Open		

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CPU SPEED CONFIGURATION (80486DX4 ONLY)			
Speed	JP9		
2x	Closed		
3x	Open		

	KE	YBOARD CON	FIGURATION			
Setting	JP1	JP4	JP5	JP6	JP27	JP28
Internal	7 & 8, 9 & 10	1&2	1&2	1&2	2&3	1&2
External	1 & 3, 2 & 4, 5 & 7, 6 & 8	2&3	2&3	2&3	1&2	2&3
Note: Pins of	Note: Pins designated should be in the closed position.					

#### MISCELLANEOUS TECHNICAL NOTE

Note: The location of pin 1 is unidentified. Jumpers are shown for location purposes only. The actual location may vary.