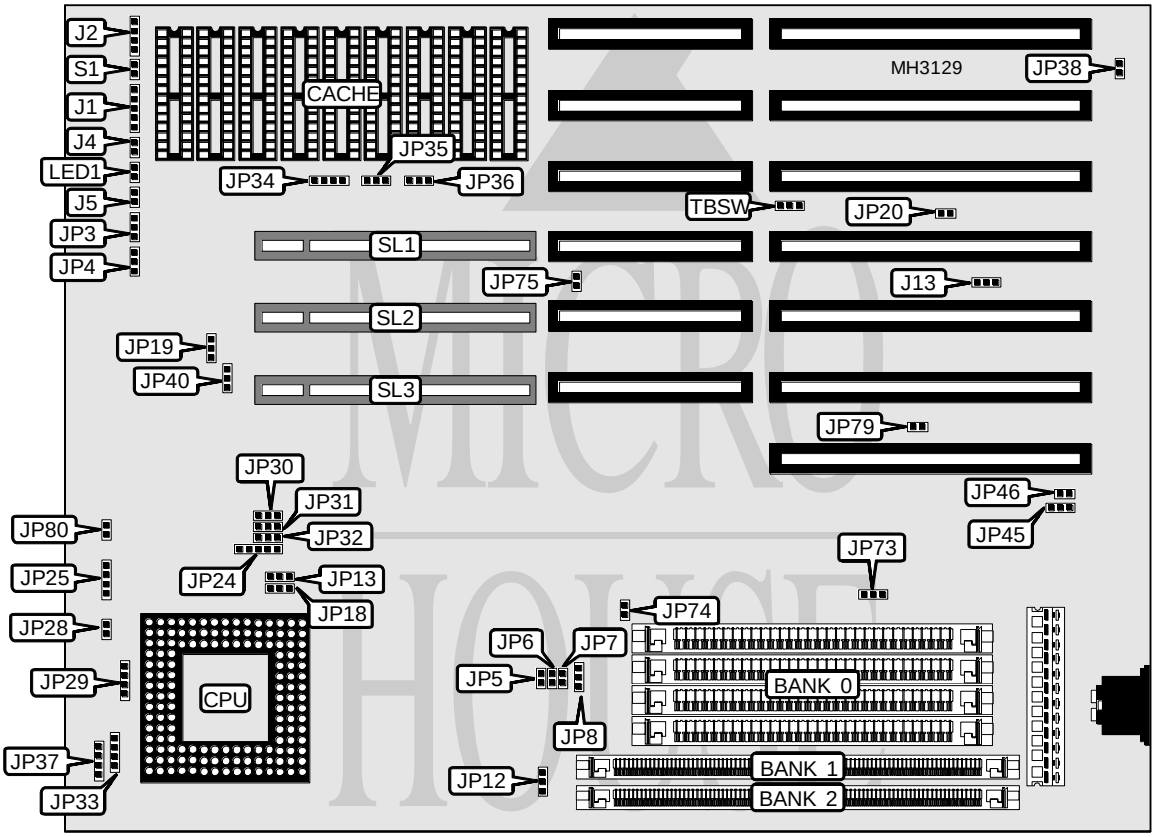
UNIDENTIFIED
S I S 4 8 6 P 3

Processor	80486SX/SL80486SX/CX486DX/AM486DX/80486DX/SL80486DX/80486DX2/ SL80486DX2/80486DX4
Processor Speed	20/25/33/40/50(internal)/50/66(internal)/75(internal)/100(internal)MHz
Chip Set	SIS
Max. Onboard DRAM	64MB
Cache	32/64/128/256KB
BIOS	AMI
Dimensions	250mm x 220mm
I/O Options	32-bit VESA local bus slots (3), green PC connector
NPU Options	None



CONNECTIONS			
Purpose	Location	Purpose	Location
Keylock	J1	Green PC connector	JP74
Speaker	J2	Green PC connector	JP75
Turbo LED	J4	Turbo switch	S1
Reset switch	J5	32-bit VESA local bus slots	SL1 - SL3
Power LED	LED1		

Continued on next page. . .

UNIDENTIFIED
S I S 4 8 6 P 3

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Factory configured - do not alter	J9	Closed
í Factory configured - do not alter	J11	Open
í Factory configured - do not alter	J12	Open
í CLK down by SMI control	JP10	pins 1 & 2 closed
CLK down by STPCLK control	JP10	pins 2 & 3 closed
í Factory configured - do not alter	JP17	pins 1 & 2 closed
í Factory configured - do not alter	JP20	pins 1 & 2 closed
Monitor type select monochrome/EGA/VGA	JP38	Open
Monitor type select CGA	JP38	Closed
í CMOS memory normal operation	JP39	pins 1 & 2 closed
CMOS memory clear	JP39	pins 2 & 3 closed
í Factory configured - do not alter	JP43	pins 2 & 3 closed
BIOS type select EPROM	JP73	pins 1 & 2 closed
BIOS type select flash	JP73	pins 2 & 3 closed
í Factory configured - do not alter	JP78	pins 1 & 2 closed
í Factory configured - do not alter	JP79	pins 2 & 3 closed
Turbo enabled	TBSW	pins 2 & 3 closed
Turbo disabled	TBSW	pins 1 & 2 closed
Note: The location of jumpers J9, J11, J12, JP10, JP17, JP39, JP43 and JP78 are unidentified.		

DRAM CONFIGURATION 1			
Size	Bank 0	Bank 1	Bank 2
2MB	NONE	(1) 256K x 36	(1) 256K x 36
4MB	NONE	(1) 512K x 36	(1) 512K x 36
8MB	NONE	(1) 1M x 36	(1) 1M x 36
12MB	NONE	(1) 1M x 36	(1) 2M x 36
16MB	NONE	(1) 2M x 36	(1) 2M x 36
24MB	NONE	(1) 2M x 36	(1) 4M x 36
32MB	NONE	(1) 4M x 36	(1) 4M x 36
36MB	NONE	(1) 1M x 36	(1) 8M x 36
48MB	NONE	(1) 4M x 36	(1) 8M x 36
64MB	NONE	(1) 8M x 36	(1) 8M x 36

DRAM CONFIGURATION 2			
Size	Bank 0	Bank 1	Bank 2
1MB	(4) 256K x 9	NONE	NONE
4MB	(4) 1M x 9	NONE	NONE
16MB	(4) 4M x 9	NONE	NONE
64MB	(4) 16M x 9	NONE	NONE

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UNIDENTIFIED
S I S 4 8 6 P 3

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DRAM CONFIGURATION 3			
Size	Bank 0	Bank 1	Bank 2
8MB	(4) 1M x 9	NONE	(1) 1M x 36
20MB	(4) 1M x 9	NONE	(1) 4M x 36
32MB	(4) 4M x 9	NONE	(1) 4M x 36

DRAM CONFIGURATION 4			
Size	Bank 0	Bank 1	Bank 2
6MB	(4) 1M x 9	(1) 256K x 36	(1) 256K x 36
8MB	(4) 1M x 9	(1) 512K x 36	(1) 512K x 36
12MB	(4) 1M x 9	(1) 1M x 36	(1) 1M x 36
24MB	(4) 4M x 9	(1) 1M x 36	(1) 1M x 36
48MB	(4) 4M x 9	(1) 4M x 36	(1) 4M x 36

DRAM JUMPER CONFIGURATION		
Configuration	JP45	JP46
1	pins 1 & 2 closed	Open
2	pins 1 & 2 closed	Open
3	pins 1 & 2 closed	Open
4	Open	Closed

CACHE CONFIGURATION			
Size	Bank 0	Bank 1	TAG
32KB	(4) 8K x 8	NONE	(1) 8K x 8
64KB	(4) 8K x 8	(4) 8K x 8	(1) 8K x 8
128KB	(4) 32K x 8	NONE	(1) 8K x 8
256KB (A)	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8
256KB (B)	(4) 64K x 8	NONE	(1) 32K x 8
Note: The orientation of Banks 0 & 1 and the TAG is unidentified.			

CACHE JUMPER CONFIGURATION						
Size	JP30	JP31	JP32	JP34	JP35	JP36
32KB	1 & 2	1 & 2	1 & 2	Open	1 & 2	1 & 2
64KB	2 & 3	1 & 2	1 & 2	1 & 2	2 & 3	1 & 2
128KB	2 & 3	2 & 3	1 & 2	2 & 3, 4 & 5	1 & 2	2 & 3
256KB (A)	2 & 3	2 & 3	2 & 3	1 & 2, 3 & 4	2 & 3	2 & 3
256KB (B)	2 & 3	2 & 3	2 & 3	2 & 3, 4 & 5	1 & 2	2 & 3
Note: Pins designated should be in the closed position.						

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UNIDENTIFIED
S I S 4 8 6 P 3

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CPU TYPE CONFIGURATION							
Type	J13	JP8	JP12	JP13	JP18	JP19	JP24
80486SX	Closed	2 & 3	Open	Open	1 & 2	2 & 3	Open
SL80486SX	Closed	2 & 3	Open	Open	1 & 2	2 & 3	4 & 5
CX486DX	Open	2 & 3	2 & 3	2 & 3	2 & 3	1 & 2	2 & 3
AM486DX	Closed	2 & 3	Open	Open	1 & 2	2 & 3	Open
80486DX	Closed	2 & 3	Open	Open	1 & 2	2 & 3	Open
SL80486DX	Closed	2 & 3	Open	Open	1 & 2	2 & 3	4 & 5
80486DX2	Closed	2 & 3	Open	Open	1 & 2	2 & 3	Open
SL80486DX2	Closed	2 & 3	Open	Open	1 & 2	2 & 3	4 & 5
80486DX4	Closed	2 & 3	Open	Open	1 & 2	2 & 3	4 & 5
Note: Pins designated should be in the closed position.							

CPU TYPE CONFIGURATION (CON'T)						
Type	JP25	JP28	JP29	JP33	JP37	JP40
80486SX	Open	Open	Open	2 & 3	Open	2 & 3
SL80486SX	2 & 3	1 & 2	3 & 4	2 & 3	Open	2 & 3
CX486DX	1 & 2, 3 & 4	Open	2 & 3	1 & 2, 3 & 4	3 & 4	2 & 3
AM486DX	Open	Open	Open	1 & 2, 3 & 4	3 & 4	1 & 2
80486DX	Open	Open	Open	1 & 2, 3 & 4	3 & 4	2 & 3
SL80486DX	2 & 3	1 & 2	3 & 4	1 & 2, 3 & 4	3 & 4	2 & 3
80486DX2	Open	Open	Open	1 & 2, 3 & 4	3 & 4	2 & 3
SL80486DX2	2 & 3	1 & 2	3 & 4	1 & 2, 3 & 4	3 & 4	2 & 3
80486DX4	2 & 3	1 & 2	3 & 4	1 & 2, 3 & 4	3 & 4	2 & 3
Note: Pins designated should be in the closed position.						

CPU SPEED CONFIGURATION	
Type	JP27
Any CPU installed	Open
CX486S2 only	Closed
Note: The location of JP27 is unidentified.	

CPU SPEED CONFIGURATION			
Speed	JP5	JP6	JP7
20MHz	Closed	Open	Closed
25MHz	Closed	Closed	Open
33MHz	Open	Closed	Closed
40MHz	Closed	Open	Open
50iMHz	Closed	Closed	Open
50MHz	Open	Open	Closed
66iMHz	Open	Closed	Closed
75iMHz	Closed	Closed	Open
100iMHz	Open	Closed	Closed

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UNIDENTIFIED
S I S 4 8 6 P 3

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CPU SPEED CONFIGURATION (80486DX4 ONLY)	
Speed	JP44
2x	pins 1 & 2 closed
2.5x	pins 2 & 3 closed
3x	Open
Note: The location of JP44 is unidentified.	

CPU VOLTAGE CONFIGURATION	
Voltage	JP80
3.45v	Open
5v	Closed

VL BUS WAIT STATE CONFIGURATION	
Wait states	JP4
0 wait states	pins 1 & 2 closed
1 wait state	pins 2 & 3 closed

VL BUS SPEED CONFIGURATION	
CPU speed	JP3
<= 33MHz	pins 1 & 2 closed
> 33MHz	pins 2 & 3 closed

MISCELLANEOUS TECHNICAL NOTE
Note: The location of pin 1 is unidentified. Many of the jumpers on this diagram are shown for location purposes only. The actual location may be different. Check mainboard for actual jumper locations.