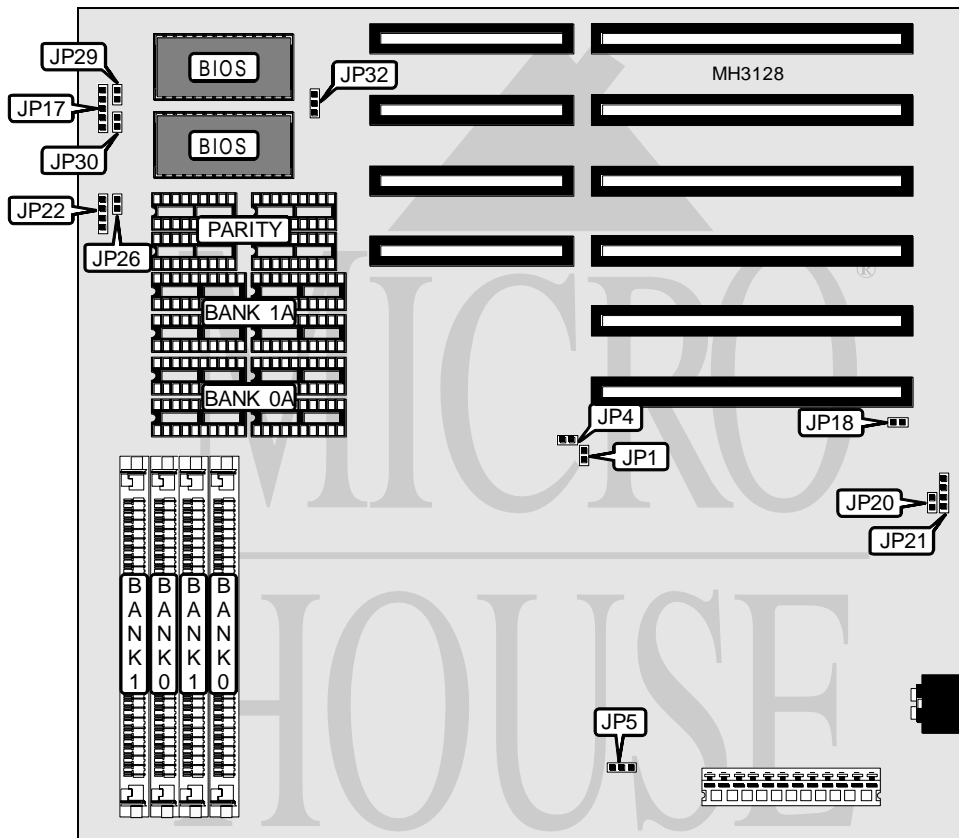


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TI 16/12

Processor	80286 (exact location unidentified)
Processor Speed	12/16MHz
Chip Set	TI
Max. Onboard DRAM	16MB (12MB on external memory card)
Cache	None
BIOS	AMI/Award
Dimensions	254mm x 218mm
I/O Options	None
NPU Options	80287 (exact location unidentified)



CONNECTIONS			
Purpose	Location	Purpose	Location
Power LED & keylock	JP17	Turbo LED	JP26
External battery	JP21	Turbo switch	JP29
Speaker	JP22	Reset switch	JP30

Continued on next page. . .

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
Memory relocation disabled	JP1	Closed
Memory relocation enabled	JP1	Open
Parity enabled	JP5	pins 1 & 2 closed
Parity disabled	JP5	pins 2 & 3 closed
Monitor type select color	JP18	Closed
Monitor type select monochrome	JP18	Open
Battery enabled	JP20	Closed
Battery disabled	JP20	Open
BIOS type select 27256	JP32	pins 1 & 2 closed
BIOS type select 27128	JP32	pins 2 & 3 closed

DRAM CONFIGURATION						
Size	Bank 0A	Parity (U25/27)	Bank 1A	Parity (U26/28)	Bank 0	Bank 1
512KB	(4) 44256	(2) 41256	NONE	NONE	NONE	NONE
640KB	(4) 44256	(2) 41256	(4) 4464	(2) 4164	NONE	NONE
1MB	(4) 44256	(2) 41256	(4) 44256	(2) 41256	NONE	NONE
2MB	NONE	NONE	NONE	NONE	(2) 1M x 9	NONE
4MB	NONE	NONE	NONE	NONE	(2) 1M x 9	(2) 1M x 9

Note: The actual location of the parity configuration is unidentified.

DRAM JUMPER CONFIGURATION	
DRAM size	JP4
256KB	Closed
1MB	Open

MISCELLANEOUS TECHNICAL NOTE
Note: The location of pin 1 is unidentified.