## CHAINTECH COMPUTER COMPANY, LTD.

## 325 SCD / 333 SCD / 340 SCD

Processor
Processor Speed
Chip Set
Max. Onboard DRAM
Cache
BIOS
Dimensions
I/O Options
NPU Options

AM386DX/AM386DXL/80386DX
$25 / 33 / 40 \mathrm{MHz}$
Unidentified
32MB
32/64/128/256KB
AMI
$330 \mathrm{~mm} \times 218 \mathrm{~mm}$
None
80387DX/3167


| CONNECTIONS |  |  |  |
| :--- | :---: | :--- | :---: |
| Purpose | Location | Purpose | Location |
| Reset switch | J 1 | Speaker | J 4 |
| Turbo switch | J 2 | Power LED \& keylock | J 5 |
| Turbo LED | J 3 | External battery | J 7 |

Continued on next page. .

## CHAINTECH COMPUTER COMPANY, LTD. <br> 325 SCD/333SCD/340SCD

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| USER CONFIGURABLE SETTINGS |  |  |
| :---: | :---: | :---: |
| Function |  |  |
| í Monitor type select color | Jumper | Position |
| Monitor type select monochrome | J6 | Closed |
| í NPU synchronous with CPU | J14 | Open |
| NPU asynchronous with CPU | J14 | pins $2 \& 2$ closed |


| DRAM CONFIGURATION |  |  |
| :---: | :---: | :---: |
| Size | Bank 0 | Bank 1 |
| 1 MB | $(4) 256 \mathrm{~K} \times 9$ | NONE |
| 2 MB | (4) $256 \mathrm{~K} \times 9$ | (4) $256 \mathrm{~K} \times 9$ |
| 4 MB | (4) $1 \mathrm{M} \times 9$ | NONE |
| 5 MB | (4) $256 \mathrm{~K} \times 9$ | (4) $1 \mathrm{M} \times 9$ |
| 8 MB | (4) $1 \mathrm{M} \times 9$ | (4) $1 \mathrm{M} \times 9$ |
| 16 MB | (4) $4 \mathrm{M} \times 9$ | NONE |
| 20 MB | (4) $1 \mathrm{M} \times 9$ | (4) $4 \mathrm{M} \times 9$ |
| 32 MB | (4) $4 \mathrm{M} \times 9$ | (4) $4 \mathrm{M} \times 9$ |


| CACHE CONFIGURATION |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Size | Bank 0 | Bank 1 | TAG0 | TAG1 |
| 32 KB | $(4) 8 \mathrm{~K} \times 8$ | NONE | $(1) 8 \mathrm{~K} \times 8$ | NONE |
| 64 KB | $(4) 8 \mathrm{~K} \times 8$ | $(4) 8 \mathrm{~K} \times 8$ | $(1) 8 \mathrm{~K} \times 8$ | $(1) 8 \mathrm{~K} \times 8$ |
| 128 KB | $(4) 32 \mathrm{~K} \times 8$ | NONE | $(1) 32 \mathrm{~K} \times 8$ | NONE |
| 256 KB | $(4) 32 \mathrm{~K} \times 8$ | $(4) 32 \mathrm{~K} \times 8$ | $(1) 32 \mathrm{~K} \times 8$ | $(1) 32 \mathrm{~K} \times 8$ |


| CACHE JUMPER CONFIGURATION |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Size | J10 | J11 | J12 | J13 |  |
| 32 KB | pins $1 \& 2$ closed | pins 1 \& 2 closed | pins 1 \& 2 closed | pins 1 \& 2 closed |  |
| 64 KB | pins $1 \& 2$ closed | pins 2 \& 3 closed | pins 1 \& 2 closed | pins 2 \& 3 closed |  |
| 128 KB | pins 1 \& 2 closed | pins 2 \& 3 closed | pins 1 \& 2 closed | pins 2 \& 3 closed |  |
| 256 KB | pins 2 \& 3 closed | pins 2 \& 3 closed | pins 2 \& 3 closed | pins 2 \& 3 closed |  |

